

# Datasheet

**APM32A103xET7**

**Arm<sup>®</sup> Cortex<sup>®</sup>-M3 based 32-bit MCU**

**Version: V1.0**

## 1. Product characteristics

### ■ Core

- 32-bit Arm® Cortex®-M3 core
- Up to 120MHz working frequency

### ■ On-chip memory

- Flash: 512KB
- SRAM: 128KB
- EMMC: Supports CF card, SRAM, PSRAM, SDRAM NOR and NAND memory

### ■ Clock

- HSECLK: 4~16MHz external crystal/ceramic oscillator supported
- LSECLK: 32.768KHz crystal/ceramic oscillator supported
- HSICLK: 8MHz RC oscillator calibrated by factory
- LSICLK: 40KHz RC oscillator supported
- PLL: Phase locked loop, 2~16 times of frequency supported

### ■ Reset and power management

- $V_{DD}$  range: 2.0~3.6V
- $V_{DDA}$  range: 2.0~3.6V
- $V_{BAT}$  range of backup domain power supply: 1.8V~3.6V
- Power-on/power-down reset (POR/PDR) supported
- Programmable power supply voltage detector supported(PVD)

### ■ Low-power mode

- Sleep, stop and standby modes supported

### ■ DMA

- Two DMA; DMA1 supports 7 channels and DMA2 supports 5 channels

### ■ Debugging interface

- JTAG
- SWD

### ■ I/O

- Up to 80 I/Os
- All I/Os can be mapped to external interrupt vector
- Up to 60 FT input I/Os

### ■ Communication peripherals

- 2 I2C interfaces (1Mbit/s), all of which support SMBus/PMBus
- 3 USART, 2 UART, support ISO7816, LIN and IrDA functions
- 3 SPI (2 reusable I2S), maximum transmission speed 18Mbps
- 2 CAN, USB D and CAN can work independently at the same time
- 1 USB D
- 1 SDIO Interface

### ■ Analog peripherals

- 3 12-bit ADCs
- 2 12-bit DACs

### ■ Timer

- 2 16-bit advanced timers TMR1/8 that can provide 7 channels PWM output, support dead zone generation and braking input functions
- 4 16-bit general-purpose timers TMR2/3/4/5, each with up to 4 independent channels to support input capture, output comparison, PWM, pulse count and other functions
- 2 16-bit basic timers TMR6/7
- 2 watchdog timers: one independent watchdog IWDG and one window watchdog WWDG
- 1 24-bit autodecrement SysTick Timer

### ■ RTC

- Support calendar and clock functions

### ■ 84Bytes backup register

### ■ FPU

### ■ CRC computing unit

### ■ 96-bit unique device ID

### ■ Chip packaging

- LQFP64/LQFP100

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## 2. Product information

See the following table for APM32A103xET7 product functions and peripheral configuration.

Table 1 Functions and Peripherals of APM32A103xET7 Series Chips

Product		APM32A103	
Model		RET7	VET7
Package		LQFP64	LQFP100
Core and maximum working frequency		Arm® 32-bit Cortex®-M3@120MHz	
Operating voltage		2.0~3.6V	
Flash(KB)		512	
SRAM(KB)		128	
EMMC		0	1 (Not supported SDRAM)
GPIOs		51	80
Communication interface	USART/UART	3/2	
	SPI/I2S	3/2	
	I2C	2	
	I2C3	1	
	USBD	1	
	CAN	2	
	SDIO	1	
Timer	16-bit advanced	2	
	16-bit general	4	
	16-bit basic	2	
	System tick timer	1	
	Watchdog	2	
Real-time clock		1	
12-bit ADC	Unit	3	
	External channel	16	
	Internal channel	2	
12-bit DAC	Unit	2	
	Channel	2	
Operating temperature		Ambient temperature: -40°C to 105°C Junction temperature: -40°C to 125°C	

### 3. Pin information

#### 3.1. Pin distribution

Figure 1 Distribution Diagram of APM32A103xET7 Series LQFP100 Pins

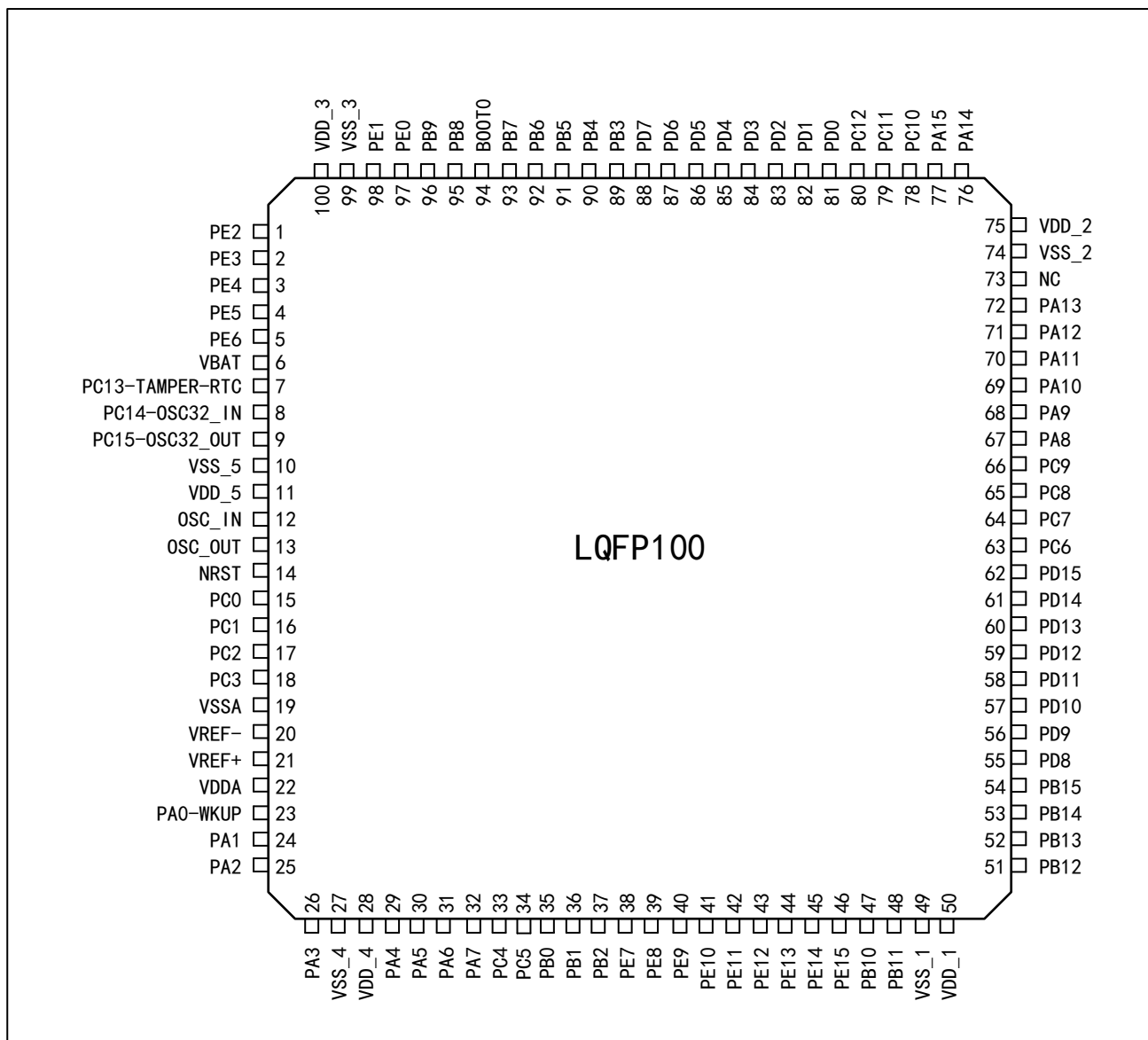
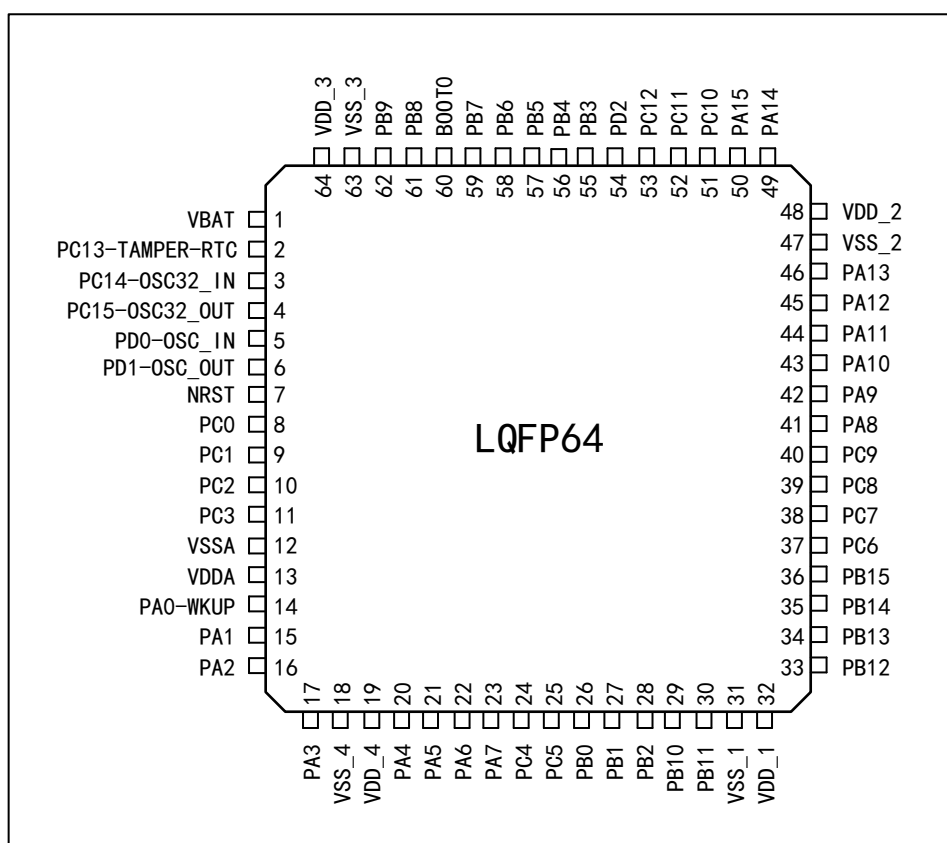


Figure 2 Distribution Diagram of APM32A103xET7 Series LQFP64 Pins



### 3.2. Pin function description

Table 2 Legends/Abbreviations Used in Output Pin Table

Name	Abbreviation	Definition
Pin name		Unless otherwise specified in parentheses below the pin name, the pin functions during and after reset are the same as the actual pin name
Pin type	P	Power pin
	I	Only input pin
	I/O	I/O pin
I/O structure	5T	FT I/O
	5Tf	FT I/O, FM+ function
	STDA	I/O with 3.3 V standard, directly connected to ADC
	STD	I/O with 3.3 V standard
	B	Dedicated Boot0 pin
	RST	Bidirectional reset pin with built-in pull-up resistor
Note		Unless otherwise specified in the notes, all I/O is set as floating input during and after reset



Name		Abbreviation	Definition
Pin function	Default multiplexing function		Function directly selected/enabled through peripheral register
	Remap		Select this function through AFIO remapping register

Table 3 Description of APM32A103xET7 by Pin Number

Name (Function after reset)	Type	Structure	Default multiplexing function	Remap	LQFP64	LQFP100
PE2	I/O	5T	TRACECK, SMC_A23	-	-	1
PE3	I/O	5T	TRACED0, SMC_A19, DMC_DQ4	-	-	2
PE4	I/O	5T	TRACED1, SMC_A20	-	-	3
PE5	I/O	5T	TRACED2, SMC_A21, DMC_DQ5	-	-	4
PE6	I/O	5T	TRACED3, SMC_A22, DMC_DQ6	-	-	5
V <sub>BAT</sub>	P	-	-	-	1	6
PC13-TAMPER-RTC (PC13)	I/O	STD	TAMPER_RTC	-	2	7
PC14-OSC32_IN (PC14)	I/O	STD	OSC32_IN	-	3	8
PC15-OSC32_OUT (PC15)	I/O	STD	OSC32_OUT	-	4	9
V <sub>SS_5</sub>	P	-	-	-	-	10
V <sub>DD_5</sub>	P	-	-	-	-	11
OSC_IN	I	STD	-	PD0	5	12
OSC_OUT	O	STD	-	PD1	6	13
NRST	I/O	RST	-	-	7	14
PC0	I/O	STDA	ADC123_IN10	-	8	15
PC1	I/O	STDA	ADC123_IN11	-	9	16
PC2	I/O	STDA	ADC123_IN12	-	10	17
PC3	I/O	STDA	ADC123_IN13	-	11	18

Name (Function after reset)	Type	Structure	Default multiplexing function	Remap	LQFP64	LQFP100
V <sub>SSA</sub>	P	-	-	-	12	19
V <sub>REF-</sub>	P	-	-	-	-	20
V <sub>REF+</sub>	P	-	-	-	-	21
V <sub>DDA</sub>	P	-	-	-	13	22
PA0-WKUP (PA0)	I/O	STDA	WKUP, USART2_CTS, ADC123_IN0, TMR2_CH1_ETR, TMR5_CH1, TMR8_ETR	-	14	23
PA1	I/O	STDA	USART2_RTS, ADC123_IN1, TMR5_CH2, TMR2_CH2	-	15	24
PA2	I/O	STDA	USART2_TX, TMR5_CH3, ADC123_IN2, TMR2_CH3	-	16	25
PA3	I/O	STDA	USART2_RX, TMR5_CH4, ADC123_IN3, TMR2_CH4	-	17	26
V <sub>SS_4</sub>	P	-	-	-	18	27
V <sub>DD_4</sub>	P	-	-	-	19	28
PA4	I/O	STDA	SPI1_NSS, USART2_CK, DAC_OUT1, ADC12_IN4	-	20	29
PA5	I/O	STDA	SPI1_SCK, DAC_OUT2, ADC12_IN5	-	21	30
PA6	I/O	STDA	SPI1_MISO, TMR8_BKIN, ADC12_IN6 TMR3_CH1	TMR1_BKIN	22	31
PA7	I/O	STDA	SPI1_MOSI, TMR8_CH1N, ADC12_IN7, TMR3_CH2	TMR1_CH1N	23	32

Name (Function after reset)	Type	Structure	Default multiplexing function	Remap	LQFP64	LQFP100
PC4	I/O	STDA	ADC12_IN14	-	24	33
PC5	I/O	STDA	ADC12_IN15	-	25	34
PB0	I/O	STDA	ADC12_IN8, TMR3_CH3, TMR8_CH2N	TMR1_CH2N	26	35
PB1	I/O	STDA	ADC12_IN9, TMR3_CH4, TMR8_CH3N	TMR1_CH3N	27	36
PB2 (PB2,BOOT1)	I/O	5T	-	-	28	37
PE7	I/O	5T	SMC_D4	TMR1_ETR	-	38
PE8	I/O	5T	SMC_D5, DMC_A4	TMR1_CH1N	-	39
PE9	I/O	5T	SMC_D6, DMC_A5	TMR1_CH1	-	40
PE10	I/O	5T	SMC_D7, DMC_A6	TMR1_CH2N	-	41
PE11	I/O	5T	SMC_D8, DMC_A7	TMR1_CH2	-	42
PE12	I/O	5T	SMC_D9, DMC_A8	TMR1_CH3N	-	43
PE13	I/O	5T	SMC_D10, DMC_A9	TMR1_CH3	-	44
PE14	I/O	5T	SMC_D11	TMR1_CH4	-	45
PE15	I/O	5T	SMC_D12, DMC_CLK	TMR1_BKIN	-	46
PB10	I/O	5T	I2C2_SCL, USART3_TX, DMC_UDQM	TMR2_CH3	29	47
PB11	I/O	5T	I2C2_SDA, USART3_RX, DMC_CKE	TMR2_CH4	30	48
V <sub>SS_1</sub>	P	-	-	-	31	49
V <sub>DD_1</sub>	P	-	-	-	32	50
PB12	I/O	5T	SPI2_NSS, I2S2_WS, I2C2_SMBAL, USART3_CK, TMR1_BKIN,	-	33	51

Name (Function after reset)	Type	Structure	Default multiplexing function	Remap	LQFP64	LQFP100
			CAN2_RX			
PB13	I/O	5T	SPI2_SCK, I2S2_CK, USART3_CTS, TMR1_CH1N, CAN2_TX	-	34	52
PB14	I/O	5T	SPI2_MISO, TMR1_CH2N, USART3_RTS	-	35	53
PB15	I/O	5T	SPI2_MOSI, I2S2_SD, TMR1_CH3N	-	36	54
PD8	I/O	5T	SMC_D13	USART3_TX	-	55
PD9	I/O	5T	SMC_D14	USART3_RX	-	56
PD10	I/O	5T	SMC_D15	USART3_CK	-	57
PD11	I/O	5T	SMC_A16	USART3_CTS	-	58
PD12	I/O	5T	SMC_A17	TMR4_CH1, USART3_RTS	-	59
PD13	I/O	5T	SMC_A18	TMR4_CH2	-	60
PD14	I/O	5T	SMC_D0	TMR4_CH3	-	61
PD15	I/O	5T	SMC_D1	TMR4_CH4	-	62
PC6	I/O	5T	I2S2_MCK, TMR8_CH1, SDIO_D6	TMR3_CH1	37	63
PC7	I/O	5T	I2S3_MCK, TMR8_CH2, SDIO_D7	TMR3_CH2	38	64
PC8	I/O	5T	TMR8_CH3, SDIO_D0	TMR3_CH3	39	65
PC9	I/O	5T	TMR8_CH4, SDIO_D1	TMR3_CH4	40	66
PA8	I/O	5T	USART1_CK, TMR1_CH1, MCO	-	41	67
PA9	I/O	5T	USART1_TX, TMR1_CH2	-	42	68
PA10	I/O	5T	USART1_RX, TMR1_CH3	-	43	69

Name (Function after reset)	Type	Structure	Default multiplexing function	Remap	LQFP64	LQFP100
PA11	I/O	5T	USART1_CTS, USBD1DM, USBD2DM, CAN1_RX, TMR1_CH4	-	44	70
PA12	I/O	5T	USART1_RTS, USBD1DP USBD2DP, CAN1_TX, TMR1_ETR	-	45	71
PA13 (JTMS,SWDIO)	I/O	5T	-	PA13	46	72
NC	-	-	Not connected	-	-	73
V <sub>SS_2</sub>	P	-	-	-	47	74
V <sub>DD_2</sub>	P	-	-	-	48	75
PA14 (JTCK,SWCLK)	I/O	5T	-	PA14	49	76
PA15 (JTDI)	I/O	5T	SPI3_NSS, I2S3_WS	TMR2_CH1_ETR, PA15, SPI1_NSS	50	77
PC10	I/O	5T	UART4_TX, SDIO_D2, DMC_DQ8	USART3_TX	51	78
PC11	I/O	5T	UART4_RX, SDIO_D3, DMC_DQ9	USART3_RX	52	79
PC12	I/O	5T	UART5_TX, SDIO_CK	USART3_CK	53	80
PD0 (OSC_IN)	I/O	5T	SMC_D2	CAN1_RX	-	81
PD1 (OSC_OUT)	I/O	5T	SMC_D3	CAN1_TX	-	82
PD2	I/O	5T	TMR3_ETR, UART5_RX, SDIO_CMD, DMC_DQ10	-	54	83
PD3	I/O	5T	SMC_CLK, DMC_DQ11	USART2_CTS	-	84
PD4	I/O	5T	SMC_NOE, DMC_DQ12	USART2_RTS	-	85

Name (Function after reset)	Type	Structure	Default multiplexing function	Remap	LQFP64	LQFP100
PD5	I/O	5T	SMC_NWE, DMC_DQ13	USART2_TX	-	86
PD6	I/O	5T	SMC_NWAIT, DMC_DQ14	USART2_RX	-	87
PD7	I/O	5T	SMC_NE1, SMC_NCE2	USART2_CK	-	88
PB3 (JTDO)	I/O	5T	SPI3_SCK, I2S3_CK	PB3, TRACESWO, TMR2_CH2, SPI1_SCK	55	89
PB4 (NJTRST)	I/O	5T	SPI3_MISO	PB4, TMR3_CH1, SPI1_MISO	56	90
PB5	I/O	STD	I2C1_SMBAL, SPI3_MOSI, I2S3_SD	TMR3_CH2, SPI1_MOSI, CAN2_RX	57	91
PB6	I/O	5T	I2C1_SCL, I2C3_SCL, TMR4_CH1	USART1_TX, CAN2_TX	58	92
PB7	I/O	5T	I2C1_SDA, I2C3_SDA, SMC_NADV, TMR4_CH2	USART1_RX	59	93
BOOT0	I	B	-	-	60	94
PB8	I/O	5T	TMR4_CH3, SDIO_D4	I2C1_SCL, I2C3_SCL, CAN1_RX	61	95
PB9	I/O	5T	TMR4_CH4, SDIO_D5	I2C1_SDA, I2C3_SDA, CAN1_TX	62	96
PE0	I/O	5T	TMR4_ETR, SMC_NBL0	-	-	97
PE1	I/O	5T	SMC_NBL1	-	-	98
V <sub>SS_3</sub>	P	-	-	-	63	99
V <sub>DD_3</sub>	P	-	-	-	64	100

Note:

- (1) The functions available depend on the selected model. For models with fewer peripheral modules, function modules with smaller numbers are always included. For example, when a model has only one SPI and two USARTs, they are SPI1, USART1 and USART2.
- (2) PC13, PC14 and PC15 are powered through the power switch. Since the switch only sinks limited current (3mA), the use of GPIO from PC13 to PC15 in output mode is limited:
  - ① The speed shall not exceed 2MHz when the heavy load is 30pF;
  - ② Not used for current source (e.g. driving LED).
- (3) These pins are in the main function state when the backup area is powered on for the first time. After that, even if they are reset, the state of these pins is controlled by the backup area registers (these registers will not be reset by the main reset system). For specific information on how to control these IO ports, please refer to the relevant sections of the battery backup area and BAKPR register in the user manual.
- (4) This kind of multiplexing function can be configured to other pins by software (if the corresponding package model has this pin). For details, please refer to the multiplexing function I/O chapter and the debugging setting chapter of the user manual.
- (5) For Pin 5 and Pin 6 of LQFP64 and LQFP48 package, the default configuration after the chip is reset is OSC\_IN and OSC\_OUT, the software can reset these two pins with PD0 and PD1 functions; for LQFP100 package, PD0 and PD1 are inherent function pins. Therefore, it is no longer necessary for the software to re-image. For more details, refer to the Reuse Function I/O section and the Debug Settings section of the reference manual. In output mode, PD0 and PD1 can only be configured as 50MHz output mode.

## 4. Functional description

This chapter mainly introduces the system architecture, interrupt, on-chip memory, clock, power supply and peripheral features of APM32A103xET7 series products; for information about the Arm® Cortex®-M3 core, please refer to the Arm® Cortex®-M3 technical reference manual, which can be downloaded from Arm's website.

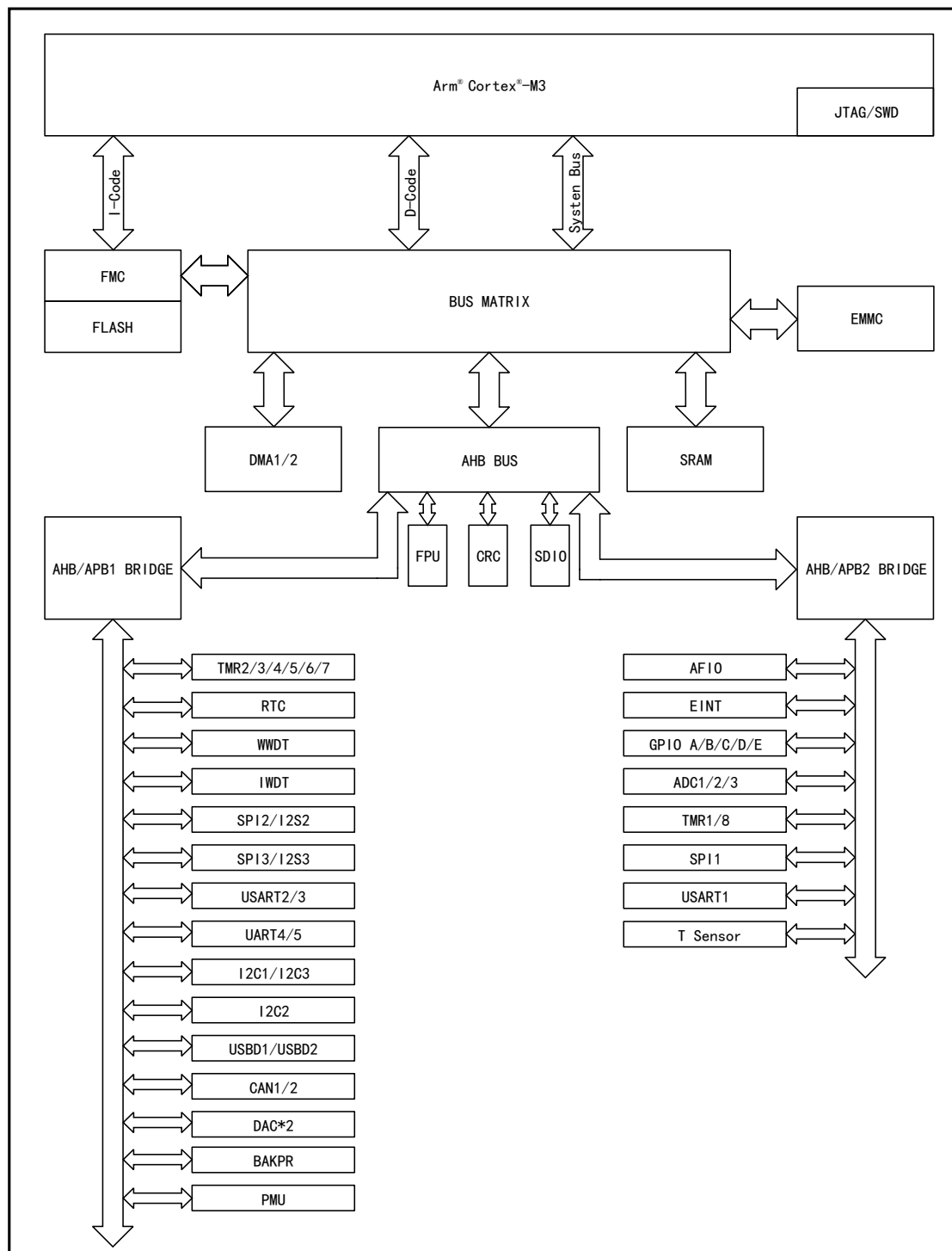
At present, APM32A103VET7, APM32A103RET7 has passed AEC-Q100 Grade1 certification.



## 4.1. System architecture

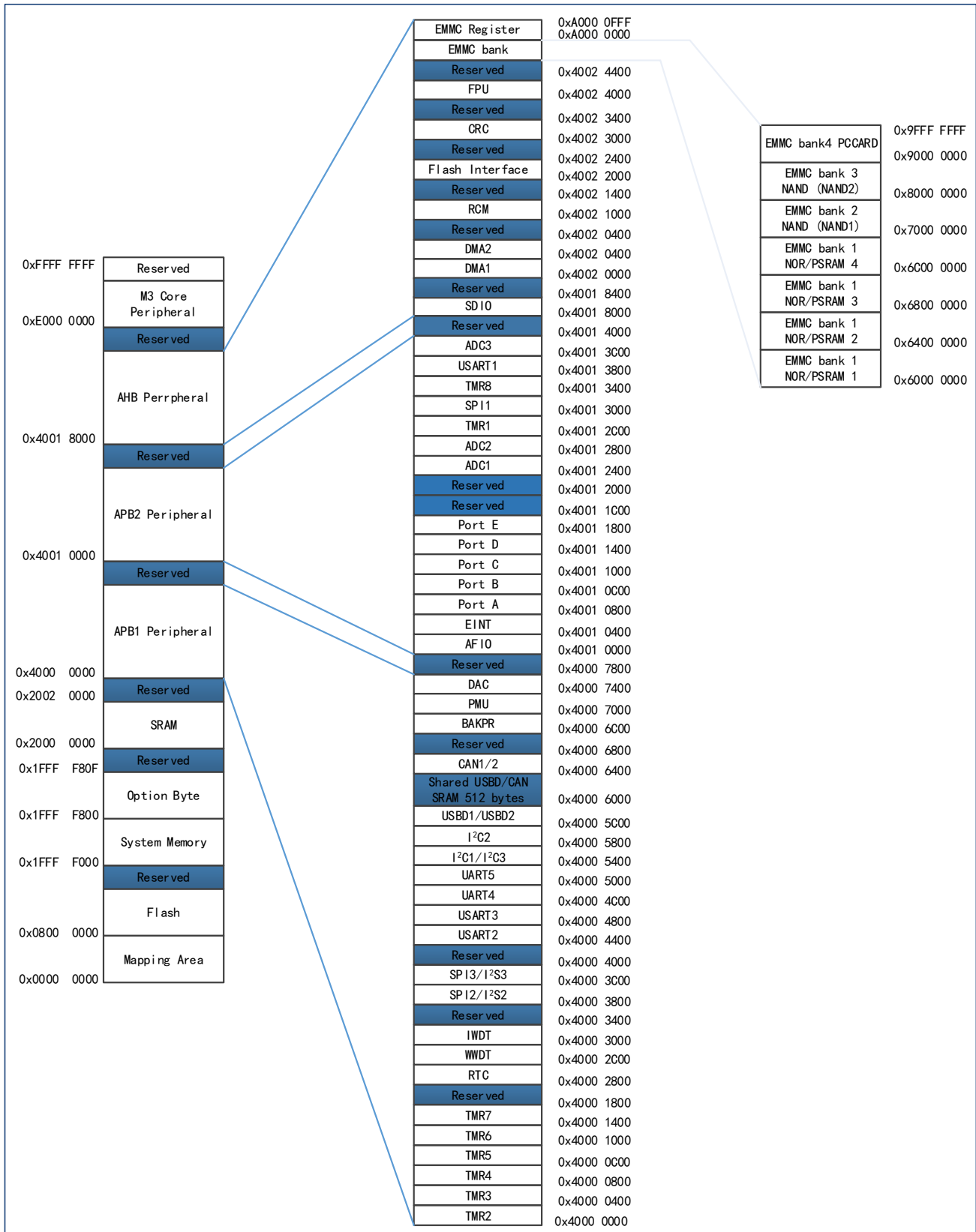
### 4.1.1. System block diagram

Figure 3 APM32A103xET7 System Block Diagram



### 4.1.2. Address mapping

Figure 4 APM32A103xET7 Series Address Mapping Diagram



### 4.1.3. Startup configuration

At startup, the user can select one of the following three startup modes by setting the high and low levels of the Boot pin:

- Startup from main memory
- Startup from BootLoader
- Startup from built-in SRAM

The user can use USART interface to reprogram the user Flash if boot from BootLoader.

## 4.2. Core

The core of APM32A103xET7 is Arm® Cortex®-M3. Based on this platform, the development cost is low and the power consumption is low. It can provide excellent computing performance and advanced system interrupt response, and is compatible with all Arm tools and software.

## 4.3. Interrupt controller

### 4.3.1. Nested Vector Interrupt Controller (NVIC)

It embeds a nested vectored interrupt controller (NVIC) that can handle up to 65 maskable interrupt channels (not including 16 interrupt lines of Cortex®-M3) and 16 priority levels. The interrupt vector entry address can be directly transmitted to the core, so that the interrupt response processing with low delay can give priority to the late higher priority interrupt.

### 4.3.2. External Interrupt/Event Controller (EINT)

The external interrupt/event controller consists of 19 edge detectors, and each detector includes edge detection circuit and interrupt/event request generation circuit; each detector can be configured as rising edge trigger, falling edge trigger or both and can be masked independently. Up to 80 GPIOs can be connected to the 16 external interrupt lines.

## 4.4. On-chip memory

On-chip memory includes main memory area, SRAM and information block; the information block includes system memory area and option byte; the system memory area stores BootLoader, 96-bit unique device ID and capacity information of main memory area; the system memory area has been written into the program and cannot be erased.

Table 4 On-chip Memory Area

Memory	Maximum capacity	Function
Main memory area	512 KB	Store user programs and data.
SRAM	128 KB	CPU can access at 0 waiting cycle (read/write).
System memory area	2KB	Store BootLoader, 96-bit unique device ID, and main memory area capacity information
Option byte	16Bytes	Configure main memory area read-write protection and MCU working mode

### 4.4.1. External Memory Controller (EMMC)

The APM32A103xET7 enhanced series integrates the EMMC module and consists of SMC (static Storage Controller), DMC (Dynamic Storage Controller), supporting PC card, SRAM, PSRAM, NOR and NAND.

Function:

- Three EMMC interrupt sources, through logic or connected to the NVIC list
- Write FIFO
- Code could run on external storage besides NAND Flash and PC card
- Connect with LCD

#### **4.4.2. LCD parallel interface**

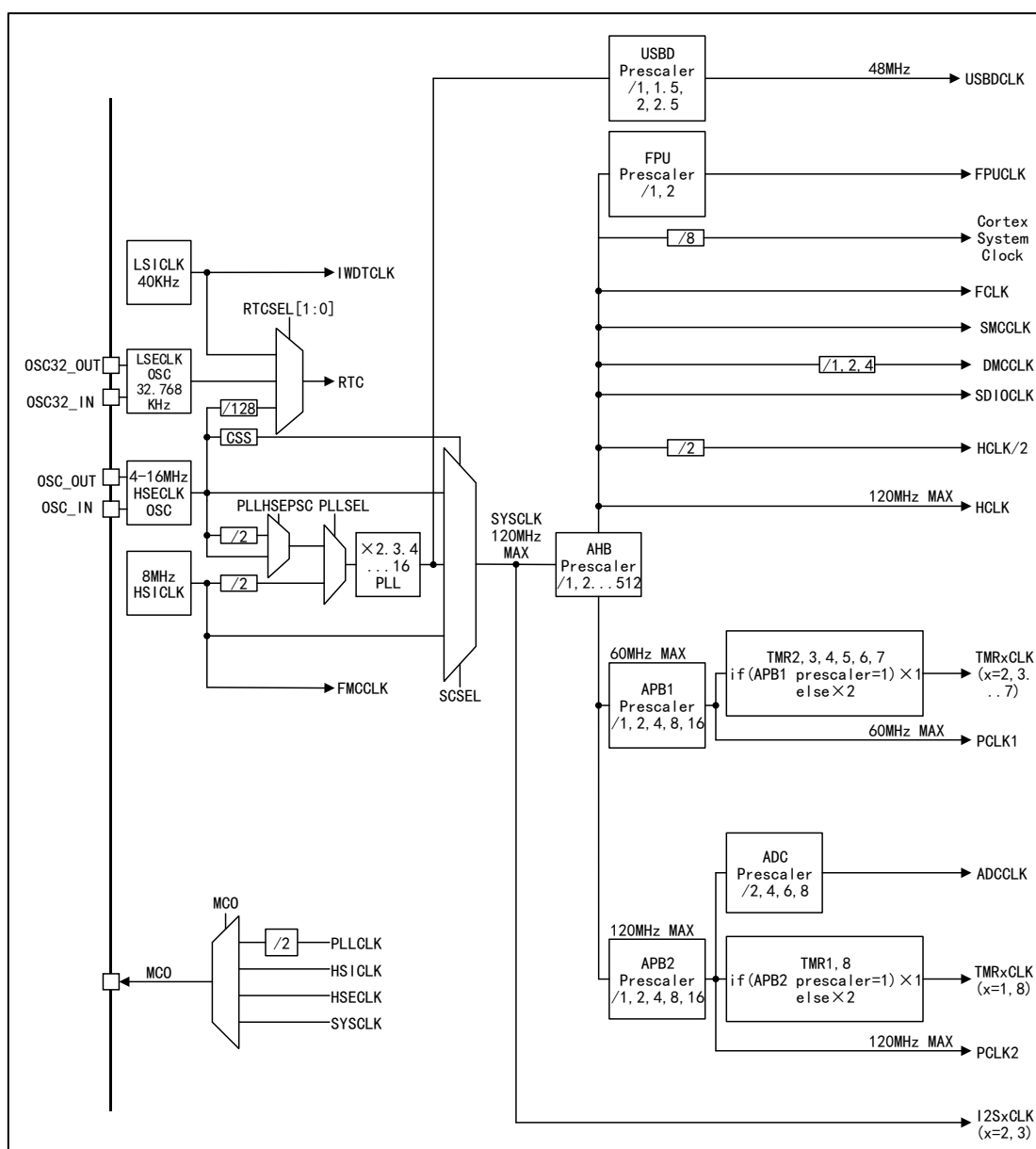
EMMC can be configured to the seamless connection with most graphic LCD controller, it supports the Intel 8080 and Motorola 6800 model, and can be flexibly with specific LCD interface. Using the parallel interface LCD can be easily build simple graphics applications, or use a special scheme of high performance speed controller.

### **4.5. Clock**

#### **4.5.1. Clock tree**

Clock tree of APM32A103xET7 is shown in the figure below:

Figure 5 APM32A103xET7 Clock Tree



### 4.5.2. Clock source

Clock source is divided into high-speed clock and low-speed clock according to the speed; the high-speed clock includes HSICLK and HSECLK, and the low-speed clock includes LSECLK and LSICLK; clock source is divided into internal clock and external clock according to the chip inside/outside; the internal clock includes HSICLK and LSICLK, and the external clock includes HSECLK and LSECLK, among which HSICLK is calibrated by the factory to  $\pm 1\%$  accuracy.

### 4.5.3. System clock

HSICLK, PLLCLK and HSECLK can be selected as system clock; the clock source of PLLCLK can be one of HSICLK and HSECLK; the required system clock can be obtained by configuring PLL clock multiplier factor and frequency dividing coefficient.

When the product is reset and started, HSICLK is selected as the system clock by default, and then the user can choose one of the above clock sources as the system clock by himself. When HSECLK failure is detected, the system will automatically switch to the HSICLK, and if an

interrupt is enabled, the software can receive the related interrupt.

#### 4.5.4. Bus clock

AHB, APB1 and APB2 are built in. The clock source of AHB is SYSCLK, and the clock source of APB1 and APB2 is HCLK; the required clock can be obtained by configuring the frequency dividing coefficient. The maximum frequency of AHB and high-speed APB2 is 120MHz, and the maximum frequency of APB1 is 60MHz.

### 4.6. Power supply and power management

#### 4.6.1. Power supply scheme

Table 5 Power Supply Scheme

Name	Voltage range	Instruction
V <sub>DD</sub>	2.0~3.6V	I/Os (see pin distribution diagram for specific IO) and internal voltage regulator are powered through V <sub>DD</sub> pin.
V <sub>DDA</sub> /V <sub>SSA</sub>	2.0~3.6V	Power supply of ADC, DAC, reset module, RC oscillator and PLL analog part; when ADC or DAC is used, V <sub>DDA</sub> shall not be less than 2.4V; V <sub>DDA</sub> and V <sub>SSA</sub> must be connected to V <sub>DD</sub> and V <sub>SS</sub> .
V <sub>BAT</sub>	1.8~3.6V	When V <sub>DD</sub> is closed, RTC, external 32KHz oscillator and backup register are supplied through internal power switch.

#### 4.6.2. Voltage regulator

Table 6 Regulator Operating Mode

Name	Instruction
Master mode (MR)	Used in run mode
Low-power mode (LPR)	Used in stop mode
Power-down mode	Used in standby mode, when the voltage regulator has high impedance output, the core circuit is powered down, the power consumption of the voltage regulator is zero, and all data of registers and SRAM will be lost.

Note: The voltage regulator is always in working state after reset, and outputs with high impedance in power-down mode.

#### 4.6.3. Power supply voltage monitor

Power-on reset (POR) and power-down reset (PDR) circuits are integrated inside the product. These two circuits are always in working condition. When the power-down reset circuit monitors that the power supply voltage is lower than the specified threshold value (V<sub>POR/PDR</sub>), even if the external reset circuit is used, the system will remain reset.

The product has a built-in programmable voltage regulator (PVD) that can monitor V<sub>DD</sub> and compare it with V<sub>PVD</sub> threshold. When V<sub>DD</sub> is outside the V<sub>PVD</sub> threshold range and the interrupt is enabled, the MCU can be set to a safe state through the interrupt service program.

### 4.7. Low-power mode

APM32A103xET7 supports three low-power modes, namely, sleep mode, stop mode and standby mode, and there are differences in power, wake-up time and wake-up mode among these three modes. The low-power mode can be selected according to the actual application requirements.

Table 7 Low Power Consumption Mode

Mode	Instruction
Sleep mode	The core stops working, all peripherals are working, and it can be woken up through interrupts/events
Stop mode	Under the condition that SRAM and register data are not lost, the stop mode can achieve the lowest power consumption; The clock of the internal 1.3V power supply module will stop, HSECLK crystal resonator, HSICLK and PLL will be prohibited, and the voltage regulator can be configured in normal mode or low power mode; Any external interrupt line can wake up MCU, and the external interrupt lines include one of the 16 external interrupt lines, PVD output, RTC and USBD.
Standby mode	The power consumption in this mode is the lowest; Internal voltage regulator is turned off, all 1.3V power supply modules are powered off, HSECLK crystal resonator, HSICLK and PLL clocks are turned off, SRAM and register data disappear, RTC area and backup register contents remain, and standby circuit still works; The external reset signal on NRST, IWDG reset, rising edge on WKUP pin or RTC event will wake MCU out of standby mode.

## 4.8. DMA

2 built-in DMAs; DMA1 supports 7 channels and DMA2 supports 5 channels. Each channel supports multiple DMA requests, but only one DMA request is allowed to enter the DMA channel at the same time. The peripherals supporting DMA requests are ADC, SPI, USART, I2C, and TMRx. Four levels of DMA channel priority can be configured. Support "memory→memory, memory→peripheral, peripheral→memory" transfer of data (the memory includes Flash、SRAM、SDRAM)

## 4.9. GPIO

GPIO can be configured as general input, general output, multiplexing function and analog input、 output. The general input can be configured as floating input, pull-up input and pull-down input; the general output can be configured as push-pull output and open-drain output; the multiplexing function can be used for digital peripherals; and the analog input and output can be used for analog peripherals and low-power mode; the enable and disable pull-up/pull-down resistor can be configured; the speed of 2MHz, 10MHz and 50MHz can be configured; the higher the speed is, the greater the power and the noise will be.

## 4.10. Communication peripherals

### 4.10.1. USART/UART

Up to 5 universal synchronous/asynchronous transmitter receivers are built in the chip. The USART1 interface can communicate at a rate of 4.5Mbit/s, while other USART/UART interfaces can communicate at a rate of 2.25Mbit/s. All USART/UART interfaces can configure baud rate, parity check bit, stop bit, and data bit length; except UART5, all the other USART/UART can support DMA. USART/UART function differences are shown in the table below:

Table 8 USART/UART Function Differences

USART mode/function	USART1	USART2	USART3	UART4	UART5
Hardware flow control of modem	√	√	√	—	—
Synchronous mode	√	√	√	—	—
Smart card mode	√	√	√	—	—
IrDASIR coder-encoder functions	√	√	√	√	√
LIN mode	√	√	√	√	√

USART mode/function	USART1	USART2	USART3	UART4	UART5
Single-line half-duplex mode	√	√	√	√	√
Support DMA function	√	√	√	√	—

Note: √ = support.

#### 4.10.2. I2C

I2C1/2 and I2C3 bus interfaces are built in. I2C1 and I2C3 share hardware interface and register base address. Therefore, I2C1 and I2C3 cannot be used at the same time.

I2C1/2 both can work in multiple master modes or slave modes, support 7-bit or 10-bit addressing, and support dual-slave addressing in 7-bit slave mode; the communication rate supports standard mode (up to 100kbit/s) and fast mode (up to 400kbit/s); hardware CRC generator/checker are built in; they can operate with DMA and support SMBus 2.0 version/PMBus.

I2C3 bus can operate in standard mode, fast mode and high-speed mode. The devices in high-speed mode and fast mode are downward compatible.

#### 4.10.3. SPI/I2S

Three built-in SPIs, support full duplex and half duplex communication in master mode and slave mode, can use DMA controller, and can configure 4~16 bits per frame, and communicate at a rate of up to 18Mbit/s.

2 built-in I2S (multiplexed with SPI2 and SPI3 respectively), support half duplex communication in master mode and slave mode, support synchronous transmission, and can be configured with 16-bit, 24-bit and 32-bit data transfer with 16-bit or 32-bit resolution. The configurable range of audio sampling rate is 8kHz~48kHz; when one or two I2S interfaces are configured as the master mode, the master clock can be output to external DAC or decoder (CODEC) at 256 times of sampling frequency.

#### 4.10.4. CAN

2 built-in CANs (CAN1 and CAN2 can be used at the same time), compatible with 2.0A and 2.0B (active) specification, and can communicate at a rate of up to 1Mbit/s. It can receive and send standard frame of 11-bit identifier and extended frame of 29-bit identifier. It has 3 sending mailboxes and 2 receiving FIFO, 28 3-level adjustable filters.

#### 4.10.5. USB

The product embeds USB modules (USB1 and USB2) compatible with full-speed USB devices, which comply with the standard of full-speed USB devices (12Mb/s), and the endpoints can be configured by software, and have standby/wake-up functions. The dedicated 48MHz clock for USB is directly generated by internal PLL. When using the USB function, the system clock can only be one of 48MHz, 72MHz, 96MHz and 120MHz, which can obtain 48MHz required for USB through 1 fractional frequency, 1.5 fractional frequency, 2 fractional frequency and 2.5 fractional frequency respectively.

#### 4.10.6. Simultaneous use of USB and CAN interfaces

This product USB1 (2) and CAN1 (2) sharing the same dedicated 512 - byte SRAM memory used to send and receive data, USB and CAN therefore be ready to use at the same time. Details are as follows:

- CAN2 and USB1 could be used at the same time
- CAN1 and USB2 could be used at the same time
- USB1 and USB2 could not be used at the same time



- CAN1 and CAN2 could be used at the same time

Note: Although there are actually 2 identical USBs (with the same pins), they can't be used together, so it's equivalent to only 1. Users can achieve "simultaneous use" by remapping (reuse of pins).

## 4.11. Analog peripherals

### 4.11.1. ADC

3 built-in ADCs with 12-bit accuracy, up to 16 external channels and 2 internal channels for each ADC. The internal channels measure the temperature sensor voltage and reference voltage respectively. ADC1 and ADC2 have 16 external channels, ADC3 generally has 8 external channels; A/D conversion mode of each channel has single, continuous, scan or intermittent modes, ADC conversion results can be left aligned or right aligned and stored in 16 bit data register; they support analog watchdog, and DMA.

#### 4.11.1.1. Temperature sensor

A temperature sensor (TSensor) is built in, which is internally connected with ADC\_IN16 channel. The voltage generated by the sensor changes linearly with temperature, and the converted voltage value can be obtained by ADC and converted into temperature.

#### 4.11.1.2. Internal reference voltage

Built-in reference voltage  $V_{REFINT}$ , internally connected to ADC\_IN17 channel, which can be obtained through ADC;  $V_{REFINT}$  provides stable voltage output for ADC.

### 4.11.2. DAC

Two built-in 12-bit DACs, and each corresponding to an output channel, which can be configured in 8-bit and 12-bit modes, and the DMA function is supported. The waveform generation supports noise wave and triangle wave. The conversion mode supports independent or simultaneous conversion and the trigger mode supports external signal trigger and internal timer update trigger.

## 4.12. Timer

2 built-in 16-bit advanced timers (TMR1/8), 4 general-purpose timers (TMR2/3/4/5), 2 basic timers (TMR6/7), 1 independent watchdog timer, one window watchdog timer and 1 system tick timer.

Watchdog timer can be used to detect whether the program is running normally.

The system tick timer is the peripheral of the core with automatic reloading function. When the counter is 0, it can generate a maskable system interrupt, which can be used for real-time operating system and general delay.

Table 9 Function Comparison between Advanced/General-purpose/Basic and System Tick Timers

Timer type	System tick timer	Basic timer		General-purpose timer				Advanced timer	
		TMR6	TMR7	TMR2	TMR3	TMR4	TMR5	TMR1	TMR8
Timer name	Sys Tick Timer								
Counter resolution	24-bit	16 bits		16 bits				16 bits	
Counter type	Down	Up		Up, down, up/down				Up, down, up/down	
Prescaler coefficient	-	Any integer between 1 and 65536		Any integer between 1 and 65536				Any integer between 1 and 65536	

Timer type	System tick timer	Basic timer	General-purpose timer	Advanced timer
General DMA request	-	OK	OK	OK
Capture/Comparison channel	-	-	4	4
Complementary outputs	-	No	No	Yes
Pin characteristics	-	-	There are 5 pins in total: 1-way external trigger signal input pins, 4-way channel (non-complementary channel) pins	There are 9 pins in total: 1-way external trigger signal input pins, 1-way braking input signal pins, 3-pair complementary channel pins, 1-way channel (non-complementary channel) pins
Function Instruction	Special for real-time operating system Automatic reloading function supported When the counter is 0, it can generate a maskable system interrupt Can program the clock source	Used to generate DAC trigger signals. Can be used as a 16-bit general-purpose timebase counter.	Synchronization or event chaining function provided Timers in debug mode can be frozen. -Can be used to generate PWM output Each timer has independent DMA request generation. It can handle incremental encoder signals	It has complementary PWM output with dead band insertion When configured as a 16-bit standard timer, it has the same function as the TMRx timer. When configured as a 16-bit PWM generator, it has full modulation capability (0~100%). In debug mode, the timer can be frozen, and PWM output is disabled. Synchronization or event chaining function provided.

Table 10 Independent Watchdog and Window Watchdog Timers

Name	Counter resolution	Counter type	Prescaler coefficient	Functional Description
Independent watchdog	12-bit	Down	Any integer between 1 and 256	The clock is provided by an internally independent RC oscillator of 40KHz, which is independent of the master clock, so it can run in stop and standby modes. The whole system can be reset in case of problems. It can provide timeout management for applications as a free-running timer. It can be configured as a software or hardware startup watchdog through option bytes. Timers in debug mode can be frozen.
Window watchdog	7-bit	Down	-	Can be set for free running. The whole system can be reset in case of problems. Driven by the master clock, it has early interrupt warning function; Timers in debug mode can be frozen.

## 4.13. RTC

1 RTC is built in, and there are LSECLK signal input pins (OSC32\_IN and OSC32\_OUT) and 1 TAMP input signal detection pin (TAMP); the clock source can select external 32.768kHz crystal oscillator, resonator or oscillator, LSICLK and HSECLK/128; it is supplied by  $V_{DD}$  by default; when  $V_{DD}$  is powered off, it can be automatically switched to  $V_{BAT}$  power supply, and RTC configuration and time data will not be lost; RTC configuration and time data are not lost in case of system resetting, software resetting and power resetting; it supports clock and calendar functions.

### 4.13.1. Backup register

84Bytes backup register is built in, and is supplied by  $V_{DD}$  by default; when  $V_{DD}$  is powered off, it can be automatically switched to  $V_{BAT}$  power supply, and the data in backup register will not be lost; the data in backup register will not be lost in case of system resetting, software resetting and power resetting.

## 4.14. CRC

A CRC (cyclic redundancy check) calculation unit is built in, which can generate CRC codes and operate 8-bit, 16-bit and 32-bit data.

## 4.15. FPU

The product has built-in independent FPU floating-point operation processing unit, supports IEEE754 standard, supports single-precision floating-point operation, and supports algorithms such as CMP, SUM, SUB, PRDCT, MAC, DIV, INVRGSQT, RGSQT, SUMSQ, DOT, floating-point to integer conversion and integer to floating point conversion.

## 5. Electrical characteristics

### 5.1. Test conditions of electrical characteristics

#### 5.1.1. Maximum and minimum values

Unless otherwise specified, all products are tested on the production line at  $T_A=25^{\circ}\text{C}$ . Its maximum and minimum values can support the worst environmental temperature, power supply voltage and clock frequency.

In the notes at the bottom of each table, it is stated that the data are obtained through comprehensive evaluation, design simulation or process characteristics and are not tested on the production line; on the basis of comprehensive evaluation, after passing the sample test, take the average value and add and subtract three times the standard deviation (average  $\pm 3\sigma$ ) to get the maximum and minimum values.

#### 5.1.2. Typical value

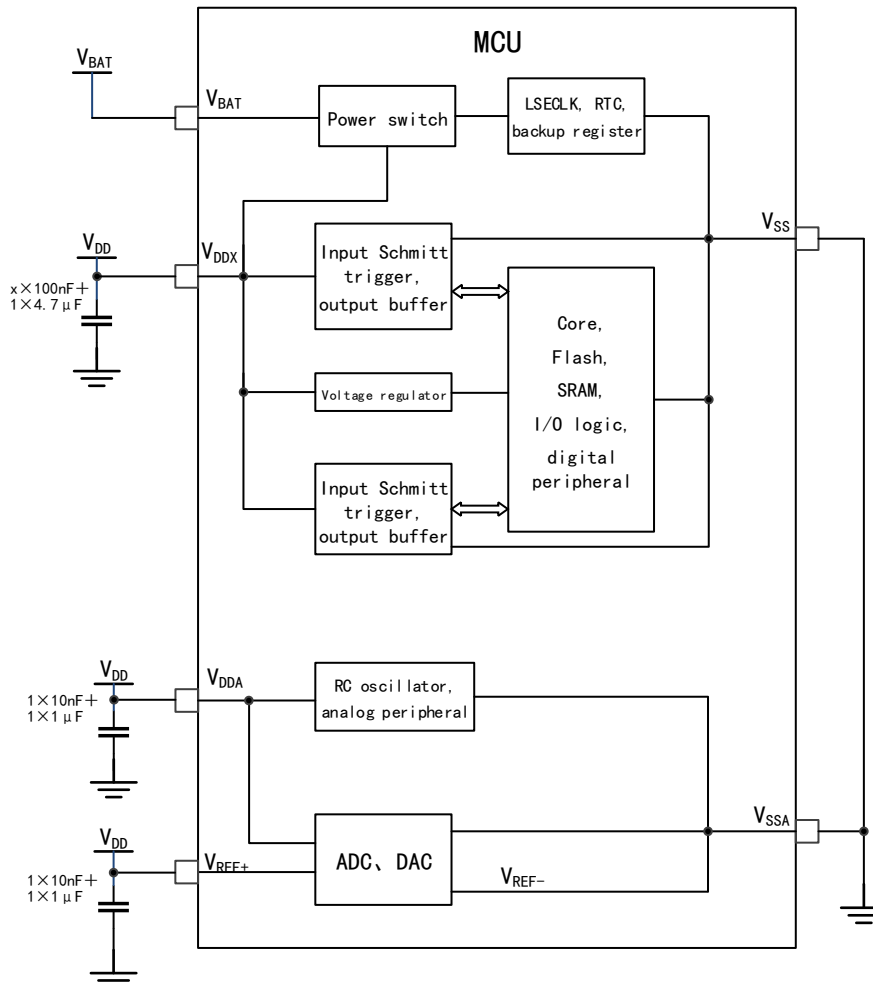
Unless otherwise specified, typical data are measured based on  $T_A=25^{\circ}\text{C}$ ,  $V_{DD}=V_{DDA}=3.3\text{V}$ . these data are only used for design guidance.

#### 5.1.3. Typical curve

Unless otherwise specified, typical curves will only be used for design guidance and will not be tested.

### 5.1.4. Power supply scheme

Figure 6 Power Supply Scheme



Notes:  $V_{DDx}$  in the figure means the number of  $V_{DD}$  is  $x$

### 5.1.5. Load capacitance

Figure 7 Load conditions when measuring pin parameters

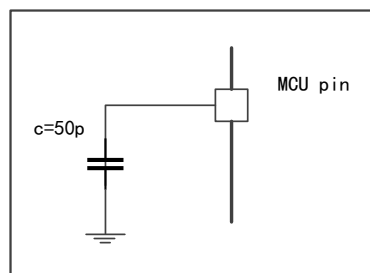


Figure 8 Pin Input Voltage Measurement Scheme

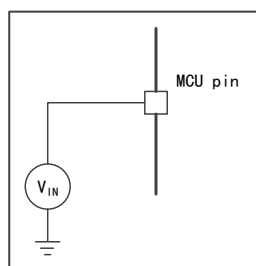
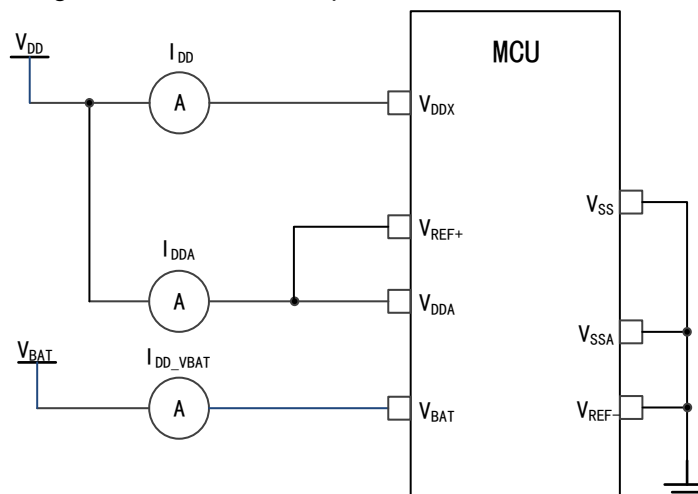


Figure 9 Power Consumption Measurement Scheme



## 5.2. Test under general operating conditions

Table 11 General Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f <sub>HCLK</sub>	Internal AHB clock frequency	-	-	120	MHz
f <sub>PCLK1</sub>	Internal APB1 clock frequency	-	-	60	
f <sub>PCLK2</sub>	Internal APB2 clock frequency	-	-	120	
V <sub>DD</sub>	Main power supply voltage	-	2	3.6	V
V <sub>DDA</sub>	Analog power supply voltage (When neither ADC nor DAC is used)	Must be the same as V <sub>DD</sub>	V <sub>DD</sub>	3.6	V
	Analog power supply voltage (When ADC and DAC are used)		2.4	3.6	
V <sub>BAT</sub>	Power supply voltage of backup domain	-	1.8	3.6	V
T <sub>A</sub>	Ambient temperature (temperature number 7)	Maximum power dissipation	-40	105	°C

## 5.3. Absolute maximum ratings

If the load on the device exceeds the absolute maximum rating, it may cause permanent damage to the device. Here, only the maximum load that can be borne is given, and there is no guarantee that the device functions normally under this condition.

### 5.3.1. Maximum temperature characteristics

Table 12 Temperature Characteristics

Symbol	Description	Numerical Value	Unit
T <sub>STG</sub>	Storage temperature range	-55 ~ +150	°C
T <sub>J</sub>	Maximum junction temperature	125	°C

### 5.3.2. Maximum rated voltage characteristics

All power supply (V<sub>DD</sub>, V<sub>DDA</sub>) and ground (V<sub>SS</sub>, V<sub>SSA</sub>) pins must always be connected to the power supply within the external limited range.

Table 13 Maximum Rated Voltage Characteristics

Symbol	Description	Minimum value	Maximum value	Unit
V <sub>DD</sub> - V <sub>SS</sub>	External main power supply voltage	-0.3	4.0	V
V <sub>DDA</sub> -V <sub>SSA</sub>	External analog power supply voltage	-0.3	4.0	
V <sub>BAT</sub> -V <sub>SS</sub>	Power supply voltage of external backup domain	-0.3	4.0	
V <sub>DD</sub> -V <sub>DDA</sub>	Voltage difference allowed by V <sub>DD</sub> >V <sub>DDA</sub>	-	0.3	
V <sub>IN</sub>	Input voltage on FT pins	V <sub>SS</sub> -0.3	5.5	
	Input voltage on other pins	V <sub>SS</sub> -0.3	V <sub>DD</sub> + 0.3	
ΔV <sub>DDx</sub>	Voltage difference between different power supply pins	-	50	mV
V <sub>SSx</sub> -V <sub>SS</sub>	Voltage difference between different grounding pins	-	50	

### 5.3.3. Maximum rated current features

Table 14 Current Characteristics

Symbol	Description	Maximum	Unit
I <sub>VDD</sub>	Total current into V <sub>DD</sub> /V <sub>DDA</sub> power lines (source) <sup>(1)</sup>	150	mA
I <sub>VSS</sub>	Total current out of V <sub>SS</sub> ground lines (sink) <sup>(1)</sup>	150	
I <sub>IO</sub>	Irrigation current on any I/O and control pins	25	
	Source current on any I/O and control pins	-25	
I <sub>INJ(PIN)</sub> <sup>(2) (3)</sup>	Injection current of 5T pin	-5/+0	
	Injection current of other pins	±5	
ΣI <sub>INJ(PIN)</sub> <sup>(2)</sup>	Total injection current on all I/O and control pins <sup>(4)</sup>	±25	

(1) All power (V<sub>DD</sub>, V<sub>DDA</sub>) and ground (V<sub>SS</sub>, V<sub>SSA</sub>) pins must always be connected to a power supply within the external allowable range.

(2) Negative injection disturbs the analog performance of the device.

(3) Positive injection is not possible on these I/Os. a negative injection is induced by V<sub>IN</sub><V<sub>SS</sub>. I<sub>INJ(PIN)</sub> must never be exceeded.

- (4) A positive injection is induced by  $V_{IN} > V_{DD}$  while a negative injection is induced by  $V_{IN} < V_{SS}$ .  $I_{INJ(PIN)}$  must never be exceeded.
- (5) When several inputs are submitted to a current injection, the maximum  $\Sigma I_{INJ(PIN)}$  is the absolute sum of the positive and negative injected currents (instantaneous values).

### 5.3.4. Electrostatic discharge (ESD)

Table 15 ESD Absolute Maximum Ratings

Symbol	Parameter	Conditions	Value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	$T_A = 18 \sim 24 \text{ }^\circ\text{C}$ , conforming to AEC-Q100-002-REV-E-2013	$\pm 5000$	V

Note: The samples are measured by a third-party testing organization and are not tested in production.

### 5.3.5. Static latch-up (LU)

Table 16 Static Latch-up

Symbol	Parameter	Conditions	Type
LU	Class of static latch-up	$T_A = +125 \text{ }^\circ\text{C}$ , conforming to AEC-Q100-004-REV-D-2012	CLASS II A

Note: The samples are measured by a third-party testing organization and are not tested in production.

## 5.4. On-chip memory

### 5.4.1. Flash characteristics

Table 17 Flash Memory Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
$t_{prog}$	16-bit programming time	$T_A = -40 \sim 105 \text{ }^\circ\text{C}$ $V_{DD} = 2.4 \sim 3.6 \text{V}$	40	46.08	70	$\mu\text{s}$
$t_{ERASE}$	Page (2KBytes) erase time	$T_A = -40 \sim 105 \text{ }^\circ\text{C}$ $V_{DD} = 2.4 \sim 3.6 \text{V}$	10	-	30	ms
$t_{ME}$	Whole erase time	$T_A = 40 \sim 105 \text{ }^\circ\text{C}$ $V_{DD} = 2.4 \sim 3.6 \text{V}$	10	-	30	ms
$V_{prog}$	Programming voltage	$T_A = -40 \sim 105 \text{ }^\circ\text{C}$	2	-	3.6	V

Note: It is obtained from a comprehensive evaluation and is not tested in production.

## 5.5. Clock

### 5.5.1. Characteristics of external clock source

#### High-speed external clock generated by crystal resonator

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.



Table 18 HSECLK4~16MHz Oscillator Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
f <sub>OSC_IN</sub>	Oscillator frequency	-	4	8	16	MHz
RF	Feedback resistance	-	-	200	-	kΩ
I <sub>DD(HSECLK)</sub>	HSECLK current consumption	V <sub>DD</sub> =3.3V, CL=10pF@8MHz	-	-	0.56	mA
t <sub>SU(HSECLK)</sub>	Startup time	V <sub>DD</sub> is stable	-	0.85	-	ms

Note: It is obtained from a comprehensive evaluation and is not tested in production.

### Low-speed external clock generated by crystal resonator

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.

Table 19 LSECLK Oscillator Characteristics (f<sub>LSECLK</sub>=32.768KHz)

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
f <sub>OSF_IN</sub>	Oscillator frequency	-	-	32.768	-	KHz
I <sub>DD(LSECLK)</sub>	LSECLK current consumption	-	-	-	0.8	μA
t <sub>SU(LSECLK)</sub> <sup>(1)</sup>	Startup time	V <sub>DDIOx</sub> is stable	-	0.93	-	s

Note: It is obtained from a comprehensive evaluation and is not tested in production.

(1) t<sub>SU(LSECLK)</sub> is the startup time, which is measured from the time when LSECLK is enabled by software to the time when stable oscillation at 32.768KHz is obtained. This value is measured using a standard crystal resonator, which may vary greatly due to different crystal manufacturers.

## 5.5.2. Characteristics of internal clock source

### High speed internal (HSICLK) RC oscillator

Table 20 HSICLK Oscillator Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit	
f <sub>HSICLK</sub>	Frequency	-	-	8	-	MHz	
A <sub>CCHSICLK</sub>	Accuracy of HSICLK oscillator	Factory calibration	V <sub>DD</sub> =3.3V, T <sub>A</sub> =25°C <sup>(1)</sup>	-1	-	1	%
			V <sub>DD</sub> =2-3.6V, T <sub>A</sub> =-40~105°C	-1.5	-	1.5	%
I <sub>DDA(HSICLK)</sub>	Power consumption of HSICLK oscillator	-	-	-	76	μA	
t <sub>SU(HSICLK)</sub>	Startup time of HSICLK oscillator	V <sub>DD</sub> =3.3V, T <sub>A</sub> =-40~105°C	3.24	-	3.4	μs	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

## Low speed internal (LSICLK) RC oscillator

Table 21 LSICLK Oscillator Characteristics

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
$f_{LSICLK}$	Frequency ( $V_{DD}=2-3.6V$ , $T_A=-40\sim 105^{\circ}C$ )	30	40	60	KHz
$I_{DD}(LSICLK)$	Power consumption of LSICLK oscillator	-	-	0.56	$\mu A$
$t_{SU}(LSICLK)$	LSICLK oscillator startup time, ( $V_{DD}=3.3V$ , $T_A=-40\sim 105^{\circ}C$ )	-	-	74.8	$\mu s$

Note: It is obtained from a comprehensive evaluation and is not tested in production.

### 5.5.3. PLL Characteristics

Table 22 PLL Characteristics

Symbol	Parameter	Numerical Value			Unit
		Minimum value	Typical value	Maximum value	
$f_{PLL\_IN}$	PLL input clock	1	8	25	MHz
	PLL input clock duty cycle	40	-	60	%
$f_{PLL\_OUT}$	PLL frequency doubling output clock, ( $V_{DD}=3.3V$ , $T_A=-40\sim 105^{\circ}C$ )	16	-	120	MHz
$t_{LOCK}$	PLL phase locking time	-	-	200	$\mu s$

Note: It is obtained from a comprehensive evaluation and is not tested in production.

## 5.6. Reset and power management

### 5.6.1. Test of embedded reset and power control block characteristics

Table 23 Embedded Reset and Power Control Block Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
$V_{POR/PDR}$	Power-on/power-down reset threshold	Falling edge	1.84	1.86	1.88	V
		Rising edge	1.90	1.92	1.93	V
$V_{PDRhyst}$	PDR hysteresis	-	50.00	54.00	60.00	mV
$T_{RSTTEMPO}$	Reset duration	-	0.90	1.39	4.90	ms

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Table 24 Programmable Power Supply Voltage Detector Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
$V_{PVD}$	Programmable power supply voltage detector	PLS[2:0]=000 (rising edge)	2.17	-	2.20	V
		PLS[2:0]=000 (falling edge)	2.06	-	2.10	V
		PLS[2:0]=000(PVD hysteresis)	100	-	110	mV
		PLS[2:0]=001 (rising edge)	2.27	-	2.30	V

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
	voltage level selection	PLS[2:0]=001 (falling edge)	2.16	-	2.19	V
		PLS[2:0]=001(PVD hysteresis)	110	-	120	mV
		PLS[2:0]=010 (rising edge)	2.37	-	2.40	V
		PLS[2:0]=010 (falling edge)	2.26	-	2.29	V
		PLS[2:0]=010(PVD hysteresis)	100	-	110	mV
		PLS[2:0]=011 (rising edge)	2.46	-	2.50	V
		PLS[2:0]=011 (falling edge)	2.36	-	2.39	V
		PLS[2:0]=011(PVD hysteresis)	100	-	110	mV
		PLS[2:0]=100 (rising edge)	2.57	-	2.60	V
		PLS[2:0]=100 (falling edge)	2.45	-	2.49	V
		PLS[2:0]=100(PVD hysteresis)	110	-	120	mV
		PLS[2:0]=101 (rising edge)	2.66	-	2.70	V
		PLS[2:0]=101 (falling edge)	2.56	-	2.59	V
		PLS[2:0]=101(PVD hysteresis)	100	-	110	mV
		PLS[2:0]=110 (rising edge)	2.76	-	2.80	V
		PLS[2:0]=110 (falling edge)	2.65	-	2.69	V
		PLS[2:0]=110(PVD hysteresis)	110	-	110	mV
		PLS[2:0]=111 (rising edge)	2.87	-	2.91	V
		PLS[2:0]=111 (falling edge)	2.75	-	2.79	V
PLS[2:0]=111(PVD hysteresis)	110	-	120	mV		

Note: It is obtained from a comprehensive evaluation and is not tested in production.

## 5.7. Power consumption

### 5.7.1. Power consumption test environment

- (1) The values are measured by executing Dhrystone 2.1, with the Keil.V5 compilation environment and the L0 compilation optimization level.
- (2) All I/O pins are in input mode with a static value at  $V_{DD}$  or  $V_{SS}$  (no load)
- (3) Unless otherwise specified, all peripherals are turned off
- (4) The relationship between Flash waiting cycle setting and  $f_{HCLK}$  :
  - 0~24MHz: 0 waiting cycle
  - 24~48MHz: 1 waiting cycle
  - 48~72MHz: 2 waiting cycles
  - 72~96MHz: 3 waiting cycles
  - 96~120MHz: 4 waiting cycles

- (5) The instruction prefetch function is enabled (Note: it must be set before clock setting and bus frequency division)
- (6) When the peripherals are enabled:  $f_{PCLK1}=f_{HCLK}/2$ ,  $f_{PCLK2}=f_{HCLK}$

## 5.7.2. Power consumption in run mode

Table 25 Power Consumption in Run Mode when the Program is Executed in Flash

Parameter	Conditions	f <sub>HCLK</sub>	Typical value <sup>(1)</sup>		Maximum value <sup>(1)</sup>	
			T <sub>A</sub> =25°C, V <sub>DD</sub> =3.3V		T <sub>A</sub> =105°C, V <sub>DD</sub> =3.6V	
			I <sub>DDA</sub> (μA)	I <sub>DD</sub> (mA)	I <sub>DDA</sub> (μA)	I <sub>DD</sub> (mA)
Power consumption in run mode	HSECLK bypass <sup>(2)</sup> , enabling all peripherals	96MHz	218.17	20.90	257.25	22.75
		72MHz	152.43	15.01	183.55	16.77
		48MHz	121.33	12.42	148.55	14.07
		36MHz	98.50	9.43	120.42	11.23
		24MHz	121.30	6.93	144.77	8.34
		16MHz	91.31	4.83	111.79	6.37
		8MHz	17.84	2.78	27.24	4.31
	HSECLK bypass <sup>(2)</sup> , turning off all peripherals	96MHz	217.99	11.61	253.19	12.85
		72MHz	152.30	8.93	179.31	10.31
		48MHz	121.29	7.70	144.81	9.00
		36MHz	98.48	5.94	119.48	7.32
		24MHz	121.24	4.53	144.81	5.85
		16MHz	91.24	3.26	111.79	4.56
		8MHz	17.84	1.98	26.08	3.30
	HSICLK <sup>(2)</sup> , enabling all peripherals	64MHz	237.41	15.13	274.23	16.00
		48MHz	206.64	11.06	241.56	12.85
		36MHz	184.46	8.96	218.40	10.49
		24MHz	163.22	6.47	197.36	7.99
		16MHz	177.22	4.53	210.87	6.22
		8MHz	102.67	2.43	131.44	3.98
	HSICLK <sup>(2)</sup> , turning off all peripherals	64MHz	237.26	8.30	272.66	9.93
		48MHz	206.69	6.48	240.48	8.09
		36MHz	184.47	5.51	217.58	6.78
		24MHz	163.15	4.10	196.21	5.33
16MHz		177.19	2.91	210.01	4.56	
8MHz		102.67	1.61	131.14	3.46	

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

(2) The external clock is 8MHz, and when f<sub>HCLK</sub>>8MHz, turn on PLL, otherwise, turn off PLL.

Table 26 Power Consumption in Run Mode when the Program is Executed in RAM

Parameter	Conditions	f <sub>HCLK</sub>	Typical value <sup>(1)</sup>		Maximum value <sup>(1)</sup>	
			T <sub>A</sub> =25°C, V <sub>DD</sub> =3.3V		T <sub>A</sub> =105°C, V <sub>DD</sub> =3.6V	
			I <sub>DDA</sub> (μA)	I <sub>DD</sub> (mA)	I <sub>DDA</sub> (μA)	I <sub>DD</sub> (mA)
Power consumption in run mode	HSECLK bypass <sup>(2)</sup> , enabling all peripherals	96MHz	218.11	18.82	254.07	19.78
		72MHz	168.27	14.51	198.01	15.31
		48MHz	121.38	10.23	145.28	11.22
		36MHz	98.49	7.91	119.64	8.85
		24MHz	121.37	5.75	145.12	6.69
		16MHz	91.32	4.23	111.49	5.54
		8MHz	17.85	2.22	26.07	3.37
	HSECLK bypass <sup>(2)</sup> , turning off all peripherals	96MHz	218.15	12.98	253.06	13.84
		72MHz	168.21	10.19	197.29	10.91
		48MHz	121.37	7.19	144.47	8.23
		36MHz	98.45	5.76	119.07	6.70
		24MHz	121.38	4.27	144.40	5.33
		16MHz	91.31	3.28	111.54	4.37
		8MHz	17.84	2.23	25.98	3.37
	HSICLK <sup>(2)</sup> , enabling all peripherals	64MHz	237.31	13.98	272.39	15.31
		48MHz	206.81	10.51	239.84	12.06
		36MHz	184.48	8.14	216.88	9.59
		24MHz	163.22	5.41	195.99	6.97
		16MHz	177.24	3.61	209.78	5.25
		8MHz	102.72	1.89	130.84	3.45
	HSICLK <sup>(2)</sup> , turning off all peripherals	64MHz	237.31	7.79	272.15	9.41
		48MHz	206.70	5.97	239.51	7.38
		36MHz	184.51	4.29	216.97	6.33
		24MHz	163.17	2.96	196.29	4.53
16MHz		177.19	2.06	209.49	3.79	
8MHz		102.68	1.10	130.88	2.92	

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

(2) The external clock is 8MHz, and when f<sub>HCLK</sub>>8MHz, turn on PLL, otherwise, turn off PLL.

### 5.7.3. Power consumption in sleep mode

Table 27 Power Consumption in Sleep Mode when the Program is Executed in Flash

Parameter	Conditions	f <sub>HCLK</sub>	Typical value <sup>(1)</sup>		Maximum value <sup>(1)</sup>	
			T <sub>A</sub> =25°C, V <sub>DD</sub> =3.3V		T <sub>A</sub> =105°C, V <sub>DD</sub> =3.6V	
			I <sub>DDA</sub> (μA)	I <sub>DD</sub> (mA)	I <sub>DDA</sub> (μA)	I <sub>DD</sub> (mA)
Power consumption in sleep mode	HSECLK bypass <sup>(2)</sup> , enabling all peripherals	96 MHz	218.32	14.26	254.68	15.10
		72MHz	152.47	9.76	180.70	10.58
		48MHz	121.43	7.47	145.37	8.33
		36MHz	98.48	5.80	119.78	6.79
		24MHz	121.32	4.11	145.35	5.03
		16MHz	91.28	2.94	112.16	3.97
		8MHz	17.84	1.70	25.92	2.69
	HSECLK bypass <sup>(2)</sup> , turning off all peripherals	96 MHz	217.98	3.23	254.24	4.08
		72MHz	152.21	2.35	180.39	3.29
		48MHz	121.22	1.92	146.02	2.87
		36MHz	98.38	1.59	119.88	2.58
		24MHz	121.23	1.27	145.50	2.28
		16MHz	91.20	1.05	112.22	2.04
		8MHz	17.81	0.78	25.89	1.75
	HSICLK <sup>(2)</sup> , enabling all peripherals	64MHz	237.16	9.60	265.57	9.76
		48MHz	206.68	6.92	232.79	7.61
		36MHz	184.45	5.30	209.44	5.83
		24MHz	163.15	3.65	187.49	4.21
		16MHz	177.10	2.53	201.95	3.10
		8MHz	102.66	1.32	122.81	1.93
	HSICLK <sup>(2)</sup> , turning off all peripherals	64MHz	237.18	1.90	266.22	2.52
		48MHz	206.62	1.48	233.01	2.10
		36MHz	184.34	1.17	209.43	1.79
		24MHz	163.05	0.84	187.62	1.50
16MHz		177.13	0.62	202.01	1.27	
8MHz		102.67	0.35	122.81	1.02	

Table 28 Power Consumption in Sleep Mode when the Program is Executed in RAM

Parameter	Conditions	f <sub>HCLK</sub>	Typical value <sup>(1)</sup>		Maximum value <sup>(1)</sup>	
			T <sub>A</sub> =25°C, V <sub>DD</sub> =3.3V		T <sub>A</sub> =105°C, V <sub>DD</sub> =3.6V	
			I <sub>DDA</sub> (μA)	I <sub>DD</sub> (mA)	I <sub>DDA</sub> (μA)	I <sub>DD</sub> (mA)
Power consumption in sleep mode	HSECLK bypass <sup>(2)</sup> , enabling all peripherals	96MHz	215.97	14.06	250.92	15.59
		72MHz	165.85	10.84	196.02	10.74
		48MHz	119.17	7.44	142.13	7.71
		36MHz	96.50	5.77	117.08	5.84
		24MHz	119.21	3.93	136.05	4.35
		16MHz	89.36	2.77	109.38	3.14
		8MHz	17.73	1.6	23.65	2.01
	HSECLK bypass <sup>(2)</sup> , turning off all peripherals	96MHz	215.53	3.12	248.57	3.64
		72MHz	165.75	2.44	192.92	3.14
		48MHz	118.99	1.80	141.57	2.24
		36MHz	96.46	1.44	117.39	1.94
		24MHz	119.11	1.15	142.46	1.63
		16MHz	89.21	0.94	109.67	1.36
		8MHz	17.71	0.66	23.00	1.14
	HSICLK <sup>(2)</sup> , enabling all peripherals	64MHz	237.15	9.31	265.75	9.74
		48MHz	206.68	7.13	232.94	7.56
		36MHz	184.39	5.44	209.27	5.87
		24MHz	163.18	3.51	187.51	4.27
		16MHz	177.19	2.45	201.95	3.12
		8MHz	102.68	1.28	122.82	1.91
	HSICLK <sup>(2)</sup> , turning off all peripherals	64MHz	237.19	1.93	266.13	2.54
		48MHz	206.65	1.47	233.12	2.10
		36MHz	184.36	1.13	209.35	1.80
		24MHz	163.10	0.82	187.67	1.50
16MHz		177.13	0.62	202.00	1.29	
8MHz		102.60	0.36	122.86	1.03	

Note:

(1) It is obtained from a comprehensive evaluation and is not tested in production.

(2) The external clock is 8MHz, and when f<sub>HCLK</sub>>8MHz, turn on PLL, otherwise, turn off PLL



### 5.7.4. Power consumption in stop mode and standby mode

Table 29 Power Consumption in Stop Mode and Standby Mode

Parameter	Conditions	Typical value <sup>(1)</sup> , (T <sub>A</sub> =25°C)						Maximum value <sup>(1)</sup> , (V <sub>DD</sub> =3.6V)		Unit
		V <sub>DD</sub> =2.4V		V <sub>DD</sub> =3.3V		V <sub>DD</sub> =3.6V		T <sub>A</sub> =105°C		
		I <sub>DDA</sub>	I <sub>DD</sub>	I <sub>DDA</sub>	I <sub>DD</sub>	I <sub>DDA</sub>	I <sub>DD</sub>	I <sub>DDA</sub>	I <sub>DD</sub>	
Power consumption in stop mode	Regulator in run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF(no independent watchdog)	3.658	43.12	4.308	42.15	4.719	43.18	7.421	614.478	μA
	Regulator in low-power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF(no independent watchdog)	3.667	36.77	4.324	36.69	4.695	37.13	7.039	552.132	
Power consumption in standby mode	Low-speed internal RC oscillator and independent watchdog ON	2.911	0.47	3.85	1.01	4.342	1.31	5.937	5.468	
	Low-speed internal RC oscillator on, independent watchdog OFF	2.919	0.27	3.846	0.75	4.336	1.15	5.918	4.587	
	Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	2.346	0.05	2.964	0.17	3.343	0.40	4.985	4.172	

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

### 5.7.5. Backup domain power consumption

Table 30 Backup Domain Power Consumption

Symbol	Conditions	Typical value <sup>(1)</sup> , T <sub>A</sub> =25°C			Maximum value <sup>(1)</sup> , V <sub>BAT</sub> =3.6V			Unit
		V <sub>BAT</sub> =2.0V	V <sub>BAT</sub> =2.4V	V <sub>BAT</sub> =3.3V	T <sub>A</sub> =25°C	T <sub>A</sub> =85°C	T <sub>A</sub> =105°C	
I <sub>DD_VBAT</sub>	The low-speed oscillator and RTC are in ON state	1.106	1.268	1.704	1.956	2.568	3.256	μA

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

### 5.7.6. Peripheral power consumption

The HSECLK Bypass 1M is adopted as clock source, f<sub>PCLK</sub>=f<sub>HCLK</sub>=1M.

Peripheral power consumption = current that enables the peripheral clock-current that disables the peripheral clock.

Table 31 Peripheral Power Consumption

Parameter	Peripheral	Typical value <sup>(1)</sup> T <sub>A</sub> =25°C, V <sub>DD</sub> =3.3V	Unit
AHB	DMA1	0.3	mA
	DMA2	0.34	
	EMMC	0.31	

Parameter	Peripheral	Typical value <sup>(1)</sup> T <sub>A</sub> =25°C, V <sub>DD</sub> =3.3V	Unit
	CRC	0.14	
	SDIO	0.52	
APB1	TMR2	0.25	
	TMR3	0.24	
	TMR4	0.4	
	TMR5	0.36	
	TMR6	0.06	
	TMR7	0.08	
	WWDT	0.04	
	IWDT	0.07	
	SPI2/I2S2	0.2	
	SPI3/I2S3	0.29	
	USART2	0.36	
	USART3	0.33	
	UART4	0.16	
	UART5	0.2	
	I2C1	0.22	
	I2C2	0.18	
	USB	0.42	
	CAN1	0.25	
	CAN2	0.25	
	BAKPR	0.02	
PMU	0.02		
DAC	0.16		
APB2	GPIOA	0.13	
	GPIOB	0.13	
	GPIOC	0.07	
	GIOD	0.05	
	GPIOE	0.06	
	GPIOF	0.16	
	GPIOG	0.24	
	ADC1	0.39	
	ADC2	0.28	

Parameter	Peripheral	Typical value <sup>(1)</sup> T <sub>A</sub> =25°C, V <sub>DD</sub> =3.3V	Unit
	ADC3	0.28	
	TMR1	0.4	
	TMR8	0.4	
	SPI1	0.13	
	USART1	0.2	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

## 5.8. Wake-up time in low power mode

The measurement of wake-up time in low power mode is from the start of wake-up event to the time when the user program reads the first instruction, in which V<sub>DD</sub>=V<sub>DDA</sub>.

Table 32 Wake Up Time in Low-power Mode

Symbol	Parameter	Conditions	Min	Typical value (T <sub>A</sub> =25°C)			Max	Unit
				2V	3.3V	3.6V		
t <sub>WUSLEEP</sub>	Wake-up from sleep mode	-	0.52	0.61	0.60	0.57	0.65	μs
t <sub>WUSTOP</sub>	Wake up from stop mode	The voltage regulator is in run mode	1.83	2.24	1.91	1.86	2.26	
		The voltage regulator is in low power mode	2.66	4.18	2.95	2.82	4.61	
t <sub>WUSTDBY</sub>	Wake up from standby mode	-	59.56	76.40	63.74	61.29	84.56	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

## 5.9. Pin characteristics

### 5.9.1. I/O pin characteristics

Table 33 DC Characteristics (test condition of V<sub>DD</sub>=2.7~3.6V, T<sub>A</sub>=-40~105°C)

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
V <sub>IL</sub>	Low level input voltage	CMOS port	-0.5	-	0.35V <sub>DD</sub>	V
V <sub>IH</sub>	High level input voltage		0.65V <sub>DD</sub>	-	V <sub>DD</sub> +0.5	
V <sub>IL</sub>	Low level input voltage	TTL port	-0.5	-	0.8	
V <sub>IH</sub>	High level input voltage, Standard I/O port		2	-	V <sub>DD</sub> +0.5	
	High level input voltage, I/O FT port	2	-	5.5		
V <sub>hys</sub>	Standard I/O Schmitt trigger voltage hysteresis	-	200	-	-	mV
	I/O FT Schmitt trigger voltage hysteresis		5%V <sub>DD</sub>	-	-	mV
I <sub>lkg</sub>	Input leakage current	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>DD</sub> Standard I/O port	-	-	±1	μA

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
		$V_{IN}=5V$ , I/O FT port	-	-	3	
$R_{PU}$	Weak pull-up equivalent resistance	$V_{IN}=V_{SS}$	30	40	50	k $\Omega$
$R_{PD}$	Weak pull-down equivalent resistance	$V_{IN}=V_{DD}$	30	40	50	k $\Omega$

Note: It is obtained from a comprehensive evaluation and is not tested in production.

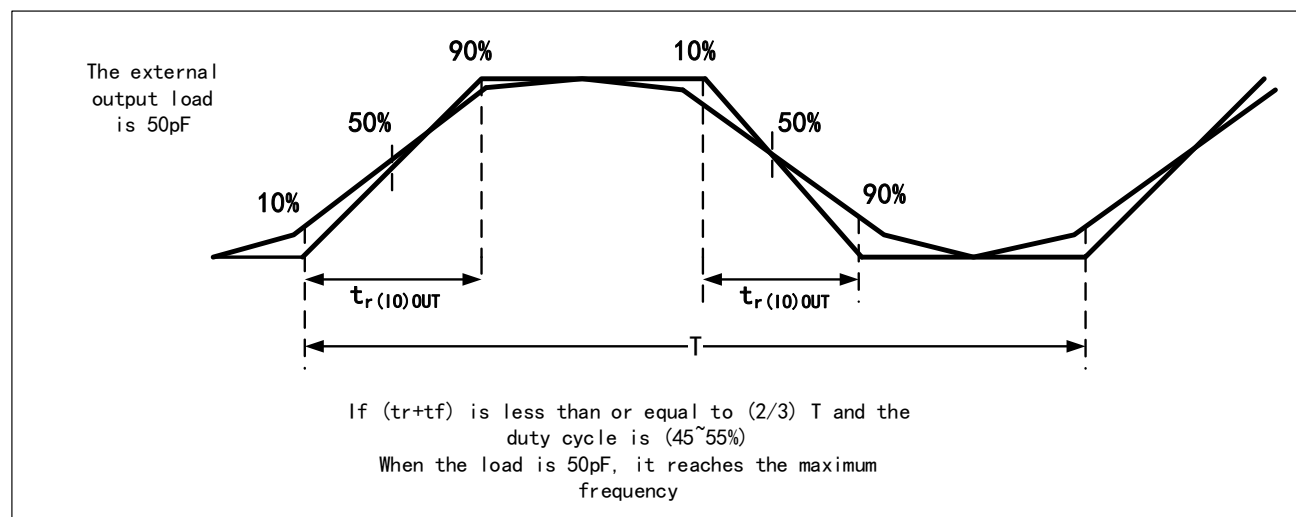
Table 34 AC Characteristics

MODEy[1:0] Configuration	Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
10 (2MHz)	fmax(IO)out	Maximum frequency	$CL=50\text{ pF}$ , $V_{DD}=2\sim3.6V$	-	2	MHz
	tf(IO)out	Output fall time from high to low level	$CL=50\text{ pF}$ , $V_{DD}=2\sim3.6V$	-	125	ns
	tr(IO)out	Output rise time from low to high level		-	125	
01 (10MHz)	fmax(IO)out	Maximum frequency	$CL=50\text{ pF}$ , $V_{DD}=2\sim3.6V$	-	10	MHz
	tf(IO)out	Output fall time from high to low level	$CL=50\text{ pF}$ , $V_{DD}=2\sim3.6V$	-	25	ns
	tr(IO)out	Output rise time from low to high level		-	25	
11 (50MHz)	fmax(IO)out	Maximum frequency	$CL=30\text{ pF}$ , $V_{DD}=2.7\sim3.6V$	-	50	MHz
	tf(IO)out	Output fall time from high to low level	$CL=30\text{ pF}$ , $V_{DD}=2.7\sim3.6V$	-	5	ns
	tr(IO)out	Output rise time from low to high level		-	5	

Note: (1) The rate of I/O port can be configured through MODEy.

(2) The data are obtained from a comprehensive evaluation and is not tested in production.

Figure 10 I/O AC Characteristics Definition



Note: It is obtained from a comprehensive evaluation and is not tested in production.

Table 35 Output Drive Current Characteristics (test condition  $V_{DD}=2.7\sim3.6V$ ,  $T_A=-40\sim105^\circ C$ )

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
$V_{OL}$	Output low level voltage for an I/O pin when 8 pins are sunk at same time	$I_{IO} = +8mA$ $2.7V < V_{DD} < 3.6V$	-	0.49	V

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
V <sub>OH</sub>	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V <sub>DD</sub> -0.4	-	
V <sub>OL</sub>	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I <sub>IO</sub> = +20mA 2.7V < V <sub>DD</sub> < 3.6V	-	1.50	V
V <sub>OH</sub>	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V <sub>DD</sub> -1.2	-	

### 5.9.2. NRST pin characteristics

The NRST pin input drive adopts CMOS process, which is connected with a permanent pull-up resistor R<sub>PU</sub>.

Table 36 NRST Pin Characteristics (test condition V<sub>DD</sub>=3.3V, T<sub>A</sub>=-40~105°C)

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
V <sub>IL(NRST)</sub>	NRST low level input voltage	-	-0.5	-	0.8	V
V <sub>IH(NRST)</sub>	NRST high level input voltage	-	2	-	V <sub>DD</sub> +0.5	
V <sub>hys(NRST)</sub>	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R <sub>PU</sub>	Weak pull-up equivalent resistance	V <sub>IN</sub> = V <sub>SS</sub>	30	40	50	kΩ

Note: It is obtained from a comprehensive evaluation and is not tested in production.

## 5.10. Communication peripherals

### 5.10.1. I2C peripheral characteristics

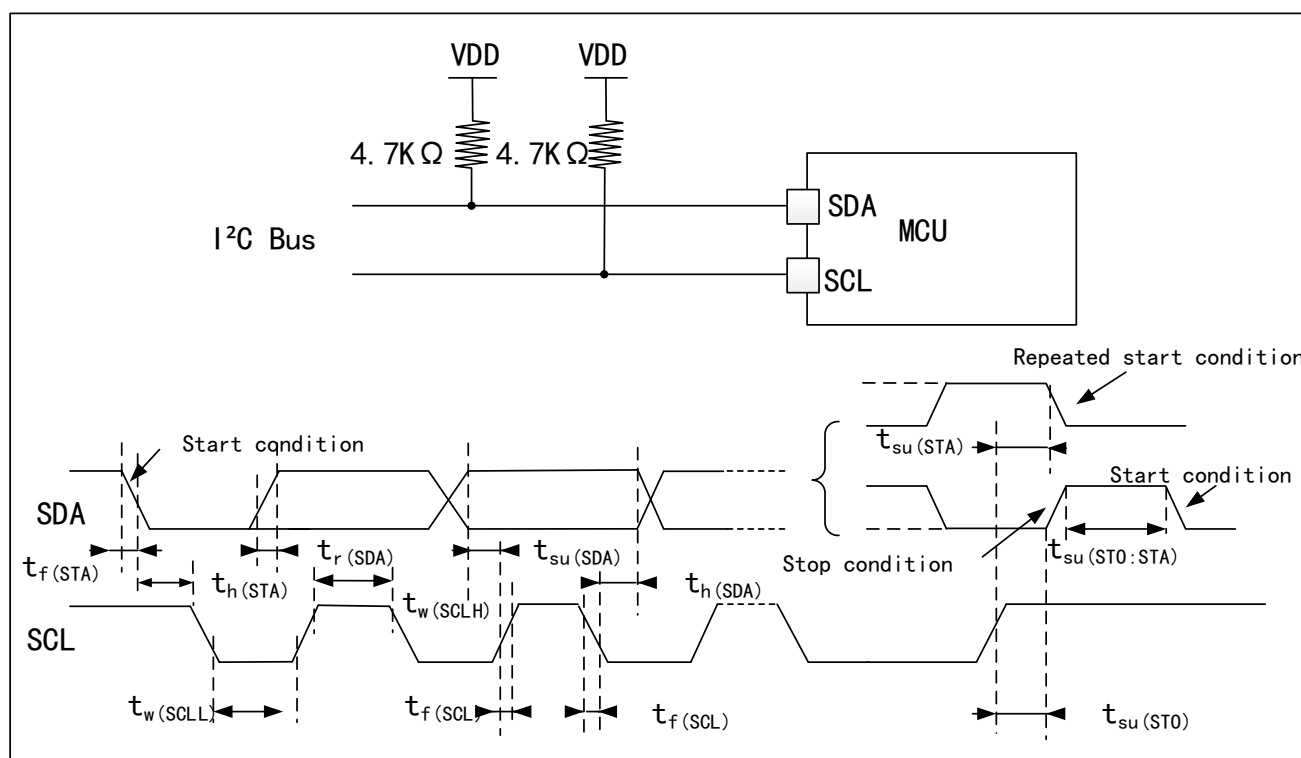
To achieve maximum frequency of I2C in standard mode, f<sub>PCLK1</sub> must be greater than 2MHz. To achieve maximum frequency of I2C in fast mode, f<sub>PCLK1</sub> must be greater than 4MHz.

Table 37 I2C Interface Characteristics (T<sub>A</sub>=25°C, V<sub>DD</sub>=3.3V)

Symbol	Parameter	Standard I2C		Fast I2C		Unit
		Min	Max	Min	Max	
t <sub>w(SCLL)</sub>	SCL clock low time	4.7	-	1.3	-	μs
t <sub>w(SCLH)</sub>	SCL clock high time	4.0	-	0.6	-	
t <sub>su(SDA)</sub>	SDA setup time	250	-	100	-	ns
t <sub>h(SDA)</sub>	SDA data hold time	-	3450	-	900	
t <sub>r(SDA)/t<sub>r(SCL)</sub></sub>	SDA and SCL rise time	-	1000	-	300	
t <sub>f(SDA)/t<sub>f(SCL)</sub></sub>	SDA and SCL fall time	-	300	-	300	
t <sub>h(STA)</sub>	Start condition hold time	4.0	-	0.6	-	μs
t <sub>su(STA)</sub>	Repeated start condition setup time	4.7	-	0.6	-	
t <sub>su(STO)</sub>	Setup time of stop condition	4.0	-	0.6	-	
t <sub>w(STO:STA)</sub>	Time from stop condition to start condition (bus idle)	4.7	-	1.3	-	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Figure 11 I2C Bus AC Waveform and Measurement Circuit



Note: The measuring points are set at CMOS levels:  $0.3V_{DD}$  and  $0.7V_{DD}$ .

### 5.10.2. SPI peripheral characteristics

Table 38 SPI Characteristics ( $T_A=25^\circ\text{C}$ ,  $V_{DD}=3.3\text{V}$ )

Symbol	Parameter	Conditions	Min	Max	Unit
$f_{SCK}$ $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SI clock rise and fall time	Load capacitance: $C = 30\text{pF}$	-	8	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	$4t_{PCLK}$	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	$2t_{PCLK}$	-	ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Main mode, $f_{PCLK} = 36\text{MHz}$ , Prescaler coefficient=4	50	60	ns
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	5	-	ns
		Slave mode	5	-	
$t_{h(MI)}$ $t_{h(SI)}$	Data input hold time	Master mode	5	-	ns
		Slave mode	4	-	
$t_{a(SO)}$	Data output access time	Slave mode, $f_{PCLK} = 20\text{MHz}$	0	$3t_{PCLK}$	ns
$t_{dis(SO)}$	Data output prohibition time	Slave mode	2	10	ns
$t_{v(SO)}$	Effective time of data output	Slave mode (after enable edge)	-	25	ns

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{v(MO)}$	Effective time of data output	Master mode (after enable edge)	-	5	ns
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge)	15	-	ns
$t_{h(MO)}$		Master mode (after enable edge)	2	-	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Figure 12 SPI Timing Diagram - Slave Mode and CPHA=0

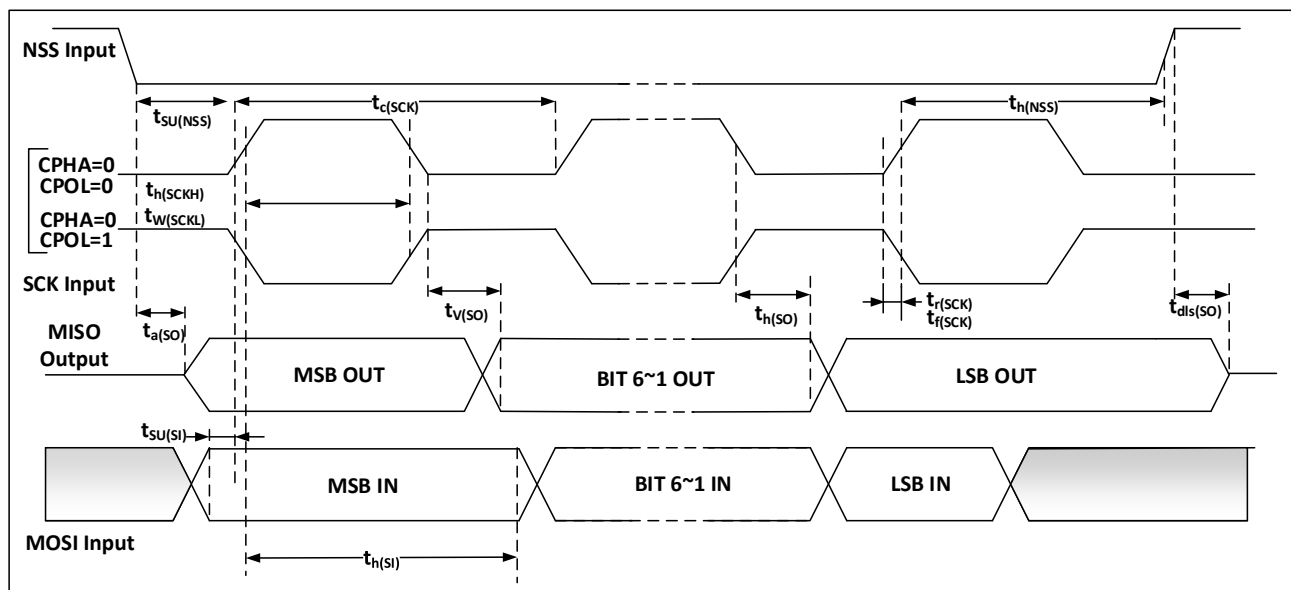
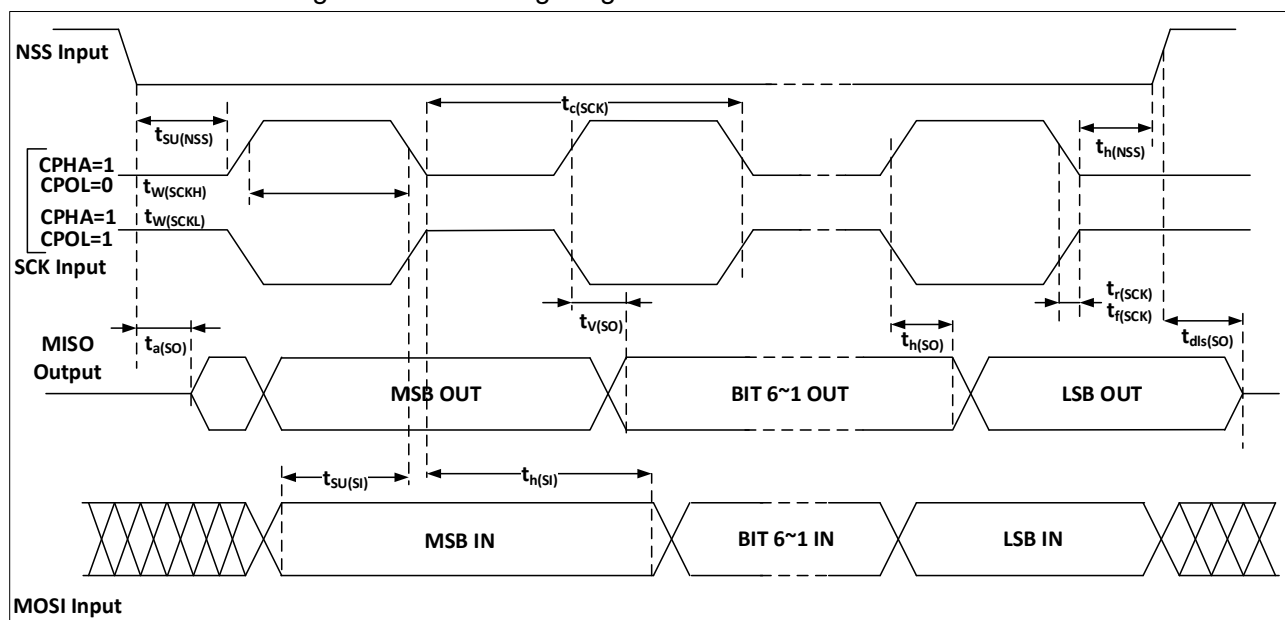
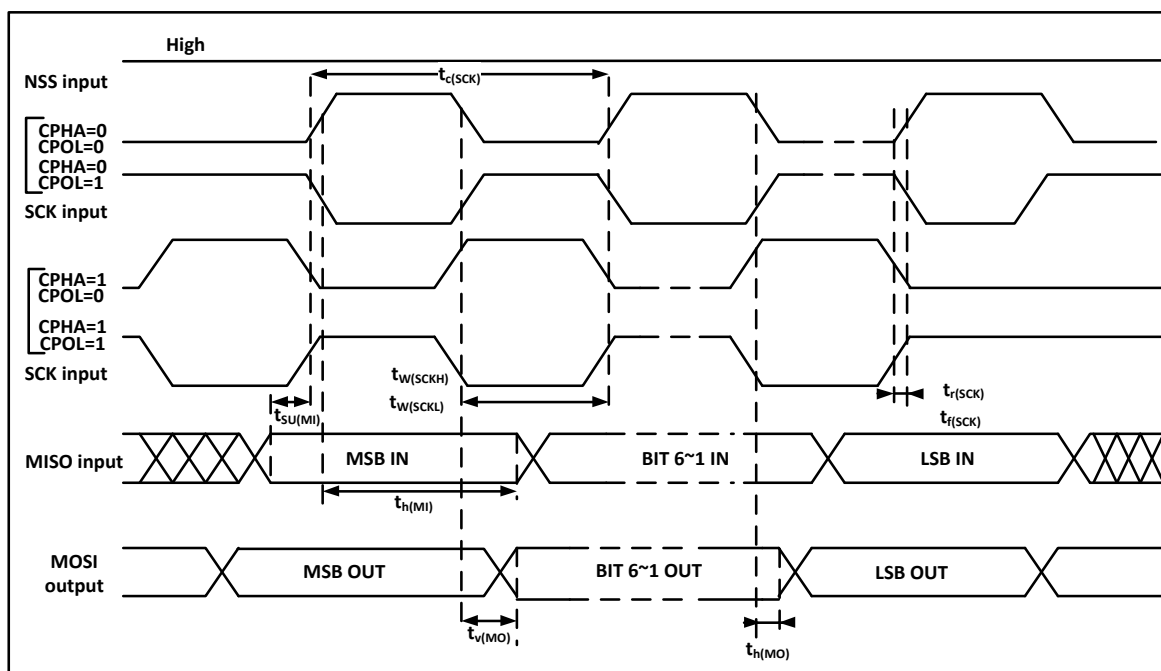


Figure 13 SPI Timing Diagram - Slave Mode and CPHA=1



Note: The measuring points are set at CMOS levels:  $0.3V_{DD}$  and  $0.7V_{DD}$ .

Figure 14 SPI Timing Diagram - Master Mode



Note: The measuring points are set at CMOS levels:  $0.3V_{DD}$  and  $0.7V_{DD}$ .

## 5.11. Analog peripherals

### 5.11.1. ADC

Test parameter description:

- Sampling rate: the number of conversion of analog quantity to digital quantity by ADC per second  

$$\text{Sample rate} = \text{ADC clock} / (\text{number of sampling periods} + \text{number of conversion periods})$$

#### 5.11.1.1. 12-bit ADC characteristics

Table 3912-bit ADC Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
$V_{DDA}$	Power supply voltage	-	2.4	-	3.6	V
$I_{DDA}$	ADC power consumption	$V_{DDA}=3.3V$ , $f_{ADC}=14MHz$ , Sampling time= $1.5 f_{ADC}$	-	1	-	mA
$f_{ADC}$	ADC frequency	-	0.6	-	14	MHz
$C_{ADC}$	Internal sampling and holding capacitance	-	-	8	-	pF
$R_{ADC}$	Sampling resistor	-	-	-	1000	$\Omega$
$t_s$	Sample Time	$f_{ADC}=14MHz$	0.107	-	17.1	$\mu s$
$T_{CONV}$	Sampling and conversion time	$f_{ADC}=14MHz$ , 12-bit conversion	1	-	18	$\mu s$



Table 4012-bit ADC Accuracy

Symbol	Parameter	Condition	Typical value	Maximum value	Unit
$E_T$	Total uncorrected error	$f_{PCLK}=56\text{MHz}$ , $f_{ADC}=14\text{MHz}$ , $V_{DDA}=2.4\text{V}-3.6\text{V}$ $T_A=-40^\circ\text{C}\sim 105^\circ\text{C}$	$\pm 2$	$\pm 5$	LSB
$E_O$	offset error		$\pm 1.5$	$\pm 2.5$	
$E_G$	Gain error		$\pm 1.5$	$\pm 3$	
$E_D$	Differential linear error		$\pm 1$	$\pm 2$	
$E_L$	Integral linearity error		$\pm 1.5$	$\pm 3$	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

### 5.11.1.2. Test of Built-in Reference Voltage Characteristics

Table 41 Embedded Reference Voltage Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
$V_{REFINT}$	Built-in Reference Voltage	$-40^\circ\text{C} < T_A < +105^\circ\text{C}$ $V_{DD}= 2-3.6\text{V}$	1.1882	1.1947	1.2002	V
$T_{S\_vrefint}$	Sampling time of ADC when reading out internal reference voltage	-	-	5.1	17.1	$\mu\text{s}$
$V_{RERINT}$	Built-in reference voltage extends to temperature range	$V_{DD}=3\text{V} \pm 10\text{mV}$	-	-	18	mV
$T_{coeff}$	Temperature coefficient	-	-	-	104	ppm/ $^\circ\text{C}$

Note: It is obtained from a comprehensive evaluation and is not tested in production.

### 5.11.2. DAC

Test parameter description:

- DNL differential non-linear error: the deviation between two consecutive codes is-1 LSB
- INL integral non-linear error: the difference between the measured value at code i and the value at code i on the connection between code 0 and the last code 4095

Table 42 DAC Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
$V_{DDA}$	Analog power supply voltage	-	2.4	-	3.6	V
$R_{LOAD}$	Resistive load	Load is connected to VSSA with buffer on	5	-	-	k $\Omega$
$R_O$	Output impedance	The resistive load between DAC_OUT and VSS is 1.5M $\Omega$ with buffer off	-	-	15	k $\Omega$

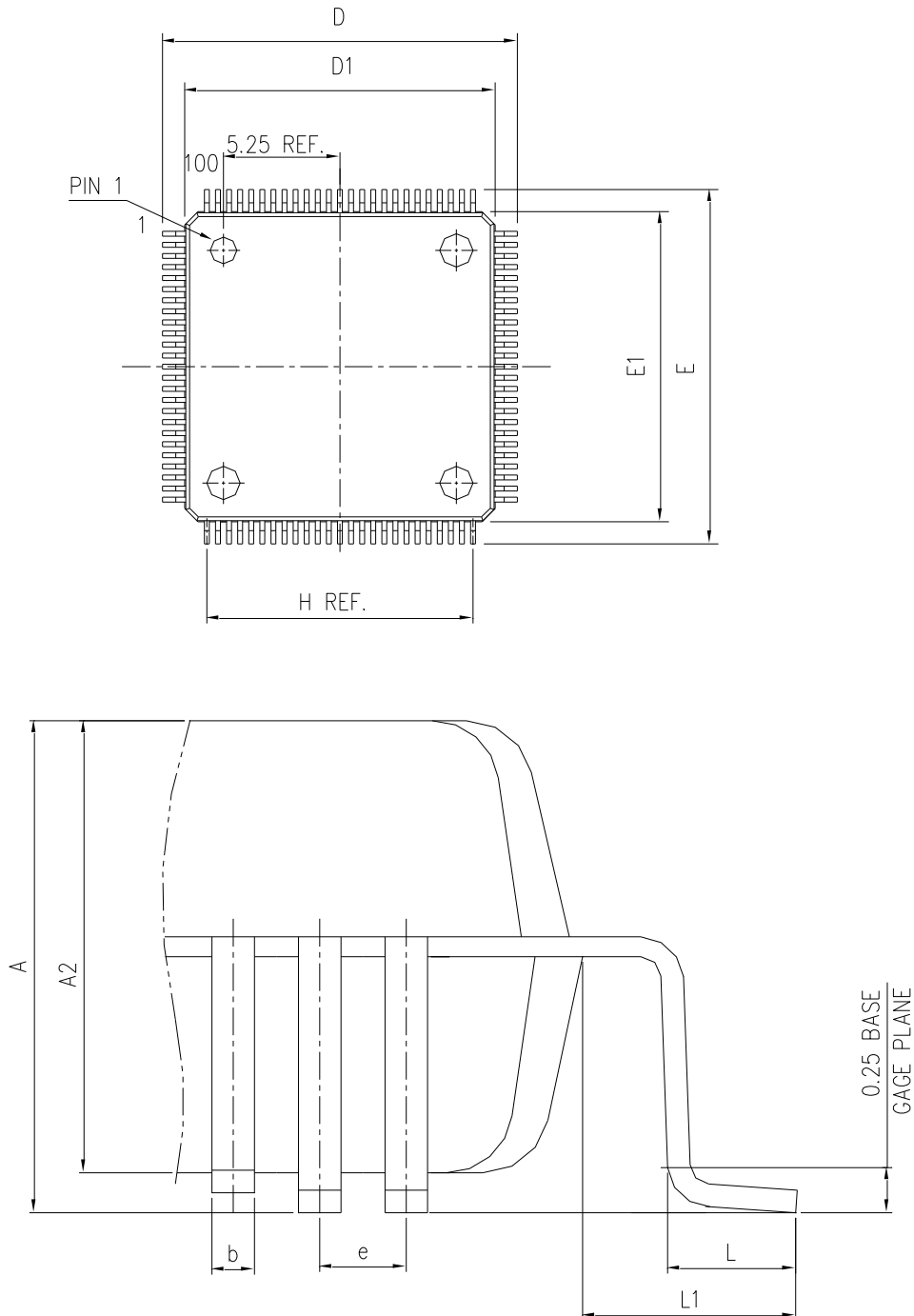
Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
C <sub>LOAD</sub>	Capacitive load	Maximum capacitive load at DAC_OUT pin with buffer on	-	-	50	pF
DAC_OUT min	Low DAC_OUT voltage with buffer	Maximum output offset of DAC, (0x0E1) corresponding to 12-bit input code to V <sub>REF+</sub> = (0xF1B) at 3.6V and V <sub>REF+</sub> = (0x154) at 2.4V and (0xEAC)	0.39	-	1.94	V
DAC_OUT max	High output voltage with buffer		-10.84	-	4.66	V
DNL	Differential non-linear error	Configured with 12-bit DAC	-1.03	-	0.79	LSB
INL	Integral non-linear error	Configured with 12-bit DAC	-3.86	-	2.46	LSB
Offset	Offset error	V <sub>REF+</sub> =3.6V, configuring 12-bit DAC	-2.57	-	9.49	LSB
Gain error	Gain error	Configured with 12-bit DAC	-0.0013	-	0.0045	%

Note: It is obtained from a comprehensive evaluation and is not tested in production.

## 6. Package information

### 6.1. LQFP100 package diagram

Figure 15 LQFP100 Package Diagram



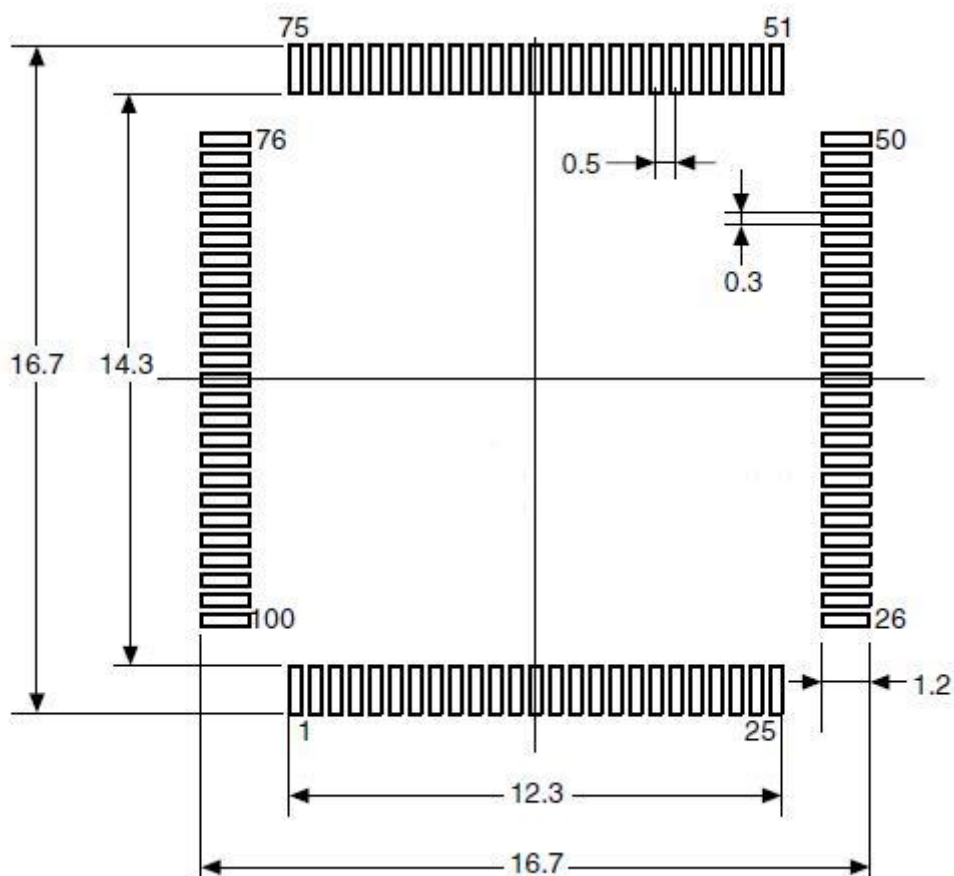
- (1) The figure is not drawn to scale.
- (2) All pins should be soldered to the PCB

Table 43 LQFP100 Package Data

DIMENSION LIST (FOOTPRINT: 2.00)			
S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX. 1.600	OVERALL HEIGHT
2	A2	1.400±0.050	PKG THICKNESS
3	D	16.000±0.200	LEAD TIP TO TIP
4	D1	14.000±0.100	PKG LENGTH
5	E	16.000±0.200	LEAD TIP TO TIP
6	E1	14.000±0.100	PKG WPTH
7	L	0.600±0.150	FOOT LENGTH
8	L1	1.000 REF	LEAD LENGTH
9	e	0.500 BASE	LEAD PITCH
10	H (REF)	(12.00)	CUM LEAD PITCH
11	b	0.22±0.050	LEAD WIDTH

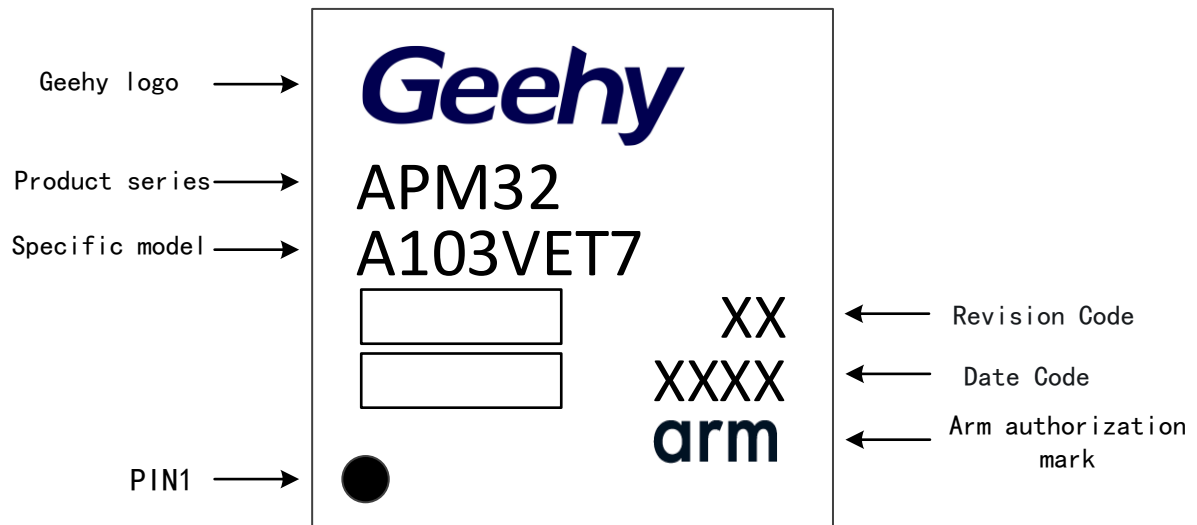
(1) Dimensions are displayed in mm

Figure 16 LQFP100-100 pins, 14×14mm recommended welding Layout



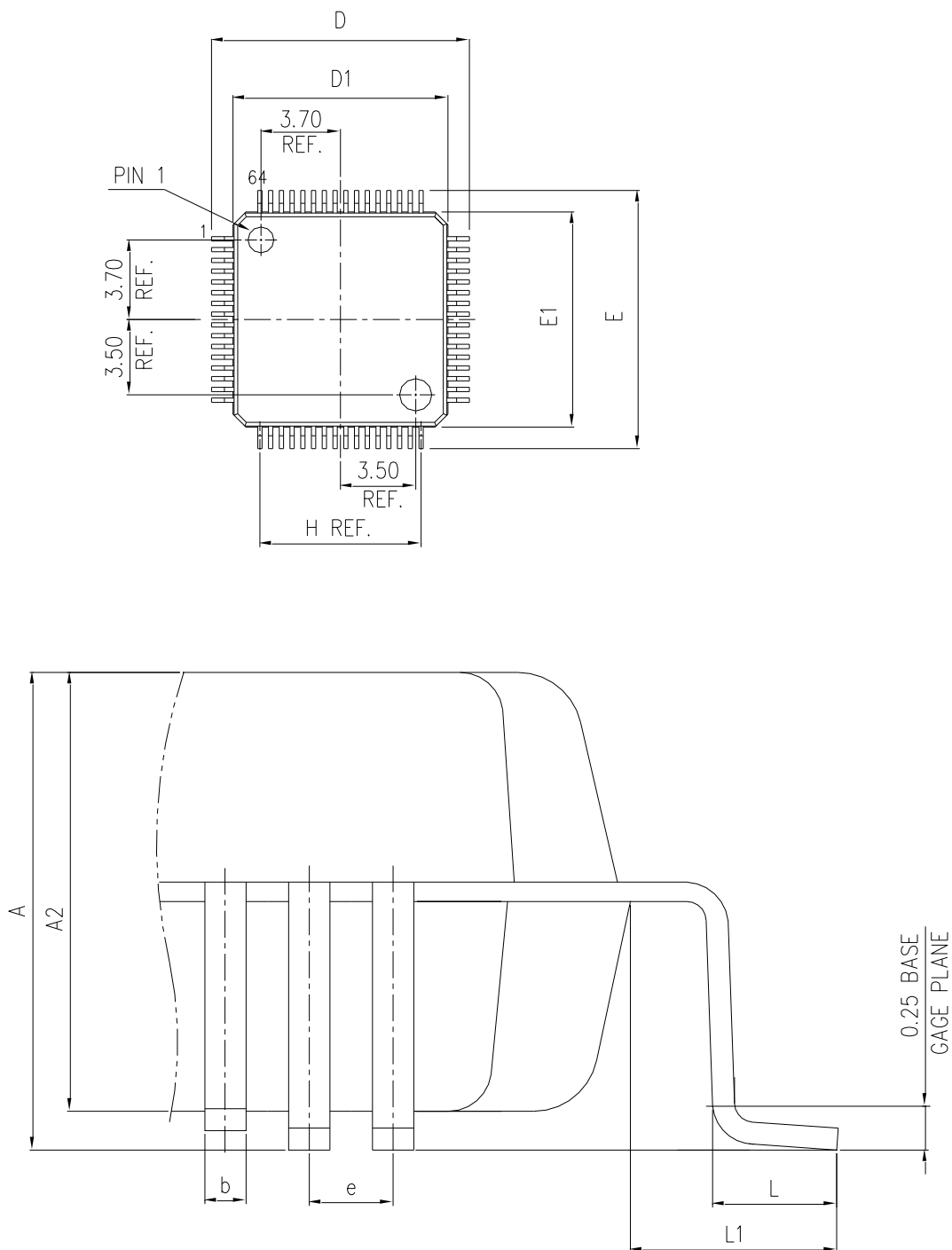
(1) Dimensions are expressed in mm

Figure 17 LQFP100-100 pins, 14×14mm package identification



## 6.2. LQFP64 package diagram

Figure 18 LQFP64 Package Diagram



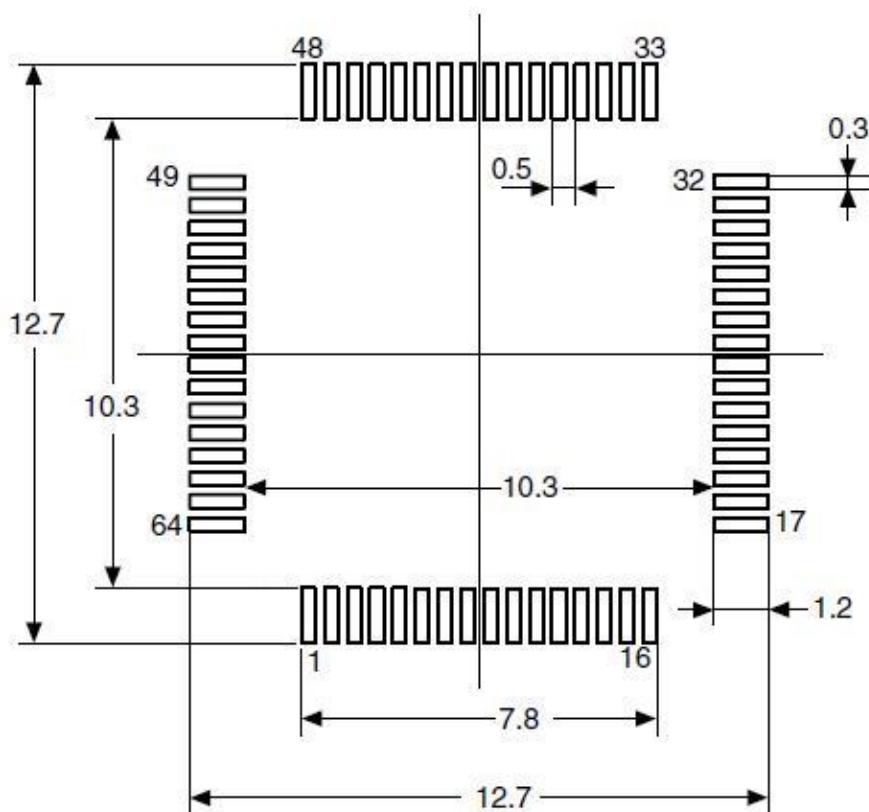
- (1) The figure is not drawn to scale.
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Table 44 LQFP64 Package Data

DIMENSION LIST (FOOTPRINT: 2.00)			
S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX. 1.600	OVERALL HEIGHT
2	A2	1.400±0.050	PKG THICKNESS
3	D	12.000±0.200	LEAD TIP TO TIP
4	D1	10.000±0.100	PKG LENGTH
5	E	12.000±0.200	LEAD TIP TO TIP
6	E1	10.000±0.100	PKG WPTH
7	L	0.600±0.150	FOOT LENGTH
8	L1	1.000 REF	LEAD LENGTH
9	e	0.500 BASE	LEAD PITCH
10	H (REF)	(7.500)	CUM LEAD PITCH
11	b	0.22±0.050	LEAD WIDTH

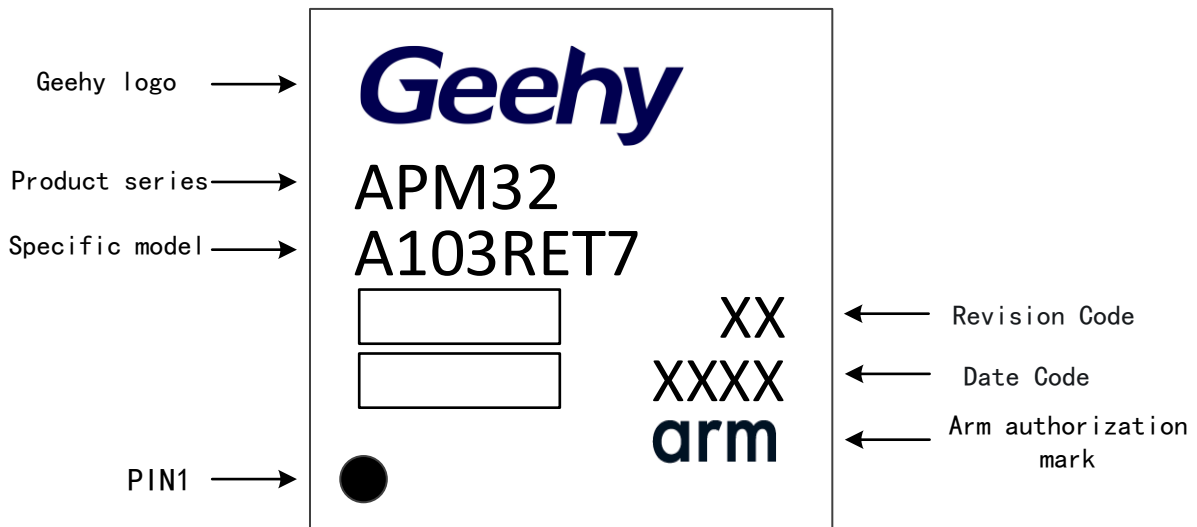
(1) Dimensions are expressed in mm

Figure 19 LQFP64-64 pins, 10×10mm recommended welding Layout



(2) Dimensions are expressed in mm

Figure 20 LQFP64-64 pins, 10×10mm package identification

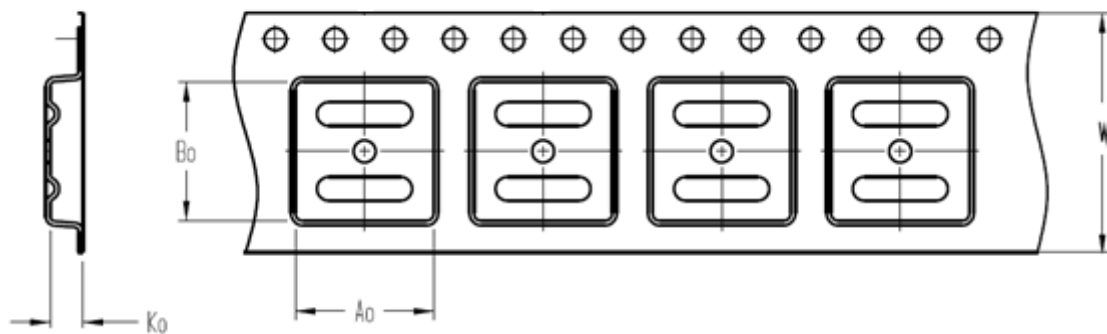




## 7. Packaging information

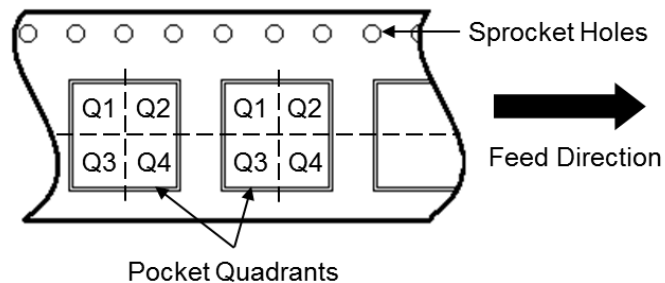
### 7.1. Reel packaging

Figure 21 Specification Drawing of Reel Packaging

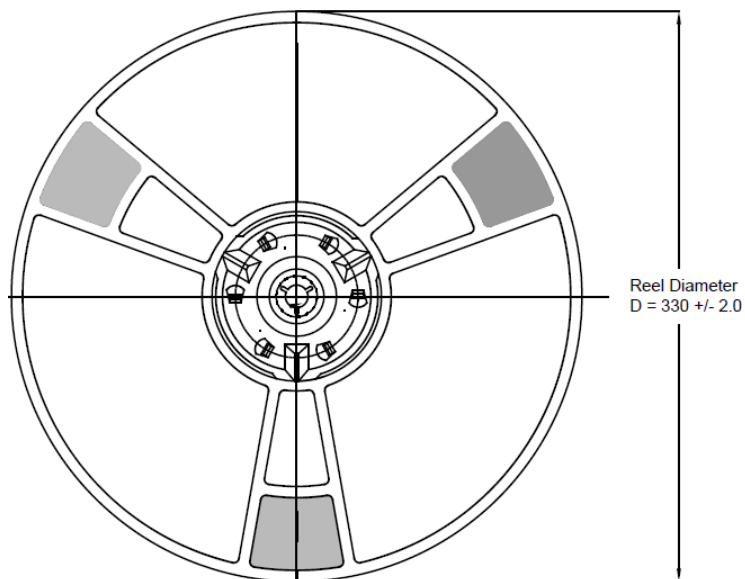


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape

#### Quadrant Assignments for PIN1 Orientation in Tape



Reel Dimensions



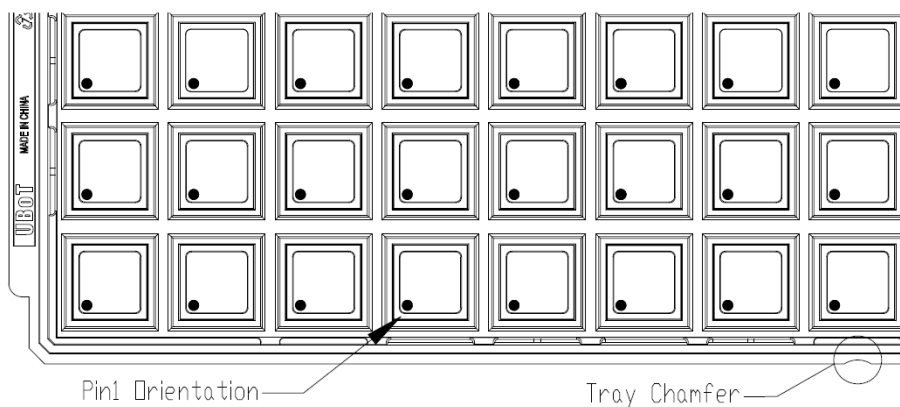
All photos are for reference only, and the appearance is subject to the product.

Table 45 Reel Packaging Parameter Specification Table

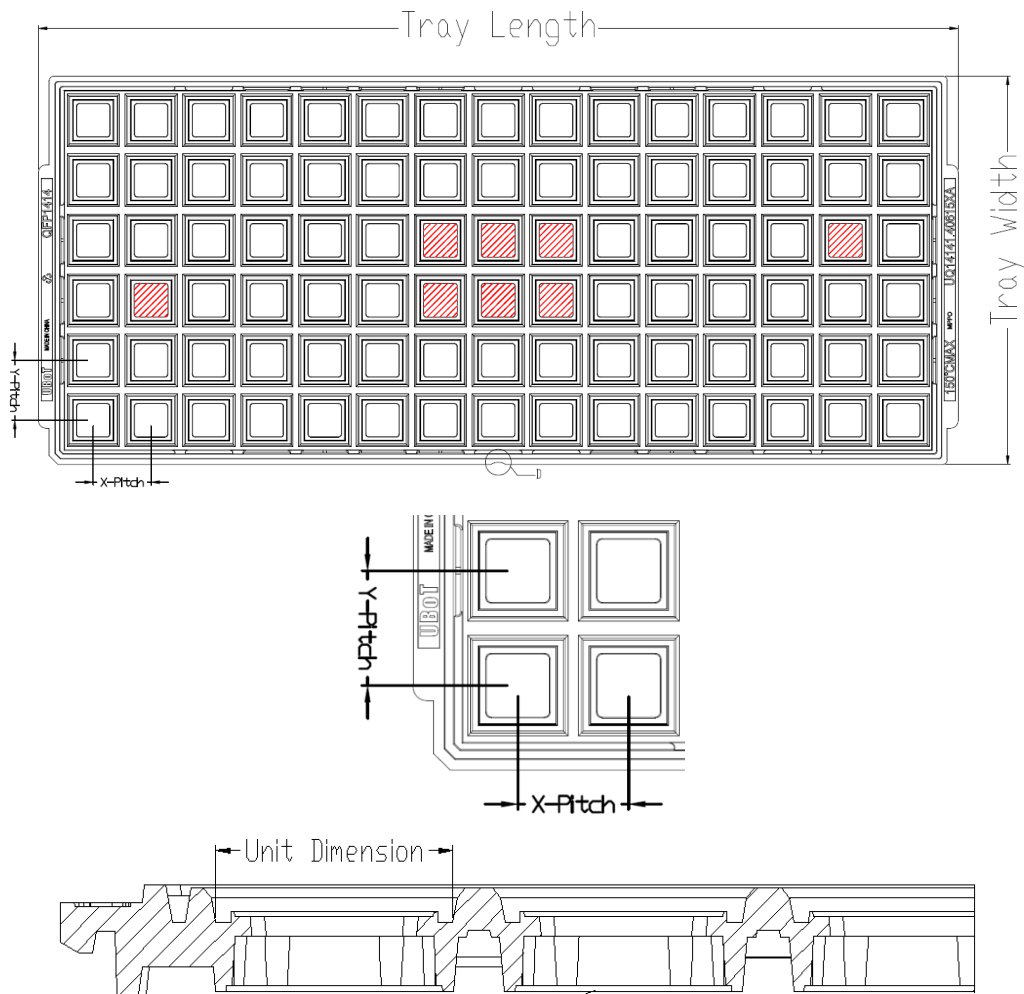
Device	Package Type	Pins	SPQ	Reel Diameter (mm)	A0 (mm)	B0 (mm)	K0 (mm)	W (mm)	Pin1 Quadrant
APM32A103RET7	LQFP	64	1000	330	12.35	12.35	2.2	24	Q1

## 7.2. Tray packaging

Figure 22 Tray Packaging Diagram



Tray Dimensions



All photos are for reference only, and the appearance is subject to the product.

Table 46 Tray Packaging Parameter Specification Table

Device	Package Type	Pins	SPQ	X-Dimension (mm)	Y-Dimension (mm)	X-Pitch (mm)	Y-Pitch (mm)	Tray Length (mm)	Tray Width (mm)
APM32A103VET7	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9
APM32A103RET7	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9

## 8. Ordering information

Figure 23 Product Naming Rules

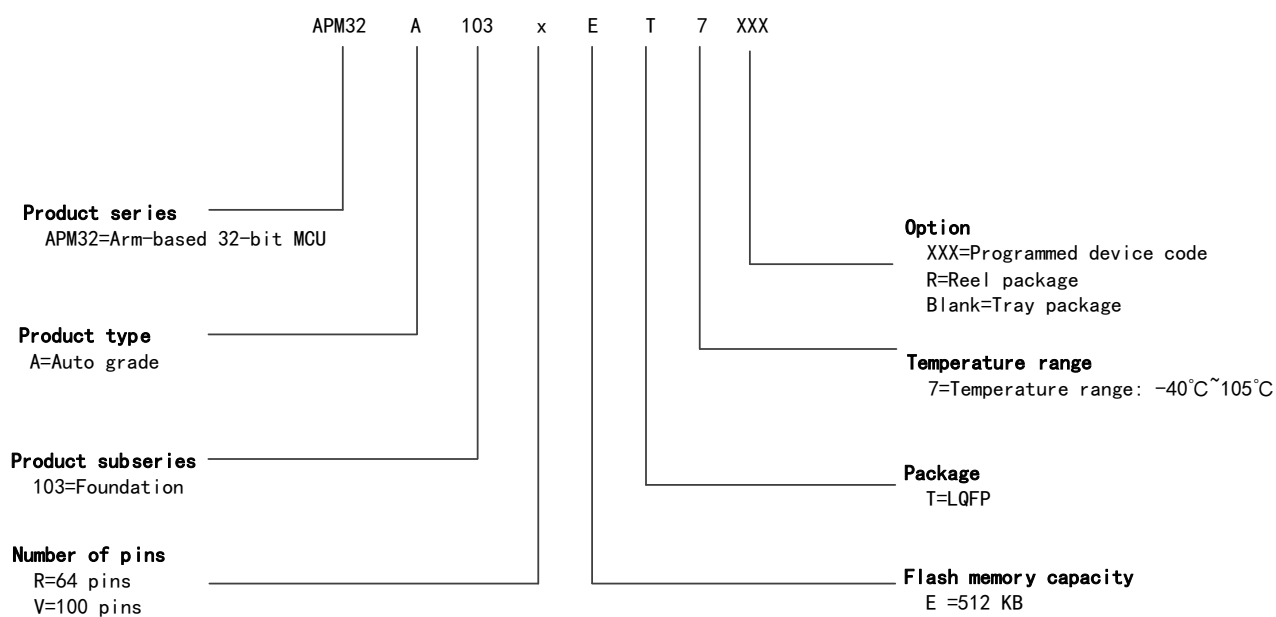


Table 47 Ordering Information Table

Order Code	Flash (KB)	SRAM (KB)	Package	SPQ	Temperature Range
APM32A103VET7	512	128	LQFP100	900	-40°C~105°C
APM32A103RET7	512	128	LQFP64	1600	-40°C~105°C
APM32A103RET7-R	512	128	LQFP64	1000	-40°C~105°C

Note :SPQ= Minimum number of package.

## 9. Commonly used function module denomination

Table 48 Commonly Used Function Module Denomination

Chinese description	Short name
Reset management unit	RMU
Clock management unit	CMU
Reset and clock management	RCM
External interrupt	EINT
Genera-purpose IO	GPIO
Multiplexing IO	AFIO
Wake up controller	WUPT
Buzzer	BUZZER
Independent watchdog timer	IWDT
Window watchdog timer	WWDT
Timer	TMR
CRC controller	CRC
Power Management Unit	PMU
DMA controller	DMA
Analog-to-digital converter	ADC
Real-time clock	RTC
External memory controller	EMMC
Controller local area network	CAN
I2C interface	I2C
Serial peripheral interface	SPI
Universal asynchronous transmitter receiver	UART
Universal synchronous and asynchronous transmitter receiver	USART
Flash interface control unit	FMC

## 10. Revision history

Table 49 Document Revision History

Date	Version	Change History
2022.12	1.0	New

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