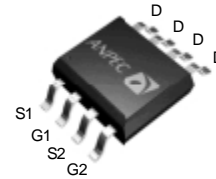


Dual Enhancement Mode MOSFET (N-and P-Channel)

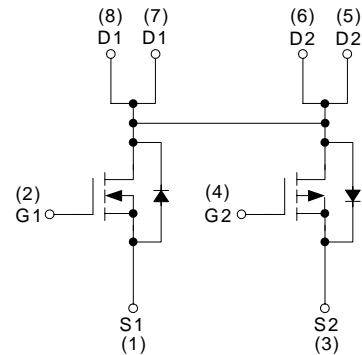
Features

- N-Channel
20V/9A,
 $R_{DS(ON)} = 12m\Omega(\text{typ.}) @ V_{GS} = 4.5V$
 $R_{DS(ON)} = 18m\Omega(\text{typ.}) @ V_{GS} = 2.5V$
- P-Channel
-20V/-6A,
 $R_{DS(ON)} = 30m\Omega(\text{typ.}) @ V_{GS} = -4.5V$
 $R_{DS(ON)} = 50m\Omega(\text{typ.}) @ V_{GS} = -2.5V$
- Super High Dense Cell Design
- Reliable and Rugged
- Lead Free Available (RoHS Compliant)

Pin Description



Top View of SOP – 8



N-P Channel MOSFET

Applications

- Power Management in Notebook Computer, Portable Equipment and Battery Powered Systems

Ordering and Marking Information

<p>APM9932C □□-□□□</p> <ul style="list-style-type: none"> □□□ : Lead Free Code □□ : Handling Code □ : Temp. Range □ : Package Code 	<p>Package Code K : SOP-8</p> <p>Operating Junction Temp. Range C : -55 to 150°C</p> <p>Handling Code TU : Tube TR : Tape & Reel</p> <p>Lead Free Code L : Lead Free Device Blank : Original Device</p>
<p>APM9932C K : APM9932C XXXXXX</p>	<p>XXXXXX - Date Code</p>

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte in plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldering operations. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	N Channel	P Channel	Unit
V_{DSS}	Drain-Source Voltage	20	-20	V
V_{GSS}	Gate-Source Voltage	± 16	± 12	
I_D^*	Continuous Drain Current	9	-6	A
I_{DM}^*	300 μs Pulsed Drain Current	30	-20	
I_S^*	Diode Continuous Forward Current	1.5	-1.2	A
T_J	Maximum Junction Temperature	150		$^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150		
P_D^*	Power Dissipation	$T_A=25^\circ\text{C}$	2	W
		$T_A=100^\circ\text{C}$	0.8	
$R_{\theta JA}^*$	Thermal Resistance-Junction to Ambient	62.5		$^\circ\text{C/W}$

Note:

*Surface Mounted on 1in² pad area, $t \leq 10\text{sec}$.

Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	APM9932CK			Unit	
			Min.	Typ.	Max.		
Static Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}, I_{DS}=250\mu\text{A}$	N-Ch	20		V	
		$V_{GS}=0\text{V}, I_{DS}=-250\mu\text{A}$	P-Ch	-20			
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=16\text{V}, V_{GS}=0\text{V}$	N-Ch		1	μA	
		$V_{DS}=-16\text{V}, V_{GS}=0\text{V}$	P-Ch		-1		
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_{DS}=250\mu\text{A}$	N-Ch	0.55	0.7	1.5	V
		$V_{DS}=V_{GS}, I_{DS}=-250\mu\text{A}$	P-Ch	-0.45	-0.6	-1	
I_{GSS}	Gate Leakage Current	$V_{GS}=\pm 16\text{V}, V_{DS}=0\text{V}$	N-Ch			± 100	nA
		$V_{GS}=\pm 12\text{V}, V_{DS}=0\text{V}$	P-Ch			± 100	
$R_{DS(ON)}^a$	Drain-Source On-State Resistance	$V_{GS}=4.5\text{V}, I_{DS}=9\text{A}$	N-Ch		12	18	m Ω
		$V_{GS}=-4.5\text{V}, I_{DS}=-6\text{A}$	P-Ch		30	45	
		$V_{GS}=2.5\text{V}, I_{DS}=6\text{A}$	N-Ch		18	27	
		$V_{GS}=-2.5\text{V}, I_{DS}=-4\text{A}$	P-Ch		50	65	
V_{SD}^a	Diode Forward Voltage	$I_{SD}=1.5\text{A}, V_{GS}=0\text{V}$	N-Ch		0.75	1.3	V
		$I_{SD}=-1.2\text{A}, V_{GS}=0\text{V}$	P-Ch		-0.8	-1.3	

Electrical Characteristics (Cont.) (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	APM9932CK			Unit	
			Min.	Typ.	Max.		
Dynamic Characteristics^b							
C _{iss}	Input Capacitance	N-Channel V _{GS} =0V, V _{DS} =20V, Frequency=1.0MHz	N-Ch		1205		pF
			P-Ch		1210		
C _{oss}	Output Capacitance	P-Channel V _{GS} =0V, V _{DS} =-20V, Frequency=1.0MHz	N-Ch		310		
			P-Ch		310		
C _{rss}	Reverse Transfer Capacitance	N-Channel V _{GS} =0V, V _{DS} =-20V, Frequency=1.0MHz	N-Ch		210		
			P-Ch		205		
t _{d(ON)}	Turn-on Delay Time	N-Channel V _{DD} =10V, R _L =10Ω, I _{DS} =1A, V _{GEN} =4.5V, R _G =6Ω	N-Ch		8	15	ns
T _r	Turn-on Rise Time		P-Ch		7	13	
T _f	Turn-off Fall Time	P-Channel V _{DD} =-10V, R _L =10Ω, I _{DS} =-1A, V _{GEN} =-4.5V, R _G =6Ω	N-Ch		10	17	
			P-Ch		9	16	
t _{d(OFF)}	Turn-off Delay Time	N-Channel V _{DD} =-10V, R _L =10Ω, I _{DS} =-1A, V _{GEN} =-4.5V, R _G =6Ω	N-Ch		29	43	
T _f	Turn-off Fall Time		P-Ch		27	42	
T _f	Turn-off Fall Time	P-Channel V _{DD} =-10V, R _L =10Ω, I _{DS} =-1A, V _{GEN} =-4.5V, R _G =6Ω	N-Ch		7	11	
			P-Ch		6	9	
Gate Charge Characteristics^b							
Q _g	Total Gate Charge	N-Channel V _{DS} =10V, V _{GS} =4.5V, I _{DS} =6A	N-Ch		14	22	nC
			P-Ch		17	25	
Q _{gs}	Gate-Source Charge	P-Channel V _{DS} =-10V, V _{GS} =-4.5V, I _{DS} =-5A	N-Ch		5		
			P-Ch		5.2		
Q _{gd}	Gate-Drain Charge	P-Channel V _{DS} =-10V, V _{GS} =-4.5V, I _{DS} =-5A	N-Ch		2.8		
			P-Ch		3.6		

Notes:

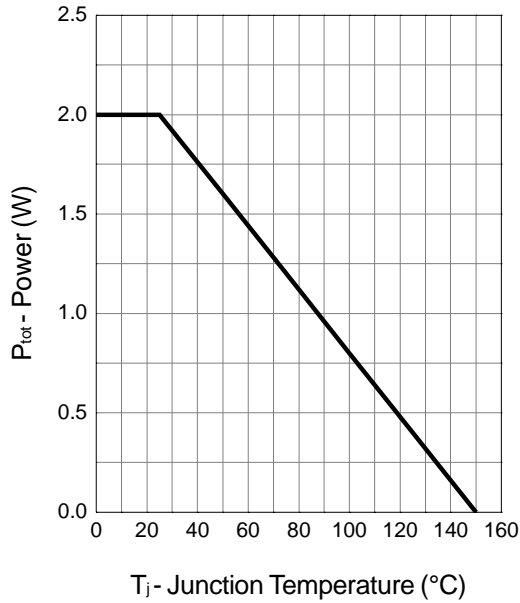
a : Pulse test ; pulse width ≤300μs, duty cycle ≤ 2%.

b : Guaranteed by design, not subject to production testing.

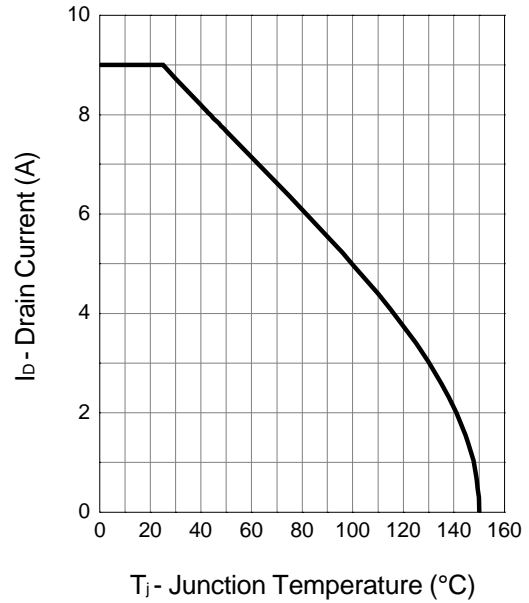
Typical Characteristics

N-Channel

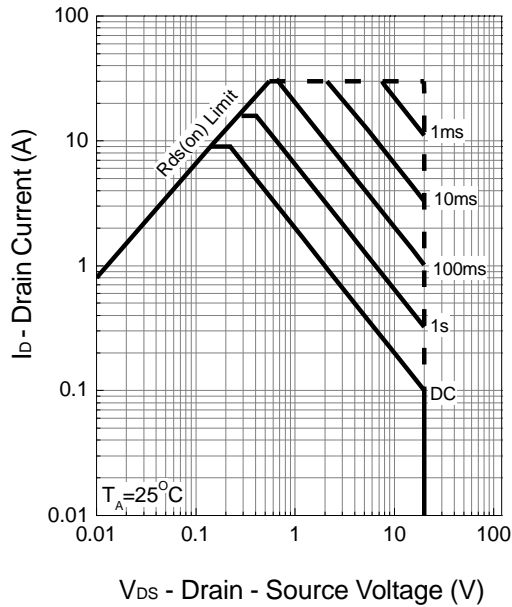
Power Dissipation



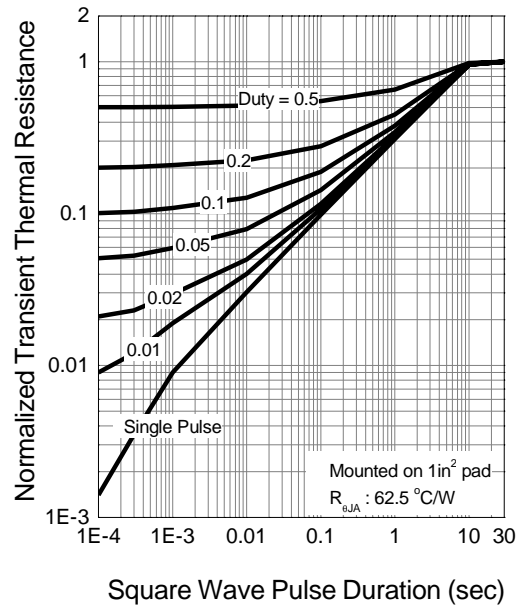
Drain Current



Safe Operation Area

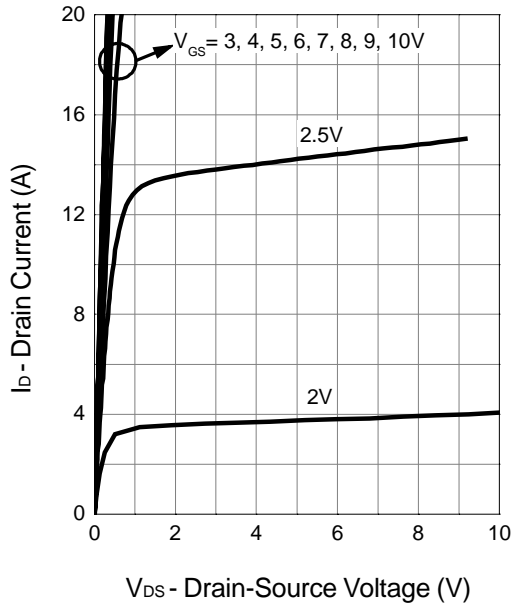


Thermal Transient Impedance

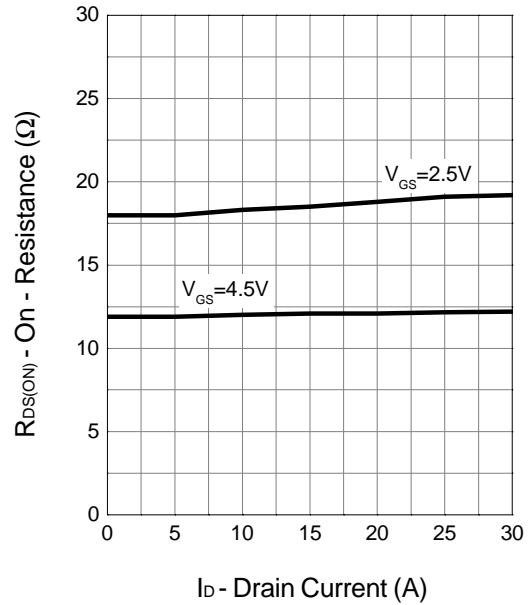


Typical Characteristics (Cont.)

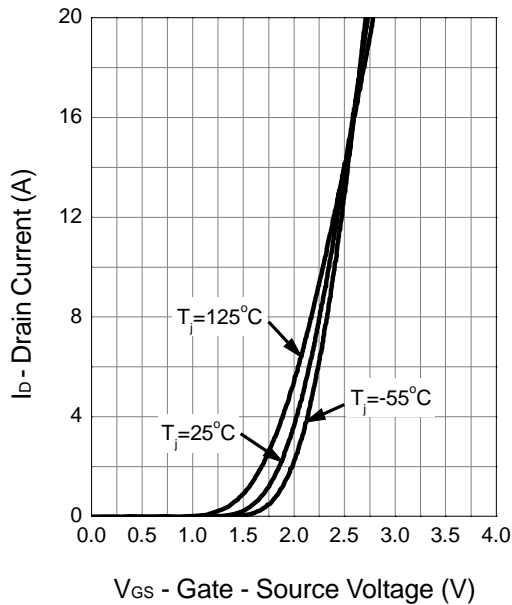
Output Characteristics



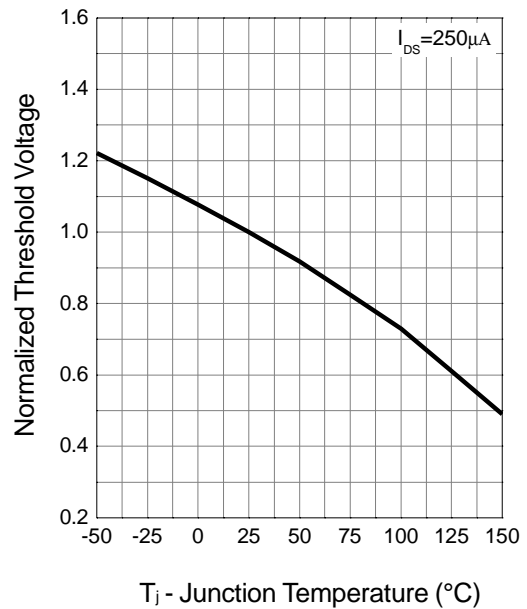
Drain-Source On Resistance



Transfer Characteristics

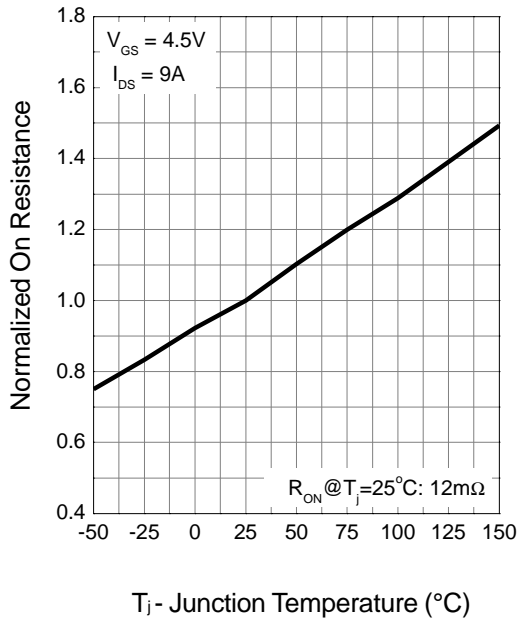


Gate Threshold Voltage

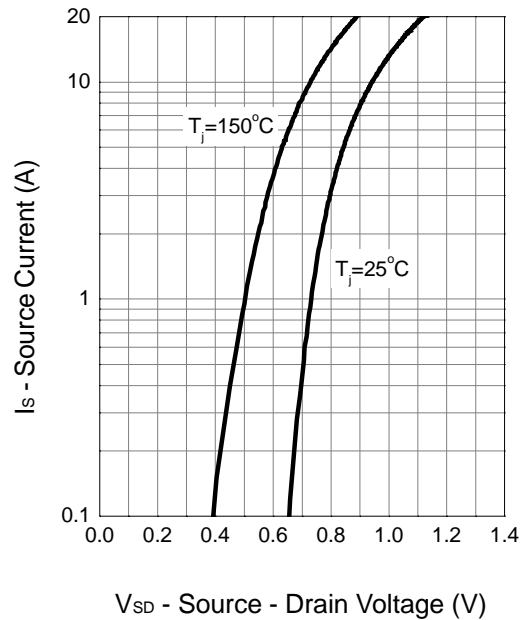


Typical Characteristics (Cont.)

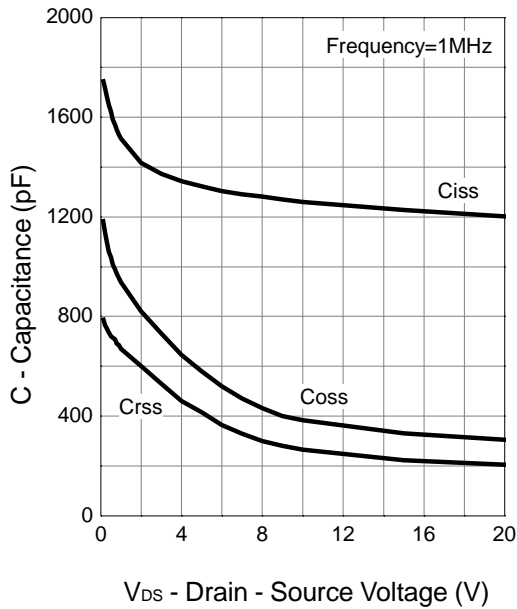
Drain-Source On Resistance



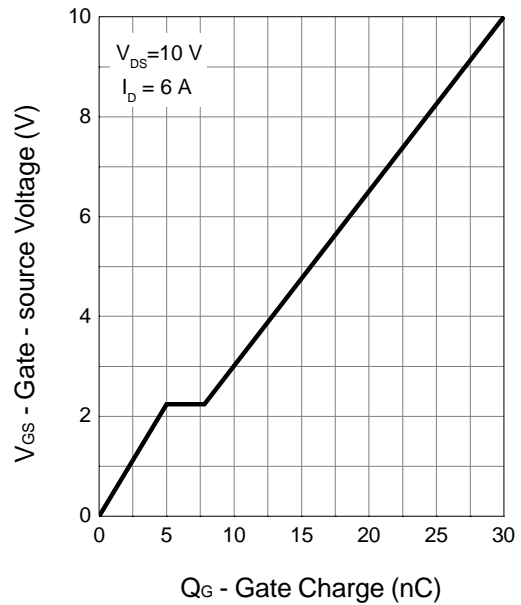
Source-Drain Diode Forward



Capacitance



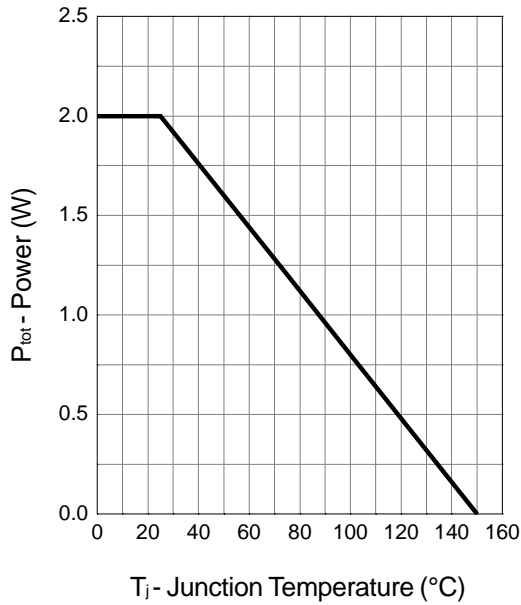
Gate Charge



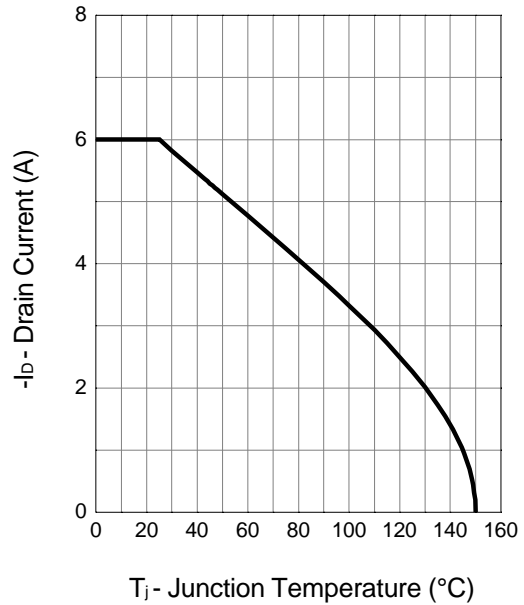
Typical Characteristics (Cont.)

P-Channel

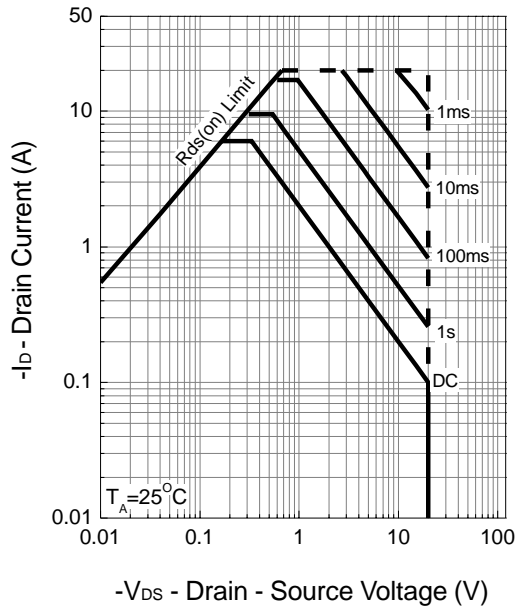
Power Dissipation



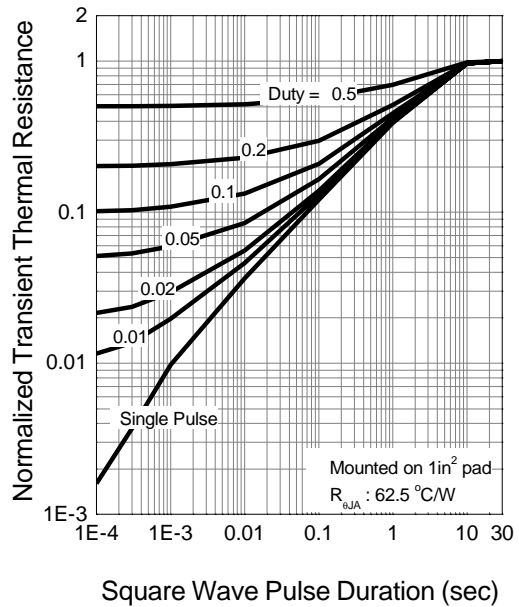
Drain Current



Safe Operation Area

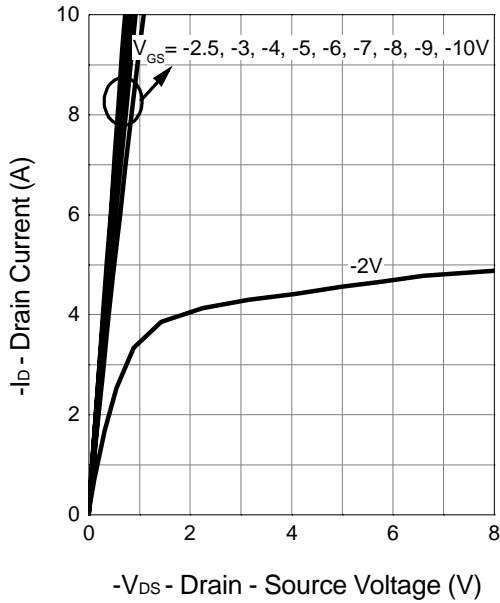


Thermal Transient Impedance

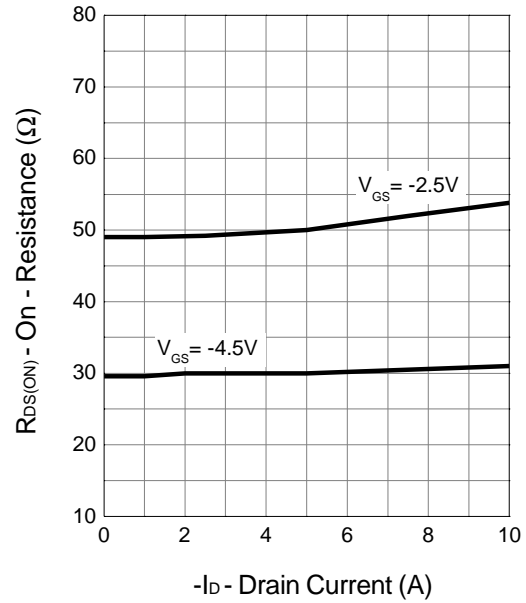


Typical Characteristics (Cont.)

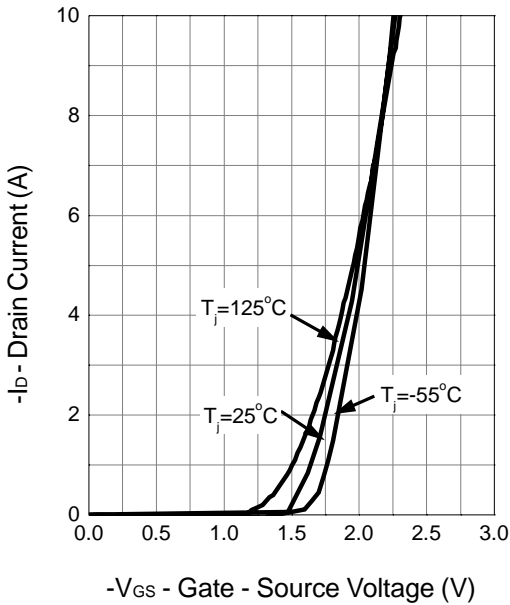
Output Characteristics



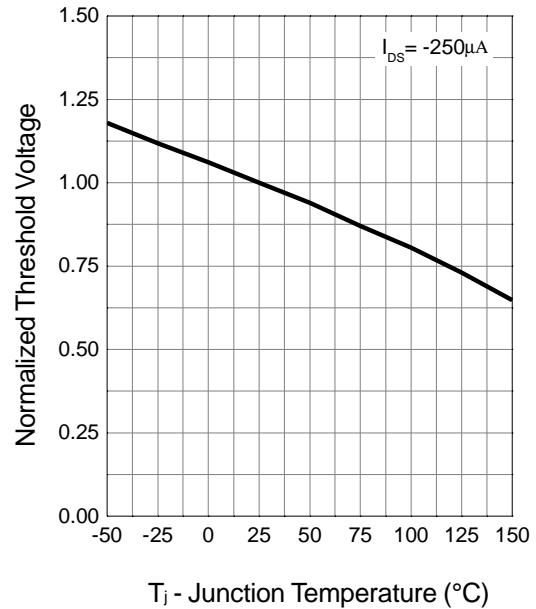
Drain-Source On Resistance



Transfer Characteristics

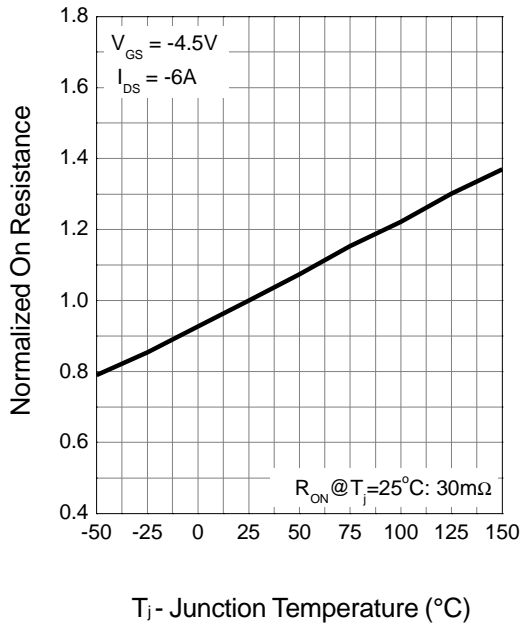


Gate Threshold Voltage

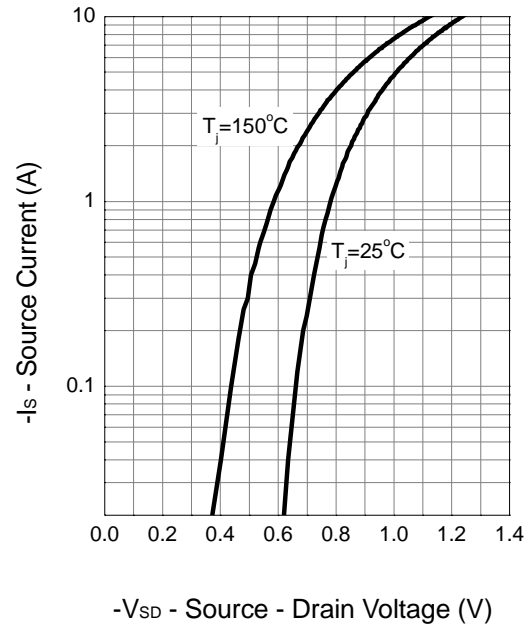


Typical Characteristics (Cont.)

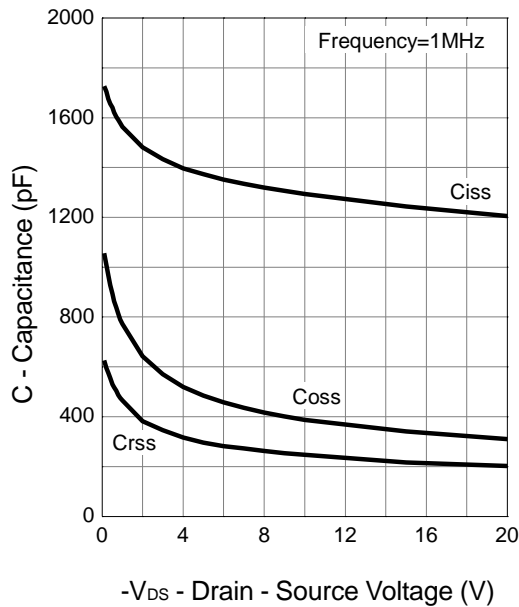
Drain-Source On Resistance



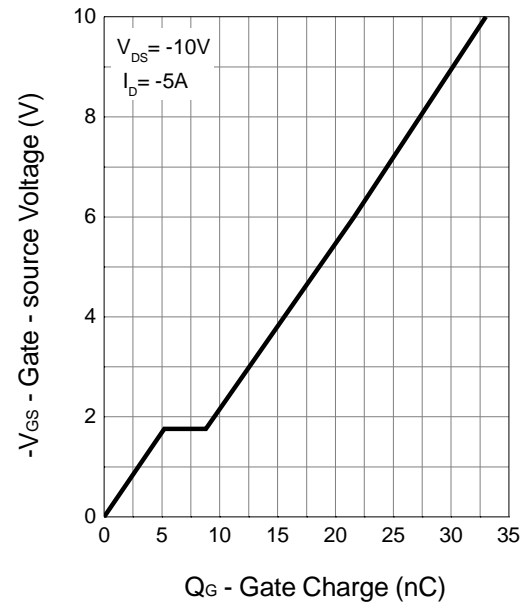
Source-Drain Diode Forward



Capacitance



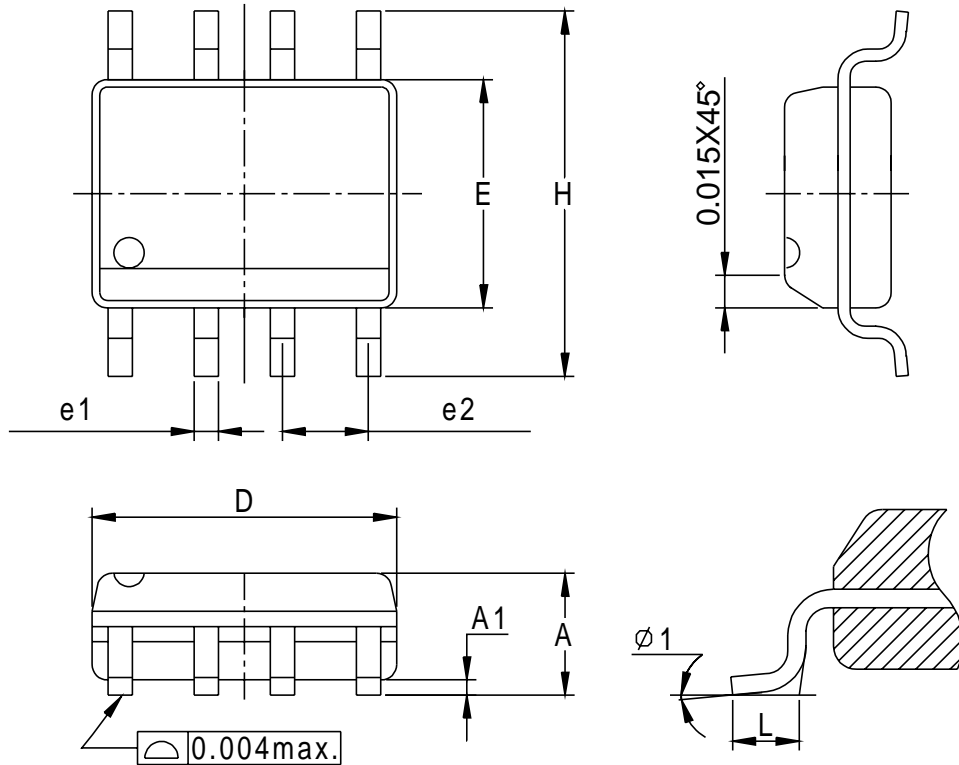
Gate Charge



Packaging Information

SOP-8 pin (Reference JEDEC Registration MS-012)

www.DataSheet4U.com

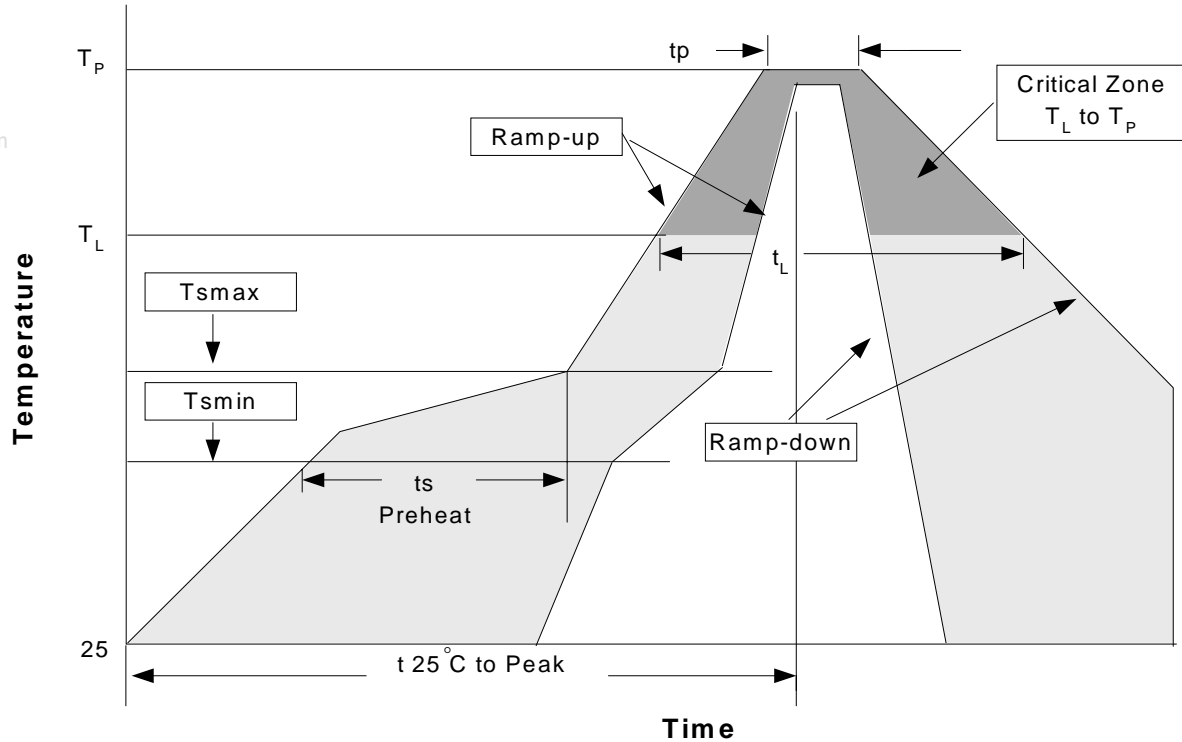


Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.80	5.00	0.189	0.197
E	3.80	4.00	0.150	0.157
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
e1	0.33	0.51	0.013	0.020
e2	1.27BSC		0.50BSC	
phi 1	8°		8°	

Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb), 100%Sn
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.

Reflow Condition (IR/Convection or VPR Reflow)



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly		Pb-Free Assembly	
	Large Body	Small Body	Large Body	Small Body
Average ramp-up rate (T_L to T_P)	3°C/second max.		3°C/second max.	
Preheat				
- Temperature Min (T_{smin})	100°C		150°C	
- Temperature Mix (T_{smax})	150°C		200°C	
- Time (min to max)(t_s)	60-120 seconds		60-180 seconds	
T_{smax} to T_L			3°C/second max	
- Ramp-up Rate				
T_{smax} to T_L				
- Temperature(T_L)	183°C		217°C	
- Time (t_L)	60-150 seconds		60-150 seconds	
Peak Temperature(T_p)	225 +0/-5°C	240 +0/-5°C	245 +0/-5°C	250 +0/-5°C
Time within 5°C of actual Peak Temperature(t_p)	10-30 seconds	10-30 seconds	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.		6°C/second max.	
Time 25°C to Peak Temperature	6 minutes max.		8 minutes max.	

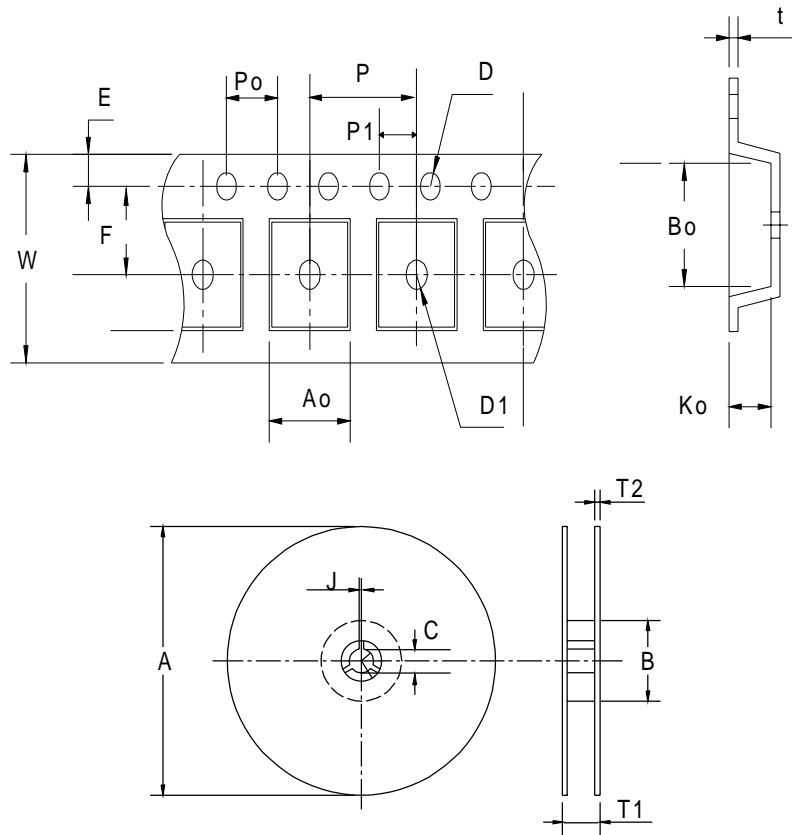
Note: All temperatures refer to topside of the package. Measured on the body surface.

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 SEC
HOLT	MIL-STD 883D-1005.7	1000 Hrs Bias @ 125°C
PCT	JESD-22-B, A102	168 Hrs, 100% RH, 121°C
TST	MIL-STD 883D-1011.9	-65°C ~ 150°C, 200 Cycles

Carrier Tape & Reel Dimensions

www.DataSheet4U.com



Application	A	B	C	J	T1	T2	W	P	E
SOP-8	330±1	62 ± 1.5	12.75 + 0.15	2 + 0.5	12.4 +0.2	2± 0.2	12 + 0.3 - 0.1	8± 0.1	1.75± 0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	5.5 ± 0.1	1.55±0.1	1.55+ 0.25	4.0 ± 0.1	2.0 ± 0.1	6.4 ± 0.1	5.2± 0.1	2.1± 0.1	0.3±0.013

(mm)

Cover Tape Dimensions

Application	Carrier Width	Cover Tape Width	Devices Per Reel
SOP- 8	12	9.3	2500

Customer Service

Anpec Electronics Corp.

Head Office :

5F, No. 2 Li-Hsin Road, SBIP,

Hsin-Chu, Taiwan, R.O.C.

Tel : 886-3-5642000

Fax : 886-3-5642050

Taipei Branch :

7F, No. 137, Lane 235, Pac Chiao Rd.,

Hsin Tien City, Taipei Hsien, Taiwan, R. O. C.

Tel : 886-2-89191368

Fax : 886-2-89191369