APPLICATION NOTE

APN1006: A Colpitts VCO for Wideband (0.95–2.15 GHz) Set-Top TV Tuner Applications

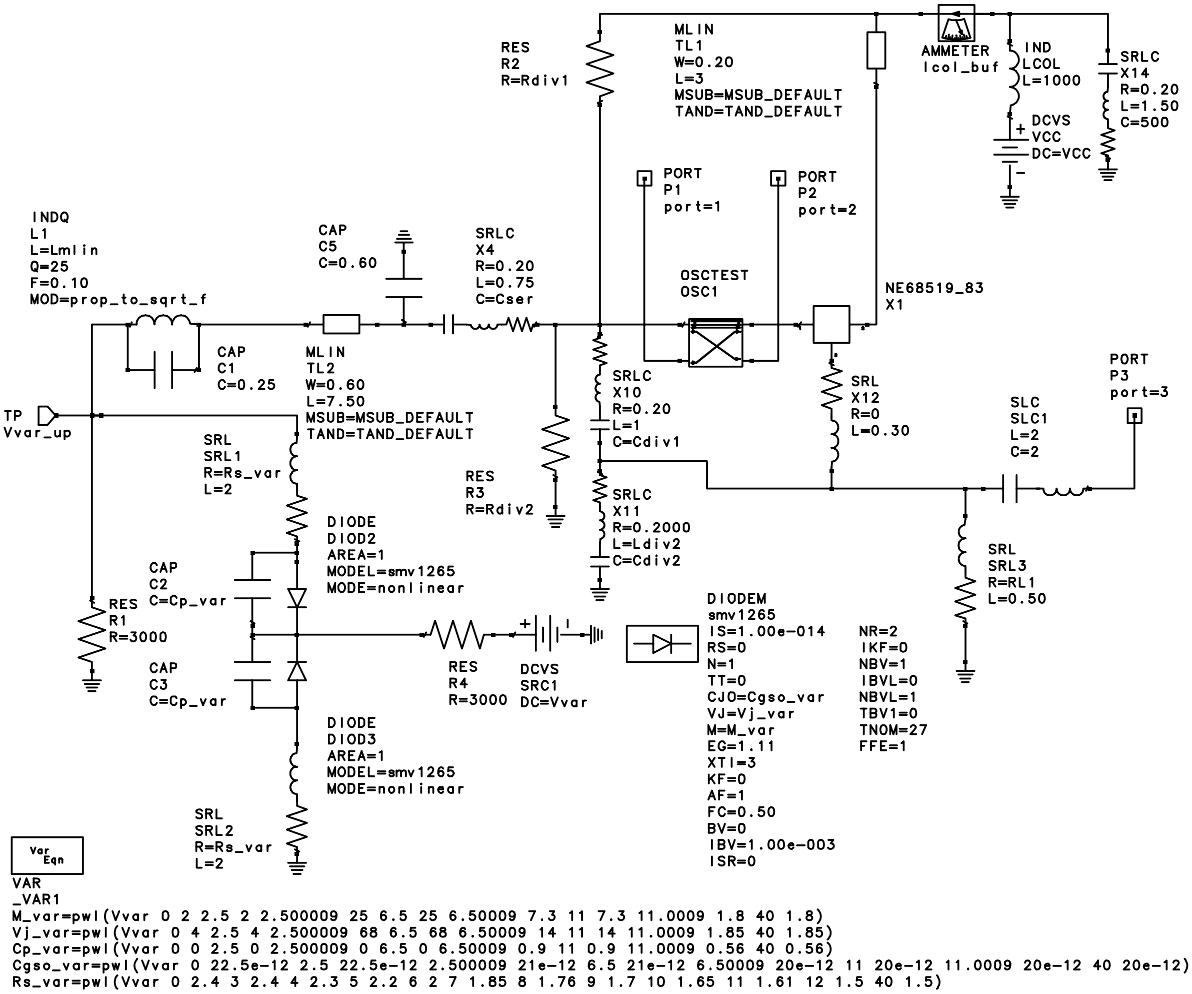
Introduction

Modern set-top DBS TV tuners require high-performance, broadband voltage control oscillator (VCO) designs at a competitive cost. To meet these goals, design engineers are challenged to create high-performance, low-cost VCOs.

The Colpitts oscillator is a traditional design used for many VCO applications. Designing a broadband Colpitts oscillator with coverage from 1–2 GHz requires the selection and interaction of an appropriate varactor diode for its resonator. This application note describes the design of a broadband Colpitts VCO that incorporates the SMV1265-011 varactor diode. This varactor diode was specifically developed at Skyworks for this application. The VCO design, based on Libra Series IV simulation, shows good correlation between measured and simulated performance. This application note includes a board layout and materials list.

VCO Model

Figure 1 shows the VCO model built for open loop analysis in Libra Series IV.



```
VAR
_VAR1
M_var=pwl(Vvar 0 2 2.5 2 2.500009 25 6.5 25 6.50009 7.3 11 7.3 11.0009 1.8 40 1.8)
Vj_var=pwl(Vvar 0 4 2.5 4 2.500009 68 6.5 68 6.50009 14 11 14 11.0009 1.85 40 1.85)
Cp_var=pwl(Vvar 0 0 2.5 0 2.500009 0 6.5 0 6.50009 0.9 11 0.9 11.0009 0.56 40 0.56)
Cgso_var=pwl(Vvar 0 22.5e-12 2.5 22.5e-12 2.500009 21e-12 6.5 21e-12 6.50009 20e-12 11 20e-12 11.0009 20e-12 40 20e-12)
Rs_var=pwl(Vvar 0 2.4 3 2.4 4 2.3 5 2.2 6 2 7 1.85 8 1.76 9 1.7 10 1.65 11 1.61 12 1.5 40 1.5)
```

Figure 1. VCO Model Built for Open Loop Analysis in Libra Series IV

This circuit schematic, which is a simple Colpitts structure, uses a series back-to-back connection of two SMV1265-011 varactors instead of a single varactor. This connection allows lower capacitance at high voltages, while maintaining the tuning ratio of a single varactor. The back-to-back varactor connection also helps reduce distortion and the effect of fringing and mounting capacitances. These parasitic capacitances are included in the model as C_5, valued at 0.6 pF. This value may change depending on the layout of the board.

DC bias is provided through resistors R_1 and R_4, both 3 kΩ, which may affect phase noise, but allows the exclusion of chokes. This reduces costs and the possibility of parasitic resonances — the common cause of spurious responses and frequency instability.

The resonator inductance was modeled as a lossy inductor (with Q = 25 at 100 MHz) in parallel with a capacitance of 0.25 pF. This is typical for a multilayer inductor of style 0603 (60 x 30 mil) footprint (TOKO Coils and Filters catalog). The inductor value of 5.6 nH was optimized to fit the desired 1–2 GHz frequency band. The DC blocking series capacitance (C_{SER}) was modeled as an SRC network, including associated parasitics; it was selected at 1000 pF to avoid affecting the resonator (Q).

The Colpitts feedback capacitances (C_{DIV1} = 1 pF and C_{DIV2} = 1.62 pF) were optimized to provide a flat power response over the tuning range. These values may also be re-optimized for phase noise if required.

The NEC NE68533 transistor was selected to fit the required bandwidth performance. Note: The circuit is very sensitive to the transistor choice (tuning range and stability) due to the wide bandwidth requirement. The output is supplied from the emitter load resistance (RL_1) through the 2 pF coupling capacitor, modeled as a series SLC_1 component.

The microstrip line (TL_1) simulates the design layout which may be incorporated in the resonator.

Figure 2 shows the Libra test bench. In the test bench, we define an open loop gain (Ku = V_{OUT}/V_{IN}) as a ratio of voltage phasors at input and output ports of an OSCTEST component. Defining the oscillation point requires the balancing of input (loop) power to provide zero gain for a zero loop phase shift. Once the oscillation point is defined, the frequency and output power can be measured. Use of the OSCTEST2 component for the close loop analysis is not recommended, since it may not converge in some cases, and doesn't allow clear insight into understanding the VCO behavior. These properties are considered an advantage of modeling over a purely experimental study.

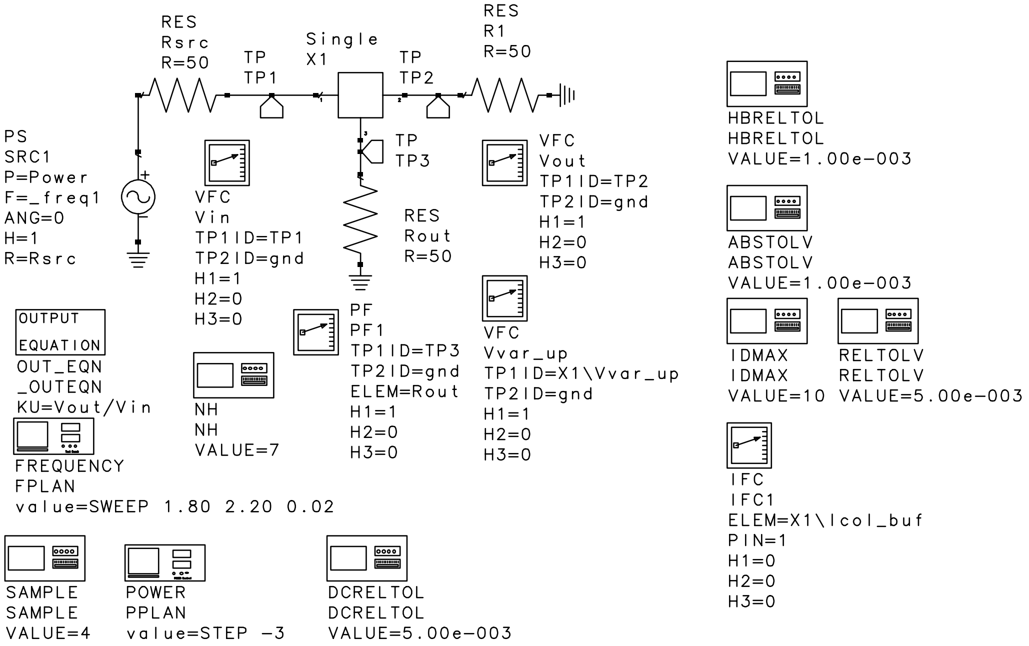


Figure 2. Libra Test Bench

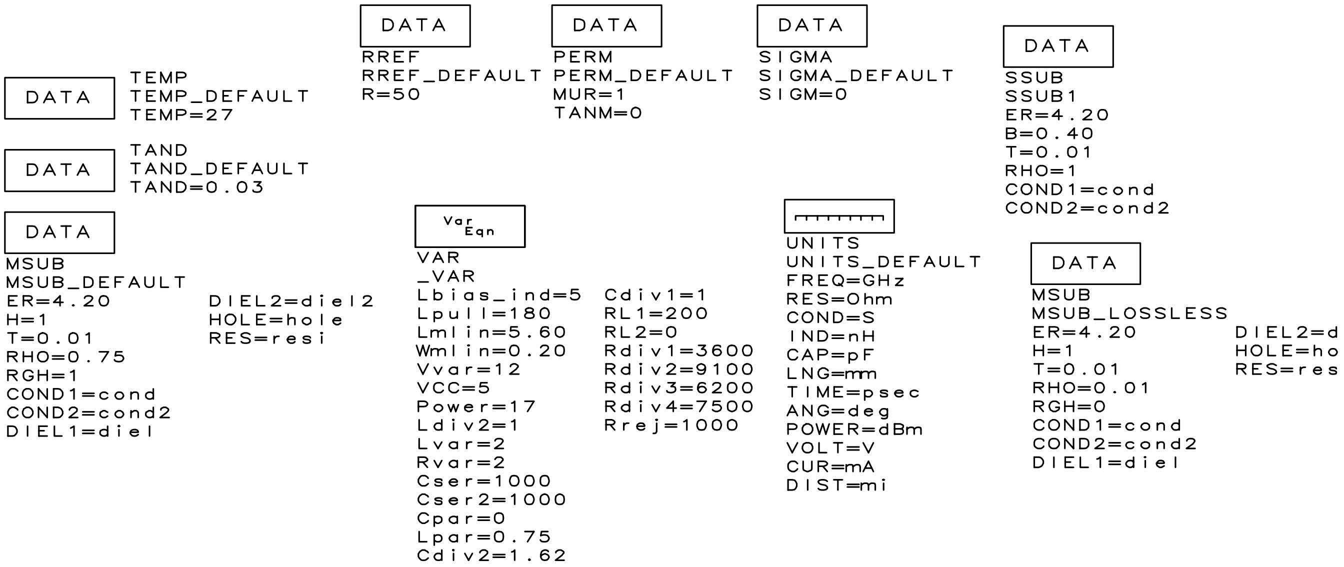


Figure 3. Default Test Bench

Figure 3 shows the default bench. The variables used for more convenient tuning during performance analysis and optimization are listed in a “variables and equations” component.

SMV1265-011 SPICE Model

Figure 4 shows a SPICE model for the SMV1265-011 varactor diode, defined for the Libra IV environment, with a description of the parameters employed.

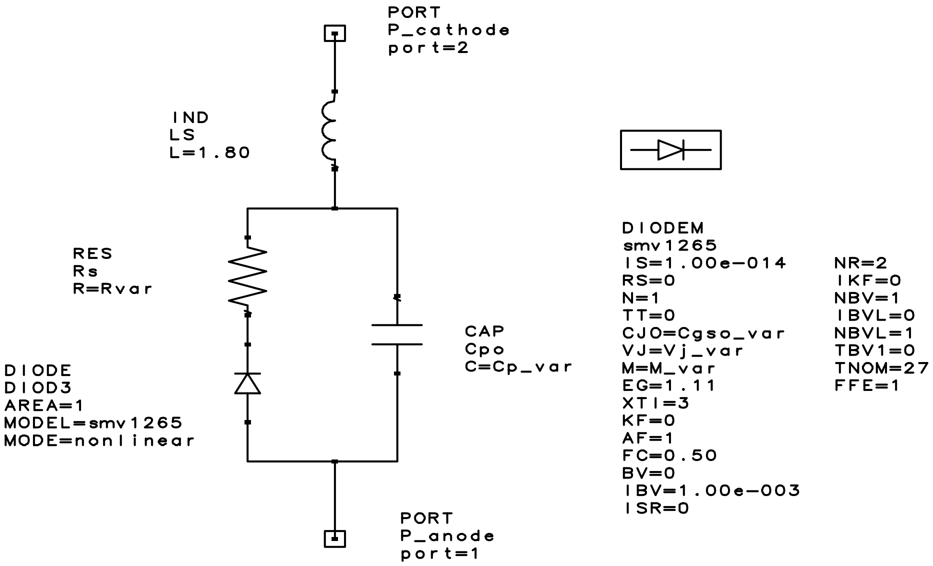


Figure 4. SMV1265-011 Libra IV SPICE Model

Parameter	Description	Unit	Default
IS	Saturation current (with N, determine the DC characteristics of the diode)	A	1e-14
R_S	Series resistance	Ω	0
N	Emission coefficient (with IS, determines the DC characteristics of the diode)	-	1
TT	Transit time	S	0
C_{J0}	Zero-bias junction capacitance (with V_J and M, defines nonlinear junction capacitance of the diode)	F	0
V_J	Junction potential (with V_J and M, defines nonlinear junction capacitance of the diode)	V	1
M	Grading coefficient (with V_J and M, defines nonlinear junction capacitance of the diode)	-	0.5
E_G	Energy gap (with XTI, helps define the dependence of IS on temperature)	EV	1.11
XTI	Saturation current temperature exponent (with E_G, helps define the dependence of IS on temperature)	-	3
KF	Flicker noise coefficient	-	0
AF	Flicker noise exponent	-	1
FC	Forward-bias depletion capacitance coefficient	-	0.5
B_V	Reverse breakdown voltage	V	Infinity
I_{BV}	Current at reverse breakdown voltage	A	1e-3
ISR	Recombination current parameter	A	0
NR	Emission coefficient for ISR	-	2
IKF	High injection knee current	A	Infinity
NBV	Reverse breakdown ideality factor	-	1
IBVL	Low-level reverse breakdown knee current	A	0
NBVL	Low-level reverse breakdown ideality factor	-	1
T_{NOM}	Nominal ambient temperature at which these model parameters were derived	°C	27
FFE	Flicker noise frequency exponent		1

Table 1. Silicon Varactor Diode Default Values

Table 1 describes the model parameters. It shows default values appropriate for silicon varactor diodes which may be used by the Libra IV simulator.

According to the SPICE model in Figure 4, the varactor capacitance (C_V) is a function of the applied reverse DC voltage (V_R) and may be expressed as follows:

$$C_V = \frac{C_{J0}}{\left(1 + \frac{V_R}{V_J}\right)^{M}} + C_P$$

This equation is a mathematical expression of the capacitance characteristic. The model is accurate for abrupt junction varactors (SMV1400 series); however, the model is less accurate for hyperabrupt junction varactors because the coefficients are dependent on the applied voltage. To make the equation fit the hyperabrupt performances for the SMV1265-011, a piece-wise approach was employed. Here the coefficients (V_J, M, C_{J0}, and C_P) are made piece-wise functions of the varactor DC voltage applied. Thus, the whole range of the usable varactor voltages is segmented into a number of subranges each with a unique set of the V_J, M, C_{J0}, and C_P parameters as given in the Table 2.

Voltage Range (V)	C_{J0} (pF)	M	V_J (V)	C_P (pF)
0–2.5	22.5	2	4	0
2.5–6.5	21	25	68	0
6.5–11	20	7.3	14	0.9
11–up	20	1.8	1.85	0.56

Table 2. Varactor Voltages

These subranges are made to overlap each other. Thus, if a reasonable RF swing (one that is appropriate in a practical VCO case) exceeds limits of the subrange, the C_V function described by the current subrange will still fit in the original curve.

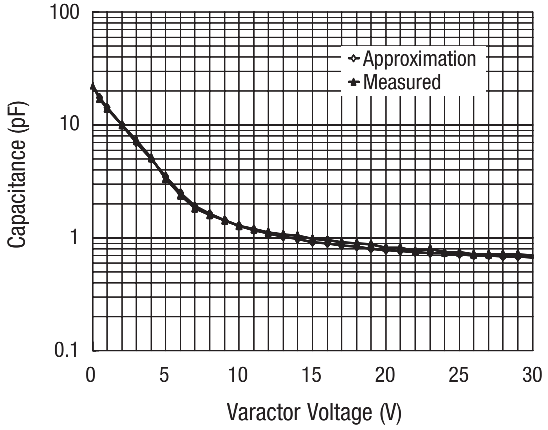


Figure 5. SMV1265 Capacitance vs. Voltage

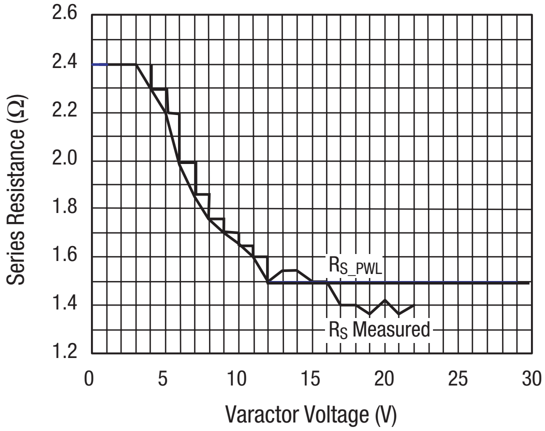


Figure 6. SMV1265 Resistance vs. Voltage

Figure 5 demonstrates the quality of the piece-wise fitting approach.

Special consideration was given to the fit at the lowest capacitance range (high-voltage area) since it dramatically affects the upper frequency limit of the VCO.

To incorporate this function into Libra, the pwl() built-in function was used in the "variables" component of the schematic bench.

M = pwl (V_{VAR} 0 2 2.5 2 2.500009 25 6.5 25 6.50009 7.3 11 7.3 11.0009 1.8 40 1.8)

V_J = pwl (V_{VAR} 0 4 2.5 4 2.500009 68 6.5 68 6.50009 14 11 14 11.0009 1.85 40 1.85)

C_P = pwl (V_{VAR} 0 0 2.5 0 2.500009 0 6.5 0 6.50009 0.9 11 0.9 11.0009 0.56 40 0.56)

C_{JO} = pwl (V_{VAR} 0 22.5 2.5 22.5 2.500009 21 6.5 21 6.50009 20 11 20 11.0009 20 40 20)*10^{12}

Note: While C_P is given in picofarads, C_{GO} is given in farads to comply with the default nominations in Libra. (For more details regarding pwl() function see Circuit Network Items, Variables and Equations, Series IV Manuals, p. 19–15).

Since the epitaxial layer for this kind of hyperabrupt varactor has relatively high resistivity, the series resistance is strongly dependent on the reverse voltage applied to varactor junction. The value of series resistance (R_S) measured at 500 MHz is shown in Figure 6, with a piece-wise approximation of R_S also given.

The piece-wise function may be used as follows:

R_S = pwl (V_{VAR} 0 2.4 3 2.4 4 2.3 5 2.2 6 2 7 1.85 8 1.76 9 1.7 10 1.65 11 1.61 12 1.5 40 1.5)

Note: The pwl() function in Libra IV is defined for the evaluation of harmonic balance parameters rather than variables. Therefore, although series resistance was defined as dependent on reverse voltage, for harmonic balance it remains parametric and linear. The same applies to capacitance, which remains the same as in the original diode model, but its coefficients (V_J, M, C_{JO}, and C_P) become parametric functions of the reverse voltage.

VCO Design Materials, Layout, and Performance

Figure 7 shows the VCO circuit diagram.

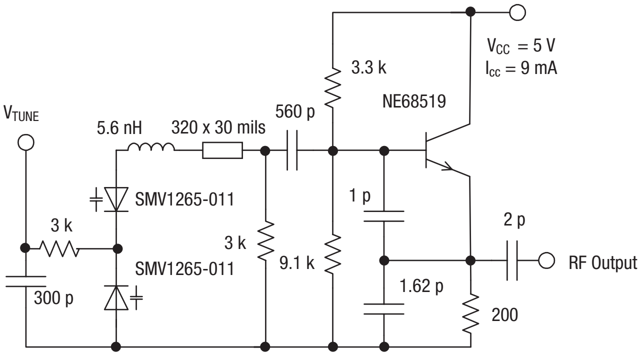


Figure 7. VCO Circuit Diagram

Table 3 shows the bill of materials used.

Designator	Part Type	Footprint
C_1	0603AU561JAT9 (AVX)	0603
C_2	0603AU2R0JAT9 (AVX)	0603
C_3	0603AU561JAT9 (AVX)	0603
C_4	0603AU201JAT9 (AVX)	0603
C_5	0603AU1R0JAT9 (AVX)	0603
C_6	0603AU1R6JAT9 (AVX)	0603
D_1	NE68519 (NEC)	SOT-419
L_1	LL1608-F5N6S (TOKO)	0603
R_1	CR10-332J-T (AVX)	0603
R_2	CR10-912J-T (AVX)	0603
R_3	CR10-201J-T (AVX)	0603
R_4	CR10-302J-T (AVX)	0603
R_5	CR10-302J-T (AVX)	0603
V_1	SMV1265-011 (Skyworks)	SOD-323
V_2	SMV1265-011 (Skyworks)	SOD-323

Table 3. Bill of Materials

Figure 8 shows the PCB layout. The board is made of standard FR4 material 60 mils thick.

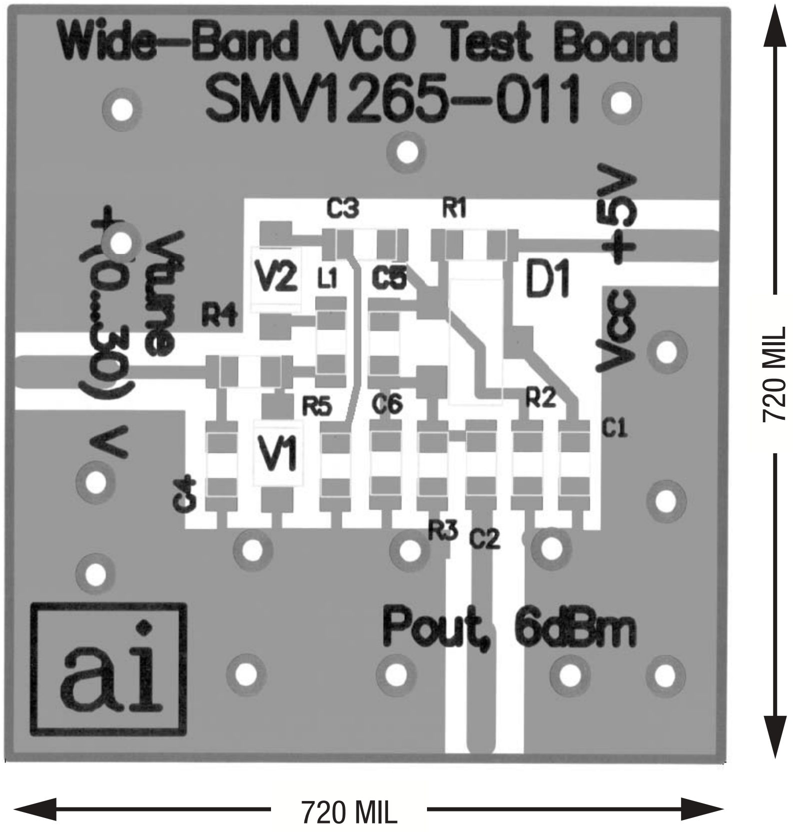


Figure 8. PCB Layout

Figure 9 shows both the measured performance of this circuit and the simulated results, obtained with the above model. The simulated tuning curve (frequency vs. voltage) is in excellent agreement with measured data, proving the effectiveness of the piece-wise approximation technique. The measured power response, shows some differences from its simulation, but is within the same range. A possible reason for the discrepancy could be the effect of higher harmonics. To simulate this would require significantly more complicated modeling of the components, board parasitics, and discontinuities. However, for most engineering purposes, the circuit performance prediction indicated here should be satisfactory.

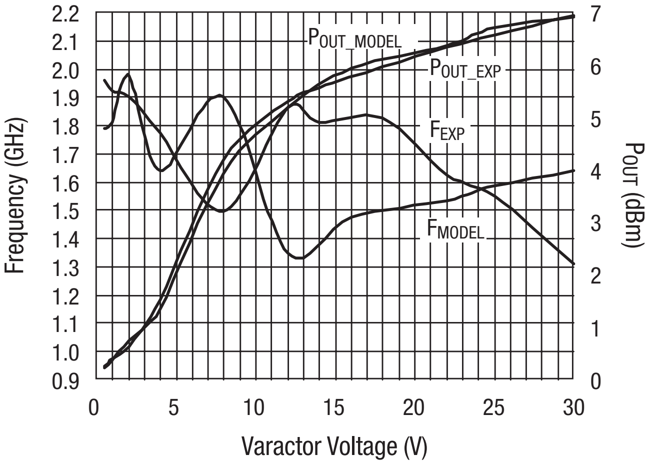


Figure 9. Measured and Simulated Frequency vs. Varactor Voltage

Table 4 shows tabulated measurement data. In voltage ranges of 1–27 V, the usable frequency coverage was estimated from 0.98–2.15 GHz.

V_{VAR} (V)	Frequency (GHz)	P_{OUT} (dBm)
0.5	0.95	5.7
1	0.974	5.5
2	1.018	5.4
4	1.184	4.7
8	1.68	3.2
12	1.886	5.2
14	1.932	4.9
18	2.008	5
22	2.076	3.9
25	2.12	3.5
30	2.188	2.2

Table 4. Tabulated Measurement Data

List of Available Documents

1. Colpitts Wideband VCO Simulation Project Files for Libra IV.
2. Colpitts Wideband VCO Circuit Schematic and PCB Layout for Protel EDA Client, 1998 version.
3. Colpitts Wideband VCO Gerber Photo-plot Files
4. A Colpitts VCO for Wideband (0.95–2.15 GHz) Set-Top TV Tuner Applications. (Current Document).
5. Detailed measurement and simulation data.

For the availability of the listed materials, please call our applications engineering staff.

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