16 min. -- Recording & Playback Voice IC

Features :

- Multi-level analog storage
  - High quality audio recording and playback
- Dual mode storage of analog and/or digital Data
  - Eliminates the need for separate digital memory
- Advanced, non-volatile Flash memory technology - No battery backup required
- SPI interface
  - Allows any commercial micro-controller to] control the device
- Programmable Sampling Clock
- Allows user to choose quality and duration leve
- Single 3V power supply
- Low power consumption
  - Playback operating current: 15mA typical
  - Standby current: 1uA maximum
  - Automatic power-down
- Multiple package options available
  - CSP, TSOP, PDIP, Bare Die
- On-board clock prescaler
  - Eliminates the need for external clock dividers
- Automatic squelch circuit
  - Reduces background noise during quiet passages

General Description :

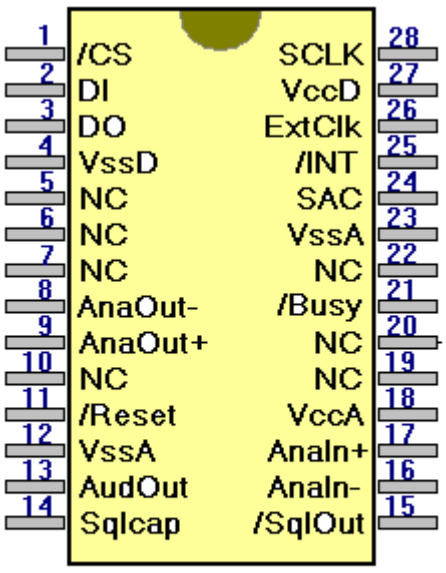
The APR6016 offers non-volatile storage of voice and/or data in advanced Multi-Level Flash memory. Up to 16 minutes of audio recording and playback can be accommodated. A maximum of 30K bits of digital data can be stored.

APR6016 devices can be cascaded for longer duration recording or greater digital storage. Device control is accomplished through an industry standard SPI interface that allows a microcontroller to manage message recording and playback. This flexible arrangement allows for the widest variety of messaging options.

The APR6016 is ideal for use in cellular and cordless phones, telephone answering devices, personal digital assistants, personal voice ecorders,and voice pagers.

APLUS achieves this high level of storage capability By using a proprietary analog multi-level storage technology implemented in an advanced on-volatile Flash memory process. Each memory cell can Typically store 256 voltage levels. This allows the APR6016 device to reproduce audio signals in their natural form,eliminating the need for encoding and compression,which can introduce distortion.

Figure 1 APR6016 Pinout Diagrams



APR6016-DIP28
-SOP28

Functional Description :

The EXTCLK pin allows the use of an external sampling clock. This input can accept a wide range of frequencies depending on the divider ratio programmed into the divider that follows the clock. Alternatively, the programmable internal oscillator can be used to supply the sampling clock. The MUX following both signals automatically selects the EXTCLK signal if a clock is present, otherwise the internal oscillator source is chosen. Detailed information on how to program the divider and internal oscillator can be found in the explanation of the *PWRUP* command, which appears in the *OpCode Command Description* section. Guidance on how to choose the appropriate sample clock frequency can be found in the *Sampling Rate & Voice Quality* section.

The audio signal containing the content you wish to record should be fed into the differential inputs ANAIN-,and ANAIN+. After pre-amplification the signal is routed into the anti-aliasing filter. The anti-aliasing filter automatically adapts its response based on the sample rate being used. No external anti-aliasing filter is therefore required.

After passing through the anti-alias filter, the signal is fed into the sample and hold circuit which works in conjunction with the Analog Write Circuit to store each analog sample in a flash memory cell.

When a read operation is desired the Analog Read Circuit extracts the analog data from the memory array and feeds the signal to the Internal Low Pass Filter. The low pass filter converts the individual samples into a continuous output. The output signal then goes to the squelch control circuit and differential output driver.

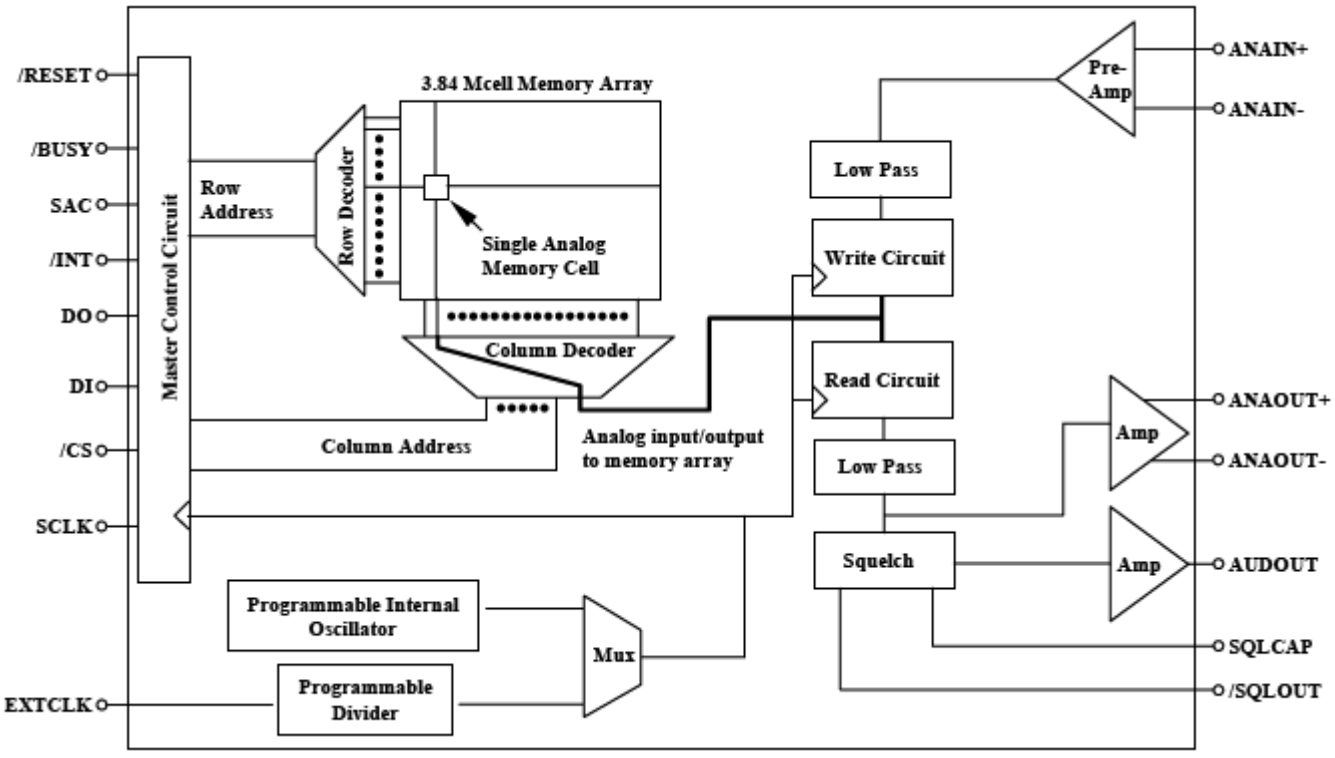
The differential output driver feeds the ANAOUT+ and ANAOUT- pins. Both differential output pins swing around a 1.23V potential.The squelch control circuit automatically reduces the output signal by 6 dB during quiet passages. A copy of the squelch control signal is present on the SQLOUT pin to facilitate reducing gain in the external amplifier as well.

For more information, refer to the Squelch section.

After passing through the squelch circuit the output signal goes to the output amplifier. The output amplifier drives a single ended output on the AUDOUT pin. The single ended output swings around a 1.23V potential.All SPI control and hand shaking signals are routed to the Master Control Circuit. This circuit decodes all the SPI signals and generates all the internal control signals.

It also contains the status register used for examining the current status of the APR6016.

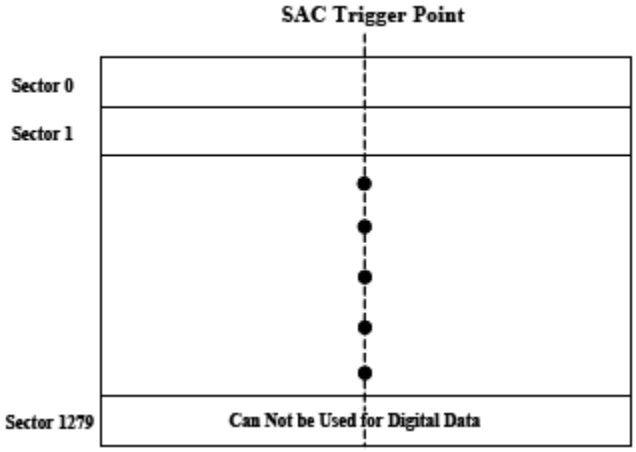
Figure 2 APR6016 Block Diagram :



Memory Organization :

The APR6016 memory array is organized to allow the greatest flexibility in message management and digital storage. The smallest addressable memory unit is called a "sector". The APR6016 contains 1280 sectors.

Figure 3 Memory Map.



Sectors 0 through 1279 can be used for analog storage.During audio recording one memory cell is used per sample clock cycle. When recording is stopped an end of data (EOD) bit is programmed into the memory. This prevents playback of silence when partial sectors are used. Unused memory that exists between the EOD bit and the end of the sector cannot be used.Sectors 0 through 9 are tested and guaranteed for digital storage. Other sectors, with the exception of sector 1279, can store data but have not been tested, and are thus not guaranteed to provide 100% good bits.This can be managed with error correction or forward check-before-store methods. Once a write cycle is initiated all previously written data in the chosen sector is lost.

Mixing audio signals and digital data within the same sector is not possible.

Note. There are a total of 15bits reserved for addressing.The APR6016 only requires 11 bits. The additional 5 bits are used for larger devices within the later APRXXfamily.

SPI Interface :

All memory management is handled by an external host processor. The host processor communicates with the APR6016 through a simple Serial Peripheral Interface (SPI) Port. The SPI port can run on as little as three wires or as many as seven depending on the amount of control necessary. This section will describe how to manage memory using the APR6016 SPI Port and associated OpCode commands. This topic is broken down into the following sections:

- Sending Commands to the Device
  - OpCode Command Description
- Receiving Device Information
  - Current Device Status (CDS)
  - Reading the Silicon Identification (SID)
- Writing Digital Data
- Reading Digital Data
- Recording Audio Data
- Playing Back Audio Data
- Handshaking Signals

Sending Commands to the Device

This section describes the process of sending OpCodes to the APR6016. All OpCodes are sent in the same way with the exception of the DIG_ WRITE and DIG_READ commands The DIG_ WRITE and DIG_READ commands are described in the Writing Digital Data and Reading Digital Data sections that follow.

The minimum SPI configuration needed to send commands uses the DI, /CS, and SCLK pins. The device will accept inputs on the DI pin whenever the /CS pin is low. OpCode commands are clocked in on the rising edge of the SPI clock. **Figure 4** shows the timing diagram for shifting OpCode commands into the device. **Figure 5** is a description of the OpCode stream.

You must wait for a command to finish executing before sending a new command. This is accomplished by monitoring the /BUSY pin.

You can substitute monitoring of the busy pin by inserting a fixed delay between commands.

The required delay is specified as T_{next1},T_{next2}, T_{next3} or T_{next4}. **Figure 6** shows the timing diagram for sending consecutive commands. **Table 1** describes which T_{next} specification to use.

Figure 4 Sending SPI Commands

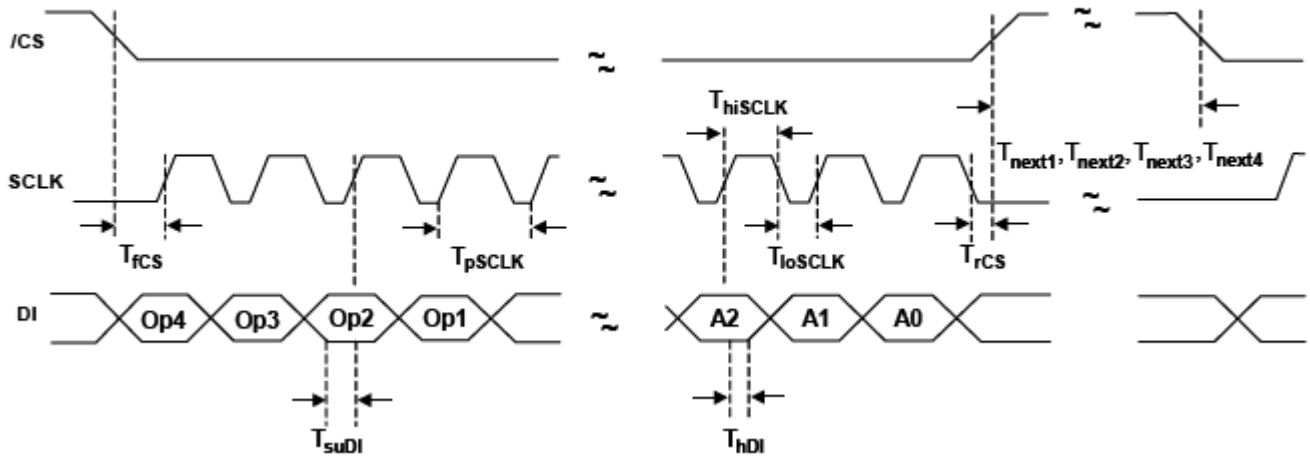
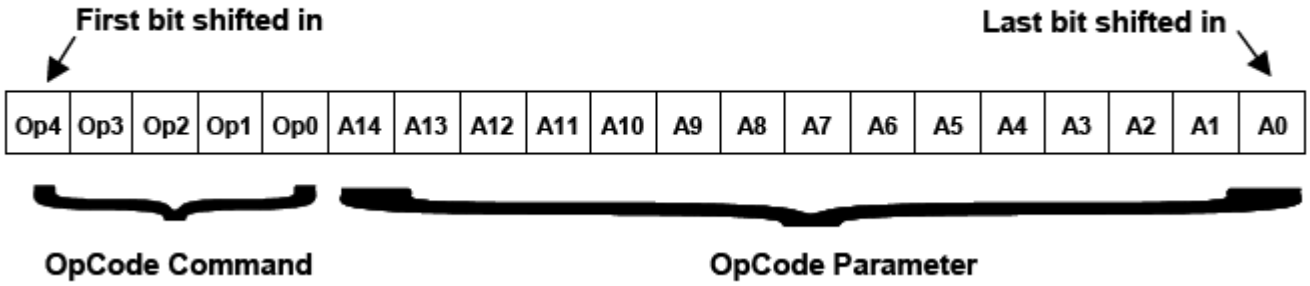


Figure 5 OpCode Format



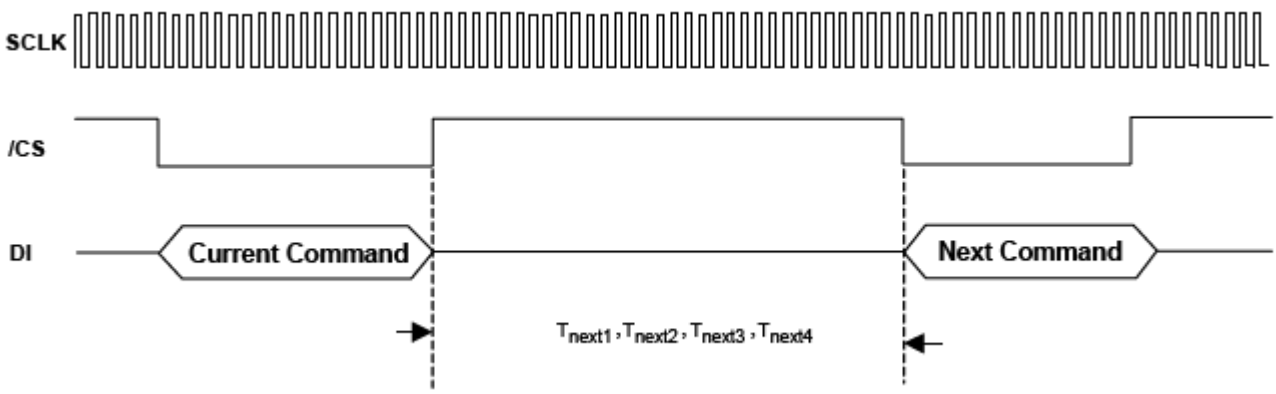


Table 1 Sequential Command Timing

Command	Next command	Timing Symbol
NOP **SID**	Any Command	Tnext1
PWRUP	Any Command	Tnext2
STOP_PWDN	PWRUP	Tnext2
SET_REC **REC**	STOP, STOP_PWDN, SET_REC, REC, NOP	Within SAC Low Time
SET_PLAY **PLAY**	STOP, STOP_PWDN, SET_FWD, FWD, SET_PLAY, PLAY, NOP	
SET_FWD **FWD**	SET_FWD, FWD, STOP, STOP_PWDN	
DIG_WRITE **DIG_READ** **DIG_ERASE**	Any Digital Command, STOP, STOP_PWDN *Note: For partial DIG_READ Tnext2 is measured from the extra clock low that follows the rise of /CS, not from the rise of /CS*	Tnext3
STOP	Any Command	Tnext4

OpCode Command Description

Designers have access to a total of 14 OpCodes. These OpCodes are listed in Table 2.
The name of the OpCode appears in the left hand column. The following two columns represent the actual binary information contained in the 20 bit data stream. Some commands have limits on which command can follow them. These limits are shown in the "*Allowable Follow on Commands"* column. The last column summarizes each command. Combinations of OpCodes can be used to accommodate almost any memory management scheme.

Table 2 APR6016 Operational Codes

Instruction Name	OpCode (5bit)	Opcode Parameters (15bit)	Allowable Follow on Commands	Summary
	[op4-op0]	*[Address MSB - Address LSB]* *[Address 14 - Address 0]*		
NOP	[00000]	[Don't care]	All Commands	No Operation
SID	[00001]	[Don't care]	All Commands	Causes the silicon ID to be read.
SET_FWD	[00010]	Sector Address [A14 - A0]	SET_FWD, FWD, STOP, STOP_PWDN	Starts a fast forward operation from the sector address specified.
FWD	[00011]	[Don't care]	SET_FWD, FWD STOP,STOP_PWDN	Starts a fast forward operation from the current sector address.
PWPUP	[00100]	[A14-A10]: all zeros [A9-A2]:EXTCLK divider ratio [AI-A0]: Sample Rate Frequency	All Commands	Resets the device to initial conditions. Sets the sample frequency and divider ratios.
STOP	[00110]	[Don't care]	All Commands	Stops the current operation.
STOP_PWDN	[00111]	[Don't care]	PWRUP	Stops the current operation. Causes the device to enter power down mode.

Instruction Name	OpCode (5bit)	Opcode Parameters (15bit)	Allowable Follow on Commands	Summary
SET_REC	[01000]	Sector Address [A14 - A0]	STOP, STOP_PWDN SET_REC, REC, NOP	Starts a record operation from the sector address specified.
REC	[01001]	[Don't care]	STOP, STOP_PWDN, SET_REC, REC, NOP	Starts a record operation from the current sector address.
DIG_ERASE	[01010]	Sector Address [A14 - A0]	All Commands	Erases all data contained in specified sector. You must not erase a sector before recording voice signals into it. You must erase a sector before storing digital data in it.
DIG_ WRITE	[01011]	[A14 - A0][XXXX] [D0 - D3004][XXXX]	All Commands	This command writes data bits D0 -D3003 starting at the specified address. All 3004 bits must be written.
DIG_READ	[01111]	Sector Address [A14 – A0]	All Commands	This command reads data bits D0 - D3003 starting at the specified address
SET PLAY	[01100]	Sector Address [A14 – A0]	STOP, STOP_PWDN, SET_FWD, FWD, SET_PLAY, PLAY, NOP	Starts a play operation from the current sector address specified..
PLAY	[01101]	[Don't care]	STOP, STOP_PWDN, SET_FWD, FWD, SET_PLAY, PLAY, NOP	Starts a play operation from the current sector address.

The **NOP** command performs no operation in the device.It is most often used when reading the current Device status. For more information on reading device Status see the *Current Device Status section*.

THE **SID** operation instructs the device to return the contents of its silicon ID register. For more Information see the Reading the *SID* section.

The **SET_FWD** command instructs the device to fast forward from the beginning of the sector specified in the OpCode parameter field.The device will fast forward until either an EOD bit or the end of the sector is reached. If no EOD bit or forthcoming command has been received when the end of the sector is reached,the device will loop back to the beginning of the same sector and begin the same process again. If an EOD bit is found the device will stop and generate an interrupt on the /INT pin. The output amplifiers are muted during this operation.

The **FWD** command instructs the device to fast forward from the start of the current sector to the next EOD marker. If no EOD marker is found within the current sector the device will increment to the next sequential sector and continue looking. The device will continue to fast forward in this manner until either an EOD is reached, a new command is sent, or the end of the memory array is reached. When an EOD is reached the device will stop and generate an interrupt on the /INT pin. The output amplifiers are muted during this operation.

The **PWRUP** command causes the device to enter power up mode and set the internal clock frequency and EXTCLK divider ratio. To select an Internal oscillator frequency set the [A1 – A0] bits according to the following binary values:

A1	A0	Sample rate
0	**0**	**6.4 KHz**
0	**1**	**4.0 KHz**
1	**0**	**8.0 KHz**
1	**1**	**5.3 KHz**

If you are using an external sample clock signal you must also set the EXTCLK divider ratio. This divider ratio is equal to N:1 where N is an integer between 1 and 256, excluding 2.The N value should be selected to satisfy the following equation as closely as possible:

EXTCLK freq =(N)*(128)*(selected sampling frequency)

Example:

Suppose that 8.0 KHz sampling is desired. Assume that the frequency of the signal present on EXTCLK

= 8MHz.

$$N = \frac{8000000}{128(8000)} = 7.8125$$

Rounding up, N = 8

The Op Code Parameter bit stream, composed of Bits [A9 - A2][A1 - A0], therefore becomes binary [00001000][10].

The **STOP** Command causes the device to stop the current operation.

The **STOP_PWDN** command causes the device to Stop the current command and enter power down mode.During power down the device consumes significantly less power. The PWRUP command must be used to force the device into power up mode before any commands can be executed.

The **SET_REC** command instructs the device to Begin recording at the sector address specified. The device will continue to record until the end of the current sector is reached. If no forthcoming command has been received when the end of the sector is reached the device will loop back to the beginning of the same sector and overwrite the previously recorded material. If the next command is another SET_REC or REC command the device will execute the command immediately following the end of the current sector so that no audio information is lost. For more information see the section entitled *Recording Audio Data*.

The **REC** command instructs the device to begin recording in the current sector. If no new command is received before the device reaches the end of the sector the device will automatically increment to the next sequential sector and continue recording. The device will continue to record in this manner until the memory is exhausted or a STOP or STOP_PWDN command is received. For more information see the section entitled *Recording Audio Data*.

The **DIG_ERASE** command erases all data Contained in the sector specified. Erase should not be done before recording voice signals into a sector. Erase must be done before storing digital data in a sector.

The **DIG_WRITE** command stores 3K bits of digital Data in the specified sector. All 3K bits must be written; no partial usage of the sector is possible. The memory acts as a FIFO, the first data bit shifted in will be the first data bit shifted out. A sector must be erased using the DIG_ERASE command EFORE data can be written to the sector. For more information on storing digital data,see the section entitled *Writing Digital Data.*

The **DIG_READ** command instructs the device to retrieve digital data that was previously written to the specified sector. The first bit shifted out is the first bit that was written. The last bit shifted out is the last bit that was written. For more information on reading digital data see the section entitled *Reading Digital Data*.

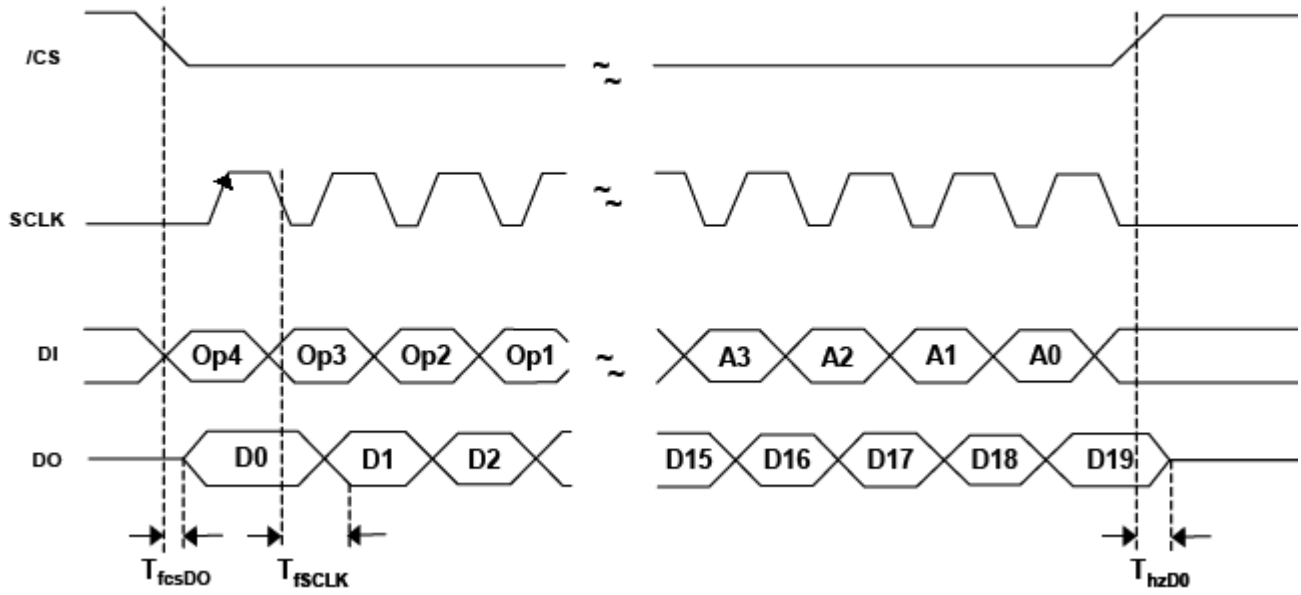
The **SET_PLAY** command instructs the device to Begin playback at the specified sector. If no Forthcoming command is received, or EOD bit encountered, before the end of the sector is reached the device will loop back to the beginning of the same sector and continue playback with no noticeable gap in the audio output. If the next command is another SET_PLAY or PLAYcommand the device will execute the commandimmediately following the end of the current sector sothat no gap in playback is present. For more information see the section entitled *Playing Back Audio Data.*

The **PLAY** command instructs the device to begin playback at the current sector. If no forthcoming command is received, or EOD bit encountered, before the device reaches the end of the sector the device will automatically increment to the next sequential sector and continue playing.
The device will continue to play in this manner until the memory is exhausted or a STOP or STOP_PWDN command is received. For more information see the section entitled *Playing Back Audio Data.*

Receiving Device Information

The device communicates data to the user by Shifting out data on the DO pin. The device will shift out data according to the timing parameters given in **Figure 7**.The device can shift out three different types of data streams: Device status, Silicon ID and user stored data.Device status and silicon ID are described in the next two sections. Retrieval of user data is described in the *Reading Digital Data section*

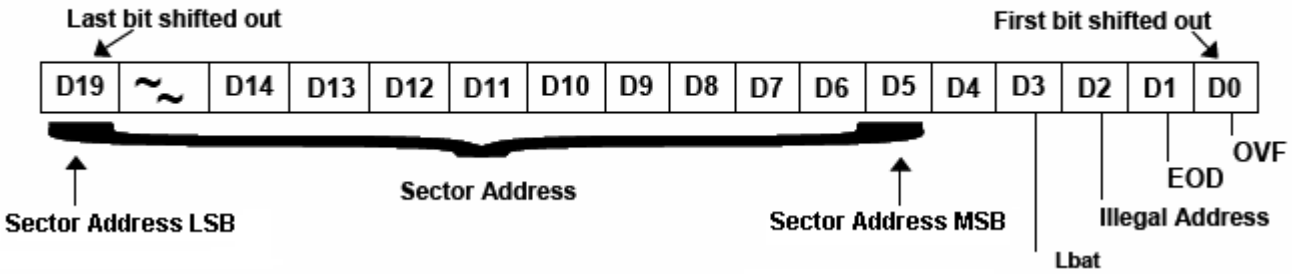
Figure7 Data Out Timing



Current Device Status (CDS)

As described in the previous section, three different types of data streams are shifted out on the DO pin as data is shifted in on the DI pin. One of these steams is the current device status. The CDS will be shifted out unless the previous command is SID command. **Figure 8** shows the format of the CDS bit stream. The first bit shifted out, DO, is the Overflow flag. The Overflow flag is set to a binary 1 if an attempt was made to record beyond the available memory. The Overflow flag is set to a 0 if an overflow has not occurred. This flag is cleared after it has been read. The D1 bit is the End of Data flag. The EOD flag is set when the device stops playing, or fast forwarding as a result of an EOD bit in memory. The EOD flag is cleared after it has been read.The D2 bit is the Illegal Address flag. The Illegal Address flag is set whenever an illegal address is sent to the device. The D3 bit is the low battery (Lbat) flag. Thisflag is set when the device senses a supply voltage below specification. The D4 bit is not used and should be ignored. The last fifteen bits represent the address of the current or last active sector.

Figure 8 Format for CDS Bit Stream

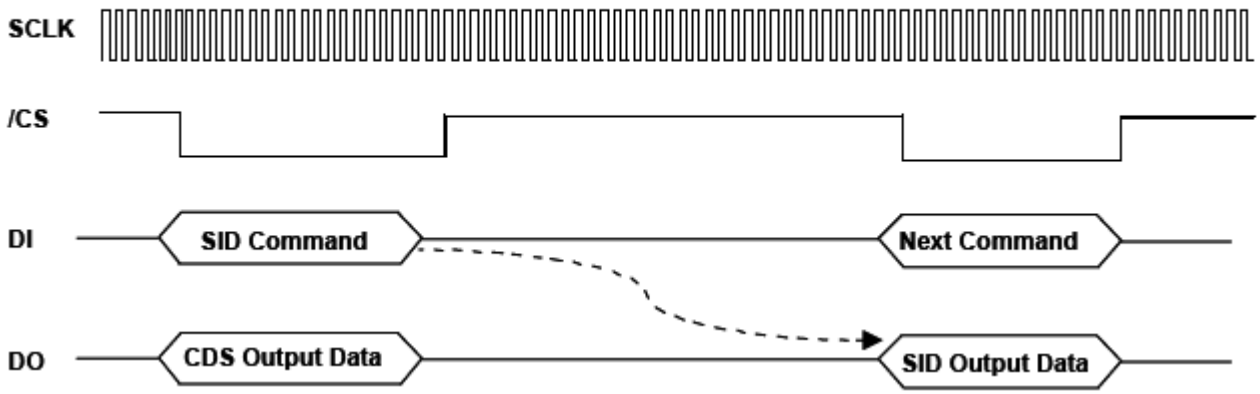


Reading the SID

Each device in the APRXX series family contains an
embedded Silicon Identification (SID). The SID can be read by the host processor to identify which family/family member is being used. Reading the device SID requires issuing two OpCode commands; a SID command followed by any other command,usually a NOP command. The device will clock the SID data out on the DO pin as the command that follows the SID command is clocked in.

Figure 9 is a diagram that describes the process necessary for reading SID information.

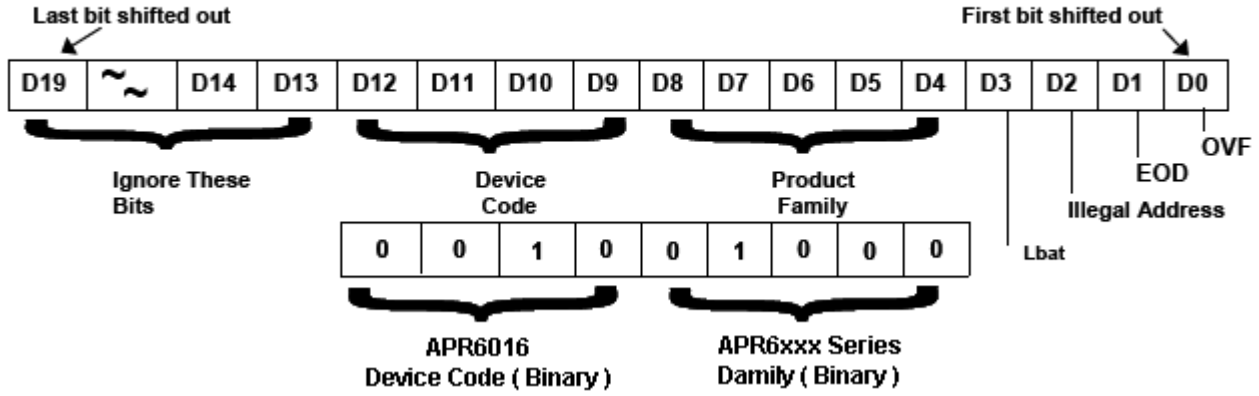
Figure 9 SID Timing



The SID information follows the format given in **Figure 10**. The first bit shifted out DO is the Overflow bit. The Overflow bit is set to a binary 1 if an attempt was made to record beyond the available memory. The Overflow bit is set to 0 if an overflow has not occurred. This bit is cleared after it has been read. The Dl bit is the End Of Data (EOD) bit.

The EOD bit is set when the device stops playing or fast-forwarding as a result of EOD bit in memory. The EOD bit cleared after it has been read. The D2 bit is the Illegal Address bit. The Illegal Address Bit is set whenever an illegal address is sent to the device. The D3 bit is the LBAT bit. This bit is set when the device senses a supply voltage below specification. The following five bits represent the product family. The APRXX product family code is binary 01000 as shown in **Figure 10**. The next four bits represent the device code. The APR6016 device code is binary 0010 as shown in **Figure 10**. The last seven bits are random data and should be ignored.

Figure 10 SID Bit Stream



Writing Digital Data

Digital data is written into the device using the DIG_WRITE command. No mixing of analog data and digital data within a sector is possible. Sectors 0 through 9 are tested and guaranteed for digital storage.Other sectors, with the exception of sector 1279, can store data but have not been tested and are thus not guaranteed to provide 100% good bits. This can be managed with error correction or forward check-before-store methods. Issuing a DIG_ERASE command on sector 1279 will cause data throughout all sectors to be lost.

A sector must be erased, using the DIG_ERASE command, before digital data can be written to it. This requirement is necessary whether analog data or digital data was previously stored in the sector. A sector should not be erased more than once between analog and digital write operations. Executing multiple erase operations on a sector will permanently damage the sector. A sector can be reallocated to either analog storage or digital storage at any time.

The process of storing digital data begins by sending a DIG_WRITE command. The DIG_WRITE command is followed immediately by four buffer bits. These bits will not be stored in the array and must be considered don't care bits.

Immediately following the four buffer bits should be the data that you wish to store. All 3004 bits must be stored.Four additional buffer bits must be clocked into the device following the stored data. These bits will not be stored in the array and must be considered don't care bits.Ending a digital write command early will permanently damage the sector.

The DO pin will clock out the normal 20 bit CDS followed by five don't care bits, a copy of the 3004 data bits, and finally three don't care bits.

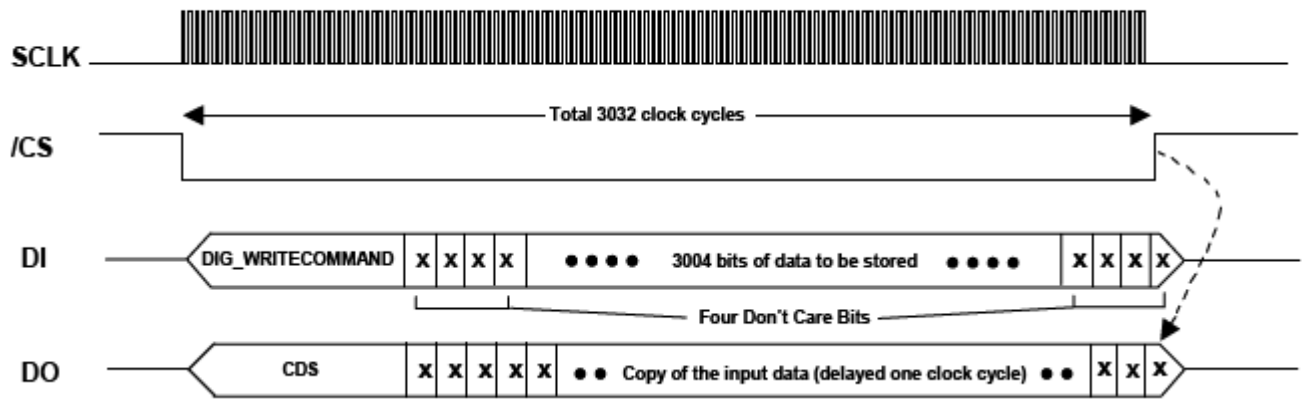
Figure 11 shows a timing diagram, which describes the digital storage process. All timing with the exception of TpSCLK should adhere to the specifications given in **Figure 4** and **Figure 7**.

The TpSCLK specification is replaced by the DTpSCLK when storing digital data.

Note: The DIG_ERASE command should not be used before storing analog data. The device will perform its own internal erase before analog storage.

Figure 11 does not show the DIG_ERASE command,which must be executed on a sector before digital data can be stored.

Figure 11 Writing Digital Data



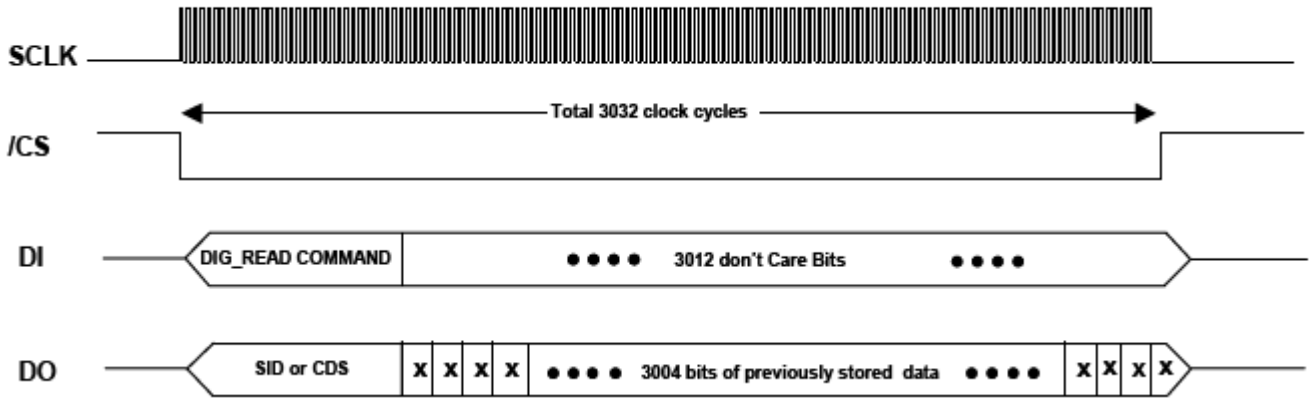
Reading Digital Data

Digital data is read from the device using the DIG_READ command. To read data you must send a DIG_READ command immediately followed by 3012 don't care bits during the same /CS cycle. The data previously stored in the specified sector will begin to appear on the DO pin after the current device status
or SID and four buffer bits. The next 3004 bits are the previously stored data. The first bit shifted out is the first bit that was written. The last bit shifted out is the last bit that was written. There are four random don't care bits following the 3004 bits of user data.

An incomplete read of the sector is allowed. An incomplete read is defined as a read with less than 3032 clock cycles. All incomplete read cycles require one extra SCLK cycle after the /CS signal returns high.

Figure 12 shows a timing diagram, which describes the entire process for a complete sector read. All timing with the exception of TpSCLK should adhere to the specifications given in **Figure 4** and **Figure 7**. The TpSCLK specification is replaced by the DT pSCLK when reading digital data.

Figure 12 Reading Digital Data



Recording Audio Data

When a SET_REC or REC command is issued the device will begin sampling and storing the data present on ANAIN+ and ANAIN- to the specified sector.

After half the sector is used the SAC pin will drop low to indicate that a new command can be accepted.

The device will accept commands as long as the SAC pin remains low. Any command received after the SAC return high will be queued up and executed during the ext SAC cycle.

Figure 13 shows a typical timing diagram and OpCode sequence for a recording operation.

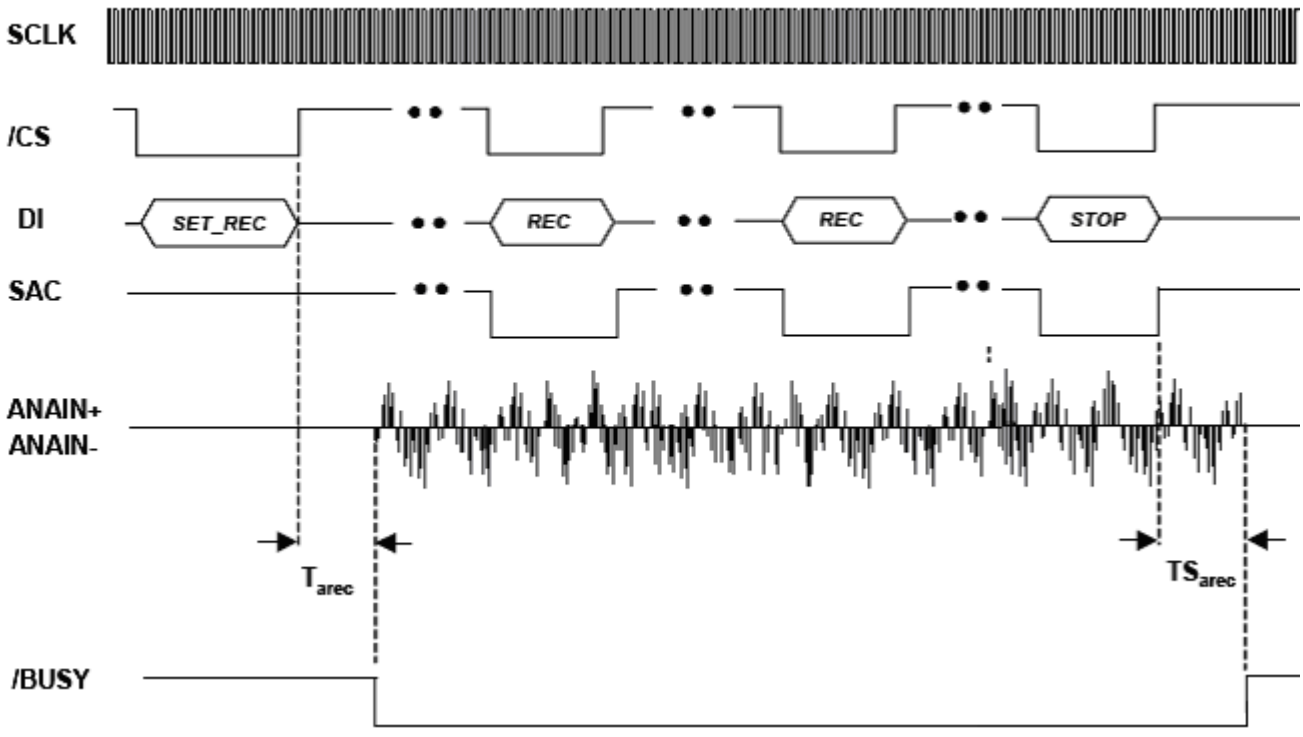
In this example the SET_REC command begins recording at the specified memory location after Tarac time has passed.

Some time later the low going edge on the SAC pin alerts the host processor that the first sector is nearly full. The host processor responds by issuing a REC command before the SAC pin returns high. The REC command instructs the APR6016 to continue recording in the sector immediately following the current sector. When the first sector is full the device automatically jumps to the next sector and returns the SAC signal to a high state to indicate that the second sector is now being used.

At this point the host processor decides to issue a STOP command during the next SAC cycle.

The device follows the STOP command and terminates recording after TSarec. The /BUSY pin indicates when actual recording is taking place.

Figure 13 Typical Recording Sequence

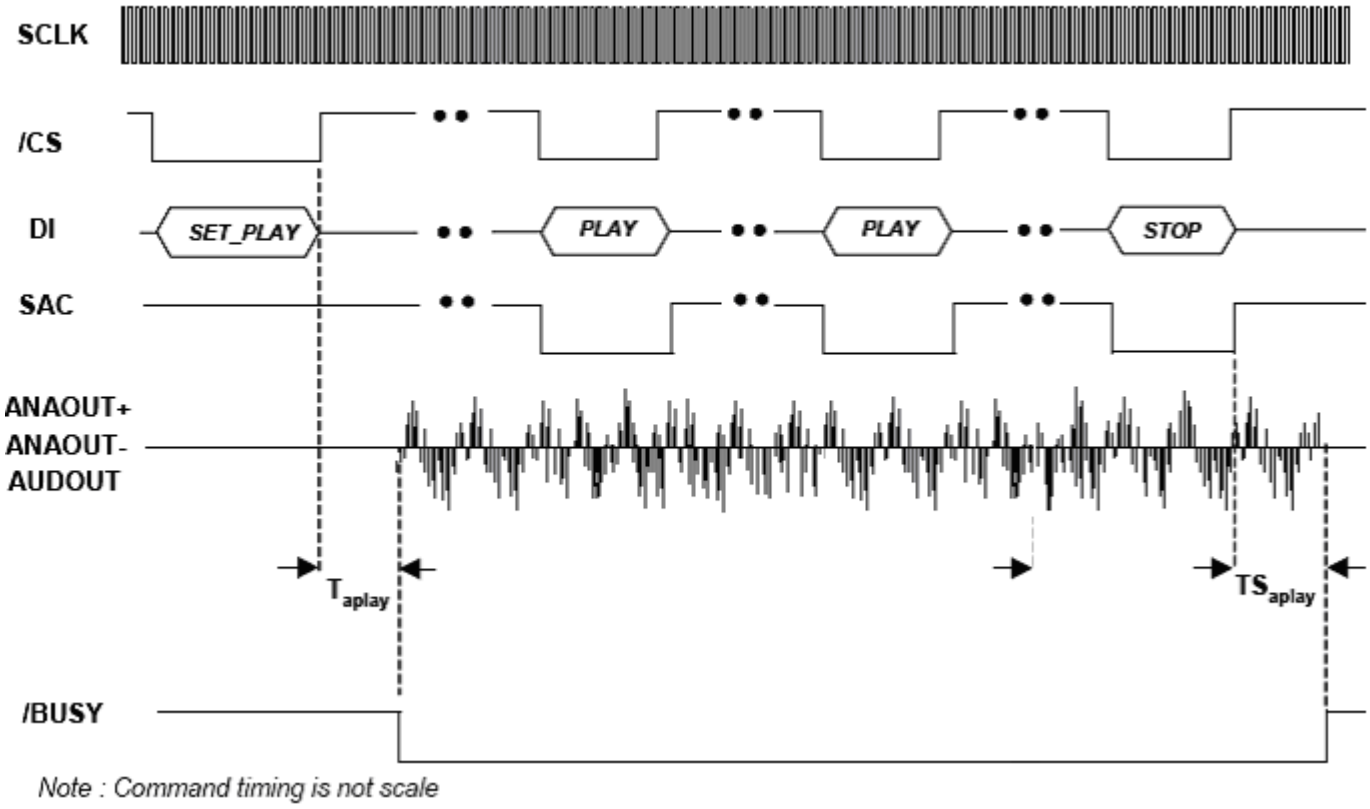


Playing Back Audio Data

When a SET_PLAY or PLAY command is issued the device will begin sampling the data in the specified sector and produce a resultant output on the AUDOUT,ANAOUT-, and ANAOUT+ pins. After half the sector is used the SAC pin will drop low to indicate that a new command can be accepted. The device will accept commands as long as the SAC pin remains low. Any command received after the SAC returns high will be queued up and executed during the next SAC cycle.

Figure 14 shows a typical timing diagram and OpCode sequence for a playback operation. The SET_PLAY command begins playback at the specified memory location after Taplay time has passed. Some time later the low going edge on the SAC pin alerts the host processor that half of the first sector has been played back. The host processor responds by issuing a PLAY command during the SAC low time. The PLAY command instructs the APR6016 to continue playback of the sector immediately following the current sector. When the first sector has been played back the device jumps to the next sector and returns the SAC signal to a high state to indicate that the second sector is now being played. At this point the host processor decides to issue a STOP command during the next available SAC low time. The device follows the STOP command and terminates playback after TSaplay The /BUSY pin indicates when actual playback is taking place.

Figure 14 Typical Playback Sequence



Note : Command timing is not scale

Handshaking signals

Several signals are included in the device that allow for handshaking. These signals can simplify message management significantly depending on the message management scheme used.The /INT signal can be used to generate interrupts to the processor when attention is required by the APR6016 This pin is normally high and goes low when an interrupt is requested. An interrupt is generated whenever an EOD or Overflow occurs. An interrupt is also generated after a PWRUP command if a low battery VCC is sensed.
The **SAC** signal is used to determine when the device is nearing the end of the current memory segment during a record, play or forward operation. The **SAC** signal is in a normally high state. The signal goes low after half the currently active segment has been played or recorded.

The signal returns to a high state after the entire segment has been played or recorded.
The microprocessor should sense the low edge of the SAC signal as an indicator that the next segment needs to be selected, and do so before the SAC signal returns high.
Failing to specify the next command before the current segment is exhausted (either during recording or playback) will result in a noticeable gap during playback.
The /BUSY pin indicates when the device is performing either a play, record or fast-forward function. The host microprocessor can monitor the busy pin to confirm the status of these commands.
The Busy pin is normally high and goes low while the device is busy. The low time is governed by the length of recording or playback specified by the user.

Sampling Rate and Voice Quality

The Nyquist Sampling Theorem requires that the highest frequency component a sampling system can accommodate without the introduction of aliasing errors is equal to half the sampling frequency. The APR6016 automatically filters its input, based on the selected sampling frequency, to meet this requirement.
Higher sampling rates increase recording bandwidth,and hence voice quality, but also use more memory cells for the same amount of recording time.The APR6016 accommodates sampling rates as high as 8kHz.Lower sampling rates use less memory cells and effectively increase the duration capabilities of the device, but also reduce recording bandwidth.The APR6016 allows sampling rates as low as 4kHz.
Designers can thus control the quality/duration trade-off by controlling the sampling frequency. Sampling frequency can be controlled by the use of the PWRUP command. This command can change sampling frequency regardless of whether the internal oscillator is used or an external clock is used.
The APR6016 derives its sampling clock from one of two sources: internal or external. If a clocking signal is present on the EXTCLK input the device would automatically use this signal as the sampling clock source. If no input is present on the EXTCLK input the device automatically defaults to the internal clock source.
When the EXTCLK pin is not used it should be tied to GND.
An internal clock divider is provided so that external clock signals can be divided down to a desired sampling rate. This allows high frequency signals of up to 10 MHz to be fed into the EXTCLK pin. Using this feature simplifies designs by allowing use of a clock already present in the system, as opposed to having to generate or externally divide down a custom clock. Details for programming the clock divider are described in the SPI interface section under the PWRUP paragraph.
The default power up condition for the APR6016 is to use the internal oscillator at sampling frequency of 6.4kHz.

Storage Technology

The APR6016 stores voice signals by sampling incoming voice data and storing the sampled signals directly into FLASH memory cells. Each FLASH cell can support voltage ranges from 1 to 256 levels. These 256 discrete voltage levels are the equivalent of eight (28=256) bit binary encoded values. During playback the stored signals are retrieved from memory, smoothed to form a continuous signal and finally amplified before being fed to an external speaker amplifier.

Squelch

The APR6016 is equipped with an internal squelch feature. The Squelch circuit automatically attenuates the output signal by 6dB during quiet passages in the playback material. Muting the output signal during quiet passages help to eliminate background noise.Background noise may enter the system in a number of ways including: present in the original signal, natural noise present in some power amplifier designs, or induced through a poorly filtered power supply.The response time of the squelch circuit is controlled by the time constant of the capacitor connected to the SQLCAP pin. The recommended value of this capacitor is 1.0 μF. The squelch feature can be disabled by the connection of the SQLCAP pin to VCC.The active low output /SQL goes low whenever the internal squelch activates. This signal can be used to squelch the output power amplifier. Squelching the output amplifier results in further reduction of noise;especially when the power amplifier is run at high gain & loud volumes.

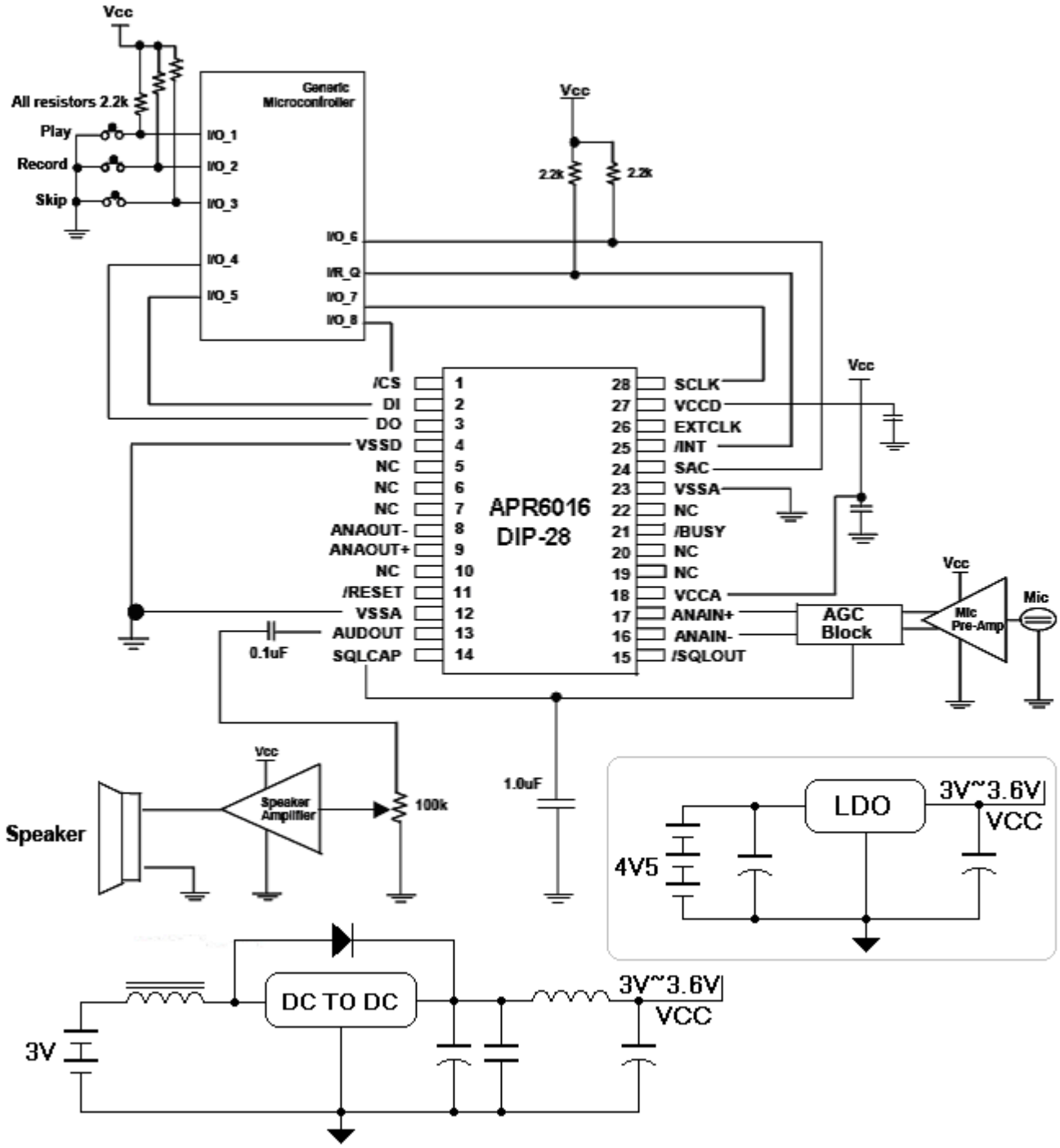
Sample Application

Figure 15 shows a sample application utilizing a generic microcontroller and SPI interface for message management.

The microcontroller uses three general-purpose inputs for the play, record and skip buttons. Five general purpose I/O signals are utilized in the SPI interface. The /RESET and /BUSY signal are not used in this design.

The output signal must be amplified in order to drive a Speaker. Several vendors supply integrated speaker amplifiers that can be used for this purpose. A microphone amplifier and AGC are recommended. Both blocks are optional. Several vendors supply integrated microphone/AGC amplifiers that can be used for this purpose. *Note that the AGC circuit can be simplified by using the SQLCAP signal as a peak detector Signal.*

Figure 15 Sample Schematic using PDIP package



Pin Descriptions

Table three shows pin descriptions for the APR6016 device. All pins are listed in numerical order with the exception of VCC, VSS and NC pins, which are listed at the end of the Table.

Table 3 APR6016 28 Pin Number & Description

Pin Name	Pin No. 28 pin DIP	Pad No. (Die)	Functionality
SAC	24	26	**Sector Address Control Output:** This active low output indicates when the device is nearing the end of the current segment.
/INT	25	29	**Interrupt Output:** This active low open drain output goes low whenever the device reaches the end of a message or the device overflows.When connected to the interrupt input of the host microcontroller this output can be used to implement powerful message management options.
EXTCLK	26	30	**External Clock Input:** This input can be used to feed the device an external sample clock instead of using the internal sampling clock. This pin should be connected to VSSA when not in use.
SCLK	28	34	**SPI Clock Input:** Data is clocked into the device through the DI pin upon the rising edge of this clock. Data is clocked out of the part through the DO pin on the falling edge
/CS	1	1	**Chip Select Input:** This active low input selects the device as the currently active slave on the SPI interface. When this pin is high the device tri-states the DO pin and ignores data on the DI pin.
DI	2	2	**Data Input:** The DI input pin receives the digital data input from the SPI bus. Data is clocked on the rising edge of the SCLK input.
DO	3	3	**Data Output:** Data is available after the falling edge of the SCLK input.
ANAOUT-	8	8	**Negative Audio Output:** This is the negative audio output for playback of prerecorded messages. This output is usually fed to the negative input of a differential input power amplifier. The power amplifier drives an external speaker.
ANAOUT+	9	9	**Positive Audio Output:** This is the positive audio output for playback of prerecorded messages. This output is usually fed to the positive input of a differential input power amplifier. The power amplifier drives an external speaker.
/RESET	11	10	**Reset Input:** This active low input clears all internal address registers and restores the device to its power up defaults.
AUDOUT	13	14	**Single Ended Audio Output:** This is the audio output for playback of pre-recorded messages. This output is usually fed to the input of a power amplifier for driving an external speaker.
SQLCAP	14	15	**Squelch Capacitor I/O:** This pin controls the attack time of the squelch circuitry. Connect his pin to GND through a 1.0 μF capacitor to enable the squelch feature. The capacitor's time constant will affect how quickly the squelch circuitry reacts. Connect this pin to VCCA to disable the squelch feature.
/SQLOUT	15	16	**Squelch Output:** This active low output indicates when the internal squelch circuitry has activated. This signal can be used to automatically squelch the external power amplifier. Squelching the external power amplifier can result in an even greater reduction of background noise.
ANAIN-	16	17	**Inverting Analog Input:** This input is the inverting input for the analog signal that the user wishes to record. When the device is used in a differential input configuration this pin should receive a 16 mV peak-to-peak input coupled through a 0.1 μF capacitor. When the device is used in a single ended input onfiguration this input should be tied to VSSA through a 0.1 μF capacitor
ANAIN+	17	18	**Non-Inverting Analog Input:** This input is the non-inverting input for the analog signal that the user wishes to record. When the device is used in a differential input configuration this pin should receive a 16 mV peak-to-peak input coupled through a 0.1 uF capacitor. When the device is used in a single ended input configuration this pin should receive a 32 mV peak-to-peak input coupled through a 0.1uF capacitor.

Pin Name	Pin No. 28 pin DIP	Pad No. (Die)	Functionality
/BUSY	21	22	**Busy Output:** This active low output is low during either a record playback or fast forward operation. The pin is tri-stated otherwise. This pin can be connected to an LED to indicate playback/record operation to the user. This pin can also be connected to an external microcontroller as an indication of the status of playback record forward or digital operation.
VCCD	27	31,32,33	**Digital Power Supply:** This connection supplies power for all on chip digital circuitry. This pin should be connected to the 3.0 V power plane through a via. This pin should also be connected to a 0.1 μF bypass cap as close to the pin as possible.
VCCA	18	19,20	**Analog Power Supply:** This connection supplies power for all on-chip analog circuitry. This pin should be connected to the 3.0 V power plane through a via. This pin should also be connected to a 0.1 uF bypass cap as close to the pin as possible
VSSA	12,23	11,12,13, 23 24,25	**Analog Ground:** These pins should be connected to the ground plane through a via. The connection should be made as close to the pin as possible.
VSSD	4	4,5	**Digital Ground:** This pin should be connected to the ground plane through a via. The connection should be made as close to the pin as possible.
NC	5,6,7, 10,19, 20,22	6,7,21, 27,28	**No Connect:** These pins should not be connected to anything on the board. Connection of these pins to any signal GND or VCC may result in incorrect device behavior or cause damage to the device.

Electrical Characteristics

The following tables list Absolute Maximum Ratings,recommended DC Characteristics, and recommend AC Characteristics for the APR6016 device.

Absolute Maximum Ratings

Stresses greater than those listed in Table 4 may cause permanent damage to the device. These specifications represent a stress rating only.

Operation of the device at these or any other conditions above

those specified in the recommended DC

Characteristics or recommended AC Characteristics of this specification is not implied. Maximum condition for extended periods may affect reliability.

Table 4 Absolute Maximum Ratings.

Item	Symbol	Condition	Min	Max	Unit
Power Supply voltage	V_{CC}	T_A = 25°C	- 0.3	7.0	V
Input Voltage	V_{IN}	T_A = 25°C Device VCC = 3.0 V	- 0.3	5.5	V
Storage Temperature	T_{STG}	--	- 65	150	°C
Temperature Under Bias	T_{BS}	--	- 65	125	°C
Lead Temperature	T_{LD}	< 10s		300	°C

Table 5 DC Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	VCCA, VCCD		2.7	3.0	3.3	V
Operating Temperature	T_A		0		+70	°C
Input High Voltage	V_{IH}	V_{CC} = 2.7V	2.4	3	5.5	V
Input Low Voltage	V_{IL}	V_{CC} = 3.3V	V_{SS} - 0.3V	0	0.4	V
Output High Voltage	V_{OH}	V_{CC} = 2.7V I_{OH}=-1.6mA	VCCD - 0.5V			V
Output Low Voltage	V_{OL}	V_{CC} = 2.7V I_{OL}=1.0mA			0.4	V
Input Leakage Current	I_{IH}	V_{CC} = 3.3V V_{IH}=VCC		0.3	1	μA
Input Leakage Current	I_{IL}	V_{CC} = 3.3V V_{IL}= VSS		0	- 1	μA
Output Tri-state Leakage Current	I_{OZ}	V_{CC} = 3.3V V_{OUT}=VCC or V_{OUT}=VSS			± 1	μA
Operating Current Consumption	I_{CC}	V_{CC} = 3.3V Recording Playback Idle		25 15 2.5		mA mA mA
Standby Current Consumption	I_{CCS}	V_{CC} = 3.3V After 20 sec			1	μA

Table 6 AC Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
ANAIN+ or ANAIN- input voltage	V_{MI}			45	50	mV_{P-P}
ANAIN+ input resistance	R_{ANAIN}			3		K
ANAIN+/ANAIN- Gain	G_{ANAIN}			22	23	DB
ANAOUT output voltage	V_{ANAOUT}			560	700	mV_{p-p}
Total Harmonic Distortion	THD	@ 1kHz & 45mV_{P-P}. input		0.5	1	%
VCC ready to fall /CS	T_{pwrup}	90% of VCC min. specification	10			ms
/RESET low time	T_{loRST}		1			ms
Rise /RESET to fall /CS	T_{Rdone}		1			ms
/CS fall to clock edge	T_{fCS}		500			ns
SPI Data set-up time	T_{suDI}		200			ns
Period SPI clock	**T_{pSCLK}**		**1000**			ns
SPI data hold time	T_{hDI}		200			ns
SPI dock low time	T_{loSCLK}		400			ns
SPI clock high time	T_{hiSCLK}		400			ns
Clock to rising edge of /CS	T_{rCS}		200			ns
Fall of /CS to DO output	$T_{f\,SCLK}$				200	ns
Fall of SCLK to data out valid	T_{fSCLK}				1000	ns
Rise of /CS to DO high Z	T_{hzDO}				500	ns
Period SPI clock for Digital read write	**DT_{pSCLK}**	@4kHz Internal sample clock @8kHz Internal sample clock External sample clock	**500** **250** equation*1*			**μs** **μs** s
First SET_REC command To start recording	T_{arec}	@4kHz Internal sample clock @8kHz Internal sample clock External sample clock	376 188 equation*2*			ms ms s

Item	Symbol	Condition	Min	Typ	Max	Unit
Rise of SAC after STOP Command to end Of recording	TS_{arec}	@4kHz Internal sample clock @8kHz Internal sample clock External sample clock	658 329 equation*2*			ms ms s
First SET_PLAY command To audio output	T_{aplay}	@4kHz Internal sample clock @8kHz Internal sample clock External sample clock	658 329 equation*2*			ms ms s
STOP after SET_PLAY or PLAY to end of audio output	TS_{aplay}	@4kHz Internal sample clock @8kHz Internal sample clock External sample clock	376 188 equation*2*			ms ms s
SAC period	T_{pSAC}	REC, PLAY @4kHz REC, PLAY @8kHz REC, PLAY @EXTCLK FWD @4kHz FWD @8kHz FWD @EXTCLK	752 376 equation*3* 2 1 equation*4*			ms ms s ms ms s
SAC low time	T_{loSAC}	REC, PLAY @4kHz REC, PLAY @8kHz REC, PLAY @EXTCLK FWD @4kHz FWD @8kHz FWD @EXTCLK	94 47 equation*5* 0.25 0.125 equation *6*			ms ms s ms ms s
See Figure 6 and Table 1	T_{next1}		5			μs
See Figure 6 and Table 1	T_{next2}		5			Ms
See Figure 6 and Table 1	T_{next3}	@4kHz Internal sample clock @8kHz Internal sample clock External sample clock		752 376 equation3		ms ms s
See Figure 6 and Table 1	T_{next4}	Previous command = SET_REC, REC, SET_PLAY, PLAY @4kHz Internal sample clock @8kHz Internal sample clock External sample clock		 470 235 方程式*7*		 ms ms s
		Previous command = SET_FWD, FWD @4kHz Internal sample clock @8kHz Internal sample clock External sample clock		 1.25 0.625 方程式*8*		 ms ms s
		Previous command = All Others @4kHz Internal sample clock @8kHz Internal sample clock External sample clock		 5 5 5		 μs μs μs

Notes:

$$Equation1 = \frac{ExternalClockPeriod}{2(PrescalerValue)}$$

$$Equation2 = \frac{1504(ExternalClockPeriod)}{PrescalerValue}$$

$$Equation3 = \frac{3008(ExternalClockPeriod)}{PrescalerValue}$$

$$Equation4 = \frac{8(ExternalClockPeriod)}{PrescalerValue}$$

$$Equation5 = \frac{376(ExternalClockPeriod)}{PrescalerValue}$$

$$Equation6 = \frac{ExternalClockPeriod}{PrescalerValue}$$

$$Equation7 = \frac{1880(ExternalClockPeriod)}{PrescalerValue}$$

$$Equation8 = \frac{5(ExternalClockPeriod)}{PrescalerValue}$$

$$Equation9 = \frac{2632(ExternalClockPeriod)}{PrescalerValue}$$

Figure 18 Bond Pad Layout and Coordinates

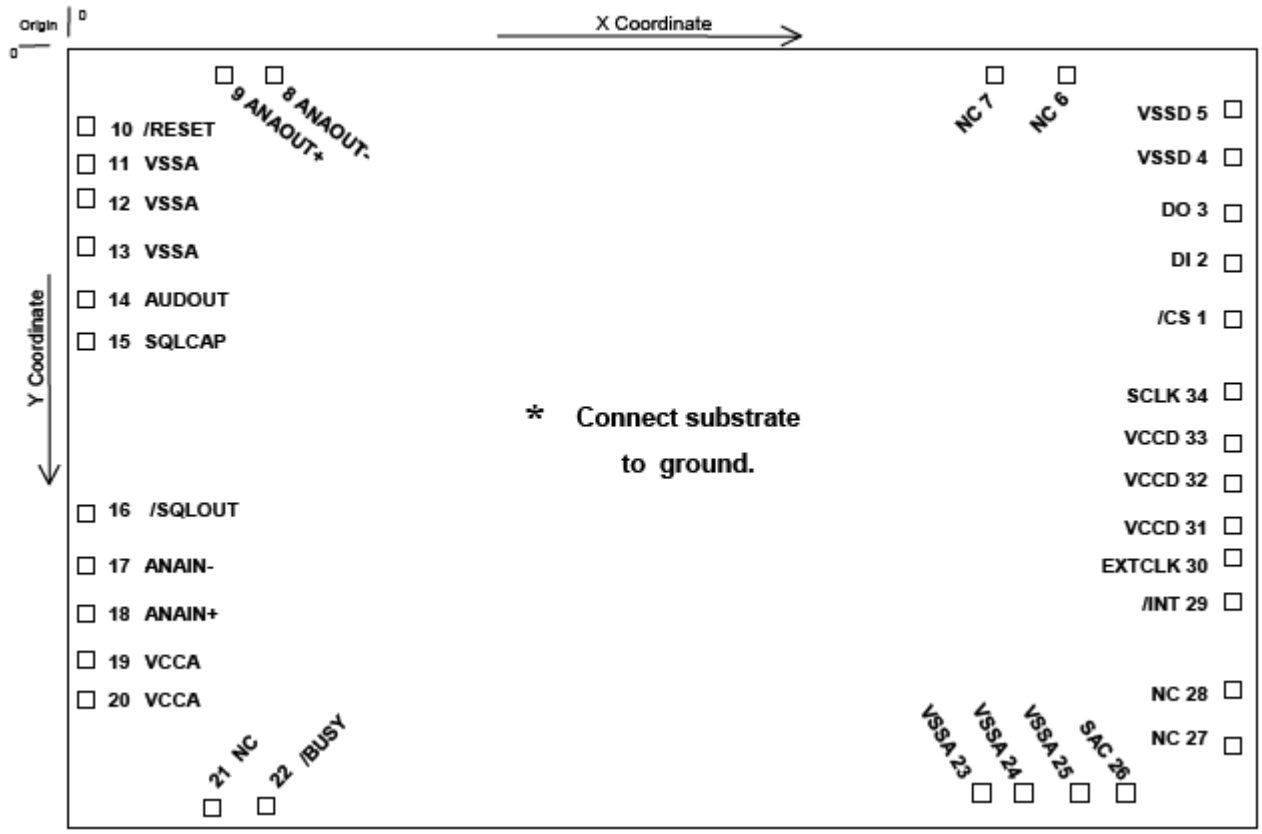
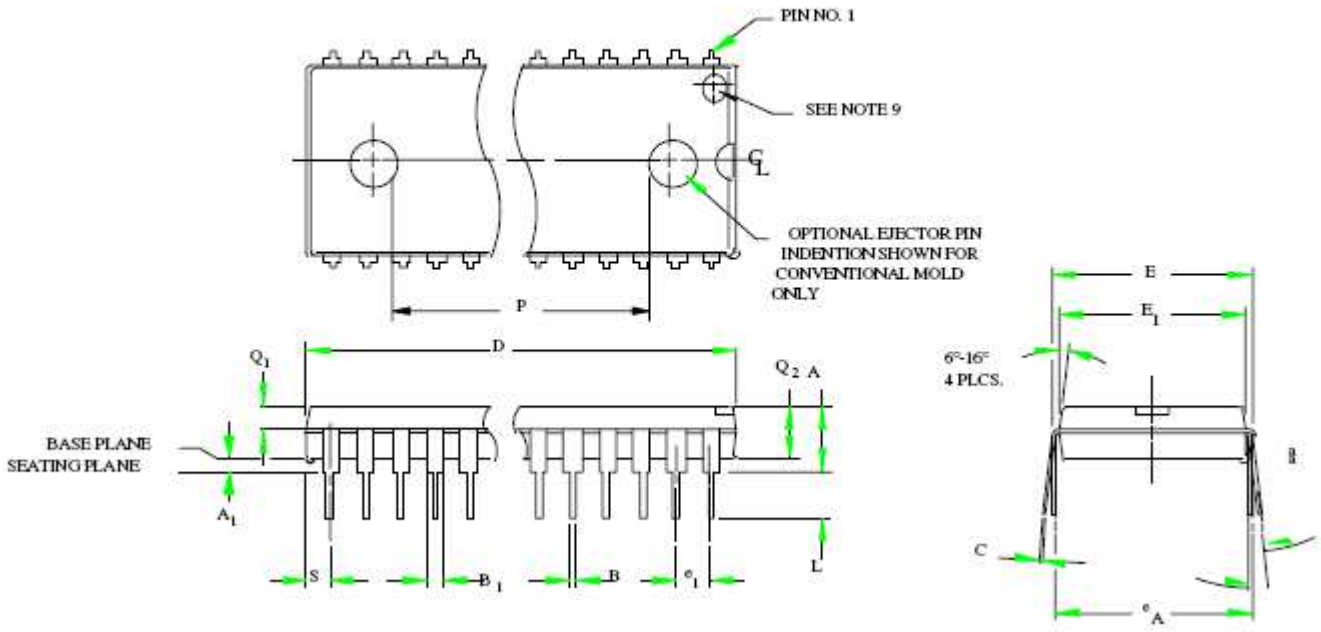


Table 7 Coordinate Information

Pad Number	Pad Name	X Coordinate	Y Coordinate
1	/CS	8008	1460
2	DI	8008	1173
3	DO	8008	865
4	VSSD	8008	620
5	VSSD	8008	393
6	NC	7654	119
7	NC	7271	119
8	ANAOUT-	570	119
9	ANAOUT+	299	119
10	/RESET	119	384
11	VSSA	119	665
12	VSSA	119	837
13	VSSA	119	1124
14	AUDOUT	119	1454
15	SQLCAP	119	1894
16	/SQLOUT	119	2528
17	ANAIN-	119	2805
18	ANAIN+	119	3076
19	VCCA	119	3407
20	VCCA	119	3637
21	NC	258	4116
22	/BUSY	558	4116
23	VSSA	7172	4116
24	VSSA	7345	4116
25	VSSA	7517	4116
26	SAC	7765	4116
27	NC	8008	3806
28	NC	8008	3506
29	/INT	8008	3114
30	EXTCLK	8008	2808
31	VCCD	8008	2433
32	VCCD	8008	2200
33	VCCD	8008	2029
34	SCLK	8008	1802

DIE SIZE : 8230μm x 4360μm
PAD SIZE : 100μm x 100μm
DIE THICKNESS : Approximately 25 mils

Figure 17 28 pin dual inline package (DIP)

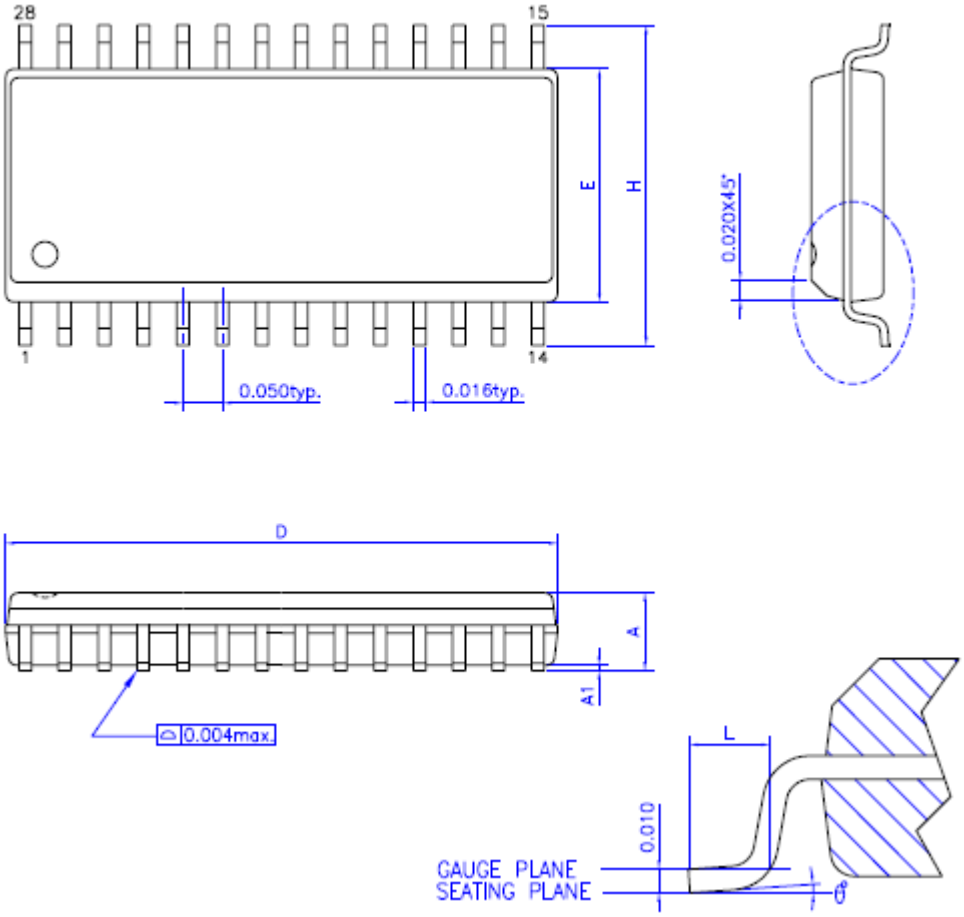


SYMBOL	INCHES			MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A			.190			4.83	
A_1	.015			0.38			
B	.015	.018	.022	0.38	0.46	0.56	
B_1	.055	.060	.065	1.40	1.52	1.65	
C	.008	.010	.012	0.20	0.25	0.30	
D	1.445	1.450	1.455	36.70	36.83	36.96	5
E	.600		.625	15.24		15.88	
E_1	.530	.540	.550	13.46	13.72	13.97	5
e_1	.100 BSC			2.54 BSC			
e_A	.600 BSC			15.24 BSC			
L	.125		.135	3.18		3.43	3
aa	0°		15°	0°		15°	4
N	28			28			
P	.685			17.40			
Q_1	.065	.070	.075	1.65	1.78	1.91	
Q_2		.150			3.18		
S	.070	.075	.080	1.78	1.91	2.03	

NOTES:

1. REFER TO APPLICABLE SYMBOL LIST.
2. DIMENSIONING AND TOLERANCE PER ANSI Y14.5-1982.
3. APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE MAXIMUM QUANTITY OF LEAD POSITIONS
5. DIMENSION D & E ARE TO BE MEASURED AT MAXIMUM MATERIAL CONDITION BUT DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 INCH/0.254 mm.
6. CONTROLLING DIMENSION: INCH
7. DIMENSION A, A1 & L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GUAGE GS-3.
8. THIS PACKAGE CONFORMS TO JEDEC REFERENCE MS-011, VARIATION AB.
9. IT IS AN OPTION TO SHOW PIN 1 IDENTIFIER.

- ***PACKAGE : SOP-28***



SYMBOLS	MIN.	MAX.
A	0.093	0.104
A1	0.004	0.012
D	0.697	0.713
E	0.291	0.299
H	0.394	0.419
L	0.016	0.050
θ°	0	8

UNIT : INCH

NOTES:
1.JEDEC OUTLINE : MS-013 AE
2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3.DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

- **REVISION HISTORY :**

Date	Revision #	Description	Page
MAY. 30.2008	1.2	Figure-8 Format for CDS bit stream,the LSB change to MSB, the MSB change to LSB	8
NOV. 19.2009	1.3	Add the package SOP-28 outline	23