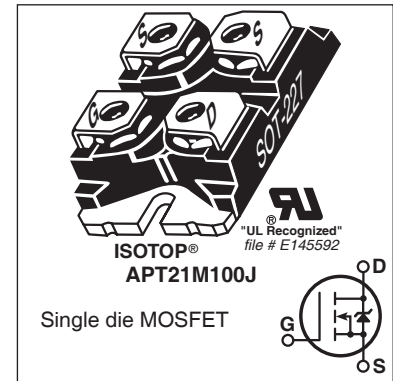



## N-Channel MOSFET

Power MOS 8™ is a high speed, high voltage N-channel switch-mode power MOSFET. A proprietary planar stripe design yields excellent reliability and manufacturability. Low switching loss is achieved with low input capacitance and ultra low  $C_{rss}$  "Miller" capacitance. The intrinsic gate resistance and capacitance of the poly-silicon gate structure help control slew rates during switching, resulting in low EMI and reliable paralleling, even when switching at very high frequency. Reliability in flyback, boost, forward, and other circuits is enhanced by the high avalanche energy capability.



www.DataSheet4U.com

### FEATURES

- Fast switching with low EMI/RFI
- Low  $R_{DS(on)}$
- Ultra low  $C_{rss}$  for improved noise immunity
- Low gate charge
- Avalanche energy rated
- RoHS compliant 

### TYPICAL APPLICATIONS

- PFC and other boost converter
- Buck converter
- Two switch forward (asymmetrical bridge)
- Single switch forward
- Flyback
- Inverters

### Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
$I_D$	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	21	A
	Continuous Drain Current @ $T_C = 100^\circ\text{C}$	13	
$I_{DM}$	Pulsed Drain Current <sup>①</sup>	120	
$V_{GS}$	Gate-Source Voltage	±30	V
$E_{AS}$	Single Pulse Avalanche Energy <sup>②</sup>	1875	mJ
$I_{AR}$	Avalanche Current, Repetitive or Non-Repetitive	16	A

### Thermal and Mechanical Characteristics

Symbol	Characteristic	Min	Typ	Max	Unit
$P_D$	Total Power Dissipation @ $T_C = 25^\circ\text{C}$			462	W
$R_{\theta JC}$	Junction to Case Thermal Resistance			0.27	°C/W
$R_{\theta CS}$	Case to Sink Thermal Resistance, Flat, Greased Surface		0.15		
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55		150	°C
$V_{Isolation}$	RMS Voltage (50-60Hz Sinusoidal Waveform from Terminals to Mounting Base for 1 Min.)	2500			V
$W_T$	Package Weight		1.03		oz
			29.2		g
Torque	Terminals and Mounting Screws.			10	in-lbf
				1.1	N-m

**Static Characteristics**
**T<sub>J</sub> = 25°C unless otherwise specified**
**APT21M100J**

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V <sub>BR(DSS)</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	1000			V
ΔV <sub>BR(DSS)</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I <sub>D</sub> = 250μA		1.15		V/°C
R <sub>DS(on)</sub>	Drain-Source On Resistance <sup>③</sup>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 16A		0.34	0.40	Ω
V <sub>GS(th)</sub>	Gate-Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 2.5mA	3	4	5	V
ΔV <sub>GS(th)</sub> /ΔT <sub>J</sub>	Threshold Voltage Temperature Coefficient			-10		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 1000V V <sub>GS</sub> = 0V			100	μA
		T <sub>J</sub> = 25°C T <sub>J</sub> = 125°C			500	
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>GS</sub> = ±30V			±100	nA

**Dynamic Characteristics**
**T<sub>J</sub> = 25°C unless otherwise specified**

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> = 50V, I <sub>D</sub> = 16A		34		S
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 25V f = 1MHz		8500		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			115		
C <sub>oss</sub>	Output Capacitance			700		
C <sub>o(cr)</sub> <sup>④</sup>	Effective Output Capacitance, Charge Related	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 667V		290		pF
C <sub>o(er)</sub> <sup>⑤</sup>	Effective Output Capacitance, Energy Related			150		
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> = 0 to 10V, I <sub>D</sub> = 16A, V <sub>DS</sub> = 500V		260		nC
Q <sub>gs</sub>	Gate-Source Charge			46		
Q <sub>gd</sub>	Gate-Drain Charge			125		
t <sub>d(on)</sub>	Turn-On Delay Time	<b>Resistive Switching</b> V <sub>DD</sub> = 667V, I <sub>D</sub> = 16A R <sub>G</sub> = 2.2Ω <sup>⑥</sup> , V <sub>GG</sub> = 15V		39		ns
t <sub>r</sub>	Current Rise Time			35		
t <sub>d(off)</sub>	Turn-Off Delay Time			130		
t <sub>f</sub>	Current Fall Time			33		

**Source-Drain Diode Characteristics**

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I <sub>S</sub>	Continuous Source Current (Body Diode)	MOSFET symbol showing the integral reverse p-n junction diode (body diode)			100	A
I <sub>SM</sub>	Pulsed Source Current (Body Diode) <sup>①</sup>				200	
V <sub>SD</sub>	Diode Forward Voltage	I <sub>SD</sub> = 16A, T <sub>J</sub> = 25°C, V <sub>GS</sub> = 0V			1	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>SD</sub> = 16A <sup>②</sup> di <sub>SD</sub> /dt = 100A/μs, T <sub>J</sub> = 25°C		1140		ns
Q <sub>rr</sub>	Reverse Recovery Charge				30	
dv/dt	Peak Recovery dv/dt	I <sub>SD</sub> ≤ 16A, di/dt ≤ 1000A/μs, V <sub>DD</sub> = 667V, T <sub>J</sub> = 125°C			10	V/ns

① Repetitive Rating: Pulse width and case temperature limited by maximum junction temperature.

② Starting at T<sub>J</sub> = 25°C, L = 14.65mH, R<sub>G</sub> = 2.2Ω, I<sub>AS</sub> = 16A.

③ Pulse test: Pulse Width < 380μs, duty cycle < 2%.

④ C<sub>o(cr)</sub> is defined as a fixed capacitance with the same stored charge as C<sub>OSS</sub> with V<sub>DS</sub> = 67% of V<sub>(BR)DSS</sub>.

⑤ C<sub>o(er)</sub> is defined as a fixed capacitance with the same stored energy as C<sub>OSS</sub> with V<sub>DS</sub> = 67% of V<sub>(BR)DSS</sub>. To calculate C<sub>o(er)</sub> for any value of V<sub>DS</sub> less than V<sub>(BR)DSS</sub>, use this equation: C<sub>o(er)</sub> = -2.47E-7/V<sub>DS</sub><sup>2</sup> + 4.36E-8/V<sub>DS</sub> + 8.44E-11.

⑥ R<sub>G</sub> is external gate resistance, not including internal gate resistance or gate driver impedance. (MIC4452)

Microsemi reserves the right to change, without notice, the specifications and information contained herein.

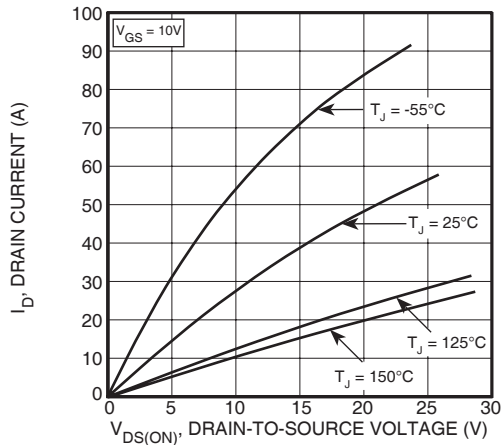


Figure 1, Output Characteristics

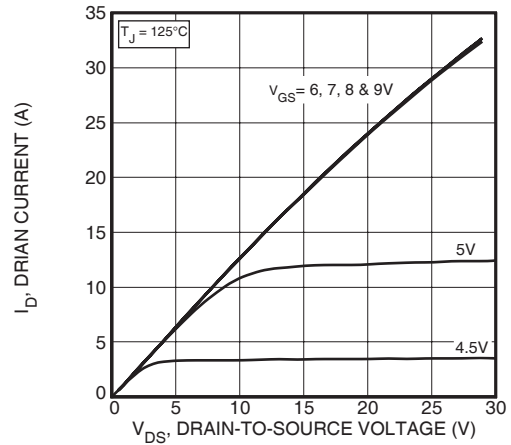


Figure 2, Output Characteristics

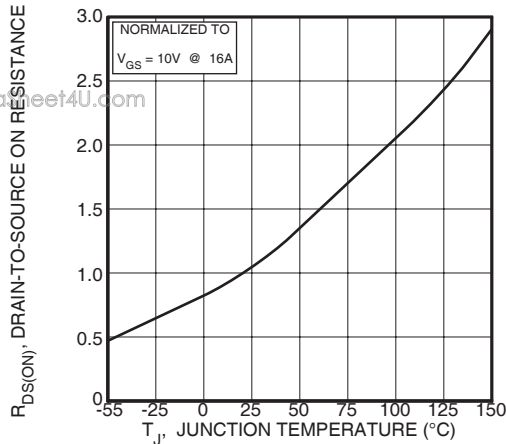


Figure 3,  $R_{DS(ON)}$  vs Junction Temperature

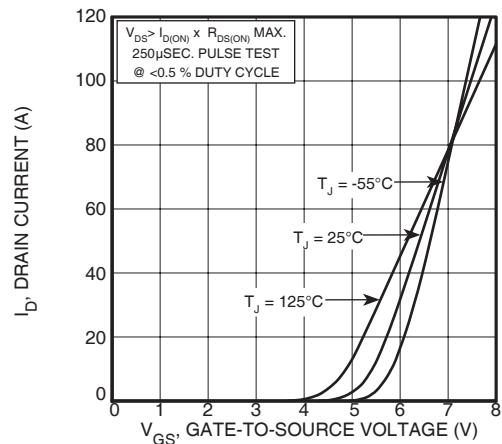


Figure 4, Transfer Characteristics

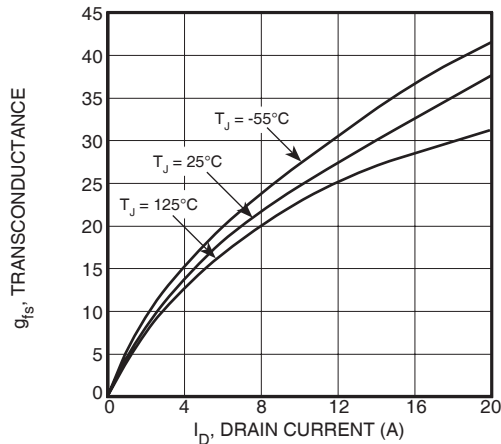


Figure 5, Gain vs Drain Current

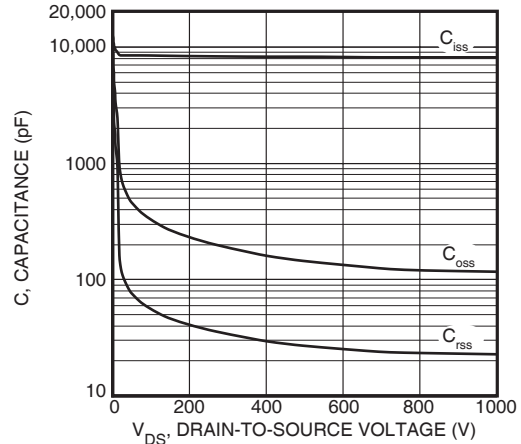


Figure 6, Capacitance vs Drain-to-Source Voltage

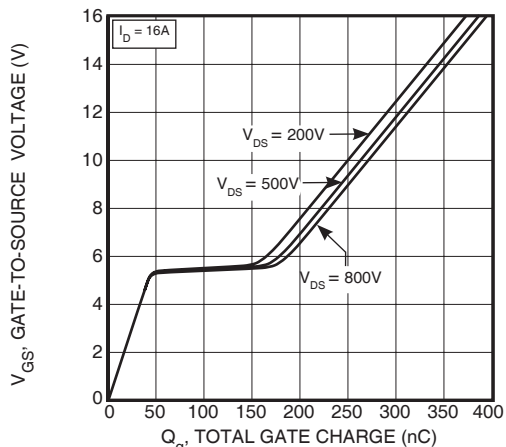


Figure 7, Gate Charge vs Gate-to-Source Voltage

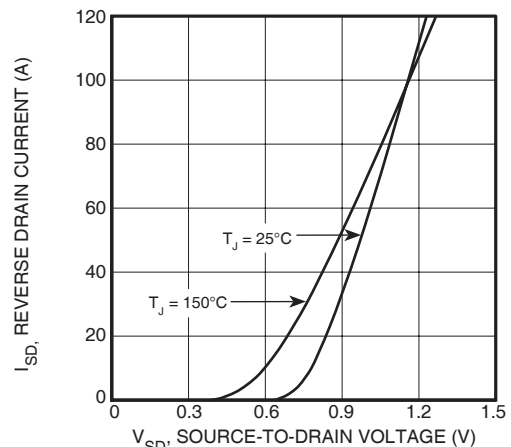


Figure 8, Reverse Drain Current vs Source-to-Drain Voltage

www.DataSheet4U.com

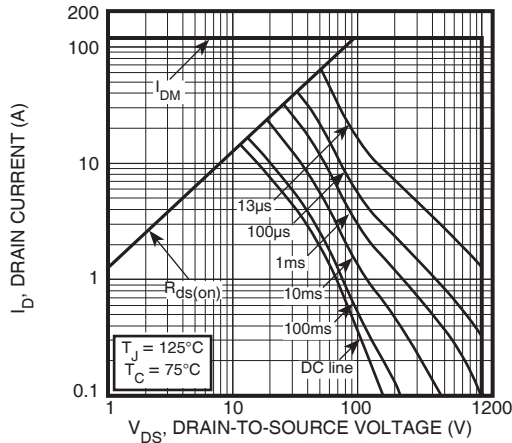


Figure 9, Forward Safe Operating Area

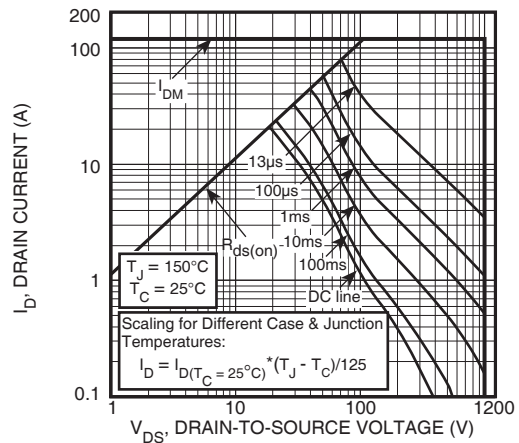


Figure 10, Maximum Forward Safe Operating Area

www.DataSheet4U.com

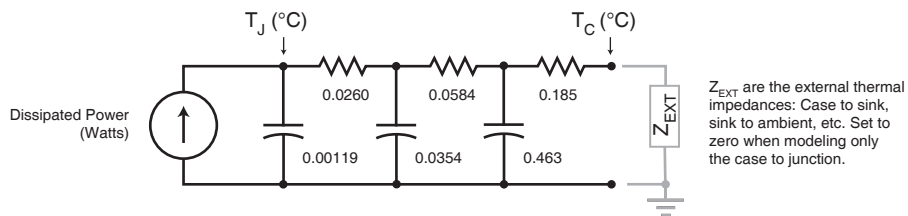


Figure 11, Transient Thermal Impedance Model

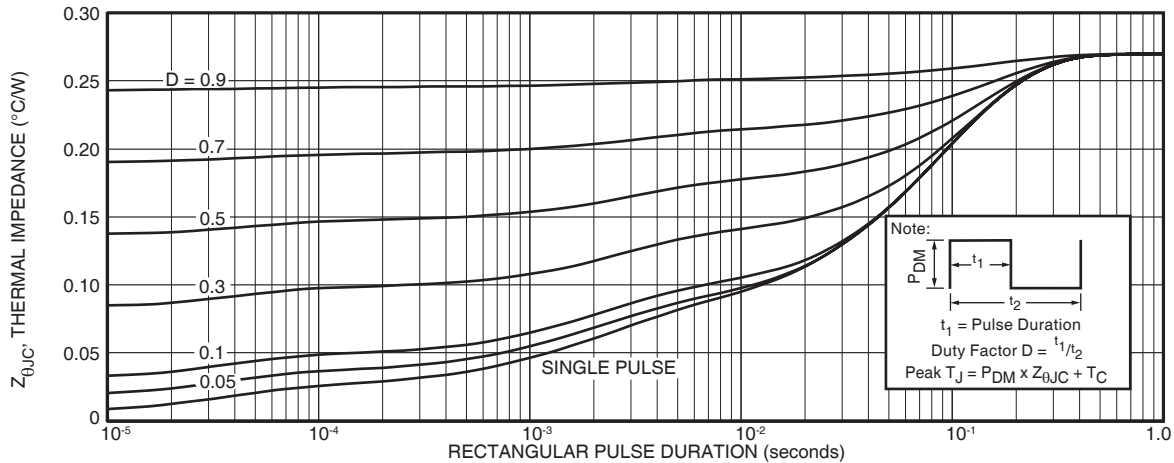
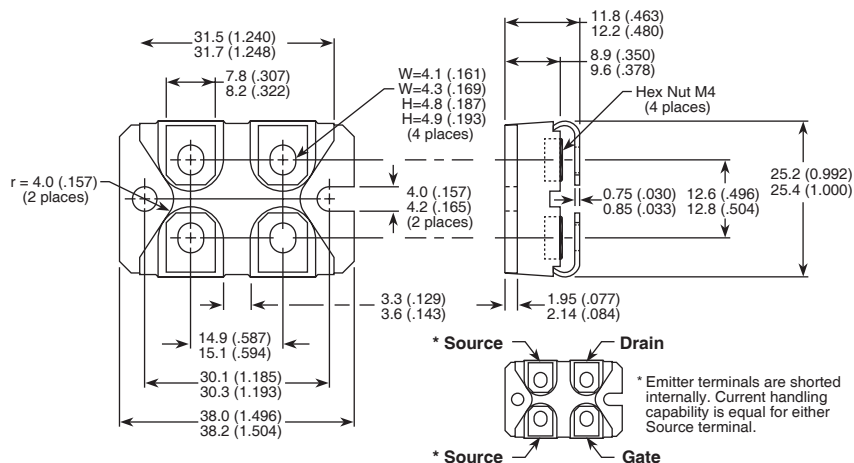


Figure 12. Maximum Effective Transient Thermal Impedance Junction-to-Case vs Pulse Duration

SOT-227 (ISOTOP®) Package Outline



\* Source Drain  
\* Source Gate  
\* Emitter terminals are shorted internally. Current handling capability is equal for either Source terminal.

Dimensions in Millimeters and (Inches)

ISOTOP® is a registered trademark of ST Microelectronics NV. Microsemi's products are covered by one or more of U.S. patents 4,895,810 5,045,903 5,089,434 5,182,234 5,019,522 5,262,336 6,503,786 5,256,583 4,748,103 5,283,202 5,231,474 5,434,095 5,528,058 and foreign patents. US and Foreign patents pending. All Rights Reserved.