8-PIN SYNCHRONOUS PWM CONTROLLER

FEATURES

- **1A Peak Output Drive Capability**
- **0.8V Reference Voltage**
- **Shuts off both drivers at shorted output and shutdown**
- Operating with single 5V or 12V supply voltage
- Stable with ceramic capacitors
- Internal 200KHz Oscillator
- Soft-Start Function
- Protects the output when control FET is shorted
- Synchronous Controller in 8-Pin Package
- RoHS Complaint

APPLICATIONS

- DDR Memory Application
- Low voltage distributed DC-DC
- Graphic Cards
- Low cost on-board DC to DC such as 5V to 2.5V, 1.8V or 0.8V

DESCRIPTION

The APU3137 controller IC is designed to provide a low cost and high performance synchronous Buck regulator for on-board DC to DC converter applications. The output voltage can be set as low as 0.8V and higher voltage can be obtained with an external voltage divider. High peak current gate drivers provide fast switching transition for applications requiring high output current in the range of 15A to 20A.

This device features an internal 200KHz oscillator, under-voltage lockout for both Vcc and Vc supplies, an external programmable soft-start function as well as output under-voltage detection that latches off the device when an output short is detected.

TYPICAL APPLICATION

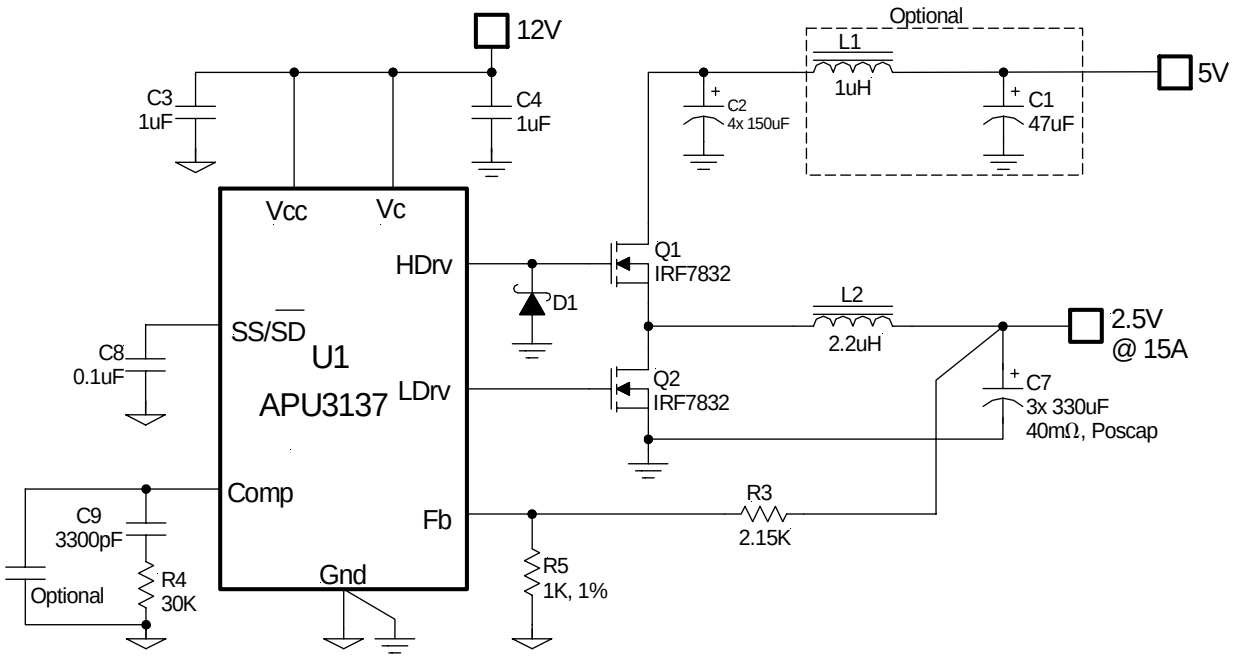


Figure 1 - Typical application of APU3137.

PACKAGE ORDER INFORMATION

T_A (°C)	DEVICE	PACKAGE	FREQUENCY
0 To 70	APU3137M	8-Pin Plastic SOIC NB (M)	200KHz

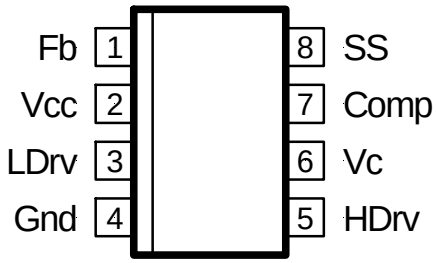
ABSOLUTE MAXIMUM RATINGS

Vcc Supply Voltage ..... -0.5V - 25V
Vc Supply Voltage ..... -0.5V - 25V
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device.

PACKAGE INFORMATION

8-PIN PLASTIC SOIC NB (M)



θ_{JA}=160°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over Vcc=5V, Vc=12V and T_A=0 to 70°C. Typical values refer to T_A=25°C.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Reference Voltage						
Fb Voltage	V_{FB}		0.784	0.800	0.816	V
Fb Voltage Line Regulation	L_{REG}	5<Vcc<12			1.6	mV
UVLO						
UVLO Threshold - Vcc	UVLO Vcc	Supply Ramping Up	4.0	4.25	4.5	V
UVLO Hysteresis - Vcc				0.25		V
UVLO Threshold - Vc	UVLO Vc	Supply Ramping Up	3.0	3.5	3.65	V
UVLO Hysteresis - Vc				0.25		V
UVLO Threshold - Fb	UVLO Fb	Fb Ramping Down	0.3	0.4	0.5	V
UVLO Hysteresis - Fb				0.25		V
Supply Current						
Vcc Dynamic Supply Current	Dyn Icc	Freq=200KHz, C_L=3000pF		6.5	8	mA
Vc Dynamic Supply Current	Dyn Ic	Freq=200KHz, C_L=3000pF		11	14	mA
Vcc Static Supply Current	I_{CCQ}	SS=0V		4	6	mA
Vc Static Supply Current	I_{CQ}	SS=0V		2.5	4	mA
Soft-Start Section						
Charge Current	SS_{IB}	SS=0V	15	22	30	μA

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Error Amp						
Fb Voltage Input Bias Current	I_{FB1}	SS=3V, Fb=1V		0.1		μA
Fb Voltage Input Bias Current	I_{FB2}	SS=0V, Fb=1V		50		μA
Transconductance	GM		600	850	1100	μmho
Oscillator						
Frequency	Freq		180		240	KHz
Ramp-Amplitude Voltage	V_{RAMP}	Note 1		1.25		V
Output Drivers						
Rise Time	Tr	C_L=3000pF (10% to 90%)		35	70	ns
Fall Time	Tf	C_L=3000pF (90% to 10%)		35	70	ns
Dead Band Time	T_{DB}			100		ns
Max Duty Cycle	T_{ON}	Fb=0.7V, Freq=200KHz	85	90		%
Min Duty Cycle	T_{OFF}	Fb=1.5V			0	%

Note 1: Guaranteed by design but not tested in production.

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	Fb	This pin is connected directly to the output of the switching regulator via resistor divider to provide feedback to the Error amplifier.
2	Vcc	This pin provides biasing for the internal blocks of the IC as well as power for the low side driver. A minimum of 1μF, high frequency capacitor must be connected from this pin to ground to provide peak drive current capability.
3	LDrv	Output driver for the synchronous power MOSFET.
4	Gnd	This pin serves as the ground pin and must be connected directly to the ground plane. A high frequency capacitor (0.1 to 1μF) must be connected from VCC and Vc pins to this pin for noise free operation.
5	HDrv	Output driver for the high side power MOSFET. This pin should not go negative (below ground), this may cause problem for the gate drive circuit. It can happen when the inductor current goes negative (Source/Sink), soft-start at no load and for the fast load transient from full load to no load. To prevent negative voltage at gate drive, a low forward voltage drop diode might be connected between this pin and ground.
6	Vc	This pin is connected to a voltage that must be at least 4V higher than the bus voltage of the switcher (assuming 5V threshold MOSFET) and powers the high side output driver. A minimum of 1μF, high frequency capacitor must be connected from this pin to ground to provide peak drive current capability.
7	Comp	Compensation pin of the error amplifier. An external resistor and capacitor network is typically connected from this pin to ground to provide loop compensation.
8	SS / $\overline{SD}$	This pin provides soft-start for the switching regulator. An internal current source charges an external capacitor that is connected from this pin to ground which ramps up the output of the switching regulator, preventing it from overshooting as well as limiting the input current. The converter can be shutdown by pulling this pin below 2.8V.

BLOCK DIAGRAM

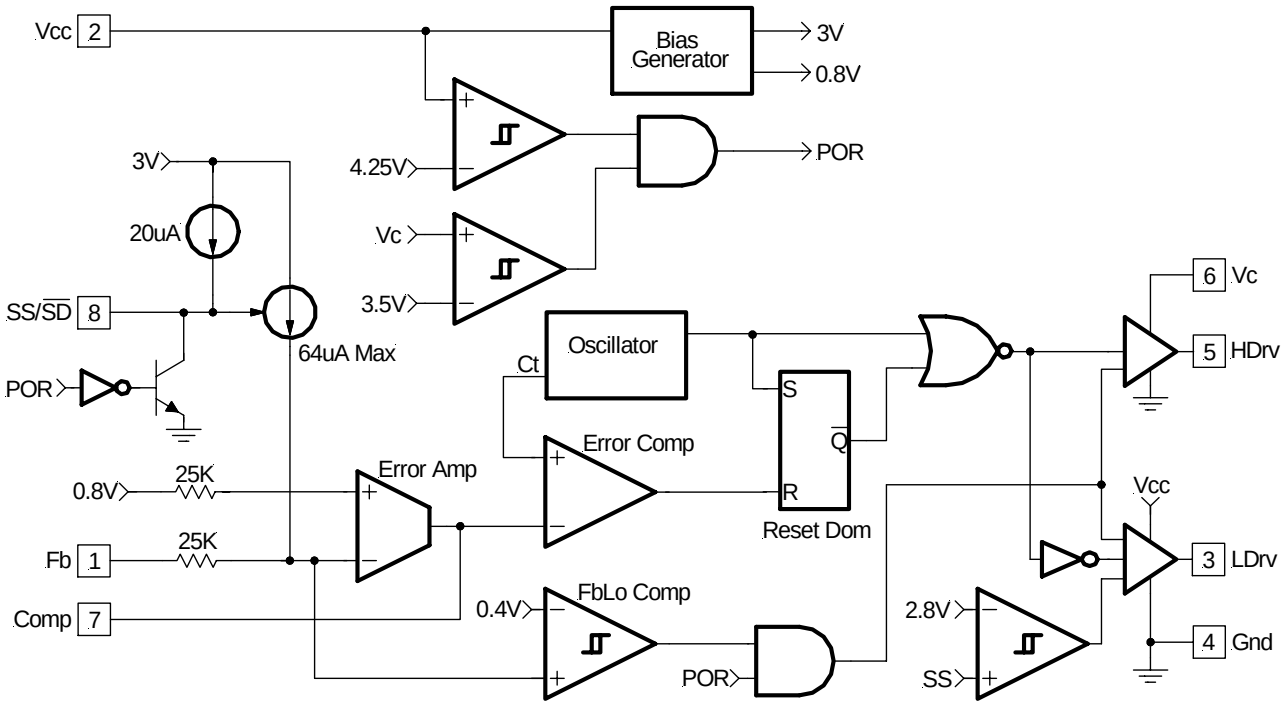


Figure 2 - Simplified block diagram of the APU3137.

THEORY OF OPERATION

Introduction

The APU3137 is a fixed frequency, voltage mode synchronous controller and consists of a precision reference voltage, an error amplifier, an internal oscillator, a PWM comparator, 1A peak gate driver, soft-start and shutdown circuits (see Block Diagram).

The output voltage of the synchronous converter is set and controlled by the output of the error amplifier; this is the amplified error signal from the sensed output voltage and the reference voltage.

This voltage is compared to a fixed frequency linear sawtooth ramp and generates fixed frequency pulses of variable duty-cycle, which drives the two N-channel external MOSFETs.The timing of the IC is provided through an internal oscillator circuit which uses on-chip capacitor to set the oscillation frequency to 200 KHz.

Soft-Start

The APU3137 has a programmable soft-start to control the output voltage rise and limit the current surge at the start-up. To ensure correct start-up, the soft-start sequence initiates when the Vc and Vcc rise above their threshold (3.5V and 4.25V respectively) and generates the Power On Reset (POR) signal. Soft-start function operates by sourcing an internal current to charge an external capacitor to about 3V. Initially, the soft-start function clamps the E/A's output of the PWM converter and disables the short circuit protection. During the power up, the output starts at zero and voltage at Fb is below 0.4V. The feedback UVLO is disabled during this time by injecting a current (64μA) into the Fb. This generates a voltage about 1.6V (64μA × 25K) across the negative input of E/A and positive input of the feedback UVLO comparator (see Fig3).

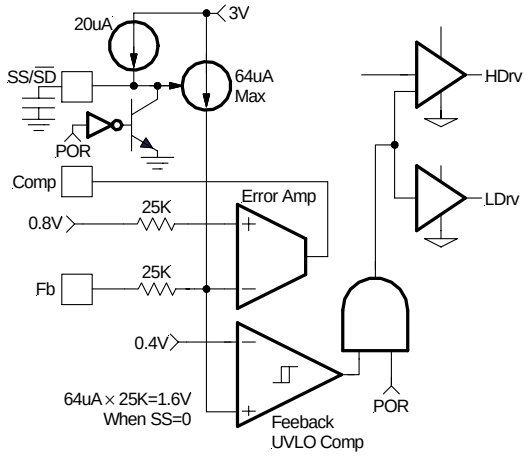


Figure 3 - Soft-start circuit for APU3137.

The magnitude of this current is inversely proportional to the voltage at soft-start pin.

The 20μA current source starts to charge up the external capacitor. In the mean time, the soft-start voltage ramps up, the current flowing into Fb pin starts to decrease linearly and so does the voltage at the positive pin of feedback UVLO comparator and the voltage negative input of E/A.

When the soft-start capacitor is around 1V, the current flowing into the Fb pin is approximately 32μA. The voltage at the positive input of the E/A is approximately:

$$32\mu A \times 25K = 0.8V$$

The E/A will start to operate and the output voltage starts to increase. As the soft-start capacitor voltage continues to go up, the current flowing into the Fb pin will keep decreasing. Because the voltage at pin of E/A is regulated to reference voltage 0.8V, the voltage at the Fb is:

$$V_{FB} = 0.8\text{-}25K \times (\text{Injected Current})$$

The feedback voltage increases linearly as the injecting current goes down. The injecting current drops to zero when soft-start voltage is around 2V and the output voltage goes into steady state.

As shown in Figure 4, the positive pin of feedback UVLO comparator is always higher than 0.4V, therefore, feedback UVLO is not functional during soft-start.

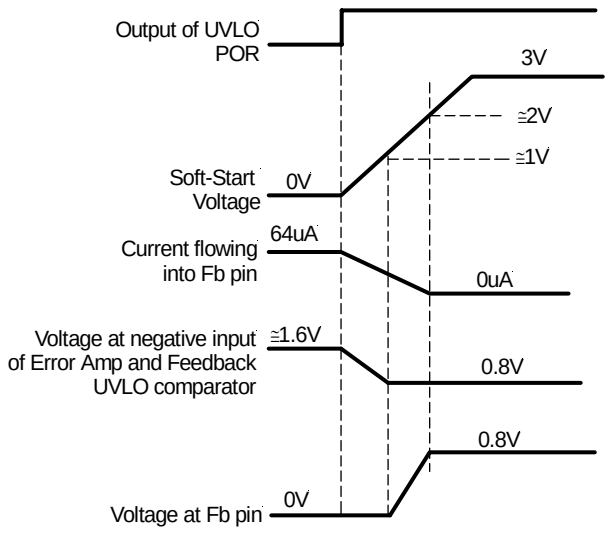


Figure 4 - Theoretical operational waveforms during soft-start.

the output start-up time is the time period when soft-start capacitor voltage increases from 1V to 2V. The start-up time will be dependent on the size of the external soft-start capacitor. The start-up time can be estimated by:

$$20\mu A \times T_{START}/C_{SS} = 2V\text{-}1V$$

For a given start up time, the soft-start capacitor can be estimated as:

$$C_{SS} \cong 20\mu A \times T_{START}/1V$$

MOSFET Drivers

The driver capabilities of both high and low side drivers are optimized to maintain fast switching transitions. They are sized to drive a MOSFET that can deliver up to 20A output current.

The low side MOSFET driver is supplied directly by V_{CC} while the high side driver is supplied by V_C.

An internal dead time control is implemented to prevent cross-conduction and allows the use of several kinds of MOSFETs.

Short-Circuit Protection

The outputs are protected against the short-circuit. The APU3137 protects the circuit for shorted output by sensing the output voltage (through the external resistor divider). The APU3137 turns off both drivers, when the output voltage drops below 0.4V.

The APU3137 also protects the output from over-voltaging when the control FET is shorted. This is done by turning on the sync FET with the maximum duty cycle.

Under-Voltage Lockout

The under-voltage lockout circuit assures that the MOSFET driver outputs remain in the off state whenever the supply voltage drops below set parameters. Lockout occurs if Vc and Vcc fall below 3.5V and 4.25V respectively. Normal operation resumes once Vc and Vcc rise above the set values.

Shutdown

The converter can be shutdown by pulling the soft-start pin below 2.8V. This can be easily done by using an external small signal transistor. During shutdown both MOSFET drivers turn off.

APPLICATION INFORMATION

Design Example:
The following example is a typical application for APU3137, the schematic is Figure 13 on page 15.

V_{IN} = 5V
V_{OUT} = 2.5V
I_{OUT} = 15A
ΔV_{OUT} = 75mV
(output voltage ripple ≅ 3% of V_{OUT})
f_S = 200KHz

Supply Voltage
$V_{CC} = V_C$ = 12V

Output Voltage Programming
Output voltage is programmed by reference voltage and external voltage divider. The Fb pin is the inverting input of the error amplifier, which is referenced to the voltage on non-inverting pin of error amplifier. The output voltage is defined by using the following equation:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_6}{R_5}\right) \quad ---(7)$$

V_{REF} = 0.8V

When an external resistor divider is connected to the output as shown in Figure 5.

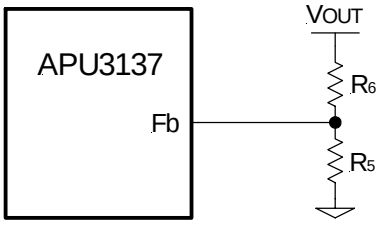


Figure 5 - Typical application of the APU3137 for programming the output voltage.

Equation (7) can be rewritten as:

$$R_6 = R_5 \times \left(\frac{V_{OUT}}{V_{REF}} - 1\right)$$

Choose R_5 = 1K
This will result to R_6 = 2.125K

If the high value feedback resistors are used, the input bias current of the Fb pin could cause a slight increase in output voltage. The output voltage set point can be more accurate by using precision resistor.

Soft-Start Programming
The soft-start timing can be programmed by selecting the soft-start capacitance value. The start-up time of the converter can be calculated by using:

$$Css = 20 \times t_{START} \ (\mu F) \quad ---(8)$$

Where t_{START} is the desired start-up time (ms)

For a start-up time of 5ms, the soft-start capacitor will be 0.1μF. Choose a ceramic capacitor at 0.1μF.

Boost Supply Vc
To drive the high side switch, it is necessary to supply a gate voltage at least 4V grater than the bus voltage. For single supply applications, this is achieved by using a charge pump configuration as shown in Figure 6. This method is simple and inexpensive. The operation of the circuit is as follows: when the lower MOSFET is turned on, the capacitor (C1) is pulled down to ground and charges, up to V_{BUS} value, through the diode (D1). The bus voltage will be added to this voltage when upper MOSFET turns on in next cycle, and providing supply voltage (Vc) through diode (D2). Vc is approximately:

$$V_C \cong 2 \times V_{BUS} - (V_{D1} + V_{D2})$$

Capacitors in the range of 0.1μF and 1μF are generally adequate for most applications. The diode must be a fast recovery device to minimize the amount of charge fed back from the charge pump capacitor into Vc. The diodes need to be able to block the full power rail voltage, which is seen when the high side MOSFET is switched on. For low voltage application, schottky diodes can be used to minimize forward drop across the diodes at start up. For this application, Vc is biased by an external 12V supply.

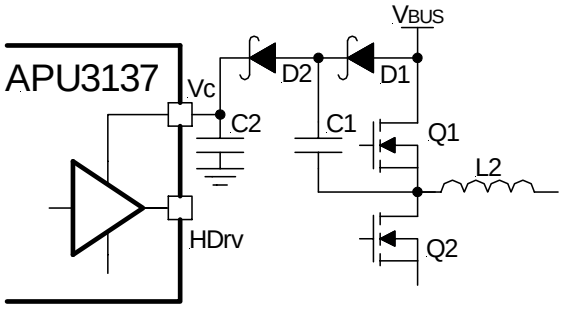


Figure 6 - Charge pump circuit.

Input Capacitor Selection
The input filter capacitor should be based on how much ripple the supply can tolerate on the DC input line. The ripple current generated during the on time of upper MOSFET should be provided by input capacitor. The RMS value of this ripple is expressed by:

$$I_{RMS} = I_{OUT}\sqrt{D \times (1-D)} \qquad ---(9)$$

Where:
D is the Duty Cycle, $D=V_{OUT}/V_{IN}$.
I_{RMS} is the RMS value of the input capacitor current.
I_{OUT} is the output current for each channel.

For V_{IN}=5V, I_{OUT}=15A and D=0.5, the I_{RMS}=7.5A

For higher efficiency, a low ESR capacitor is recommended. Choose four Poscap from Sanyo 6TPC150M (6.3V, 150μF, 40mΩ) with a maximum allowable ripple current of 7.6A.

Inductor Selection
The inductor is selected based on operating frequency, transient performance and allowable output voltage ripple.

Low inductor value results to faster response to step load (high Δi/Δt) and smaller size but will cause larger output ripple due to increase of inductor ripple current. As a rule of thumb, select an inductor that produces a ripple current of 10-40% of full load DC.

For the buck converter, the inductor value for desired operating ripple current can be determined using the following relation:

$$V_{IN} - V_{OUT} = L \times \frac{\Delta i}{\Delta t} \;;\; \Delta t = D \times \frac{1}{f_S} \;;\; D = \frac{V_{OUT}}{V_{IN}}$$

$$L = (V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{V_{IN} \times \Delta i \times f_S} \qquad ---(11)$$

Where:
V_{IN} = Maximum Input Voltage
V_{OUT} = Output Voltage
Δi = Inductor Ripple Current
f_S = Switching Frequency
Δt = Turn On Time
D = Duty Cycle

If $\Delta i = 20\%(I_O)$, then the output inductor will be:

L = 2μH

The Panasonic PCCN6B series provides a range of inductors in different values, low profile suitable for large currents, 2.17μH, 17A is a good choice for this application. This will result to a ripple approximately 19.2% of output current.

Output Capacitor Selection
The criteria to select the output capacitor is normally based on the value of the Effective Series Resistance (ESR). In general, the output capacitor must have low enough ESR to meet output ripple and load transient requirements, yet have high enough ESR to satisfy stability requirements. The ESR of the output capacitor is calculated by the following relationship:

$$ESR \le \frac{\Delta V_O}{\Delta I_O} \qquad ---(10)$$

Where:
ΔV_O = Output Voltage Ripple
Δi = Inductor Ripple Current
ΔV_O = 75mV and $\Delta I \cong 20\%$ of 15A = 3A
This results to: ESR=25mΩ

The Sanyo TPC series, Poscap capacitor is a good choice. The 6TPC330M, 330μF, 6.3V has an ESR 40mΩ. Selecting three of these capacitors in parallel, results to an ESR of ≅ 13.3mΩ which achieves our low ESR goal.

The capacitor value must be high enough to absorb the inductor's ripple current. The larger the value of capacitor, the lower will be the output ripple voltage.

Power MOSFET Selection
The APU3137 uses two N-Channel MOSFETs. The selections criteria to meet power transfer requirements is based on maximum drain-source voltage (V_{DSS}), gate-source drive voltage (V_{GS}), maximum output current, On-resistance $R_{DS(ON)}$ and thermal management.

The MOSFET must have a maximum operating voltage (V_{DSS}) exceeding the maximum input voltage (V_{IN}).

The gate drive requirement is almost the same for both MOSFETs. Logic-level transistor can be used and caution should be taken with devices at very low V_{GS} to prevent undesired turn-on of the complementary MOSFET, which results a shoot-through current.

The total power dissipation for MOSFETs includes conduction and switching losses. For the Buck converter, the average inductor current is equal to the DC load current. The conduction loss is defined as:

$$P_{COND}(\text{Upper Switch}) = I^2_{LOAD} \times R_{DS(ON)} \times D \times \vartheta$$

$$P_{COND}(\text{Lower Switch}) = I^2_{LOAD} \times R_{DS(ON)} \times (1 - D) \times \vartheta$$

$\vartheta = R_{DS(ON)}$ Temperature Dependency

The $R_{DS(ON)}$ temperature dependency should be considered for the worst case operation. This is typically given in the MOSFET data sheet. Ensure that the conduction losses and switching losses do not exceed the package ratings or violate the overall thermal budget.

Choose IRF7832 for both control MOSFET and synchronous MOSFET. This device provides low on-resistance in a compact SOIC 8-Pin package.

The MOSFET has the following data:

IRF7832
V_{DSS} = 30V
I_D = 20A @ 25°C
$R_{DS(ON)}$ = 4mΩ @ V_{GS}=10V

The total conduction losses will be:

$$P_{CON(TOTAL)} = P_{CON(UPPER)} + P_{CON(LOWER)}$$

$P_{CON(TOTAL)}$ = 1.166W

The switching loss is more difficult to calculate, even though the switching transition is well understood. The reason is the effect of the parasitic components and switching times during the switching procedures such as turn-on / turnoff delays and rise and fall times. The control MOSFET contributes to the majority of the switching losses in synchronous Buck converter. The synchronous MOSFET turns on under zero voltage conditions, therefore, the turn on losses for synchronous MOSFET can be neglected. With a linear approximation, the total switching loss can be expressed as:

$$P_{SW} = \frac{V_{DS(OFF)}}{2} \times \frac{t_r + t_f}{T} \times I_{LOAD} \qquad ---(12)$$

Where:
$V_{DS(OFF)}$ = Drain to Source Voltage at off time
t_r = Rise Time
t_f = Fall Time
T = Switching Period
I_{LOAD} = Load Current

The switching time waveform is shown in Figure 7.

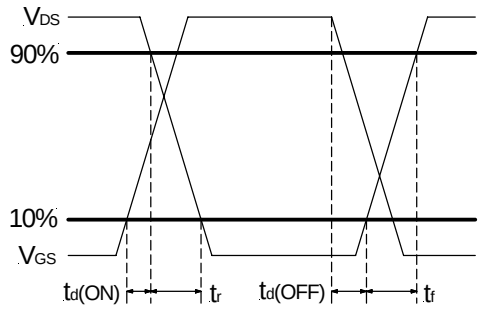


Figure 7 - Switching time waveforms.

From IRF7832 data sheet we obtain:

IRF7832
t_r = 12.3ns
t_f = 21ns

These values are taken under a certain condition test. For more details please refer to the IRF7466 and IRF7458 data sheets.

By using equation (12), we can calculate the total switching losses.

$P_{SW(TOTAL)}$ = 250mW

Feedback Compensation

The APU3137 is a voltage mode controller; the control loop is a single voltage feedback path including error amplifier and error comparator. To achieve fast transient response and accurate output regulation, a compensation circuit is necessary. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency and adequate phase margin (greater than 45°).

The output LC filter introduces a double pole, –40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180° (see Figure 8). The Resonant frequency of the LC filter is expressed as follows:

$$F_{LC} = \frac{1}{2\pi \times \sqrt{L_O \times C_O}} \qquad ---(13)$$

Figure 9 shows gain and phase of the LC filter. Since we already have 180° phase shift just from the output filter, the system risks being unstable.

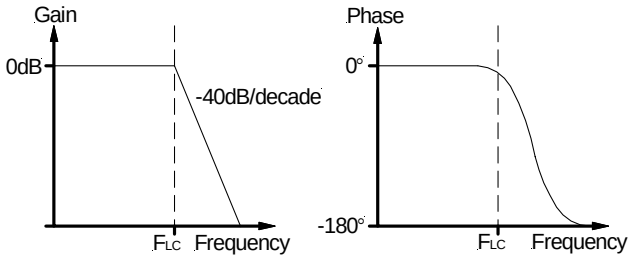


Figure 8 - Gain and phase of LC filter.

The APU3137's error amplifier is a differential-input transconductance amplifier. The output is available for DC gain control or AC phase compensation.

The E/A can be compensated with or without the use of local feedback. When operated without local feedback, the transconductance properties of the E/A become evident and can be used to cancel one of the output filter poles. This will be accomplished with a series RC circuit from Comp pin to ground as shown in Figure 9.

Note that this method requires that the output capacitor should have enough ESR to satisfy stability requirements. In general, the output capacitor's ESR generates a zero typically at 5KHz to 50KHz which is essential for an acceptable phase margin.

The ESR zero of the output capacitor expressed as follows:

$$F_{ESR} = \frac{1}{2\pi \times ESR \times Co} \qquad ---(14)$$

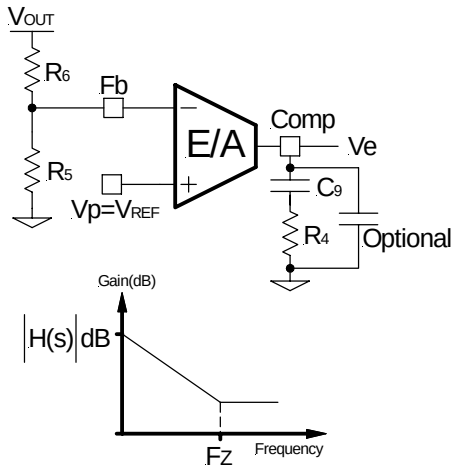


Figure 9 - Compensation network without local feedback and its asymptotic gain plot.

The transfer function (Ve / V_{OUT}) is given by:

$$H(s) = \left(g_m \times \frac{R_5}{R_6 + R_5}\right) \times \frac{1 + sR_4C_9}{sC_9} \qquad ---(15)$$

The (s) indicates that the transfer function varies as a function of frequency. This configuration introduces a gain and zero, expressed by:

$$|H(s=j \times 2\pi \times F_O)| = g_m \times \frac{R_5}{R_6 \times R_5} \times R_4 \qquad ---(16)$$

$$F_Z = \frac{1}{2\pi \times R_4 \times C_9} \qquad ---(17)$$

|H(s)| is the gain at zero cross frequency.

First select the desired zero-crossover frequency (Fo):

$$Fo > F_{ESR} \text{ and } F_O \le (1/5 \sim 1/10) \times f_S$$

Use the following equation to calculate R_4:

$$R_4 = \frac{V_{OSC}}{V_{IN}} \times \frac{Fo \times F_{ESR}}{F_{LC}^2} \times \frac{R_5 + R_6}{R_5} \times \frac{1}{g_m} \qquad ---(18)$$

Where:
V_{IN} = Maximum Input Voltage
V_{OSC} = Oscillator Ramp Voltage
Fo = Crossover Frequency
F_{ESR} = Zero Frequency of the Output Capacitor
F_{LC} = Resonant Frequency of the Output Filter
R_5 and R_6 = Resistor Dividers for Output Voltage Programming
g_m = Error Amplifier Transconductance

For:

V_{IN} = 5V	F_{LC} = 3.43KHz
V_{OSC} = 2.5V	R_5 = 1K
Fo = 20KHz	R_6 = 2.15K
F_{ESR} = 12KHz	g_m = 600μmho

This results to R_4=26.7K
Choose R_4=30K

To cancel one of the LC filter poles, place the zero before the LC filter resonant frequency pole:

$$F_Z \cong 75\% F_{LC}$$

$$F_Z \cong 0.75 \times \frac{1}{2\pi\sqrt{L_O \times C_O}} \qquad ---(19)$$

For:

Lo = 2.17μH	F_Z = 2.57KHz
Co = 990μF	R_4 = 20K

Using equations (17) and (19) to calculate C_9, we get:

$$C_9 \cong 2006pF; \text{ Choose } C_9 = 3300pF$$

One more capacitor is sometimes added in parallel with C_9 and R_4. This introduces one more pole which is mainly used to suppress the switching noise. The additional pole is given by:

$$F_P = \frac{1}{2\pi \times R_4 \times \frac{C_9 \times C_{POLE}}{C_9 + C_{POLE}}}$$

The pole sets to one half of switching frequency which results in the capacitor C_{POLE}:

$$C_{POLE} = \frac{1}{\pi \times R_4 \times f_S - \frac{1}{C_9}} \cong \frac{1}{\pi \times R_4 \times f_S}$$

For $F_P << f_S/2$
R_4=30K and F_S=200KHz will result to C_{POLE}=53pF.
Choose C_{POLE}=47pF.

For a general solution for unconditionally stability for ceramic capacitor with very low ESR and any type of output capacitors, in a wide range of ESR values we should implement local feedback with a compensation network. The typically used compensation network for voltage-mode controller is shown in Figure 10.

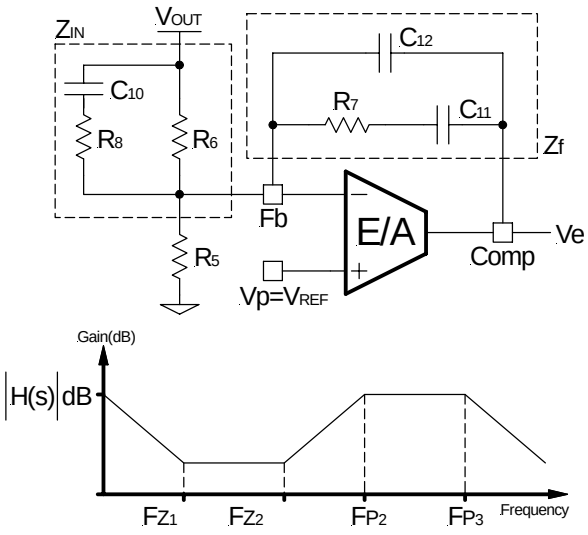


Figure 10 - Compensation network with local feedback and its asymptotic gain plot.

In such configuration, the transfer function is given by:

$$\frac{Ve}{V_{OUT}} = \frac{1 - g_m Z_f}{1 + g_m Z_{IN}}$$

The error amplifier gain is independent of the transconductance under the following condition:

$$g_m Z_f >> 1 \quad \text{and} \quad g_m Z_{IN} >> 1 \qquad \text{---(20)}$$

By replacing Z_{IN} and Z_f according to Figure 7, the transformer function can be expressed as:

$$H(s) = \frac{1}{sR_6(C_{12}+C_{11})} \times \frac{(1+sR_7C_{11}) \times [1+sC_{10}(R_6+R_8)]}{\left[1+sR_7\left(\frac{C_{12}C_{11}}{C_{12}+C_{11}}\right)\right] \times (1+sR_8C_{10})}$$

As known, transconductance amplifier has high impedance (current source) output, therefore, consider should be taken when loading the E/A output. It may exceed its source/sink output current capability, so that the amplifier will not be able to swing its output voltage over the necessary range.

The compensation network has three poles and two zeros and they are expressed as follows:

$$F_{P1} = 0$$

$$F_{P2} = \frac{1}{2\pi \times R_8 \times C_{10}}$$

$$F_{P3} = \frac{1}{2\pi \times R_7 \times \left(\frac{C_{12} \times C_{11}}{C_{12}+C_{11}}\right)} \cong \frac{1}{2\pi \times R_7 \times C_{12}}$$

$$F_{Z1} = \frac{1}{2\pi \times R_7 \times C_{11}}$$

$$F_{Z2} = \frac{1}{2\pi \times C_{10} \times (R_6 + R_8)} \cong \frac{1}{2\pi \times C_{10} \times R_6}$$

Cross Over Frequency:

$$F_O = R_7 \times C_{10} \times \frac{V_{IN}}{V_{OSC}} \times \frac{1}{2\pi \times Lo \times Co} \qquad \text{---(21)}$$

Where:
V_{IN} = Maximum Input Voltage
V_{OSC} = Oscillator Ramp Voltage
Lo = Output Inductor
Co = Total Output Capacitors

The stability requirement will be satisfied by placing the poles and zeros of the compensation network according to following design rules. The consideration has been taken to satisfy condition (20) regarding transconductance error amplifier.

These design rules will give a crossover frequency approximately one-tenth of the switching frequency. The higher the band width, the potentially faster the load transient speed. The gain margin will be large enough to provide high DC-regulation accuracy (typically -5dB to -12dB). The phase margin should be greater than 45° for overall stability.

Based on the frequency of the zero generated by ESR versus crossover frequency, the compensation type can be different. The table below shows the compensation type and location of crossover frequency.

Compensator Type	Location of Zero Crossover Frequency (F_O)	Typical Output Capacitor
Type II (PI)	$F_{PO} < F_{ZO} < F_O < f_S/2$	Electrolytic, Tantalum
Type III (PID) Method A	$F_{PO} < F_O < F_{ZO} < f_S/2$	Tantalum, Ceramic
Type III (PID) Method B	$F_{PO} < F_O < f_S/2 < F_{ZO}$	Ceramic

Table - The compensation type and location of zero crossover frequency.

Detail information is dicussed in application Note AN-1043 which can be downloaded from the IR Web-Site.

Layout Consideration

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Start to place the power components. Make all the connections in the top layer with wide, copper filled areas. The inductor, output capacitor and the MOSFET should be close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place input capacitor directly to the drain of the high-side MOSFET. To reduce the ESR, replace the single input capacitor with two parallel units. The feedback part of the system should be kept away from the inductor and other noise sources and be placed close to the IC. In multilayer PCB, use one layer as power ground plane and have a separate control circuit ground (analog ground), to which all signals are referenced. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point.

TYPICAL APPLICATION

Single Supply 5V Input

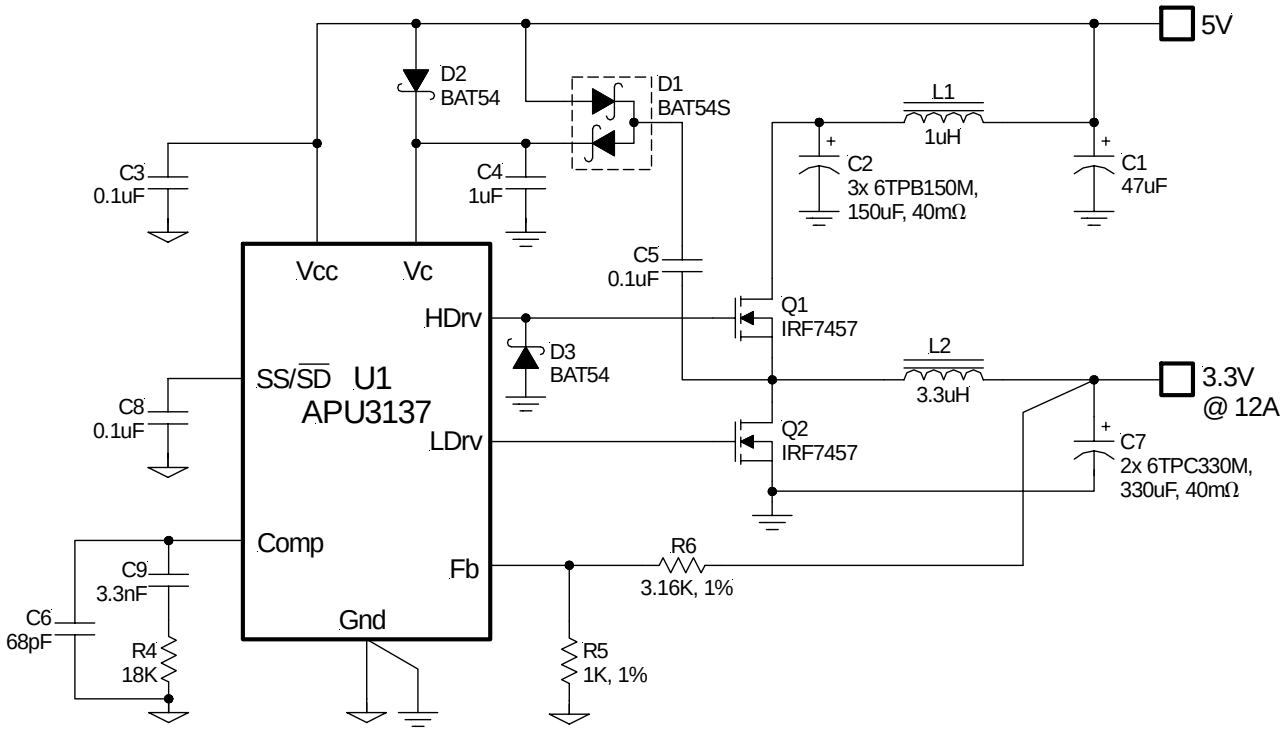


Figure 11 - Typical application of APU3137 in an on-board DC-DC converter using a single 5V supply.

TYPICAL APPLICATION

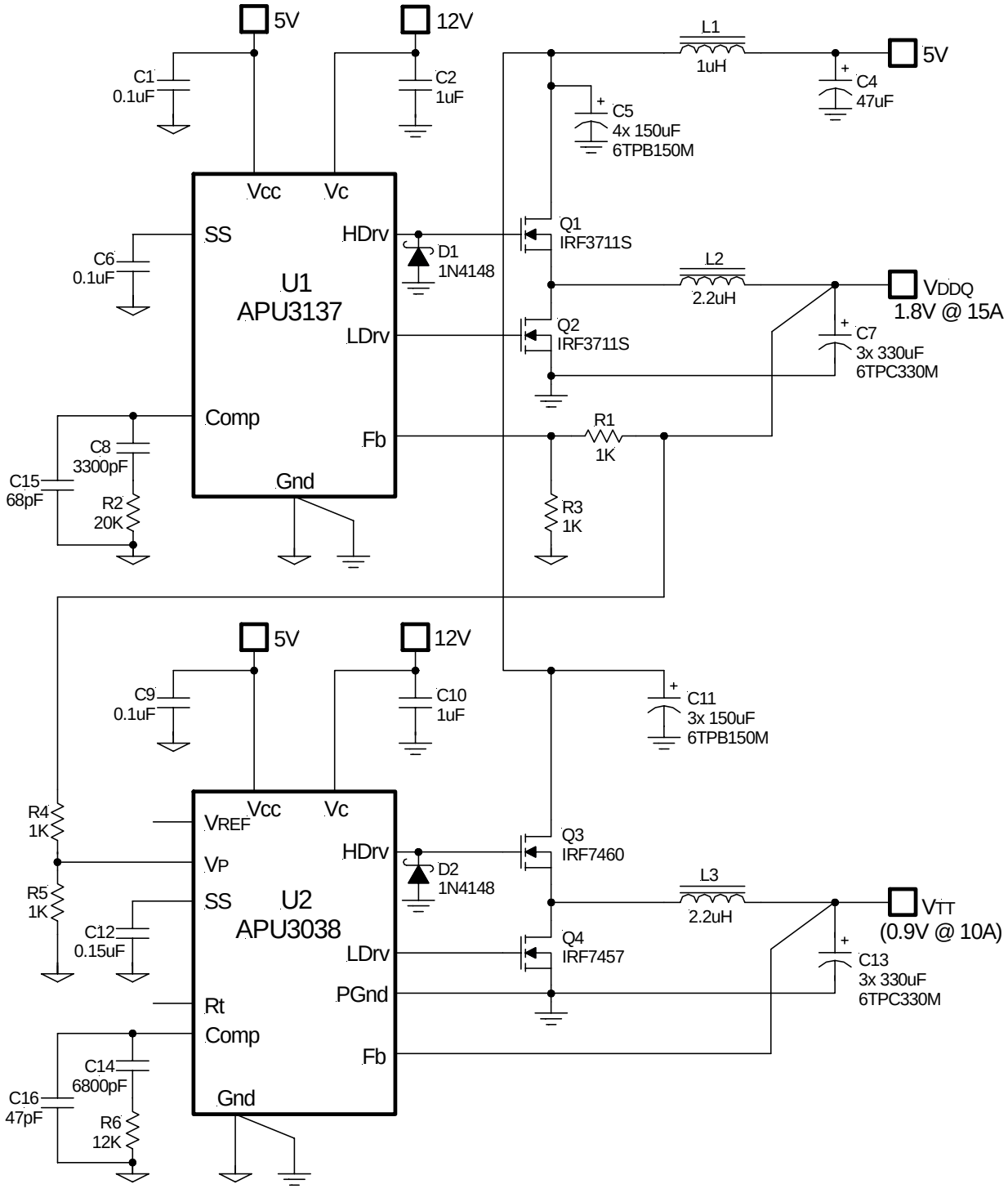


Figure 12 - Typical application of APU3137 for DDR memory when the termination voltage, generated by APU3038, tracks the core voltage.

DEMO-BOARD APPLICATION

5V to 2.5V @ 15A

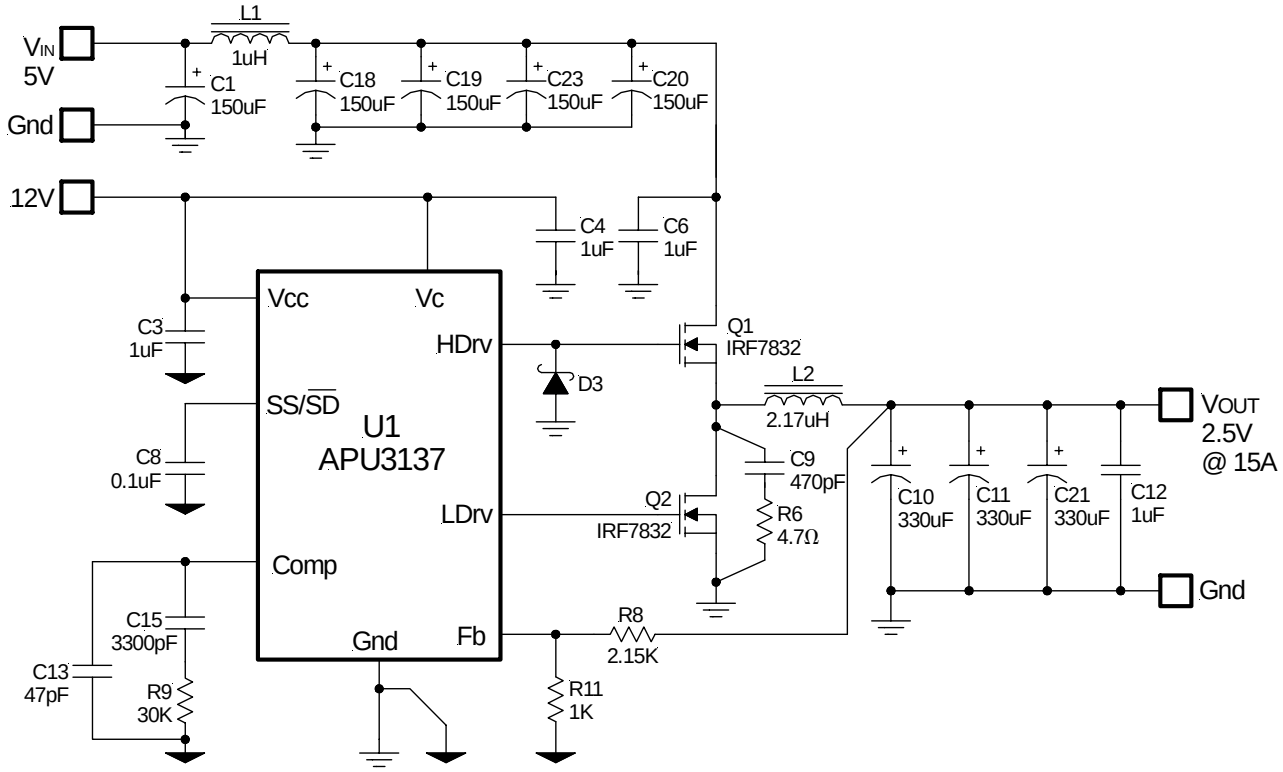


Figure 13 - Demo-board application of APU3137.

Application Parts List

Ref Desig	Description	Value	Qty	Part#	Manuf
Q1, Q2	MOSFET	30V, 4mΩ, 15A	2	IRF7832	IR
U1	Controller	Synchronous PWM	1	APU3137	APEC
D3	Diode	Fast Switching	1	BAT54	IR
L1	Inductor	1μH, 10A	1	D03316P-102HC	Coilcraft
L2	Inductor	2.17μH, 17A	1	ETQP6F2R5BFA	Panasonic
C1,C18,C19,C20,C23	Capacitor, Poscap	150μF, 6.3V, 40mΩ	5	6TPC150M	Sanyo
C10,C11,C21	Capacitor, Poscap	330μF, 6.3V, 40mΩ	3	6TPC330M	Sanyo
C8	Capacitor, Ceramic	0.1μF, Y5V, 25V	1	ECJ-2VF1E104Z	Panasonic
C3,C4,C12,C6	Capacitor, Ceramic	1μF, Y5V, 16V	4	ECJ-3YB1E105K	Panasonic
C9	Capacitor, Ceramic	470pF, X7R	1	ECJ-2VB2D471K	Panasonic
C15	Capacitor, Ceramic	3300pF, X7R, 50V	1	ECJ-2VB1H332K	Panasonic
C13	Capacitor, Ceramic	47pF, NPO	1	ECJ-2VC1H470J	Panasonic
R8	Resistor	2.15K, 1%	1		
R6	Resistor	4.7Ω, 5%	1		
R11	Resistor	1K, 1%	1		
R9	Resistor	30K, 1%	1		

TYPICAL OPERATING CHARACTERISTICS

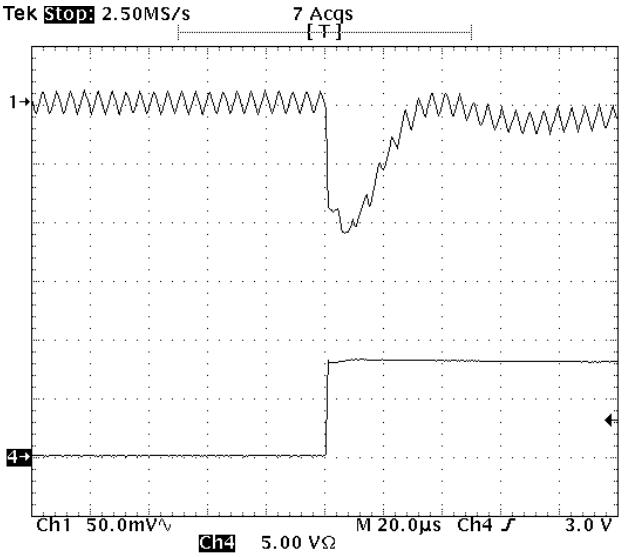


Figure 14 - Transient load response at I_{OUT}=0A - 8A.
Ch1: V_{OUT}
Ch4: I_{OUT} (5A/div)

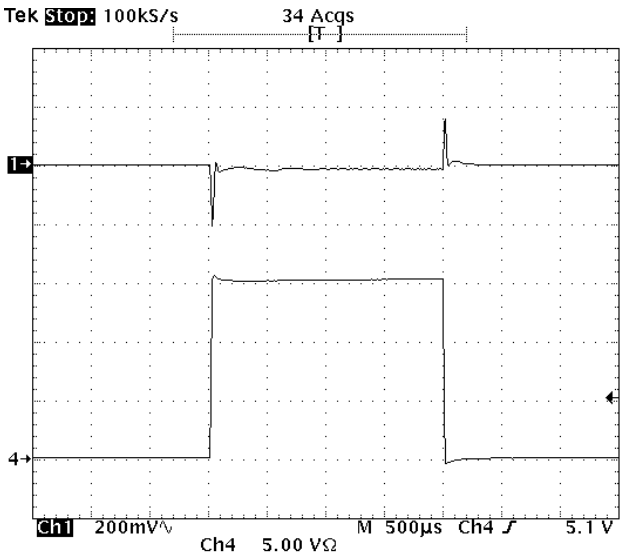


Figure 16 - Transient load response at I_{OUT}=0A - 15A.
Ch1: V_{OUT}
Ch4: I_{OUT} (5A/div)

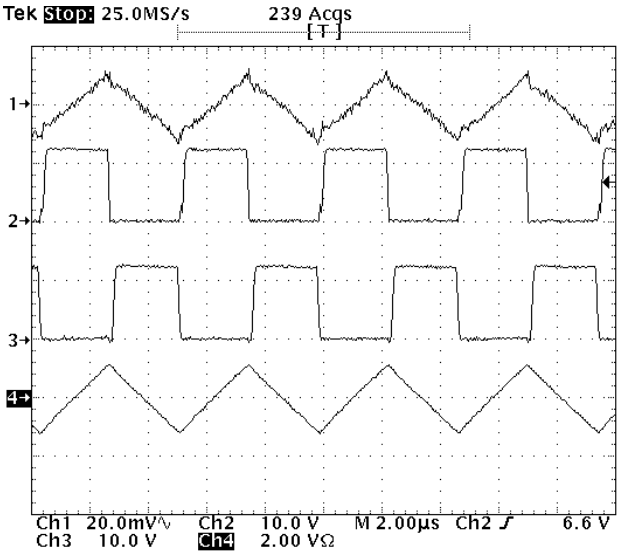


Figure 15 - Normal condition at N/L.
Ch1: Output Voltage Ripple (20mV/div)
Ch2: HDrv
Ch3: LDrv
Ch4: Inductor Current (2A/div)

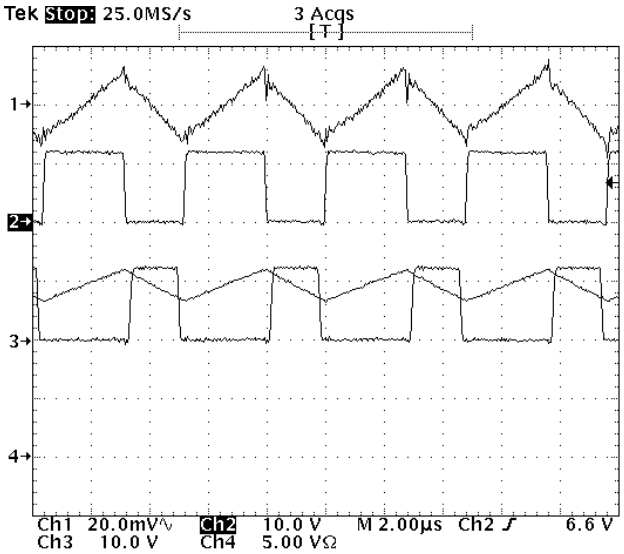


Figure 17 - Normal condition at 15A.
Ch1: Output Voltage Ripple (20mV/div)
Ch2: HDrv
Ch3: LDrv
Ch4: Inductor Current (5A/div)

TYPICAL OPERATING CHARACTERISTICS

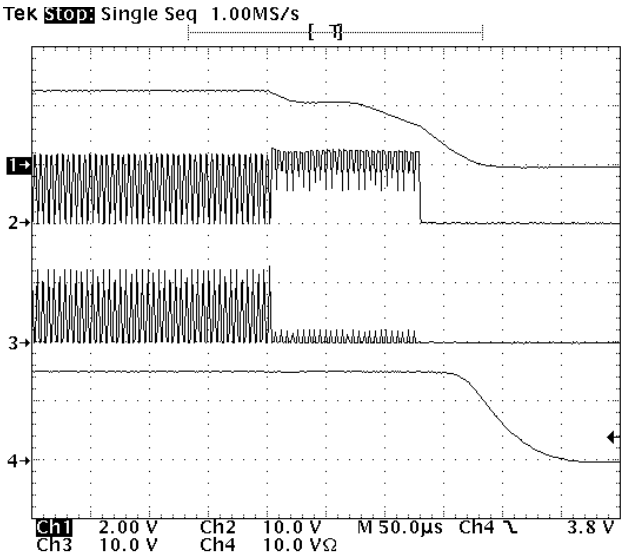


Figure 18 - Shutdown by pulling down the soft-start pin.
Ch1: V_{OUT}
Ch2: HDrv
Ch3: LDrv
Ch4: I_{OUT} (10A/div)

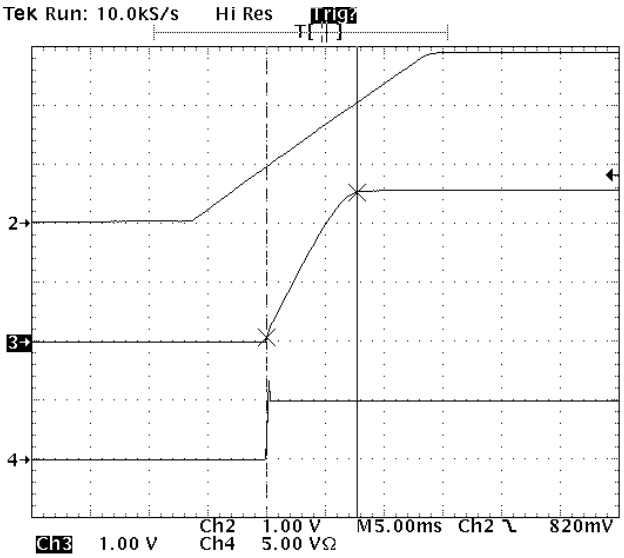


Figure 19 - Start-Up.
Ch2: V_{SS} (Soft-Start Voltage)
Ch3: V_{OUT}
Ch4: I_{OUT} (5A/div)

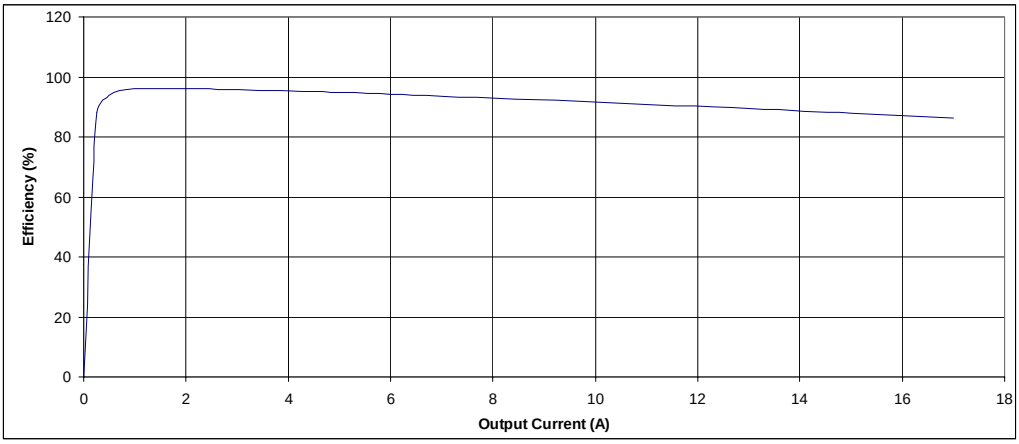


Figure 20 - Application circuit efficiency at ambient temperature.
5V to 2.5V