2.5A SWITCH STEP DOWN SWITCHING REGULATOR

Features

- 2.5A Internal Switch
- Operating Input Voltage from 4.7V to 22V
- 3.3V ±2% Reference Voltage
- Output Voltage:
  APW1172 - adjustable from 1.235V to 20V
- Low Dropout Operation: 100% Duty Cycle
- 250kHz Internally Fixed Frequency
- Voltage Feed-Forward
- Zero Load Current Operation
- Internal Current-Limit
- Inhibit for Zero Current Consumption
- Synchronization
- Protection against Feedback Disconnection
- Thermal Protection
- External Soft-Start
- Over-Voltage Protection
- Lead Free and Green Devices Available
  (RoHS Compliant)

Applications

- Consumer: STB, DVD, TV, VCR, Car Radio, LCD monitors
- Networking: XDSL, Modems, DC-DC Modules
- Computer: Printers, Audio/Graphic Cards, Optical Storage, Hard Disk Drive
- Industrial: Chargers, Car Battery DC-DC Converters

General Description

The APW1172 is a step down monolithic power switching regulator with a switch current limit of 3.8A so it is able to deliver more than 2.5A DC current to the load depending on the application conditions.

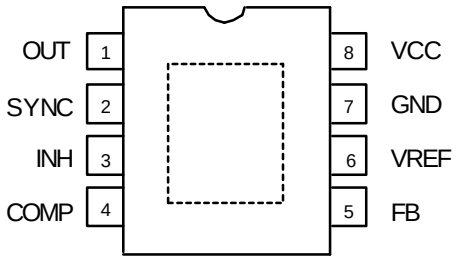
The output voltage can be set from 1.235V to 22V.The high current level is also achieved thanks to an SOP-8 package with exposed pad frame. The type of package allows to reduce the Rth (j-amb) down to approximately 45°C/W.

An internal oscillator fixes the switching frequency at 250kHz.

Having a minimum input voltage of 4.7V only, it is particularly suitable for 5V bus, available in all computer related applications.

Pulse by pulse current-limit with the internal frequency modulation offers an effective constant current short circuit protection.

Pin Configuration



SOP-8-P (Top View)

= Thermal Pad
(connected to GND plane for better heat dissipation)

Ordering and Marking Information

APW1172 □□□-□□ □ Assembly Material Handling Code Temperature Range Package Code	Package Code KA : SOP-8P Operating Ambient Temperature Range C : 0 to 70 °C I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material L : Lead Free Device G : Halogen and Lead Free Device
APW1172 KA : APW1172 XXXXX	XXXXX - Date Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Input voltage (VCC to GND)	25	V
V_{OUT}	Output DC voltage	-1 to 25	V
V_{INH}	INH to GND	-0.3 ~ VCC	V
VIO	COMP and FB to GND	-0.3 ~ VCC	V
I_{OUT}	Output current	0 to current limit	A
V_{REF}	VREF to GND	-0.3 ~ VCC	V
PD	Average Power Dissipation, T_A < 50°	2.2	W
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction to Ambient Thermal Resistance in Free Air	45.7	°C/W

* The area of the thermal pad is 4.5mm X 2mm and the GND plane is 60mm X 60mm. Connect the thermal pad and the GND plane by 8 vias. T_A=25°C.

Electrical Characteristics

The * denotes the specifications that apply over T_A = -40 ~ 85°C. Typical values are at T_A = 25°C. V_{CC} = 12V unless otherwise specified.

Symbol	Parameter	Test conditions		APW1172			Unit
				Min	Typ	Max	
V_{CC}	Operating Input Voltage Range	V_O = 1.235V; I_O = 2A	*	4.7	-	22	V
V_{UVLO}	UVLO Threshold Voltage	V_{CC} rising	*	3.8	4.2	4.6	V
	Hysteresis			-	0.3	-	V
V_d	Dropout Voltage	V_{CC} = 4.8V; I_O = 2A	*	-	1.0	1.2	V
ILIM	Maximum Limiting Current	V_{CC} = 4.8V to 22V	*	3.3	3.8	4.3	A
f_S	Switching Frequency		*	200	250	300	kHz
				205	250	295	
	Duty Cycle			0	-	100	%
DYNAMIC CHARACTERISTICS							
V_{FB}	Voltage Feedback	4.8V < V_{CC} < 22V, 20mA < I_O < 2A		1.22	1.235	1.25	V
			*	1.198	1.235	1.272	
η	Efficiency	V_O = 5V, V_{CC} = 12V, I_{OUT} = 1A		-	84	-	%
DC CHARACTERISTICS							
I_{qop}	Total Operating Quiescent Current		*	-	-	12	mA
I_q	Quiescent Current	Duty Cycle = 0; V_{FB} = 1.5V		-	-	10	mA
Iqst-by	Total Stand-by Quiescent Current	V_{INH} > 2.2V	*	-	50	100	µA
		V_{CC} = 22V; V_{INH} > 2.2V	*	-	80	150	µA
INHIBIT							
V_{INH}	INH Threshold Voltage	Device ON		-	-	0.8	V
		Device OFF		2.2	-	-	V
	INH Pull-Up Current	V_{INH} < 3V		-	1	-	µA
	Maximum INH Voltage	I_{INH} = 0A		-	4.3	-	V
ERROR AMPLIFIER							
V_{OH}	High Level Output Voltage	V_{FB} = 1V		3.5	3.8	-	V
V_{OL}	Low Level Output Voltage	V_{FB} = 1.5V		-	-	0.4	V
$I_{O\ source}$	Source Output Current	V_{COMP} = 1.9V; V_{FB} = 1V		200	300	-	µA
$I_{O\ sink}$	Sink Output Current	V_{COMP} = 1.9V; V_{FB} = 1.5V		1	1.5	-	mA
I_{FB}	Source Bias Current	V_{FB} = 1.5V		-	2.5	4	µA
	Maximum FB Voltage	I_{FB} = 0µA		-	2.1	-	V
gm	Trans-conductance	V_{FB} = 1.255V to 1.215V, I_{COMP} = -0.1mA to 0.1mA V_{COMP} = 1.9V		-	2.3	-	mA/V

Electrical Characteristics (Cont.)

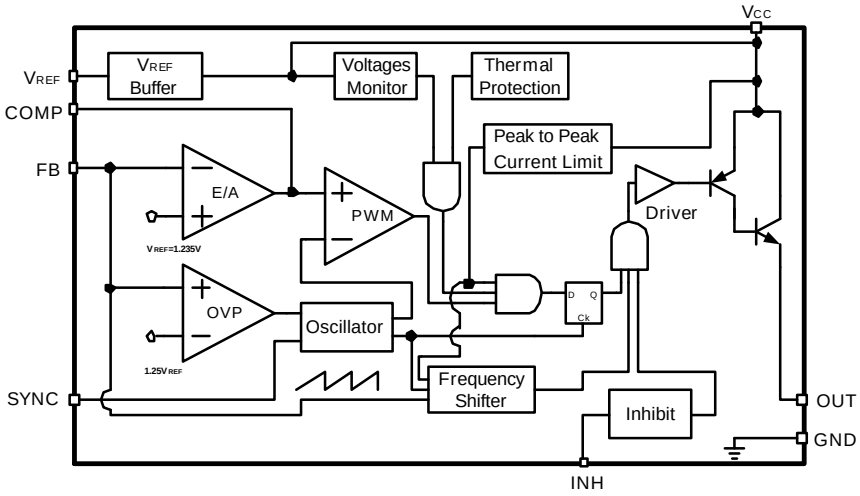
The * denotes the specifications that apply over T_A = -40 ~ 85°C. Typical values are at T_A = 25°C. V_{CC} = 12V unless otherwise specified.

Symbol	Parameter	Test conditions		APW1172			Unit
				Min.	Typ.	Max.	
SYNC FUNCTION							
	High Input Voltage	V_{CC} = 4.8V to 22V		2.5	-	V_{REF}	V
	Low Input Voltage	V_{CC} = 4.8V to 22V		-	-	0.74	V
	Slave Sink Current	V_{SYNC} = 0.74V		0.11	-	0.25	mA
		V_{SYNC} = 2.33V		0.21	-	0.45	
	Master Output Amplitude	I_{SOURCE} = 3mA		2.75	3	-	V
	Output Pulse Width	No load, V_{SYNC} = 1.65V		0.2	0.35	-	µs
REFERENCE SECTION							
V_{REF}	VREF Output Voltage	I_{REF} = 0mA		3.234	3.3	3.366	V
		I_{REF} = 0mA to 5mA, V_{CC} = 4.8V to 22V	*	3.2	3.3	3.399	V
	Line Regulation	I_{REF} = 0mA, V_{CC} = 4.8V to 22V		-	5	10	mV
	Load Regulation	I_{REF} = 0mA to 5mA		-	8	15	mV
	Short Circuit Current			10	18	30	mA
OTHER							
	Thermal Limiting Protection			-	160	-	°C
	Hysteresis			-	30	-	°C
	Over-Voltage Protection Threshold Voltage	V_{COMP} = 0.8V	*	120	125	130	%

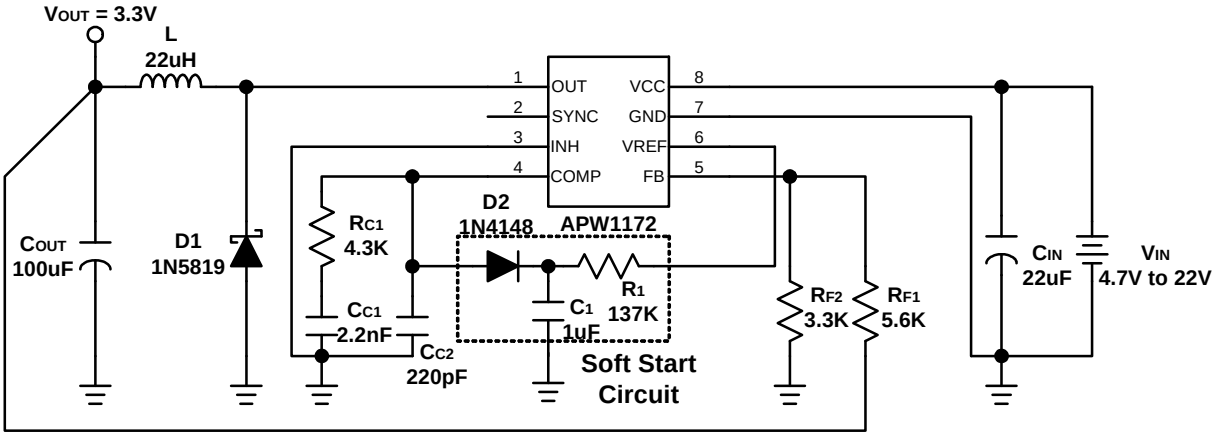
Pin Description

No.	PIN	FUNCTION
1	OUT	Regulator Output.
2	SYNC	Master/Slave synchonization.
3	INH	A logical signal (active high) disables the device. If INH not used the pin must be connected to GND. When it is open an internal pull-up disable the device.
4	COMP	E/A output for frequency compensation.
5	FB	Feedback input. Connecting directly to this pin results in an output voltage of 1.235V. An external resistive divider is required for higher output voltages.
6	VREF	3.3V reference voltage output, no Capacitor Is requested for stability.
7	GND	Ground.
8	VCC	Unregulated DC input voltage.

Block Diagram

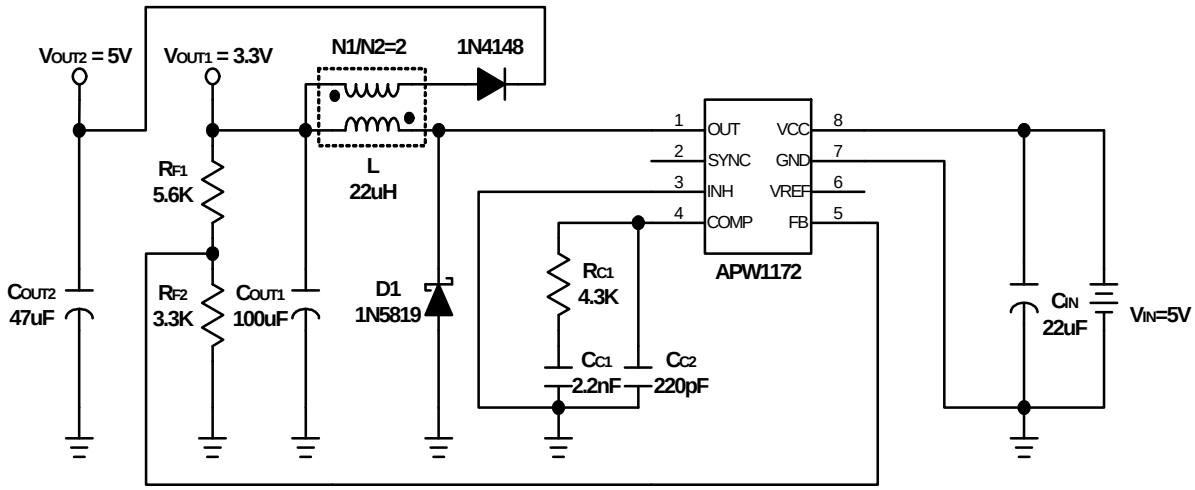


Typical Application Circuit

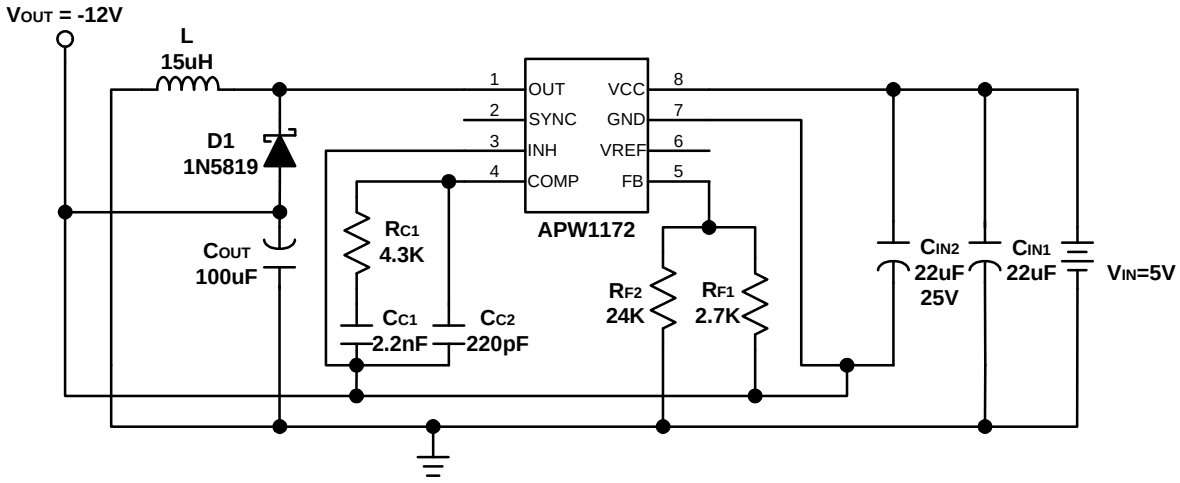


Typical Application Circuit (Cont.)

Dual output voltage application

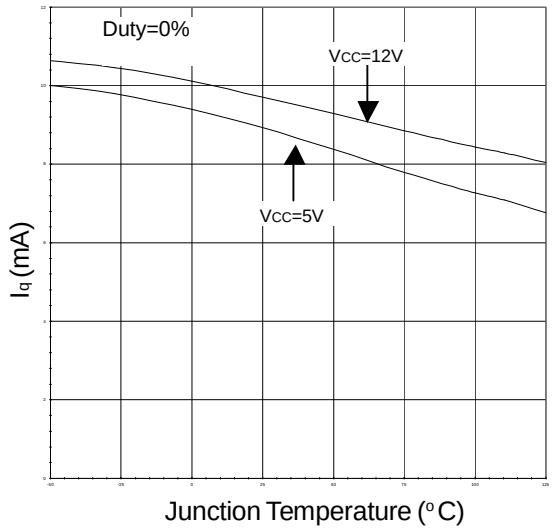


BuckBoost regulator

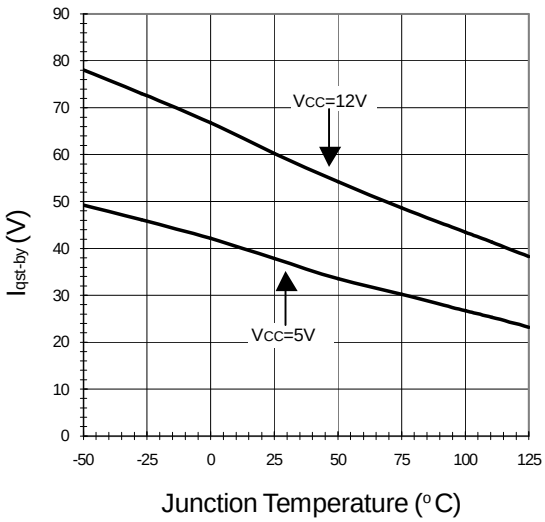


Typical Operating Characteristics

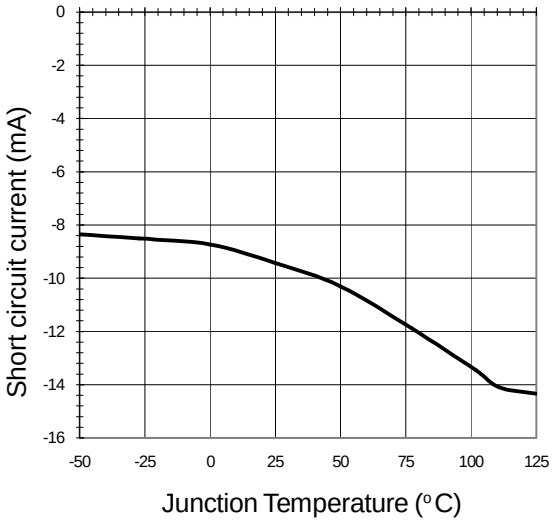
Quiescent Current



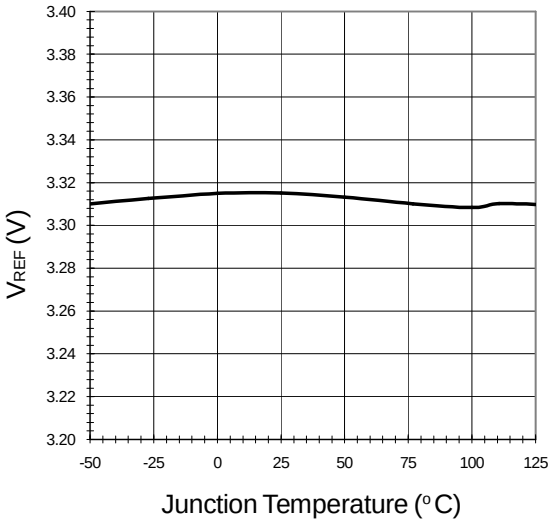
Quiescent Standby Current



Short Circuit Current of V_{REF}

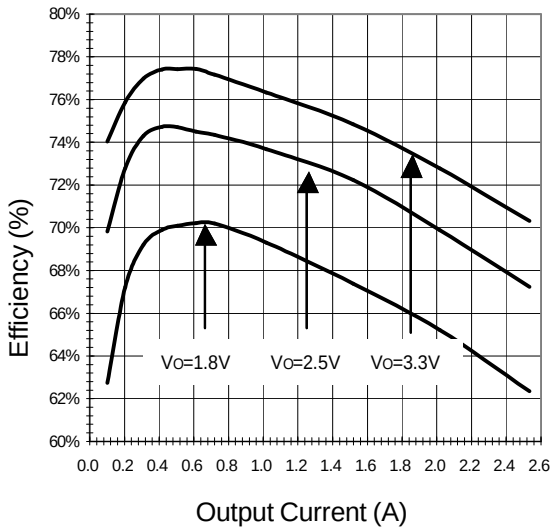


V_{REF}

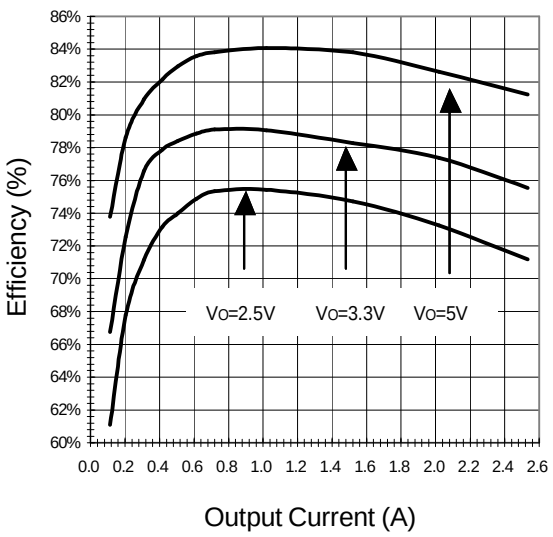


Typical Operating Characteristics (Cont.)

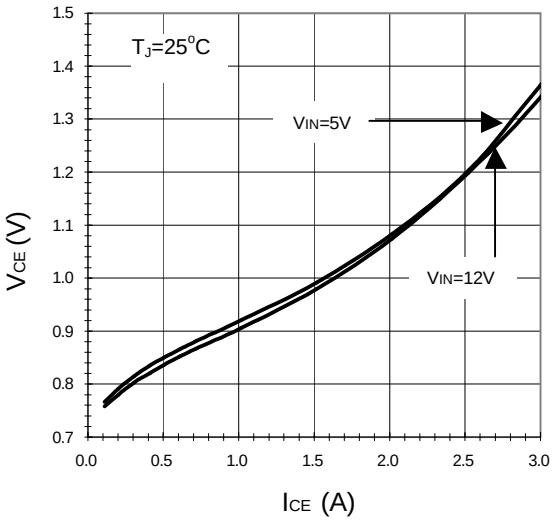
Efficiency vs. Output Current at V_{IN}=5V



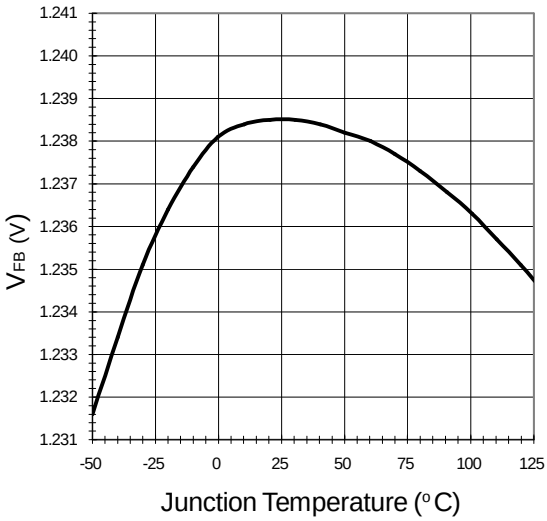
Efficiency vs. Output Current at V_{IN}=12V



V_{CE} vs. I_{CE}

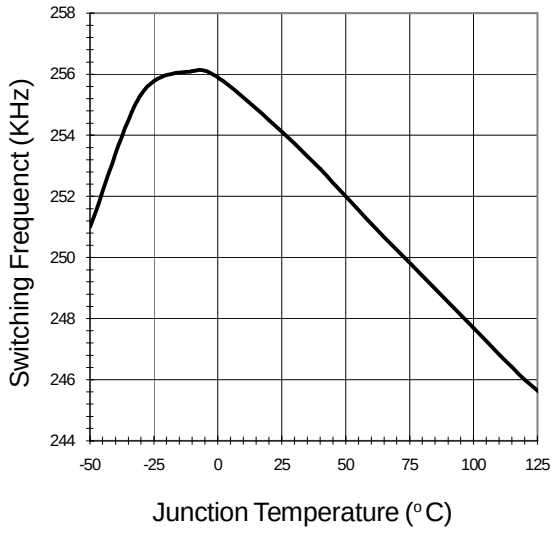


V_{FB} vs. Temperature



Typical Operating Characteristics (Cont.)

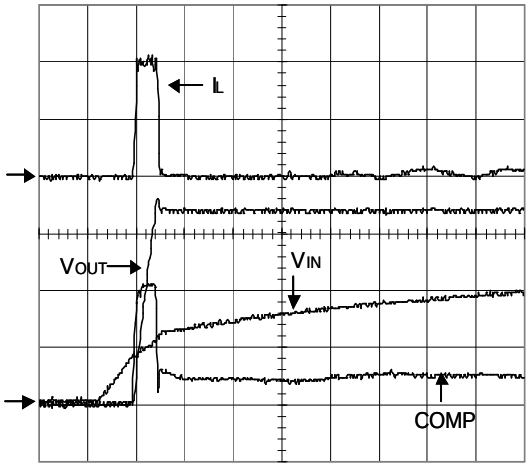
Switching Frequency



Operating Waveforms

1. Power ON (no SS) :

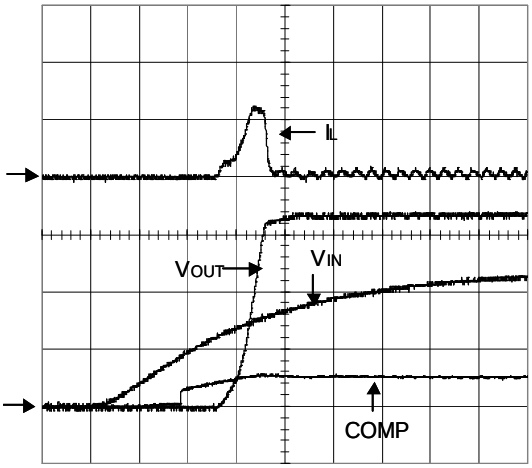
- V_{IN} = 12V,V_{OUT} = 3.3V
- C_{IN} = 22µF, C_{OUT} = 220µF, L = 15 µH



Ch1 : V_{OUT},1V/div
Ch2 : COMP,2V/div
Ch3 : V_{IN},5V/div
Ch4 : I_L,2A/div
Time : 400us/div

2. Power ON (external SS) :

- V_{IN} = 12V,V_{OUT} = 3.3V
- C_{IN} = 22µF, C_{OUT} = 220µF, L = 15 µH

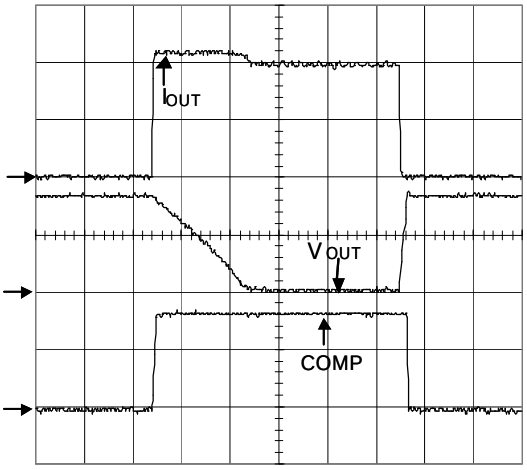


Ch1 : V_{OUT},1V/div
Ch2 : COMP,2V/div
Ch3 : V_{IN},5V/div
Ch4 : I_L,2A/div
Time : 1ms/div

Operating Waveforms (Cont.)

3. Current Limit :

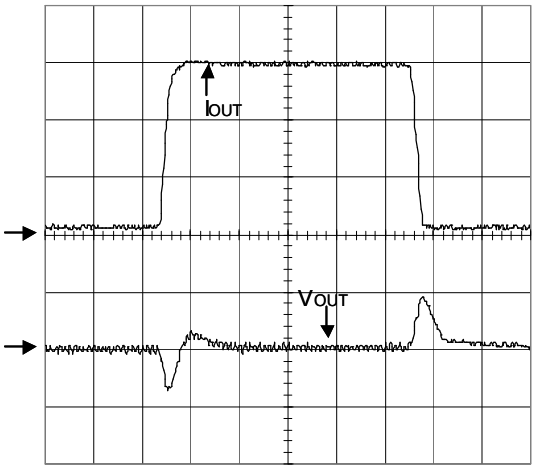
- V_{IN} = 12V,V_{OUT} = 3.3V
- C_{IN} = 22µF, C_{OUT} = 220µF, L = 15 µH



Ch1 : V_{OUT},2V/div
Ch2 : COMP,2V/div
Ch3 : I_{OUT},2A/div
Time : 2ms/div

4. Load Transient :

- V_{IN} = 12V,V_{OUT} = 3.3V
- C_{IN} = 22µF, C_{OUT} = 220µF, L = 15 µH



Ch1 : V_{OUT},200mV/div,offset 3.3V
Ch2 : I_{OUT},1A/div,100mA-3A
Ch2 rising time : 4us
Ch2 falling time : 4us
Time : 10us/div

Function Description

Power-On-Reset

A Power-On-Reset circuit monitors input voltages at VCC pin to prevent wrong logic controls. The POR function initiates immediately by the inductor current with its limit after the supply voltage exceeds firstly its threshold voltage after powering on.

Output Voltage Regulation

An error amplifier working with a temperature-compensated 1.235V reference. The error amplifier designed with high bandwidth and DC gain provides very fast transient response and less load regulation. It compares the reference with the feedback voltage and amplifies the difference in its output called error signal. The error signal feeds into the input terminal of PWM comparator and compared with internal saw tooth wave. It generates a PWM control signal by the PWM comparator. The PWM signal feeds into the logic circuit and turns on or off the pass element. The Buck type output stage regulates the correct output voltage depends on the previous mechanism.

Current-Limit

The APW1172 monitors the current flow through the pass element and limits the maximum output current to prevent damages during overload or short-circuit conditions.

Over-Voltage Protection (OVP)

The over-voltage protection is realized by using an in-

Function Description (Cont.)

Over-Voltage Protection (OVP) (Cont.)

ternal comparator. The input of the OVP comparator connects to the feedback, that turns off the pass element when the OVP threshold is reached. This threshold is typically 25% higher than the feedback voltage.

Thermal protection

The thermal protection function generates a control signal to shut off the APW1172. It prevents the damages caused by over heat situation. The thermal function was acted when the temperature of chip reaching 160°C. A hysteresis of the thermal protection function is approximately 30°C in order to avoid pass element turns on and off immediately.

Voltage Feed Forward

The Voltage Feed Forward is acting when VCC goes higher than 10V. This will increase the upper bond of the internal sawtooth wave and results duty keeping constant. The change of the upper bond is linear and proportion with VCC.

Frequency Fold Back

The Frequency Fold Back function acts when both the current-limit function acting and VOUT dropping. This results the switching frequency decreased. In the practical application, when the load current increases big enough, current-limit occurring. In this situation, more load current cause the output voltage getting away the regulatory point and begin dropping until it's limitation. In this time, the actual duty was very small in general. However, the on time period is limited by the minimum on time limitation of the control circuit. This on time limitation induces the load current running away the limiting boundary. To prevent this drawback, the frequency fold back is used to ensure that load current was limited by the setup value.

Inhibit Function

The Inhibit function disables when the Inhibit voltage is lower than 1.3V. APW1172 enteres the standby mode with Inhibit voltage higher than 1.4V. The quiescent current in the standby mode is less than 100uA to saving power. If the Inhibit pin left floating, the Inhibit voltage will be pull up by internal current source.

Application Information

Input Capacitor

The APW1172 requires proper input capacitors to supply current surge during stepping load transients to prevent the input rail from dropping. Due to the wide range of input voltage, the input capacitor must be able to support the input operating voltage. Ultra-low-ESR capacitors, such as ceramic chip capacitors, are very good for the input capacitors. An aluminum electrolytic capacitor(>100μF, ESR<300mΩ) is recommended as the input capacitor. It is not necessary to use low-ESR capacitors. More capacitance reduce the variations of the input voltage of VCC pin.

Inductor

Inductor is an important component in the application. In the switching regulator, energy is stored in the inductor by magnetic field when the pass element conducting. This behavior causes the ripple current cycle by cycle, the ripple current flowing through the

Application Information (Cont.)

Inductor (Cont.)

output capacitor induces the output ripple voltage. In general, the ripple current is usually fixed at 20%~40% of maximum output current, that is 0.6A~1.2A with maximum output current equals to 3A. The value of inductor can be approximate by (1)

$$L = \frac{V_{IN} - V_{CE} - V_O}{\Delta I} T_{on} \quad (1)$$

Where V_{IN} is the input voltage, V_{CE} is the voltage across the pass element when it conducts, V_O is the output voltage, ΔI is the ripple current flowing through the inductor and Ton is the on period that determined by V_O and V_{IN}. The exact Ton can be obtained by (2) and (3)

$$D = \frac{V_O + V_D}{V_{IN} - V_{CE} + V_D} \quad (2)$$

Where VD is the forward voltage of the wheeling diode.

$$T_{on} = DT_S \quad (3)$$

Where T_S is the period of whole cycle. It equals to $1/F_S$ where F_S is the switching frequency of APW1172. For example, V_{IN} = 12V, V_O = 3.3V, V_D = 0.7V, I_O = 3A, ripple current is I_O (20%~40%) = 0.6A ~ 1.2A, V_{CE} =1.2V, F_S = 250kHz

$$D = \frac{3.3V + 0.7V}{12V - 1.2V + 0.7V} = 34.78\% \quad \text{by (2)}$$

$$T_{on} = DT_S = 34.78\% \times 4\mu s = 1.3912\mu s \quad \text{by (3)}$$

For the worst case ripple current equals to 0.6A ~ 1.2A

$$L_1 = \frac{12V - 1.2V - 3.3V}{0.6A} 1.3912\mu s = 17.39\mu H$$

for ripple current is 0.6A…… by (1)

$$L_2 = \frac{12V - 1.2V - 3.3V}{1.2A} 1.3912\mu s = 8.695\mu H$$

for ripple current is 1.2A…… by (1)

Use the worst case to approximate the minimum value of inductor. In worst ripple current condition, smaller dimension of inductor to save the board space. In other way, devote the performance by higher ripple current. If selects a greater inductor, the ripple current will be smaller and a better performance is got. This tradeoff is an useful method to decide a better performance or a smaller inductor size.

Output Capacitor

The APW1172 requires a proper output capacitor to maintain stability and improve transient response over temperature and current. The output capacitor selection is dependent upon ESR (equivalent series resistance) and capacitance of the output capacitor over the operating temperature.

Consider the output ripple voltage that absorbed in the application. Output ripple voltage consists of two parts.It is shown as (4)

$$V_{ripple} = V_1 + V_2 \quad (4)$$

In previously, use the parameter ΔI to decide the value of the inductor. As the same manner, use the parameter ΔI to approximate the value of output capacitor.
The first part of output ripple voltage, V_1, is related to the ESR of output capacitor.It is shown as (5)

$$V_1 = ESR \times \Delta I \quad (5)$$

The second part of output ripple voltage, V_2, can be calculated by (6)

$$V_2 = \frac{\Delta I}{8C} T_S \quad (6)$$

These two parameters determine the value of output ripple voltage and the efficiency. More output ripple voltage cause the efficiency decreased.The output ripple voltage means the energy loss in the ESR and the energy loss in the transition path while the energy is stored and removed in the output capacitor. In other

Application Information (Cont.)

Output Capacitor (Cont.)

aspect, the ESR and the value of output capacitor generate a zero to provide a positive phase for control loop.This zero improves the stability without extra PID compensator if the zero is lower enough.

Switch diode

APW1172 is an non-synchronous type buck regulator and needs a Shottky diode as the wheeling diode. This diode will conduct when the pass element turned off. Current flows through the diode in the conducted period, the order of the maximum peak current reaches few Amperes. The diode requires the ability to flow the great forward current. The peak forward current of the diode denote in the specification must greater than 15A, and the conducting time in this situation must greater than 8ms. 1N5818 is a suitable component.

Thermal Consideration

APW1172 is a switching regulator whose pass element inside, it has the ability to provide 3 Amperes. As the show in the block diagram, the structure of the pass element consists of a NPN and a PNP transistors. The voltage across the pass element, V_{CE}, is about 0.8V to 1.3V in the light load to heavy load. The product of V_{CE} and I_L, where I_L is current flowing through the inductor, generate thermal cause the junction temperature increased. The thermal stream conduct via the thermal pad of SOP-8P to the printed circuit board.The power dissipation of APW1172 can be approximated by (7)

$$P = (V_{CE} \times I_L \times D) + (V_{IN} \times I_L \times F_S)(T_R + T_F) \quad (7)$$

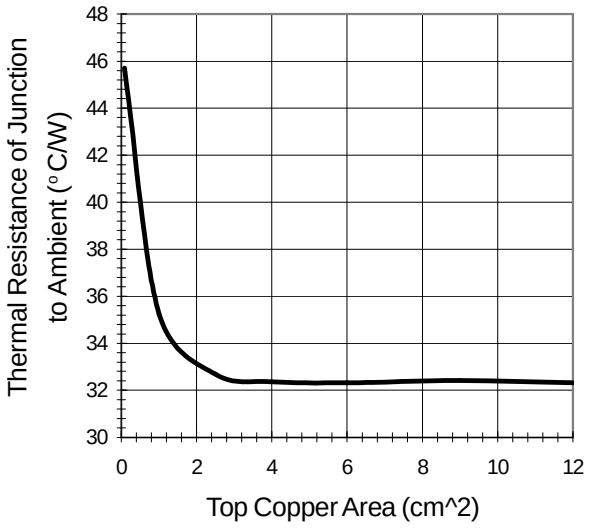
Where V_{CE} is the voltage across the pass element, I_L is the current flowing through the inductor, D is the duty. T_R and T_F are the transition time.

The wheeling diode is another thermal source. It's power dissipation approximated by (8)

$$P_D = V_D \times I_D \times (1 - D) \quad (8)$$

Where VD is the forward voltage of the wheeling diode, ID is current flowing through the wheeling diode when it conducting. In the PCB layout, usually place the wheeling diode near the APW1172, the power dissipation of wheeling diode will increase the ambient temperature and limit the maximum power dissipation of APW1172. These power dissipations are the major energy loss in the voltage conversion.

To improve the thermal resistance by increasing copper area is a suitable method. Design a copper area according to the following curve to improve the thermal resistance.



Frequency Compensation

In the Buck converter, there is a LPF (Low Pass Filter) in the output stage to filter the switching noise. The LPF consists of an inductor and a capacitor. These two components generate the double poles in the frequency domain.

$$f_{natural} = \frac{1}{2p\sqrt{LC}} \quad (9)$$

Where L is the inductance of the LPF, and C is the capacitance of the output capacitor. These double poles

Application Information (Cont.)

Frequency Compensation (Cont.)

cause the phase decreasing rapidly at the natural frequency and leading the phase margin not enough to maintain the stable status. The stable issue is improved by apply a zero in the frequency domain to increase the phase margin.

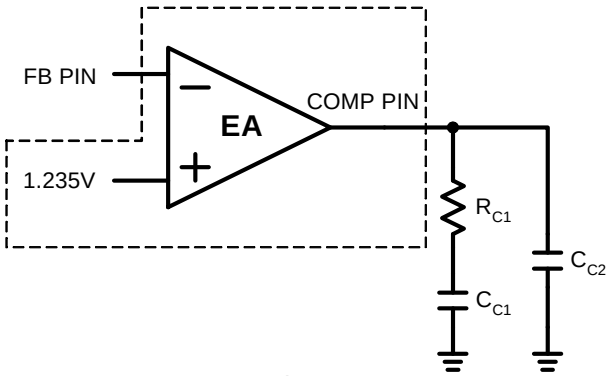


Figure-1

Adding a resistor and a capacitor to the COMP pin is the simplest way to generate a zero. The placement of the components is shown in Figure-1. The frequency of the zero is

$$f_{zero} = \frac{1}{2pR_{C1}C_{C1}} \quad (10)$$

The relation of the zero and the natural frequency is

$$f_{zero} = 0.8 \cdot f_{natural} \quad (11)$$

Locate the zero before the natural frequency to compensate the phase. Another capacitor, C_{C2}, is used to bypass the noise. In general

$$C_{C2} = \frac{1}{10} C_{C1} \quad (12)$$

In other applications, use the ceramic capacitor as the output capacitor is very popular. Because the small dimension of the ceramic capacitor save the PCB (Printed Circuit Board) area, the low ESR (Equivalent Series Resistance) of the ceramic one decreases the power dissipation of the output capacitor. But the serious drawbacks of the ceramic one is the stable issue.

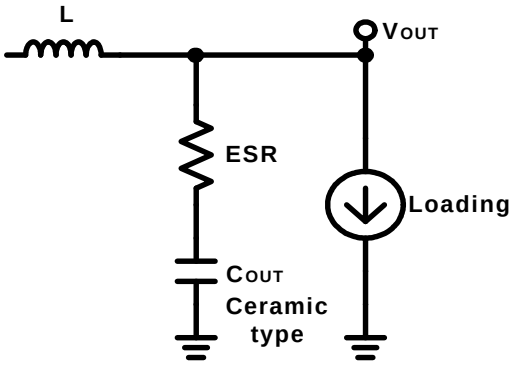


Figure-2

Consider the Figure-2, find the transfer function H (s) as:

$$H(s) = \frac{SC_{OUT}(ESR)+1}{S^2 LC_{OUT} + SC_{OUT}(ESR)+1}$$

$$pole_{1,2} = \frac{1}{2\pi\sqrt{LC_{OUT}}}$$

$$zero_1 = \frac{1}{2\pi(ESR)C_{OUT}}$$

$$Q = \frac{1}{(ESR)}\sqrt{\frac{L}{C_{OUT}}}$$

The pole1 and pole2 are the conjugate roots of the denominator and the zero1 is the root of the numerator. Find the Q factor from the quadratic function and the description of Q factor as above.

The frequency response of the output stage is shown as Figure-3.

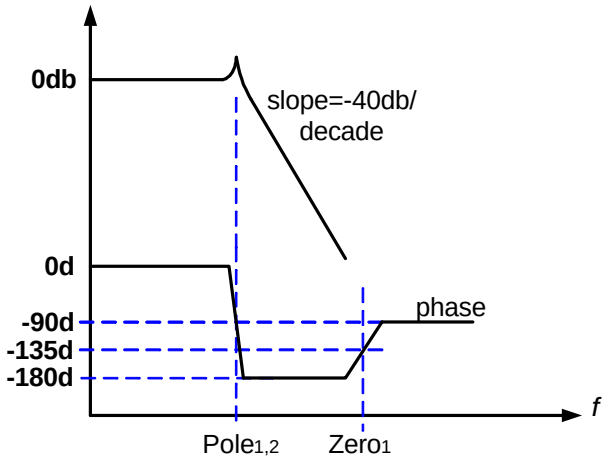


Figure-3

Application Information (Cont.)

Frequency Compensation (Cont.)

The problem is the phase nearly –180 degrees at the natural frequency especially in the high Q situation. If the Q factor is high, the phase decreases vary sharp at the location of the double poles. This problem leads the regulator oscillating when using ceramic one as the output capacitor without compensation. The purpose of the compensation is to save the phase. The manner is added additional zeros to achieve the goal. A zero has the ability to contribute the maximum phase of 90 degrees. According to this characteristic, needs two zeros to compensate the phase loss. The PID compensator is good for this. It is shown as Figure-4.

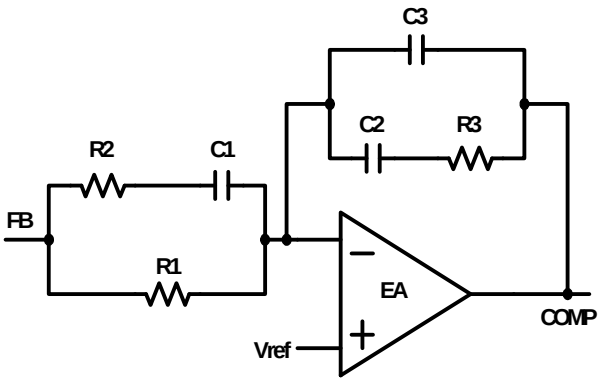


Figure-4

The transfer function H(s) is

$$H(s)=\frac{(SC_2R_3+1)[SC_1(R_1+R_2)+1]}{S(SC_1R_2+1)[SC_2C_3R_3+(C_2+C_3)]}$$

$$zero_2=\frac{1}{2p\cdot C_2R_3}$$

$$zero_3=\frac{1}{2p\cdot C_1(R_1+R_2)}$$

$$pole_3=\frac{1}{2p\cdot C_1R_2}$$

$$pole_4=\frac{C_2+C_3}{2p\cdot C_2C_3R_3}$$

The frequency response of the PID compensator is presented as Figure-5:

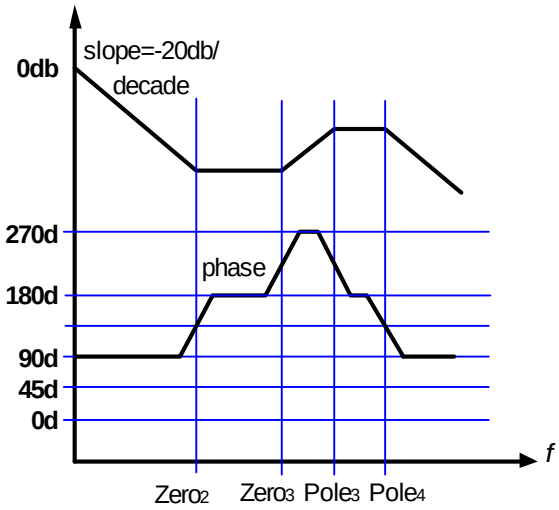


Figure-5

The assumption is 10(zero2)<zero3,10(zero3)<pole3, and 10(pole3)<pole4. In order to compensate the phase, place the two zeros closely and located before the natural frequency. In general

$$zero_2\cong zero_3=k\cdot pole_{1,2} \qquad (11)$$

Where k is a constant, the value of k is almost 0.7 to 0.8.

The useful rules are:

(1) Determine the value of C2, the value must smaller than 5nF to get fast response time.

(2) Find R3 by the equation

$$R_3=(2p\cdot C_2\cdot k\cdot pole_{1,2})^{-1}$$

(3) Determine the value of C1 from 470pF to 1µF. This range of C1 is for reference.

(4) The range of pole3 is from 150kHz to 300kHz. Use this range to find the value of R2.

(5) Find R1 by the equation

$$R_1=(2\pi\cdot C_1\cdot k\cdot pole_{1,2})^{-1}-R_2$$

(6) The location of pole4 is 5 times pole3. Use this result to find the value of R3.

Layout Consideration

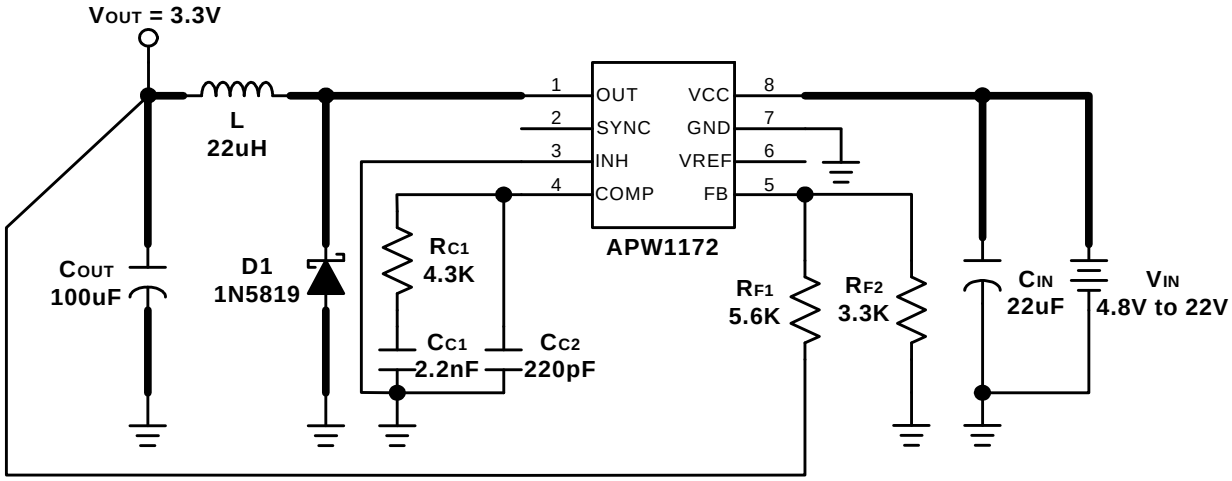
1. Please solder the Exposed Pad on the PCB.The heat generated by the power consumption will conduct by the thermal pad.

2. Please place the input capacitors for VCC pin nearly as close as possible.

3. Connect the switching inductor and the Schottky diode and OUT pin by a wide track.

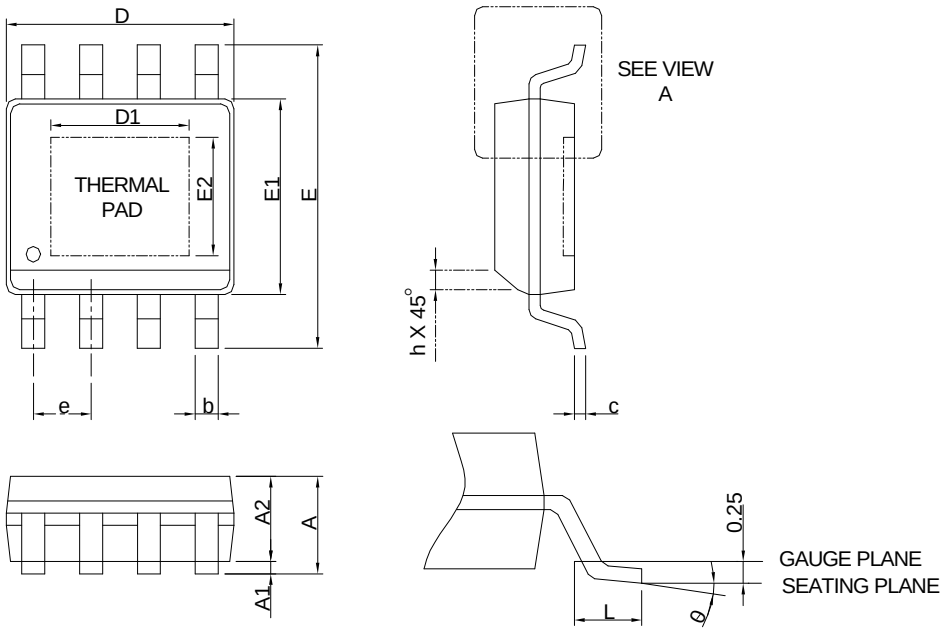
4. Place the output capacitor close to the inductor as possible and with a wide and short track.

5.The thermal pad is needed to improve the power dissipation.



Package Information

SOP-8P



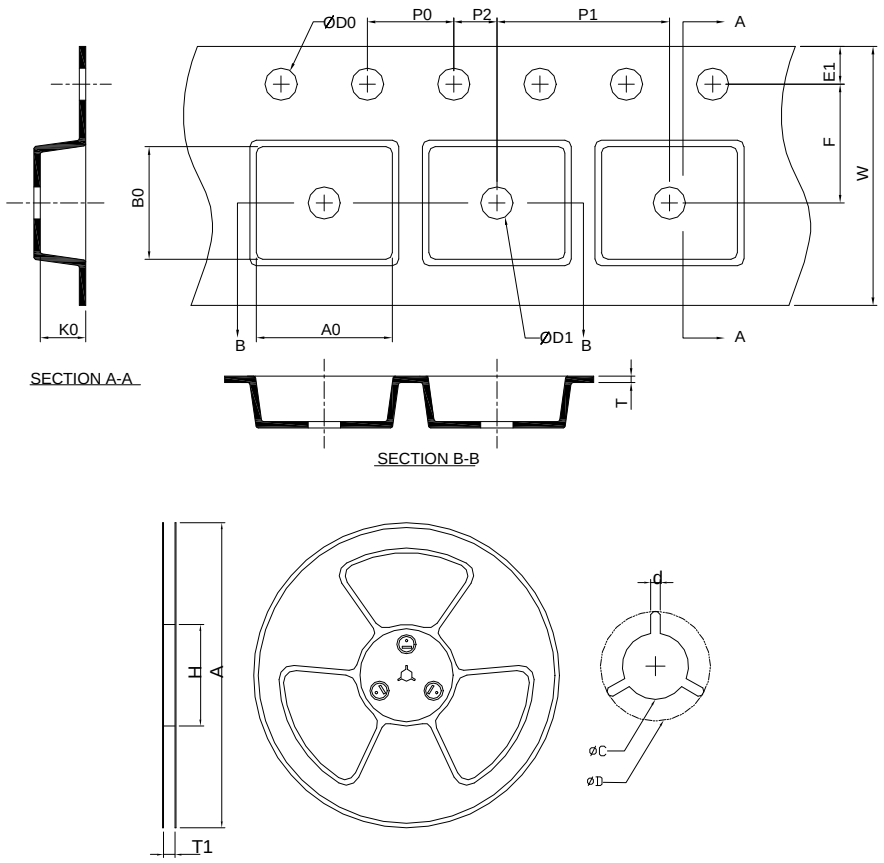
SYMBOL	SOP-8P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.60		0.063
A1	0.00	0.15	0.000	0.006
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
D1	2.25	3.50	0.098	0.138
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
E2	2.00	3.00	0.079	0.118
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note : 1. Follow JEDEC MS-012 BA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .

3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



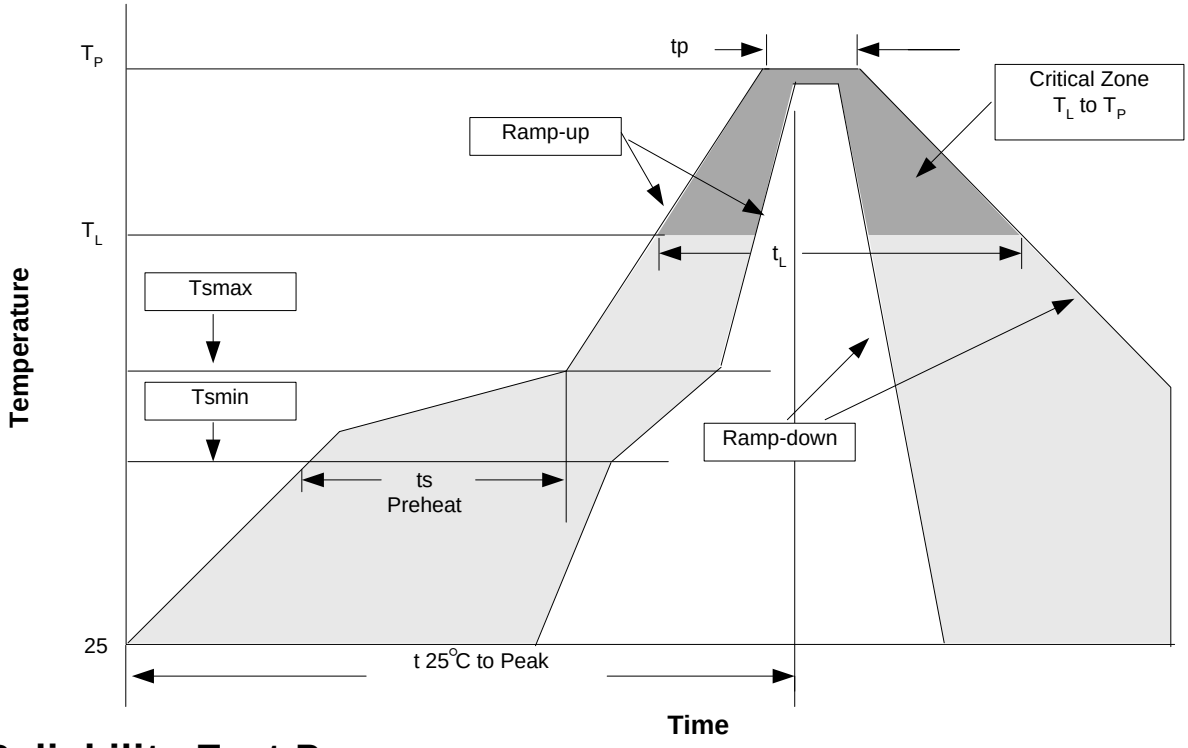
Application	A	H	T1	C	d	D	W	E1	F
SOP-8P	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20

(mm)

Devices Per Unit

Package Type	Unit	Quantity
SOP-8P	Tape & Reel	2500

Reflow Condition (IR/Convection or VPR Reflow)



Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 sec
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B, A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1_{tr} > 100mA

Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classification Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Notes: All temperatures refer to topside of the package. Measured on the body surface.

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*

* Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.

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