1.5A, DC/DC Switching Regulators

Features

- Operation from 3.0V to 40V Input
- Low Standby Current
- Current Limiting
- Output Switch Current to 1.5A
- Output Voltage Adjustable
- Frequency Operation to 100kHz
- Precision 2% Reference
- SOP-8 and PDIP-8 packages
- Lead Free Available (RoHS Compliant)

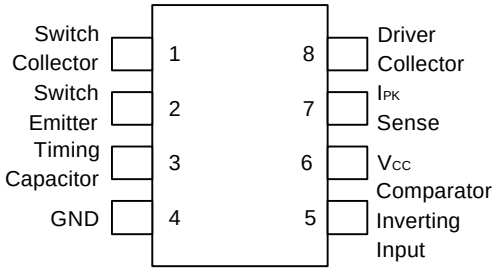
Applications

- DC/DC Converters

General Description

The APW34063 is a monolithic control circuit containing the primary functions required for DC-to-DC converters. This device consists of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This device was specifically designed to be incorporated in Step-Down and Step-Up and Voltage-Inverting applications with a minimum number of external components.

Pin Description



Ordering and Marking Information

APW34063 □□-□□□

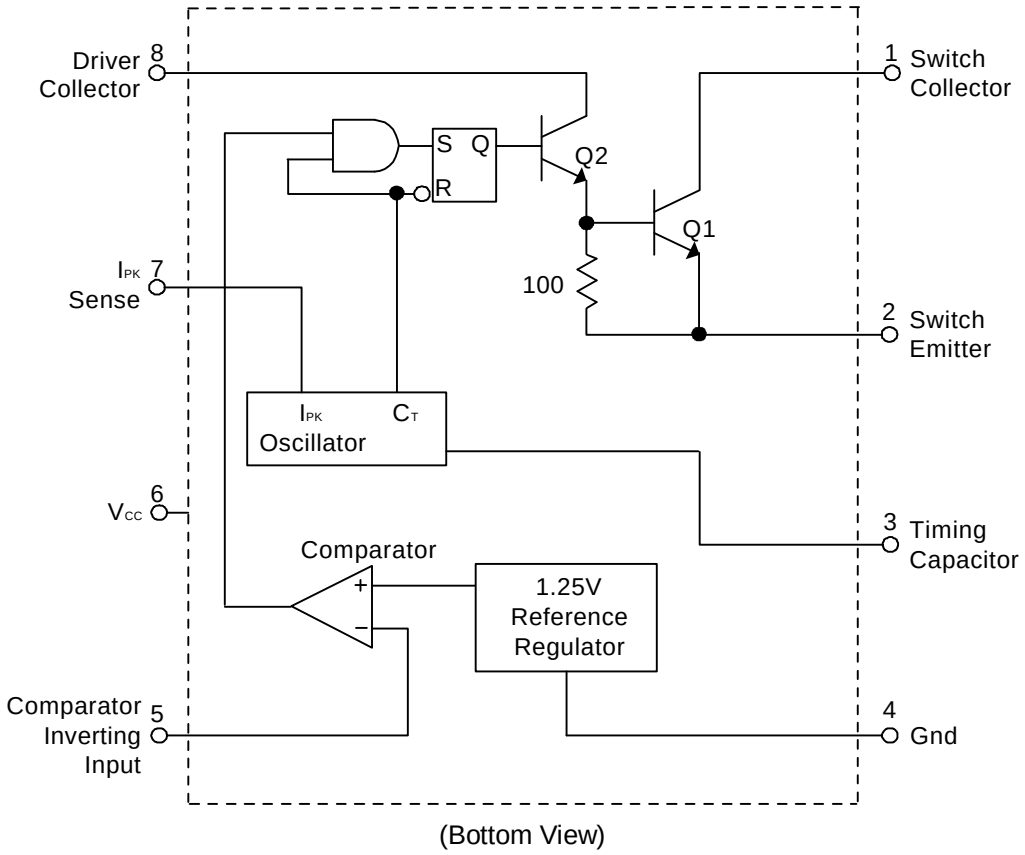
- Lead Free Code
- Handling Code
- Temp. Range
- Package Code

Package Code
J : PDIP - 8 K : SOP-8
Temp. Range
C : 0 to 70 °C
Handling Code
TU : Tube TR : Tape & Reel
Lead Free Code
L : Lead Free Device Blank : Original Device

APW34063 J :	APW34063 XXXXX	XXXXX - Date Code
APW34063 K :	APW34063 XXXXX	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldiering operations. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

Block Diagram



(Bottom View)

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Voltage	40	Vdc
V_{IR}	Comparator Input Voltage Range	-0.3 to +40	Vdc
$V_{C(Switch)}$	Switch Collector Voltage	40	Vdc
$V_{E(Switch)}$	Switch Emitter Voltage (V_{PIN1}=40V)	40	Vdc
$V_{CE(Switch)}$	Switch Collector to Emitter Voltage	40	Vdc
$V_{C(driver)}$	Driver Collector Voltage	40	Vdc
$I_{C(driver)}$	Driver Collector Current (Note1)	100	mA
I_{SW}	Switch Current	1.5	A
P_D	Power Dissipation PDIP-8 SOP-8	 1.25 625	 W mW

Note :

1. Maximum package power dissipation limits must be observed.

Absolute Maximum Ratings (Cont.)

Symbol	Parameter	Value	Unit
T_J	Operating Junction Temperature	+150	°C
T_A	Operating Ambient Temperature Range	0 to +70	°C
T_{Stg}	Storage Temperature Range	-65 to +150	°C

Thermal Characteristics

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance – Junction to Ambient PDIP-8 SOP-8	 100 160	°C/W

Electrical Characteristics

V_{CC}=5.0V, T_A=T_{low} to T_{high} (Note2), unless otherwise specified.

Symbol	Parameter	Test Conditions	APW34063			Unit
			Min.	Typ.	Max.	
Oscillator						
F_{OSC}	Frequency	V_{PIN5} = 0V, C_T = 1.0nF, T_A = 25°C	24	33	42	kHz
I_{chg}	Charge Current	V_{CC} = 5.0V to 40V, T_A = 25°C	24	35	42	µA
I_{dischg}	Discharge Current	V_{CC} = 5.0V to 40V, T_A = 25°C	140	220	260	µA
$I_{dischg/Ichg}$	Discharge to Charge Current Ratio	Pin7 to V_{CC}, T_A=25°C	5.2	6.5	7.5	
$V_{ipk(sense)}$	Current Limit Sense Voltage	I_{chg} = I_{dischg}, T_A = 25°C	250	300	350	mV
Output Switch (Note3)						
$V_{CE(sat)}$	Saturation Voltage, Darlington Connection	I_{SW} = 1.0A, Pins 1,8 connected		1.0	1.3	V
	Saturation Voltage(Note4)	I_{SW} = 1.0A, R_{PIN8} = 82Ω to V_{CC}, Forced β = 20		0.45	0.7	
h_{FE}	DC Current Gain	I_{SW} = 1.0A, V_{CE} = 5.0V, T_A = 25°C	50	75		
$I_{C(off)}$	Collector Off-State Current	V_{CE} = 40V		0.01	100	µA
Comparator						
V_{TH}	Threshold Voltage	T_A = 25°C	1.225	1.25	1.275	V
		T_A = T_{low} to T_{high}	1.21		1.29	
Reg_{line}	Threshold Voltage Line Regulation	V_{CC} = 3.0V to 40V		1.4	5.0	mV
I_{IB}	Input bias Current	V_{IN} = 0V		-20	-400	nA
Total Device						
I_{CC}	Supply Current	V_{CC}=5.0V to 40V, C_T=1.0nF, Pin7= V_{CC}, V_{pin5}> V_{IN}, Pin2=Gnd, remaining pins open			4.0	mA

Electrical Characteristics (Cont.)

Note :

2.T_{low}=0°CV, T_{high}=+70°C

3.Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

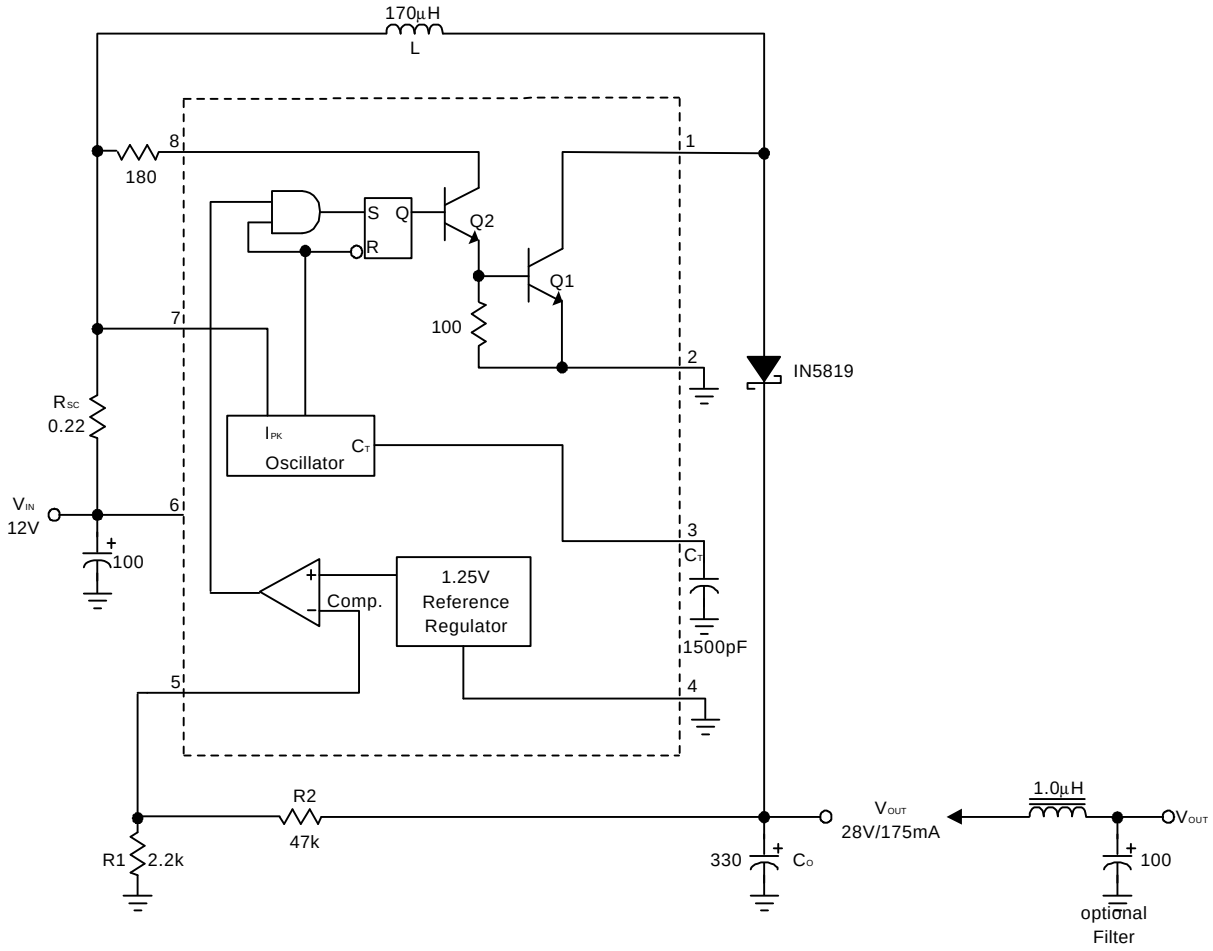
4.If the output switch is driven into hard saturation (non-Darlington configuration) at low switch currents (≤300mA) and high driver currents (≥30mA), it may take up to 2.0μs for it to come out of saturation. This condition will shorten the off time at frequencies≥30kHz, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non-Darlington configuration is used, the following output drive condition is recommended :

Forced β of output switch : $\frac{I_C \text{ output}}{I_C \text{ driver - 7.0mA*}} \geq 10$

* The 100Ω resistor in the emitter of the driver device requires about 7.0mA before the output switch conducts.

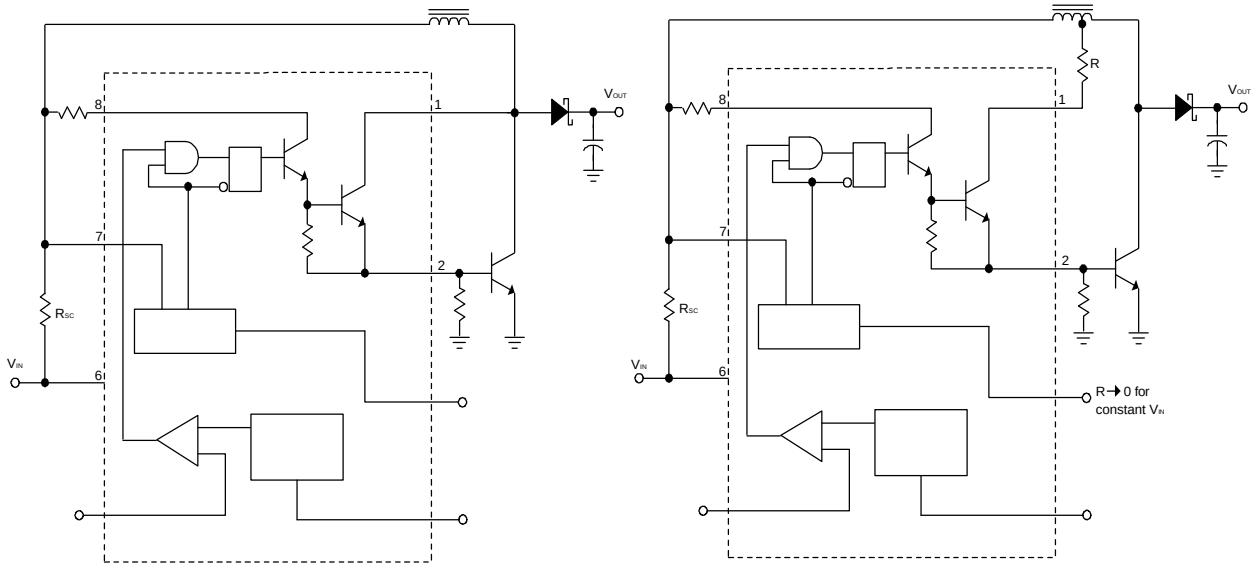
Typical Application Circuits

Step-Up Converter



Typical Application Circuits (Cont.)

External Current Boost Connections for I_C Peak Greater than 1.5A



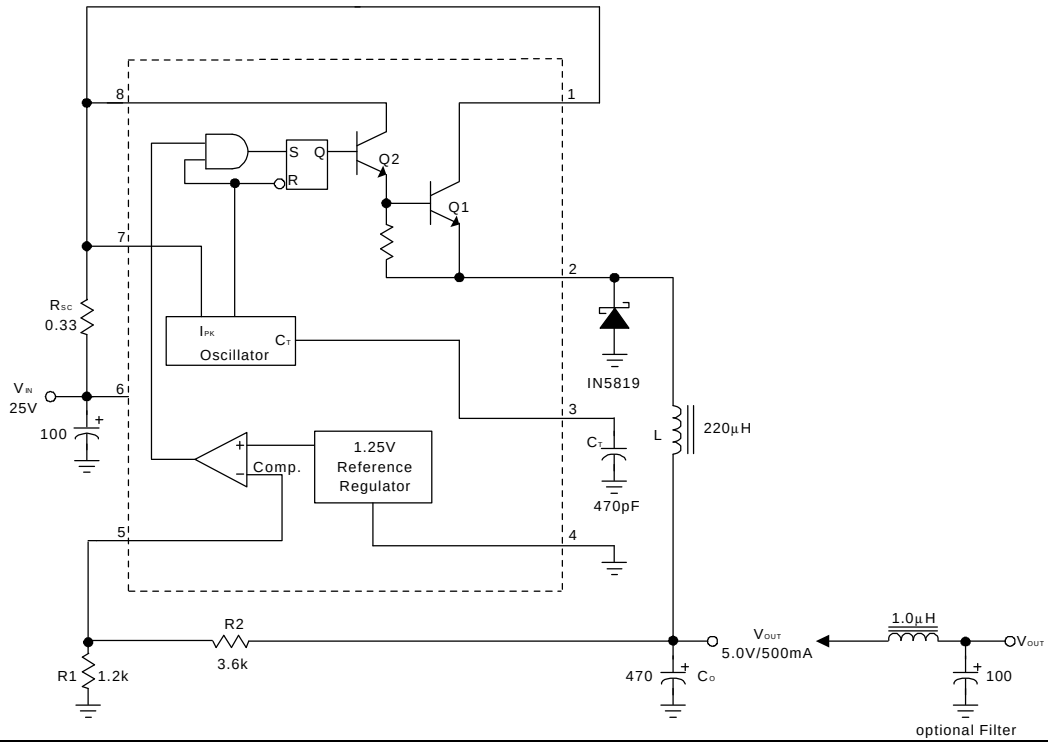
External NPN Switch

External NPN Saturated Switch (see Note5)

Note :

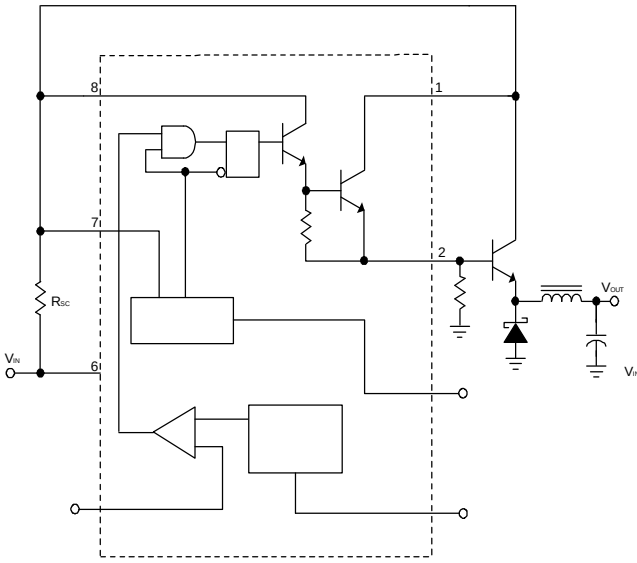
5.If the output switch is driven into hard saturation (non-Darlington configuration) at low switch currents (≤300mA) and high driver currents (≥30mA), it may take up to 2.0µs to come out of saturation. This condition will shorten the off time at frequencies≥30kHz, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non-Darlington configuration is used, the following output drive condition is recommended.

Step-Down Converter

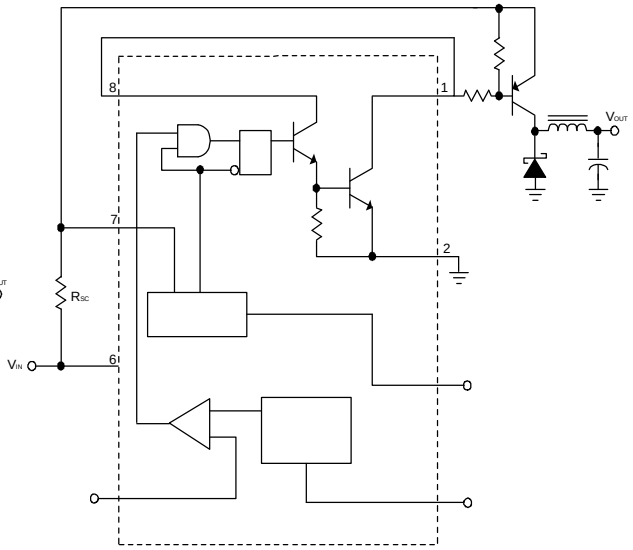


Typical Application Circuits (Cont.)

External Current Boost Connections for I_C Peak Greater than 1.5A

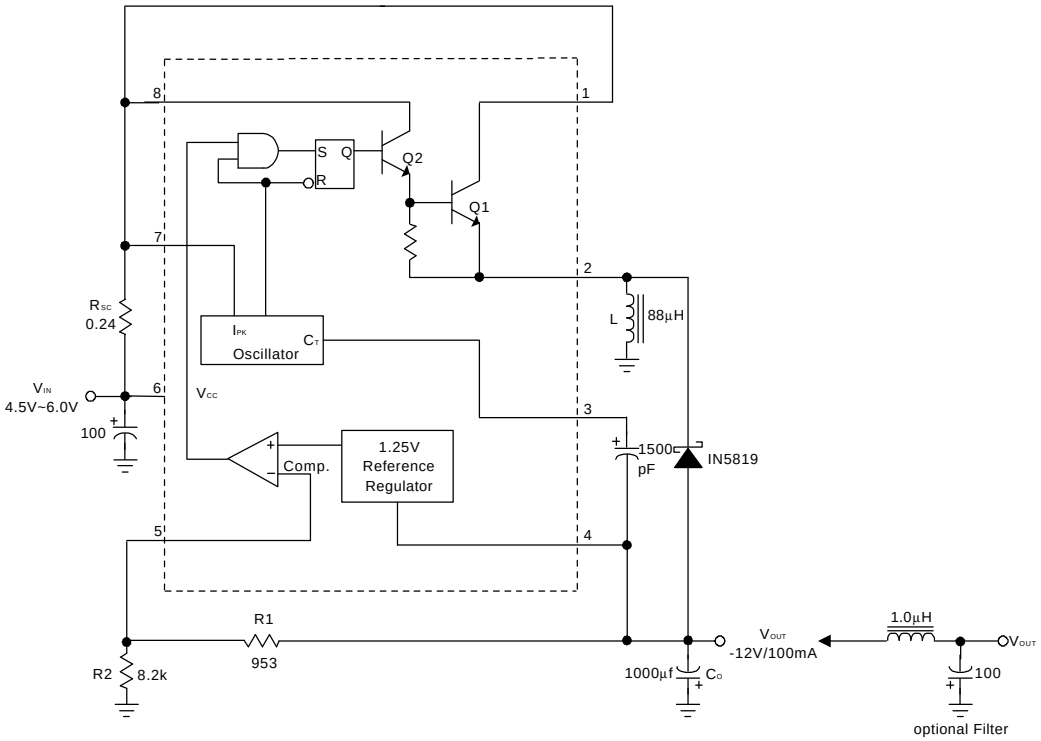


External NPN Switch



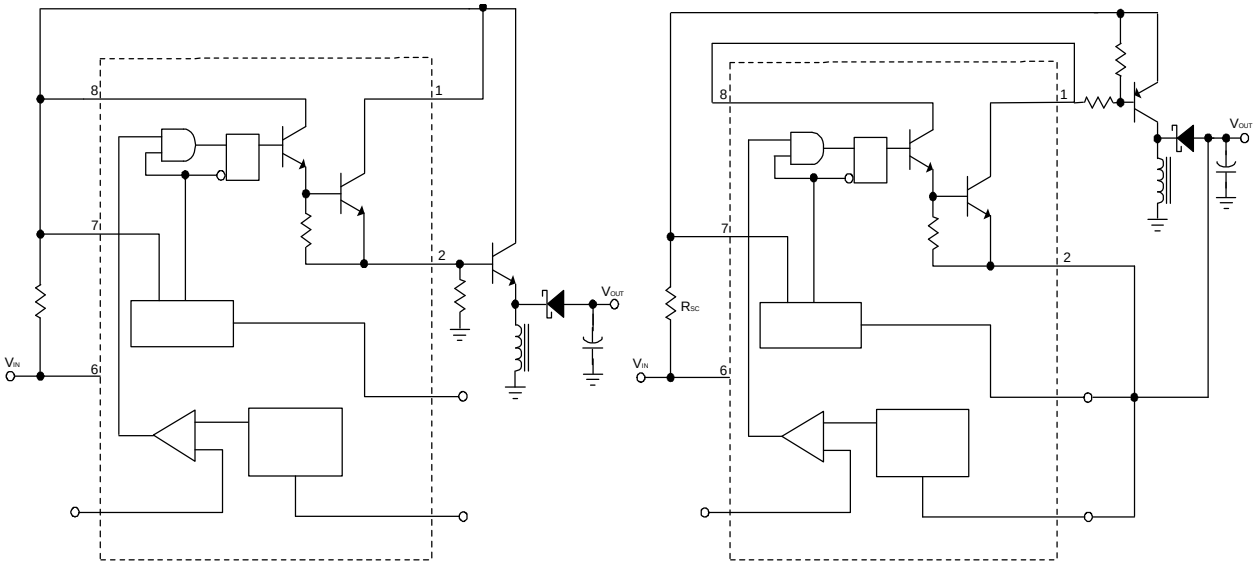
External PNP Saturated Switch

Voltage Inverting Converter



Typical Application Circuits (Cont.)

External Current Boost Connections for I_C Peak Greater than 1.5A



External NPN Switch

External PNP Saturated Switch

Design Formula Table

Calculation	Set-Up	Step-Down	Voltage-Inverting
t_{on} / t_{off}	$\frac{V_{out} + V_F - V_{in(min)}}{V_{in(min)} - V_{sat}}$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$	$\frac{\lvert V_{out}\rvert + V_F}{V_{in} - V_{sat}}$
$t_{on} + t_{off}$	$\frac{1}{f}$	$\frac{1}{f}$	$\frac{1}{f}$
t_{off}	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$
t_{on}	$(t_{on} + t_{off}) - t_{off}$	$(t_{on} + t_{off}) - t_{off}$	$(t_{on} + t_{off}) - t_{off}$
C_T	$4.0 \times 10^{-5}\ t_{on}$	$4.0 \times 10^{-5}\ t_{on}$	$4.0 \times 10^{-5}\ t_{on}$
$I_{pk(switch)}$	$2I_{out(max)} \left(\frac{t_{on}}{t_{off}} + 1\right)$	$2I_{out(max)}$	$2I_{out(max)} \left(\frac{t_{on}}{t_{off}} + 1\right)$
R_{sc}	$0.3 / I_{pk(switch)}$	$0.3 / I_{pk(switch)}$	$0.3 / I_{pk(switch)}$
$L_{(min)}$	$\left(\frac{V_{in(min)} - V_{Sat}}{I_{pk(switch)}}\right) t_{on(max)}$	$\left(\frac{V_{in(min)} - V_{Sat} - V_{out}}{I_{pk(switch)}}\right) t_{on(max)}$	$\left(\frac{V_{in(min)} - V_{Sat}}{I_{pk(switch)}}\right) t_{on(max)}$
C_O	$9 \frac{I_{out} t_{on}}{V_{ripple(pp)}}$	$\frac{I_{pk(switch)}(t_{on} + t_{off})}{8V_{ripple(pp)}}$	$9 \frac{I_{out} t_{on}}{V_{ripple(pp)}}$

Design Formula Table (Cont.)

V_{sat} = Saturation voltage of the output switch.

V_F = Forward voltage drop of the output rectifier.

The following power supply characteristics must be chosen :

V_{in} - Nominal input voltage.

V_{out} - Desired output voltage, $|V_{out}| = 1.25 \left(1 + \frac{R_2}{R_1} \right)$

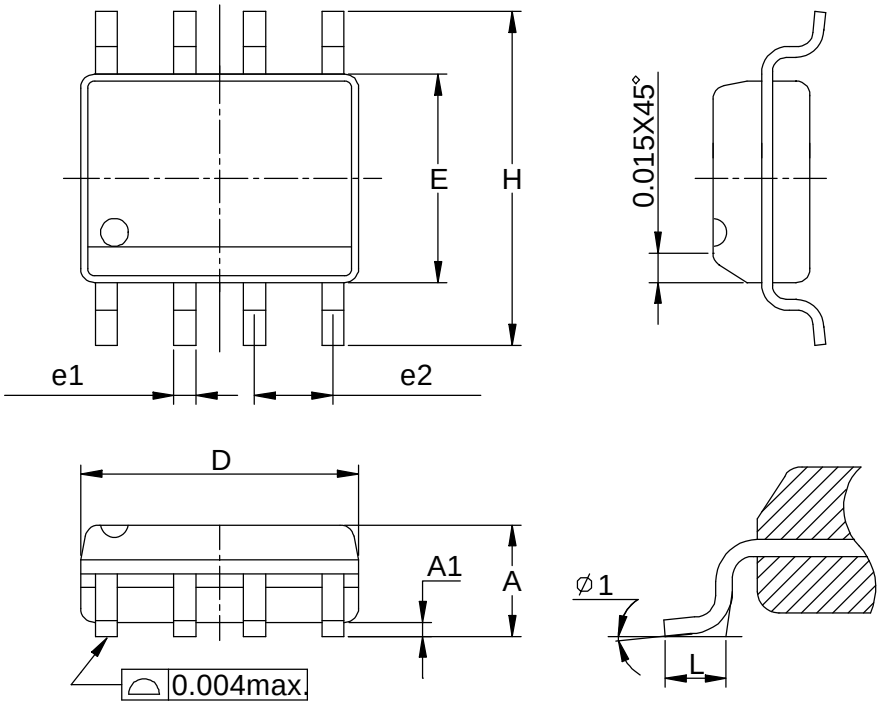
I_{out} - Desired output current.

f_{min} - Minimum desired output switching frequency at the selected values of Vin and Io.

$V_{ripple(pp)}$ - Desired peak-to-peak output ripple voltage. In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.

Packaging Information

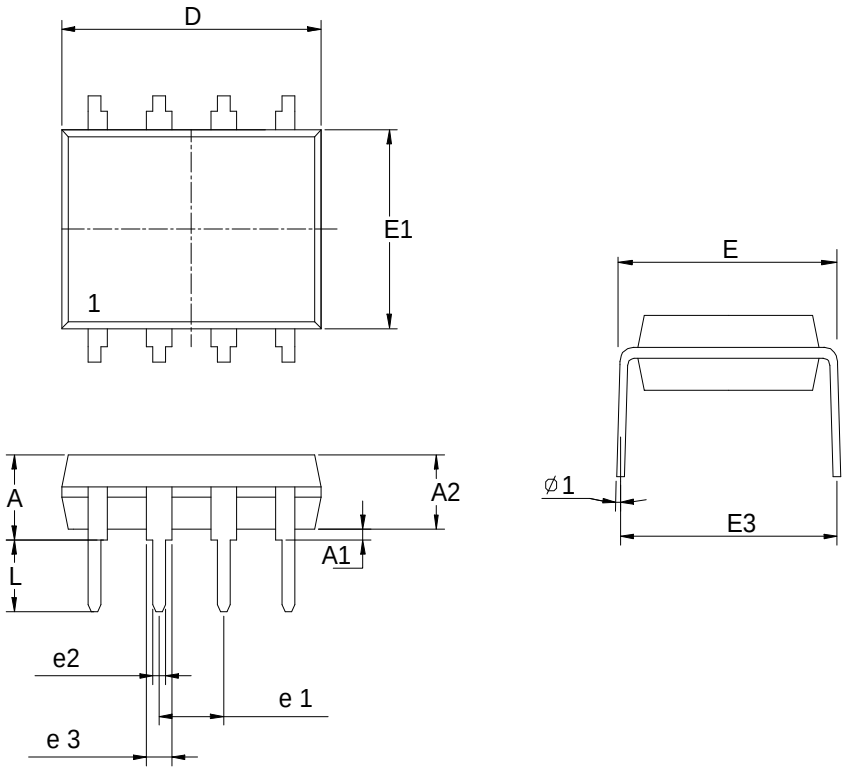
SOP-8 pin (Reference JEDEC Registration MS-012)



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.80	5.00	0.189	0.197
E	3.80	4.00	0.150	0.157
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
e1	0.33	0.51	0.013	0.020
e2	1.27BSC		0.50BSC	
ϕ 1	0°	8°	0°	8°

Packaging Information

PDIP-8 pin (Reference JEDEC Registration MS-001)

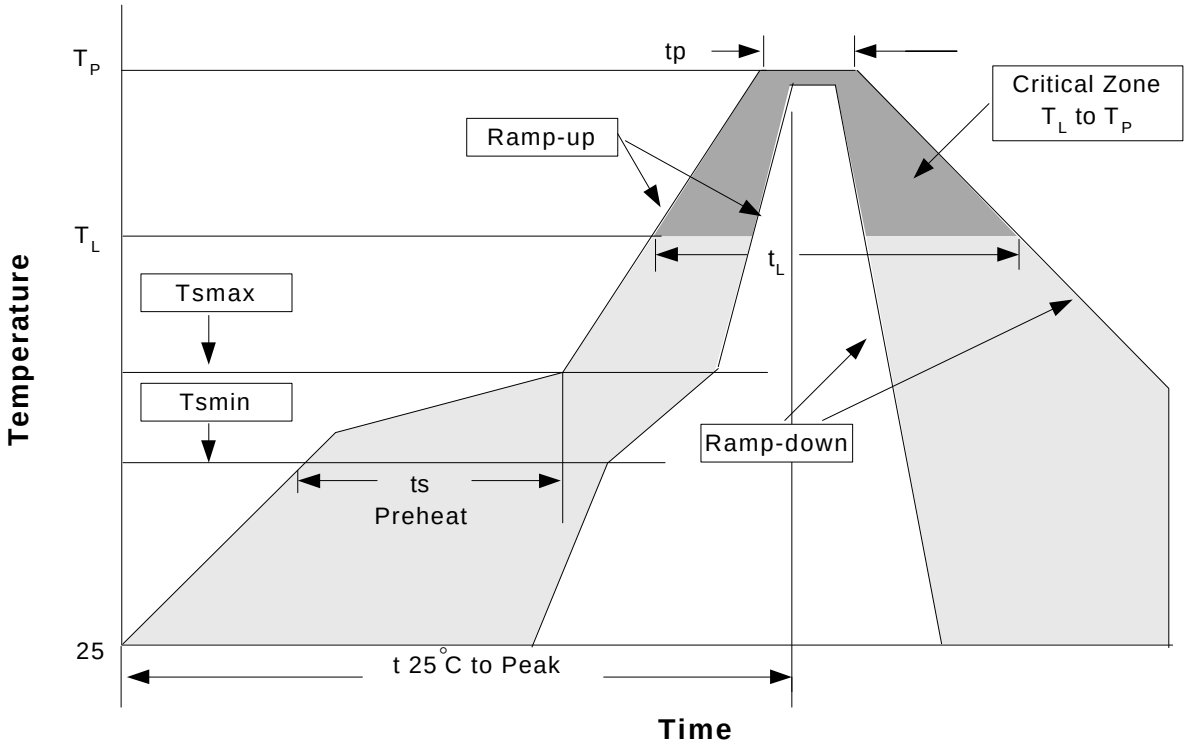


Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A		5.33		0.210
A1	0.38		0.015	
A2	2.92	3.68	0.115	0.145
D	9.02	10.16	0.355	0.400
e1	2.54 BSC		0.100 BSC	
e2	0.36	0.56	0.014	0.022
e3	1.14	1.78	0.045	0.070
E	7.62 BSC		0.300 BSC	
E1	6.10	7.11	0.240	0.280
E3		10.92		0.430
L	2.92	3.81	0.115	0.150
ϕ1	15° REF		15° REF	

Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb), 100%Sn
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.

Reflow Condition (IR/Convection or VPR Reflow)



Classificatin Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classificatioon Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Notes: All temperatures refer to topside of the package .Measured on the body surface.

(mm)

Classification Reflow Profiles(Cont.)

Table 1. SnPb Entectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

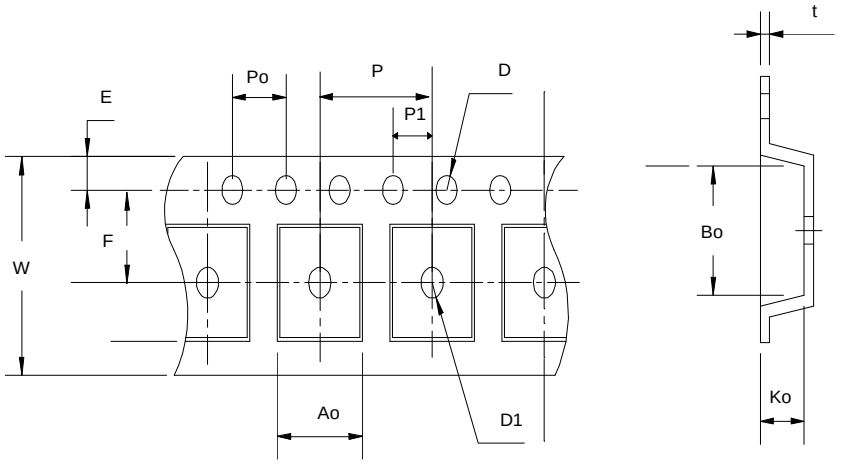
Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*
*Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.			

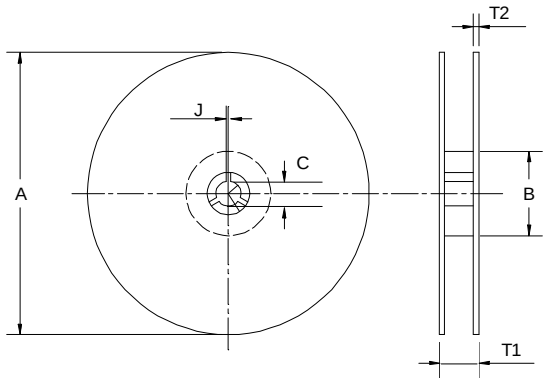
Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B,A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1_{tr} > 100mA

Carrier Tape & Reel Dimensions



Carrier Tape & Reel Dimensions(Cont.)



Application	A	B	C	J	T1	T2	W	P	E
SOP- 8	330 ± 1	62 +1.5	12.75+ 0.15	2 ± 0.5	12.4 ± 0.2	2 ± 0.2	12± 0. 3	8± 0.1	1.75±0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	5.5± 1	1.55 +0.1	1.55+ 0.25	4.0 ± 0.1	2.0 ± 0.1	6.4 ± 0.1	5.2± 0. 1	2.1± 0.1	0.3±0.013

(mm)

Cover Tape Dimensions

Application	Carrier Width	Cover Tape Width	Devices Per Reel
SOP- 8	12	9.3	2500

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