Advanced Dual PWM and Dual Linear Power Controllers

Features

- 4 Regulated Voltages are provided
  - Microprocessor Core (1.3V to 3.5V)
  - AGP Bus (1.5V or 3.3V)
  - Memory (1.8V) , GTL Bus (1.5V)
- Simple Single-Loop Control Designs
  Voltage-Mode PWM Control
- Fast PWM Converter Transient Response
  High-Bandwidth Error Amplifiers
  - Full 0% to 100% Duty Ratios
- Excellent Output Voltage Regulation
  - Core PWM Output : ± 1% Over Temperature
  - Other Outputs : ± 3% Over Temperature
- TTL-Compatible 5- Bit DAC Microprocessor Core Output Voltage Selection
  - Wide Range - 1.3V_{DC} to 3.5 V_{DC}
- Power-Good Output Voltage Monitor
- Over-Voltage and Over-Current Fault Monitors
- Small Converter Size
  - Constant Frequency Operation
  - 200kHz Free-Running Oscillator ; Programmable From 50kHz to Over 800kHz
  - Small External Component Count

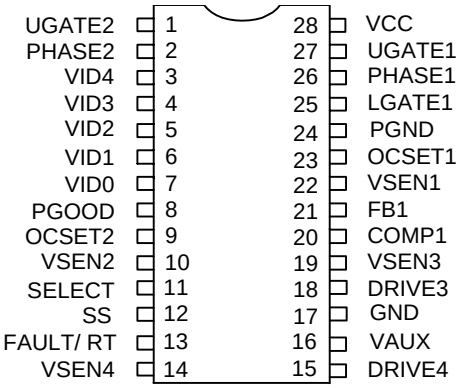
Applications

- Motherboard Power Regulation for Computers

General Description

The APW6020 provides the power control and protection for four output voltages in high-performance , graphics intensive microprocessor and computer applications. The IC integrates two voltage-mode PWM controllers and two linear controllers , as well as the monitoring and protection functions into a single package. One PWM controller regulates the microprocessor core voltage with a synchronous-rectified buck converter. The second PWM controller supplies the computer's AGP 1.5V or 3.3V bus power with a standard Buck converter. The linear controllers requlate the power for the 1.5V GTL bus , and the 1.8V power for the North/South Bridge core voltage and/or cache memory circuits. The APW6020 includes an Intel-compatible , TTL 5-input digital-to-analog converter (DAC) that adjusts the core PWM output voltage from 1.3 V_{DC} to 2.05 V_{DC} in 0.05V steps and from 2.1 V_{DC} to 3.5 V_{DC} in 0.1V increments. The precision reference and voltage-mode control provide ±1% static regulation. The second PWM controller's output is user-selectable , through a TTL-compatible signal applied at the SELECT pin , for levels of 1.5V or 3.3V with ±3% accuracy. The two linear regulators provide fixed output voltages of 1.5V± 3% (V_{OUT3}) and 1.8V±3% (V_{OUT4}).
The APW6020 monitors all the output voltages. A single Power Good signal is issued when the core is within ±10% of the DAC setting and all other outputs are above their under-voltage levels. Additional built-in over-voltage protection for the core output uses the lower MOSFET to prevent output voltages above 115% of the DAC setting. The PWM controller's over-current function monitors the output current by using the voltage drop across the upper MOSFET's $r_{DS(ON)}$.

Pin Description



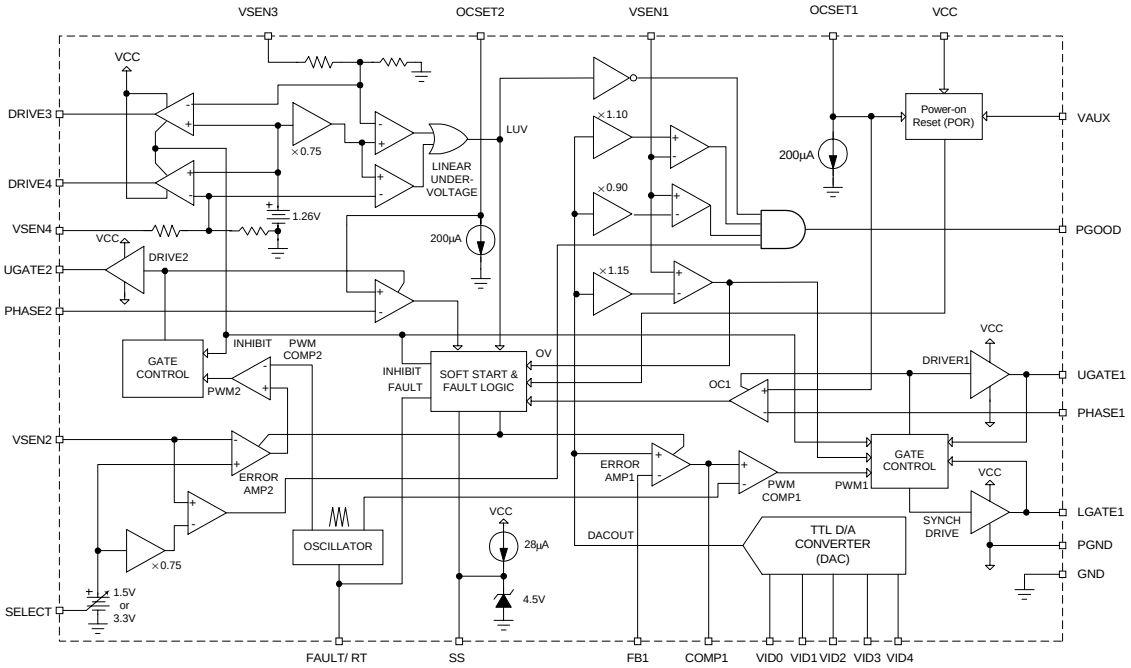
Ordering Information

APW6020 □□-□□

- Handling Code
- Temp. Range
- Package Code

Package Code
K : SOP - 28
Temp. Range
C : 0 to 70°C
Handling Code
TU : Tube TR : Tape & Reel

Block Diagram



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CC}	Supply Voltage	15	V
V_I, V_O	Input , Output or I/O Voltage	GND -0.3 V to V_{CC}	V
T_A	Operating Ambient Temperature Range	0 to 70	°C
T_J	Junction Temperature Range	0 to 125	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_S	Soldering Temperature	300 ,10 seconds	°C

Thermal Characteristics

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance in Free Air SOIC SOIC (with 3in^2 of Copper)	 75 65	°C/W

Electrical Characteristics

(Recommended operating conditions , Unless otherwise noted) Refer to Block and Simplified Power System Diagrams , and Typical Application Schematic

Symbol	Parameter	Test Conditions	APW6020			Unit
			Min.	Typ.	Max.	
V_{CC} Supply Current						
I_{CC}	Nominal Supply Current	UGATE1, LGATE1, UGATE2, DRIVE3, and DRIVE4 open		9		mA
Power-on Reset						
	Rising VCC Threshold	Vocset=4.5V			10.4	V
	Falling VCC Threshold	Vocset=4.5V	8.2			V
	Rising VAUX Threshold	Vocset=4.5V		2.5		V
	VAUX Threshold Hysteresis	Vocset=4.5V		0.5		V
	Rising V_{OCSET1} Threshold			1.26		V
Oscillator						
F_{OCS}	Free Running Frequency	RT= Open	185	200	215	kHz
ΔV_{OSC}	Ramp Amplitude	RT= Open		1.9		V_{P-P}
DAC and Standard Buck Regulator Reference						
	DAC(VID0-VID4) Input Low Voltage				0.8	V

Electrical Characteristics Cont.

Symbol	Parameter	Test Conditions	APW6020			Unit
			Min.	Typ.	Max.	
DAC and Standard Buck Regulator Reference						
	DAC(VID0-VID4) Input High Voltage		2.0			V
	DACOUT Voltage accuracy		-1.0		+1.0	%
V_{REG2}	PWM2 Reference Voltage	SELECT<0.8V		1.5		V
V_{REG2}	PWM2 Reference Voltage	SELECT>2.0V		3.3		V
	PWM2 Reference Voltage Tolerance			3		%
Linear Regulators (V_{OUT3} and V_{OUT4})						
	Regulation (All Linears)			3		%
$VREG_3$	VSEN3 Regulation Voltage			1.5		V
$VREG_4$	VSEN4 Regulation Voltage			1.8		V
$VSEN_{UV}$	Under-Voltage Level (VSEN/ VREG)	VSEN Rising		75		%
	Under-Voltage Hysteresis (VSEN/ VREG)	VSEN Falling		7		%
	Output Drive Current (All Liners)	V_{DRIVE} =4.0V	20	40		mA
Synchronous PWM Controller Error Amplifier						
	DC Gain			88		dB
GBWP	Gain-Bandwidth Product			15		MHz
SR	Slew Rate	COMP1=10pF		6		V/µs
PWM Controllers Gate Drivers						
I_{UGATE}	UGATE1,2 Source	V_{CC}=12V, $V_{UGATE\ 1,2}$=6V		1		A
R_{UGATE}	UGATE1,2 Sink	$V_{UGATE1,2}$=1V			3.5	Ω
I_{LGATE}	LGATE1 Source	V_{CC}=12V, $V_{LGATE\ 1}$=1V		1		A
R_{LGATE}	LGATE1 Sink	V_{LGATE1}= 1V			3	Ω
Protection						
	VSEN1 Over-Voltage (VSEN1/DACOUT)	VSEN1 Rising		115	120	%
I_{OVP}	FAULT Souring Current	$V_{FAULT/RT}$=2.0V		8.5		mA
I_{OCSET}	OCSET1,2 Current Source	V_{OCSET}= 4.5V_{DC}	170	200	230	µA
I_{SS}	Soft Start Current			28		µA
Power Good						
	VSEN1 Upper Threshold (VSEN1/DACOUT)	VSEN1 Rising	108		110	%
	VSEN1 Under Voltage (VSEN1/DACOUT)	VSEN1 Rising	92		94	%
	VSEN1 Hysteresis (VSEN1 DACOUT)	Upper /Lower Threshold		2		%
V_{PGOOD}	PGOOD Voltage Low	I_{PGOOD}= -4mA			0.8	V

Functional Pin Description

UGATE2 (Pin 1)

Connect UGATE2 pin to the standard BUCK PWM converter's MOSFET gate. This pin provides the gate drive for the MOSFET.

PHASE2 (Pin 2)

Connect the PHASE2 pin to the standard BUCK PWM converter's MOSFET source. This pin is used to monitor the voltage drop across the MOSFET for over-current protection.

VID0 , VID1 , VID2 , VID3 , VID4 (Pins 7, 6 , 5 , 4 and 3)

VID0-4 are the TTL-compatible input pins to the 5-bit DAC. The logic states of these five pins program the internal voltage reference (DACOUT). The level of DACOUT sets the microprocessor core converter output voltage , as well as the coresponding PGOOD and OVP thresholds.

PGOOD (Pin 8)

PGOOD is an open drain output used to indicate the status of the output voltages. This pin is pulled low when the synchronous regulator output is not within 10% of the DACOUT reference voltage or when any of the other outputs are below their under-voltage thresholds.
The PGOOD output is open for '11111' VID code.

OCSET2 (Pin 9)

Connect a resistor (R_{OCSET}) from this pin to the drain of the standard BUCK converter's MOSFET. R_{OCSET} , an internal 200µA current source (I_{OCSET}) , and the MOSFET's on-resistance($r_{DS(ON)}$) set the converter over-current (OC) trip point according to the following equation :

$$I_{PEAK} = \frac{I_{OCSET} * R_{OCSET}}{r_{DS(ON)}}$$

An over-current trip cycles the soft-start function.

VSEN2 (Pin 10)

Connect this pin to the output of the standard Buck PWM converter. The voltage at this pin is regulated to the level predetermined by the logic-level status of the SELECT pin. This pin is also monitored by the PGOOD comparator circuit.

SELECT (Pin 11)

This pin determines the output voltage of the AGP bus switching regulator. A low TTL input sets the output voltage to 1.5V , while a high input sets the output voltage to 3.3V.

SS (Pin 12)

Connect a capacitor from this pin to ground. This capacitor , along with an internal 28µA current source , sets the soft-start interval of the converter.

FAULT / RT (Pin 13)

This pin provides oscillator switching frequency adjustment. By placing a resistor (R_T) from this pin to GND , the nominal 200kHz switching frequency is increased. Conversely , connecting a pull-up resistor (R_T) from this pin to VCC reduces the switching frequency.
Nominally , the voltage at this pin is 1.26V. In the event of an over-voltage or over-current condition , this pin is internally pulled to VCC.

VSEN4 (Pin 14)

Connect this pin to the output of the linear 1.8V regulator. This pin is monitored for under-voltage events.

DRIVE4 (Pin 15)

Connect this pin to the gate of an external MOSFET. This pin provides the drive for the 1.8V regulator's pass transistor.

VAUX (Pin 16)

The +3.3V input voltage at this pin is monitored for

Functional Pin Description Cont.

power-on reset (POR) purposes.

GND (Pin 17)

Signal ground for the IC. All voltage levels are measured with respect to this pin.

DRIVE3 (Pin 18)

Connect this pin to the gate of an external MOSFET. This pin provides the drive for the 1.5V regulator's pass transistor.

VSEN3 (Pin 19)

Connect this pin to the output of the 1.5V linear regulator. This pin is monitored for under-voltage events.

COMP1 and FB1 (Pins 20 , and 21)

COMP1 and FB1 are the available external pins of the synchronous PWM regulator error amplifier. The FB1 pin is the inverting input of the error amplifier. Similarly , the COMP1 pin is the error amplifier output. These pins are used to compensate the voltage-mode control feedback loop of the synchronous PWM converter.

VSEN1 (Pin 22)

This pin is connected to the synchronous PWM converters's output voltage. The PGOOD and OVP comparator circuits use this signal to report output voltage status and for over-voltage protection.

OCSET1 (Pin 23)

Connect a resistor (R_{OCSET}) from this pin to the drain of the synchronous PWM converter's upper MOSFET. R_{OCSET} , an internal 200µA current source (I_{OCSET}) , and the MOSFET's on-resistance($r_{DS(ON)}$) set the converter over-current (OC) trip point according to the following equation :

$$I_{PEAK} = \frac{I_{OCSET} * R_{OCSET}}{r_{DS(ON)}}$$

An over-current trip cycles the soft-start function. The voltage at OCSET1 pin is monitored for power-on reset (POR) purposes.

PGND (Pin 24)

This is the power ground connection. Tie the synchronous PWM converter's lower MOSFET source to this pin.

LGATE1 (Pin 25)

Connect LGATE1 to the synchronous PWM converter's lower MOSFET gate. This pin provides the gate drive for the lower MOSFET.

PHASE1 (Pin 26)

Connect the PHASE1 pin to the synchronous PWM converter's upper MOSFET source. This pin is used to monitor the voltage drop across the upper MOSFET for over-current protection.

UGATE1 (Pin 27)

Connect UGATE1 pin to the synchronous PWM converter's upper MOSFET gate. This pin provides the gate drive for the upper MOSFET.

VCC (Pin 28)

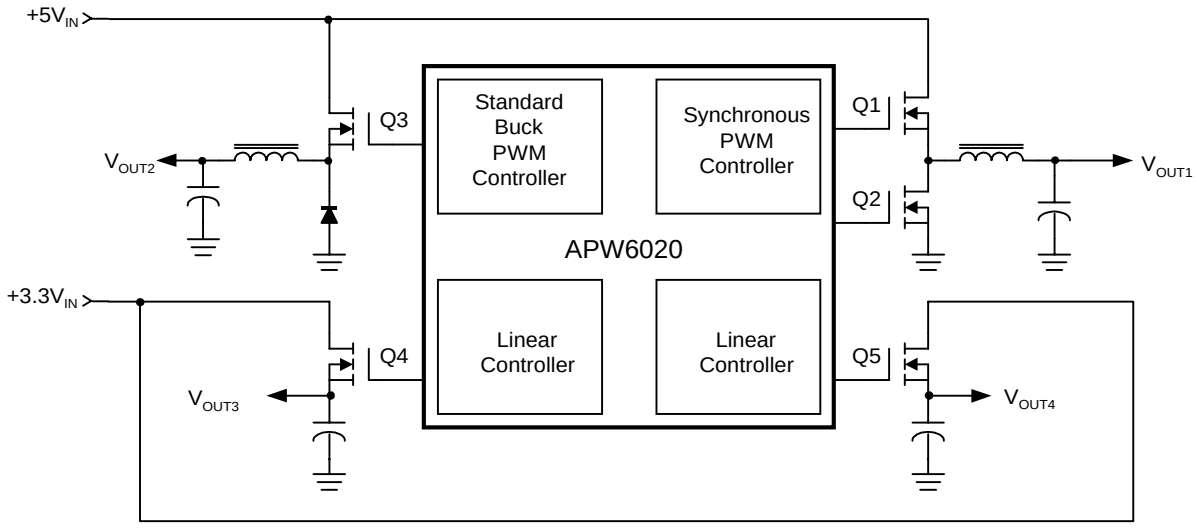
Provide a 12V bias supply for the IC to this pin. This pin also provides the gate bias charge for all the MOSFETs controlled by the IC. The voltage at this pin is monitored for Power-On Reset (POR) purposes.

Table1 Output Voltage Program

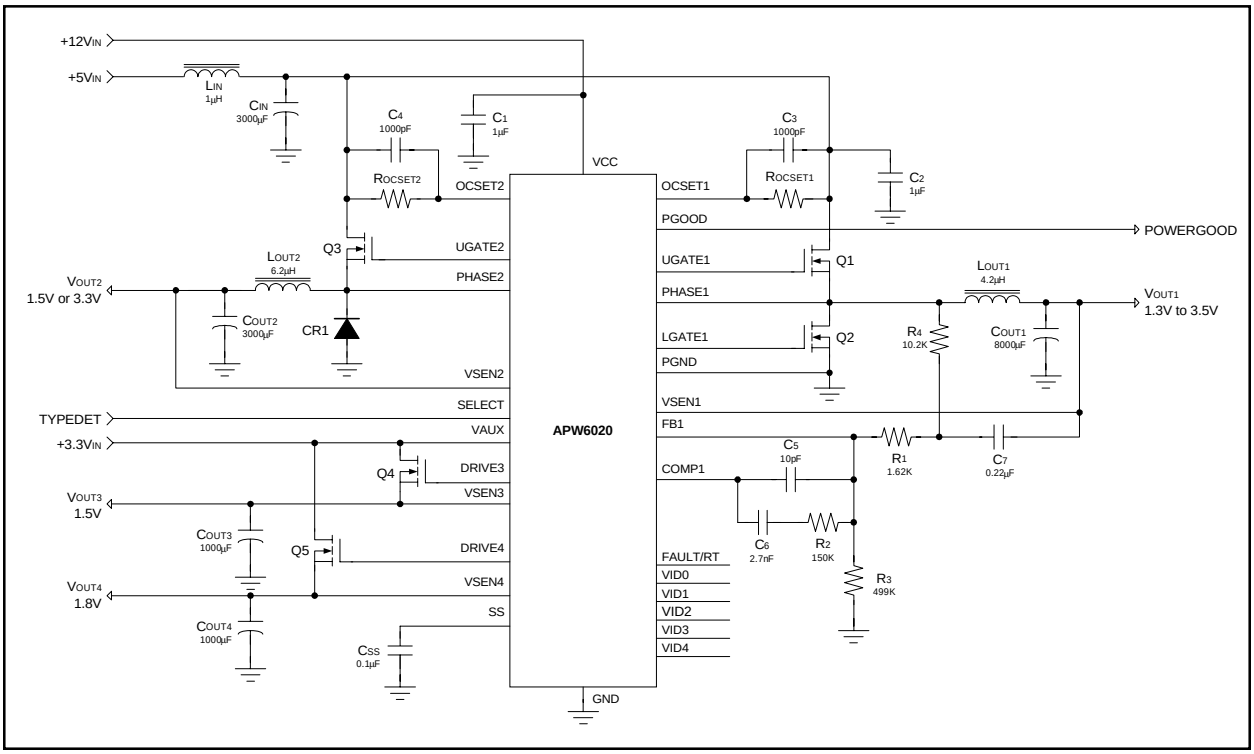
Pin Name					Nominal DACOUT Voltage	Pin Name					Nominal DACOUT Voltage
VID4	VID3	VID2	VID1	VID0		VID4	VID3	VID2	VID1	VID0	
0	1	1	1	1	1.30	1	1	1	1	1	0
0	1	1	1	0	1.35	1	1	1	1	0	2.1
0	1	1	0	1	1.40	1	1	1	0	1	2.2
0	1	1	0	0	1.45	1	1	1	0	0	2.3
0	1	0	1	1	1.50	1	1	0	1	1	2.4
0	1	0	1	0	1.55	1	1	0	1	0	2.5
0	1	0	0	1	1.60	1	1	0	0	1	2.6
0	1	0	0	0	1.65	1	1	0	0	0	2.7
0	0	1	1	1	1.70	1	0	1	1	1	2.8
0	0	1	1	0	1.75	1	0	1	1	0	2.9
0	0	1	0	1	1.80	1	0	1	0	1	3.0
0	0	1	0	0	1.85	1	0	1	0	0	3.1
0	0	0	1	1	1.90	1	0	0	1	1	3.2
0	0	0	1	0	1.95	1	0	0	1	0	3.3
0	0	0	0	1	2.00	1	0	0	0	1	3.4
0	0	0	0	0	2.05	1	0	0	0	0	3.5

NOTE : 0 = connected to GND , 1 = open or connected to 5V through pull-up resistors

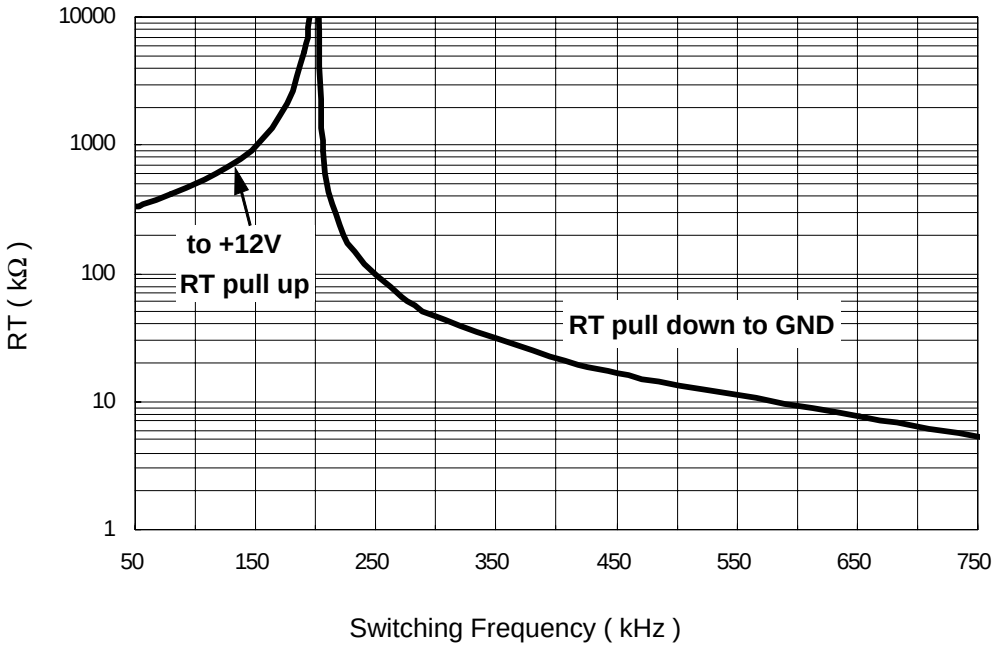
Simplified Power System Diagram



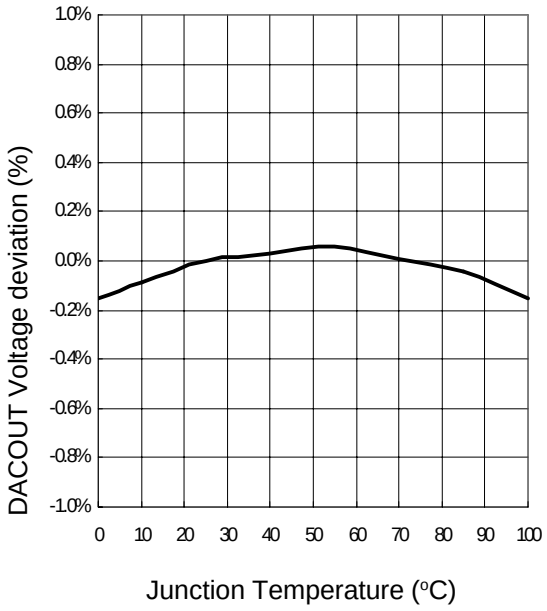
Typical Characteristics

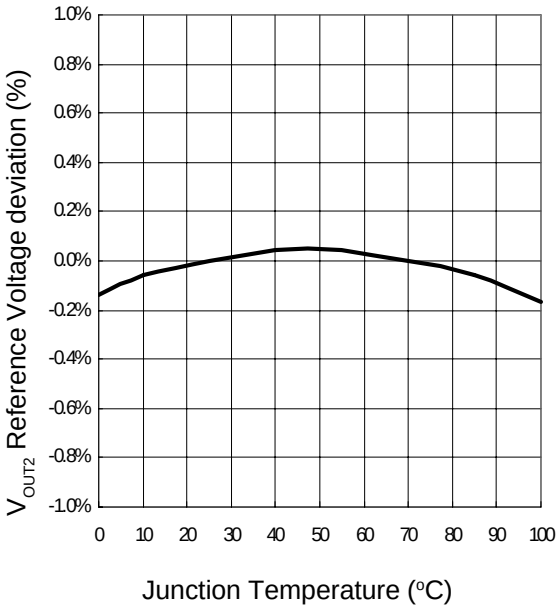


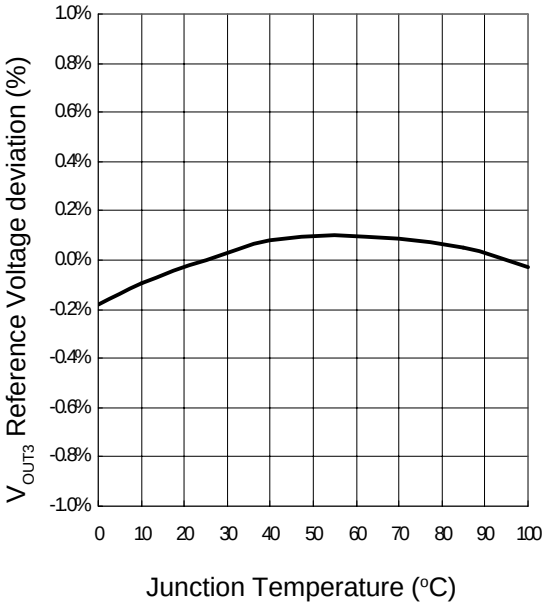
Typical Characteristics

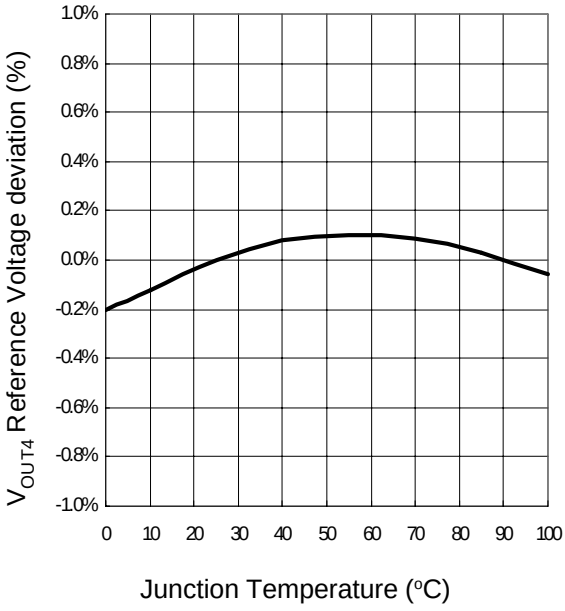


Typical Characteristics Cont.







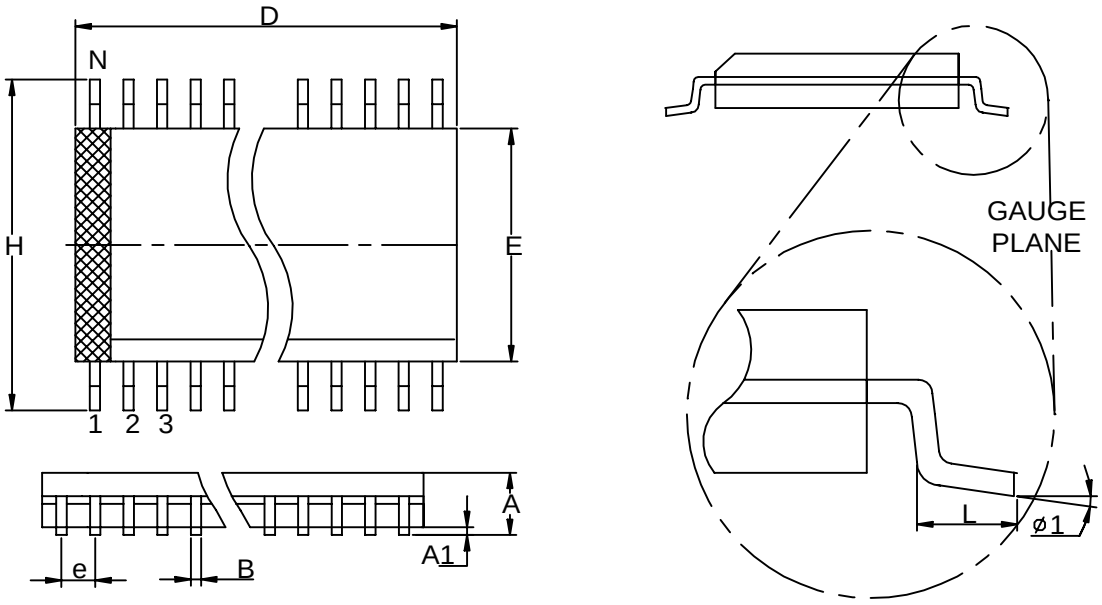


Note : The Referance Voltage(V_{REF}) Deviation is $\frac{V_{REF}(T_J) - V_{REF}(25^oC)}{V_{REF}(25^oC)} \times 100\%$

T_J : Junction Temperature

Package Information

SO – 300mil (Reference JEDEC Registration MS-013)



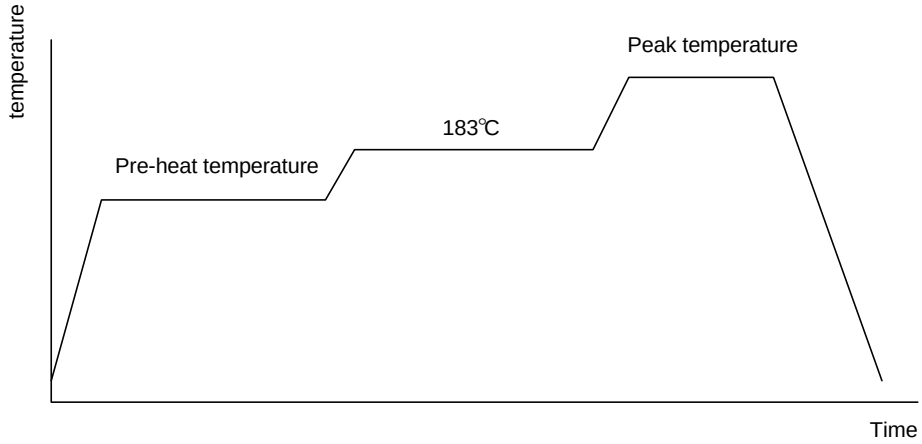
Dim	Millimeters		Variations- D			Dim	Inches		Variations- D		
	Min.	Max.	Variations	Min.	Max.		Min.	Max.	Variations	Min.	Max.
A	2.35	2.65	SO-16	10.10	10.50	A	0.093	0.1043	SO-16	0.398	0.413
A1	0.10	0.30	SO-18	11.35	11.76	A1	0.004	0.0120	SO-18	0.447	0.463
B	0.33	0.51	SO-20	12.60	13	B	0.013	0.020	SO-20	0.496	0.512
D	See variations		SO-24	15.20	15.60	D	See variations		SO-24	0.599	0.614
E	7.40	7.60	SO-28	17.70	18.11	E	0.2914	0.2992	SO-28	0.697	0.713
e	1.27BSC		SO-14	8.80	9.20	e	0.050BSC		SO-14	0.347	0.362
H	10	10.65				H	0.394	0.419			
L	0.40	1.27				L	0.016	0.050			
N	See variations					N	See variations				
ϕ 1	0°	8°				ϕ 1	0°	8°			

Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb)
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.
Packaging	1000 devices per reel

Refolw Condition (IR/ Convection or VPR Reflow)

Reference JEDEC Standard J-STD-020A APRIL 1999



Classification Reflow Profiles

	Convection or IR/ Convection	VPR
Average ramp-up rate(183°C to Peak)	3°C/second max.	10 °C /second max.
Preheat temperature 125 ± 25°C)	120 seconds max.	
Temperature maintained above 183°C	60 ~ 150 seconds	
Time within 5°C of actual peak temperature	10 ~ 20 seconds	60 seconds
Peak temperature range	220 +5/-0°C or 235 +5/-0°C	215~ 219°C or 235 +5/-0°C
Ramp-down rate	6 °C /second max.	10 °C /second max.
Time 25°C to peak temperature	6 minutes max.	

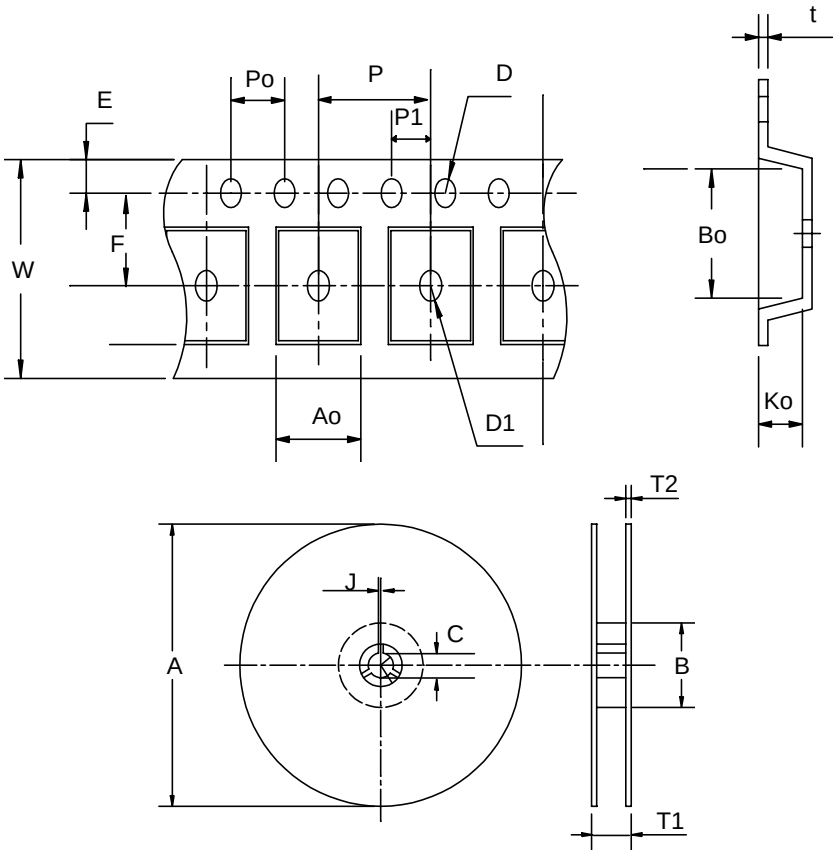
Package Reflow Conditions

pkg. thickness ≥ 2.5mm and all bags	**pkg. thickness < 2.5mm and pkg. volume ≥ 350 mm³**	**pkg. thickness < 2.5mm and pkg. volume < 350mm³**
Convection 220 +5/-0 °C		Convection 235 +5/-0 °C
VPR 215-219 °C		VPR 235 +5/-0 °C
IR/Convection 220 +5/-0 °C		IR/Convection 235 +5/-0 °C

Reliability test program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C , 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @ 125 °C
PCT	JESD-22-B, A102	168 Hrs, 100 % RH , 121°C
TST	MIL-STD-883D-1011.9	-65°C ~ 150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms , I_{tr} > 100mA

Tape & Reel Dimensions



Application	A	B	C	J	T1	T2	W	P	E
SOP- 28	330±1	62 ±1.5	12.75 ± 0. 5	2 ± 0.6	24.4 ± 0.2	2± 0.2	24 ± 0.3	12 ± 0.1	1.75± 0.1
Application	F	D	D1	Po	P1	Ao	Bo	Ko	t
SOP- 28	11.5 ± 0.1	1.5 +0.1	1.5+ 0.25	4.0 ± 0.1	2.0 ± 0.1	10.85 ± 0.1	18.34± 0.1	2.97± 0.1	0.35±0.01

Cover Tape Dimensions

Carrier Width	24
Cover Tape Width	21.3

Customer Service

Anpec Electronics Corp.
Head Office :
5F, No. 2 Li-Hsin Road, SBIP,
Hsin-Chu, Taiwan, R.O.C.
Tel : 886-3-5642000
Fax : 886-3-5642050

Taipei Branch :
7F, No. 137, Lane 235, Pac Chiao Rd.,
Hsin Tien City, Taipei Hsien, Taiwan, R. O. C.
Tel : 886-2-89191368
Fax : 886-2-89191369