3A, 1MHz, Step Down DC/DC Regulator

Features

- Source/Sink 3A
- Up to 1MHz Switches Frequency
- Up to 94% Efficiency
- Internal PMOS/NMOS Switches
  - 70mΩ/40mΩ On-Resistance at V_{IN} = 4.5V
  - 90mΩ/60mΩ On-Resistance at V_{IN} = 3V
- ±1% Output Accuracy
- 1.1V to V_{IN} Adjustable Output Voltage
- 3V to +5.5V Input Voltage Range
- <1μA Shutdown Supply Current
- Programmable Constant-Off-Time Operation
- Thermal Shutdown
- Adjustable Soft-Start Inrush Current Limiting
- Output Short-Circuit Protection
- Lead Free Available (RoHS Compliant)

Applications

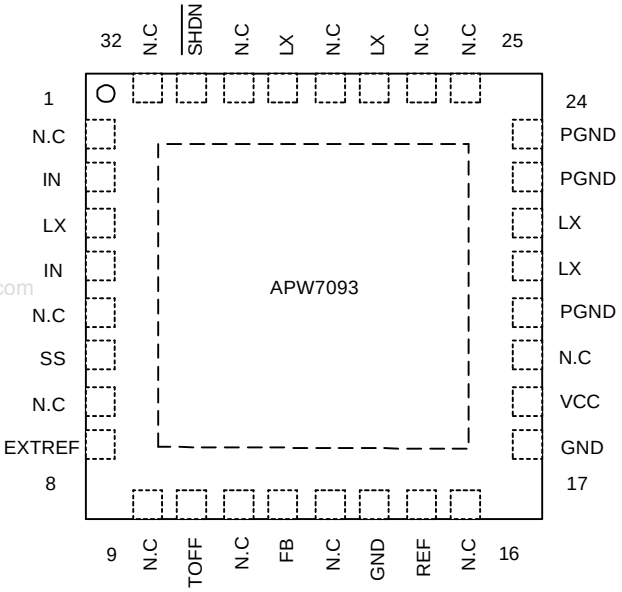
- Motherboard
- Graphics Cards
- Cable or DSL Modems, Set Top Boxes
- DSP Supplies
- Memory Supplies
- 5V Input DC-DC Regulators
- Distributed Power Supplies

General Description

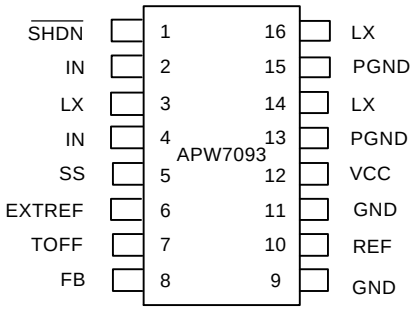
The APW7093 is a reversible energy flow, constant-off-time, pulse-width modulated (PWM), step-down DC-DC converter. It is ideal for use in notebook and sub-notebook computers that require 1.1V to 5V active termination power supplies. This device features an internal PMOS power switch and internal synchronous rectifier for high efficiency and reduced component count. The internal 90mΩ PMOS power switch and 60mΩ NMOS synchronous-rectifier switch easily deliver continuous load currents up to 3A. The APW7093 accurately tracks an external reference voltage, produces an adjustable output from 1.1V to VIN, and achieves efficiencies as high as 94%.

The APW7093 uses a unique current-mode, constant-off-time, PWM control scheme that allows the output to source or sink current. This feature allows energy to return to the input power supply that otherwise would be wasted. The programmable constant-off-time architecture sets switching frequencies up to 1MHz, allowing the user to optimize performance trade-offs between efficiency, output switching noise, component size, and cost. The APW7093 features an adjustable soft-start to limit surge currents during startup, a 100% duty-cycle mode for low-dropout operation, and a low-power shutdown mode that disables the power switches and reduces supply current below 1μA. The APW7093 is available in a 32-pin QFN with an exposed backside pad or a 16-pin SSOP.

Pin Description



QFN - 32



SSOP - 16

Ordering and Marking Information

APW7093 □□-□□□ Lead Free Code Handling Code Temp. Range Package Code	Package Code N : SSOP-16 QA : QFN -32 Operating Ambient Temp. Range I : -45 to 85 °C Handling Code TU : TubeTR : Tape & Reel Lead Free Code L : Lead Free Device Blank : Original Device
APW7093 N : APW7093 XXXXX	XXXXX - Date Code
APW7093 QA : APW7093 XXXXX	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldiering operations. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

Block Diagram

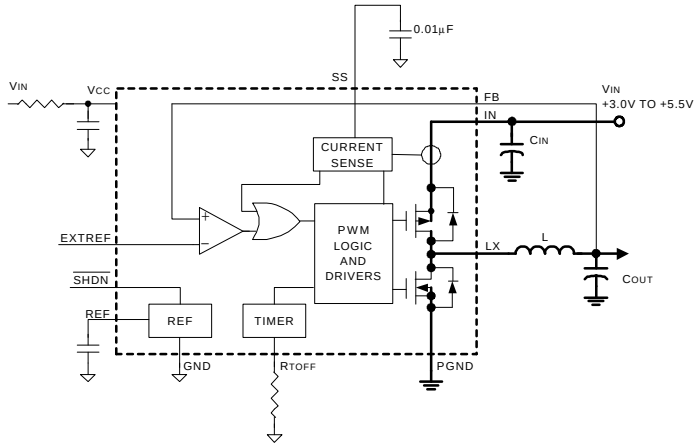


Fig1. Block Diagram

Absolute Maximum Ratings

Parameter	Rating	Unit
V_{CC} to GND	-0.3 ~ +6	V
IN to V_{CC}	±0.3	V
GND to PGND	±0.3	V
$\overline{SHDN}$, SS, FB, T_{OFF}, V_{REF} to GND	-0.3 ~ V_{CC}+0.3	V
EXTREF to GND	-0.3 ~ V_{IN}-1.7	V
Power dissipation; Part mount on 1in^2 of 1oz copper; QFN-28	1.6	W
Power dissipation; Part mount on 1in^2 of 1oz copper; SSOP-16	1	W
LX Current	-3.5 ~ +4.1	A
Operating Temperature Range	-40 ~ +85	°C
Junction Temperature	+150	°C
Storage Temperature Range	-65~+150	°C
Lead Temperature (soldering,10s)	+300	°C

Recommend Operating Condition

Recommend Operating Condition

Symbol	Parameter	MIN	TYP	MAX	UNIT	NOTE
V_{IN}	Input Voltage Range	3		5.5	V	
V_{OUT}	Output Voltage Range	1.1		V_{IN}	V	V_{EXTREF}<= V_{IN}-1.7V
C_{OUT}	Output Capacitor	220	330		uF	
C_{IN}	Input Capacitor	22	33		uF	Low ESR Capacitor
L	Inductor	0.56	1		uH	
R_{TOFF}	Programmed off-time Resistance	–	–	–	KΩ	Refer to Application section for further Information.

Electrical Characteristics

(V_{IN}=V_{CC}=3.3V, V_{EXTREF}=+1.1V, T_A=-45 to +85°C, unless otherwise noted, Typical values are at T_A =+25°C.)

Symbol	Parameter	Test Conditions		APW7093			Unit
				Min	Typ	Max	
V_{IN}, V_{CC}	Input Voltage			3.0		5.5	V
	Feedback Voltage Accuracy (V_{FB} –V_{EXTREF})	V_{IN}=V_{CC}=+3.0V to +5.5V, I_{LOAD}=0,V_{EXTREF}=1.25V (Note2)		-12		+12	mV
ΔV_{FB}	Feedback Load Regulation Error	I_{LOAD}=-3A to +3A, V_{EXTREF}=+1.25V			20		mV
V_{EXTREF}	External Reference Voltage Range	V_{IN}=V_{CC}=+3.0 to +5.5V		V_{REF} - 0.01		V_{IN} - 1.7	V
V_{REF}	Reference Voltage			1.078	1.100	1.122	V
	Reference Load Regulation	I_{REF}= -1µA to +10µA			0.3	2	mV
R_{PMOS}	PMOS Switch On-Resistance	I_{LX}=0.5A	V_{IN}=+4.5V		70	140	mΩ
			V_{IN}=+3.0V		90	180	
R_{NMOS}	NMOS Switch On-Resistance	I_{LX}=0.5A	V_{IN}=+4.5V		50	100	mΩ
			V_{IN}=+3.0V		60	120	
I_{LIMIT}	Current Limit Threshold	V_{IN} > V_{LX}		3.5	4.1	4.7	A
f_{SW}	Switching Frequency	(Note3)				1	MHz
I_{CC}	No Load Supply Current	f_{SW} =500kHz			1		mA
I_{IN}		f_{SW} =500kHz			32		
$I_{\overline{SHDN}}$	Shutdown Supply Current	$\overline{SHDN}$ = GND, I_{CC}+ I_{IN}			<1	15	µA
	Thermal Shutdown Threshold	Hysteresis =15°C			150		°C
UVLO	Under Voltage Lockout Threshold	V_{CC} falling, hysteresis = 90mV		2.5	2.6	2.7	V
I_{FB}	FB Input Current	V_{FB}=V_{EXTREF}+0.1V		0	60	250	nA
T_{OFF}	Off-Time	R_{TOFF}=30.1kΩ		0.40	0.44	0.48	µs
		R_{TOFF}=110kΩ		1.10	1.20	1.30	
		R_{TOFF}=499kΩ		4.3	4.8	5.3	
	Startup Off-Time			4×TOFF			µs
T_{ON}	On-Time	(Note3)		0.34			µs
I_{SS}	SS Source Current			4	5	6	µA
I_{SS}	SS Sink Current	V_{SS}=1V		2			mA
	$\overline{SHDN}$ Input Current	$V_{\overline{SHDN}}$ =0, V_{CC}		-1		+1	µA
V_{IL}	$\overline{SHDN}$ Logic Levels					0.8	V
V_{IH}				2.0			
$I_{OUT(RMS)}$	Maximum Output RMS Current					3.1	A_{RMS}

Electrical Characteristics (Cont.)

(V_{IN}=V_{CC}=3.3V, V_{EXTREF}=+1.1V, T_A = -45 to +85°C, unless otherwise noted, Typical values are at T_A =+25°C.)

Symbol	Parameter	Test Conditions	APW7093			Unit
			Min	Typ	Max	
V_{IL}	SHDN Logic Levels				0.8	V
V_{IH}			2.0			
$I_{OUT(RMS)}$	Maximum Output RMS Current				3.1	A_{RMS}

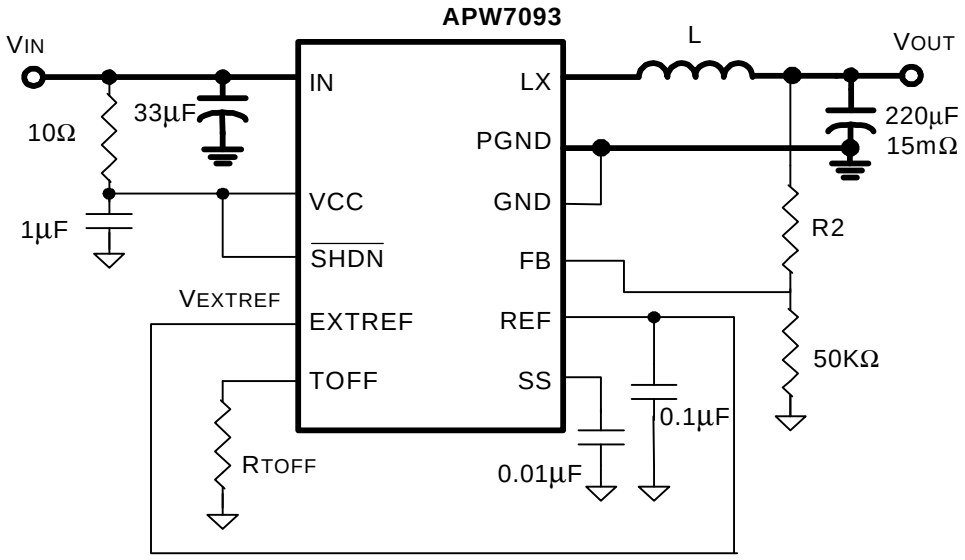
Note2: The output voltage will have a DC-regulation level lower than the feedback error comparator threshold by 50% of the ripple.

Note3: Recommended operating frequency, not production tested.

Functional Pin Description

Name	PIN (QFN)	PIN (QSOP)	FUNCTION
N.C	1,5,7,9,11,13,16,19, 25,26,28,30,32	X	No Connection, Not internally connected.
IN	2,4	2,4	Supply Voltage Input for the internal PMOS Power Switch. Not internally connected. Externally connect all pins for proper operation.
LX	3,21,22,27,29	3,14,16	Inductor Connection. Connection for the drains of the PMOS power switch and NMOS synchronous-rectifier switch. Connect the inductor from this node to the output filter capacitor and load. Not internally connected. Externally connect all pins for proper operation.
SS	6	5	Soft-Start Connect a capacitor from SS to GND to limit inrush current during startup.
EXTREF	8	6	External Reference Input Feedback input regulates to V_{EXTREF}. The PWM controller remains off until EXTREF is greater than REF.
TOFF	10	7	Off-Time Select Input. Sets the PMOS power switch constant-off-time. Connect a resistor from TOFF to GND to adjust the PMOS switch off-time.
FB	12	8	Feedback Input. Connect directly to output for fixed-voltage operation or to a resistive-divider for adjustable operating modes.
GND	14,17,backside pad, corner tabs	9	Analog Ground. Connect exposed backside pad and corner tabs to analog GND.
REF	15	10	Reference Output. Bypass REF to GND with a 0.1µF capacitor.
GND	17	11	Tie to GND (pin 13 QFN; pin 9 SSOP)
V_{CC}	18	12	Analog Supply Voltage Input. Supplies internal analog circuitry. Bypass V_{CC} with a 10Ω and 1µF low-pass filter. See Figure2.
PGND	20,23,24	13,15	Power Ground. Internally connected to the internal NMOS synchronous-rectifier switch.
$\overline{SHDN}$	31	1	Shutdown control Input Drive $\overline{SHDN}$ low to disable the reference, control circuitry, and internal MOSFETs. Drive high or connect to V_{CC} for normal operation.

Typical Application



FOR VIN =5V: L=1mH, RTOFF=100kW

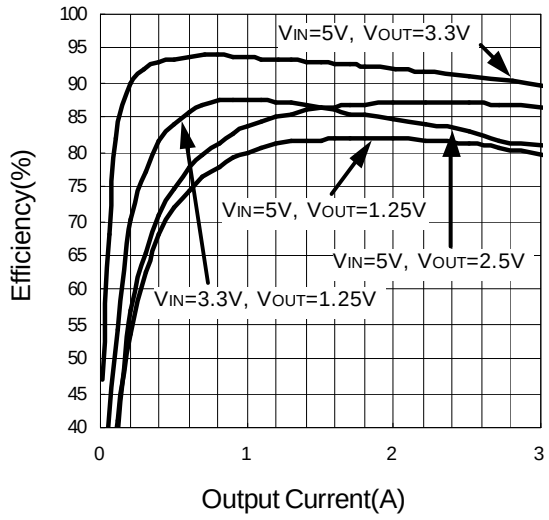
FOR VIN=3.3V: L=0.68mH, RTOFF=68kW

Fig2. Typical Applicatin Circuit

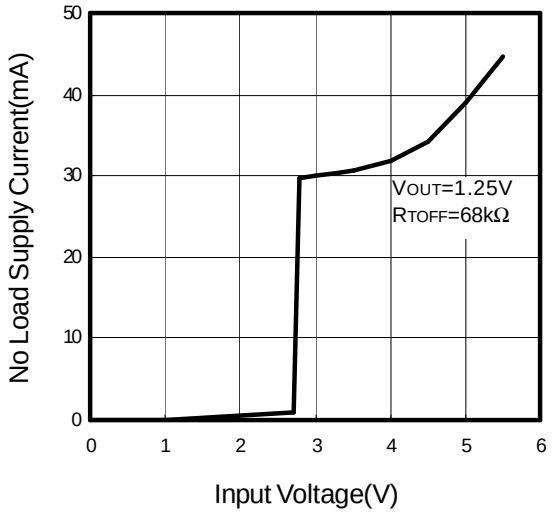
Typical Characteristics

(Circuit of Figure2, V_{OUT}=1.25V, for V_{IN}=3.3V: L: 0.68µH, R_{TOFF}=68kΩ; for V_{IN}=5V: L=1µH, T_{OFF}=100kΩ. T_A=25C if not specially)

Effiencicy vs. Output Current



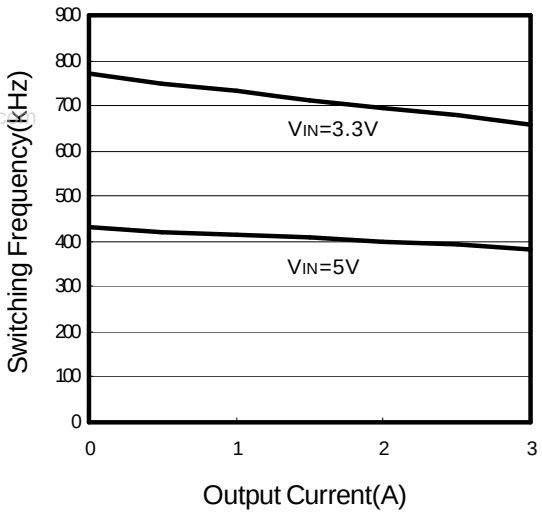
No Load Supply Current vs. Input Voltage



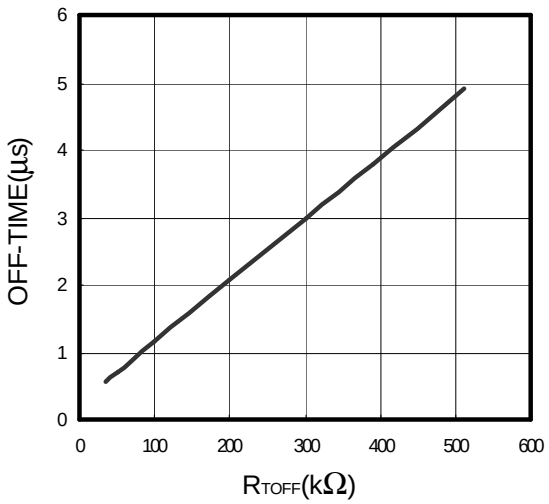
Typical Characteristics (Cont.)

(Circuit of Figure2, V_{OUT}=1.25V, for V_{IN}=3.3V: L: 0.68µH, R_{TOFF}=68kΩ; for V_{IN}=5V: L=1µH, T_{OFF}=100kΩ. T_A=25C if not specially)

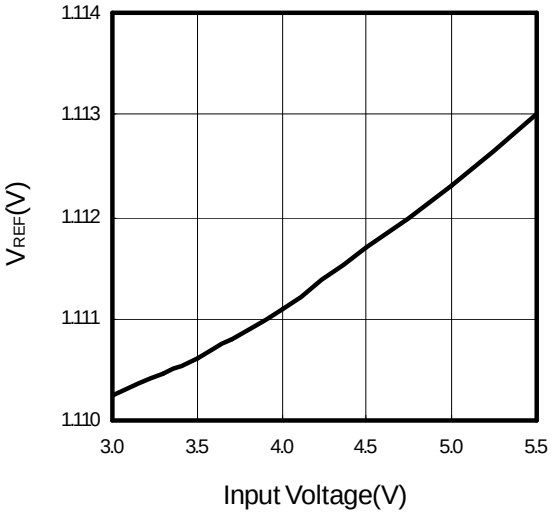
Switching Frequency vs. Output Current



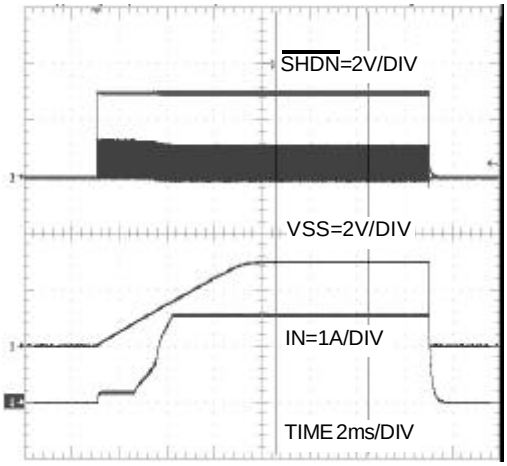
OFF-TIME vs. R_{TOFF}



VREF vs. Input Voltage



Start Up and Shut Down

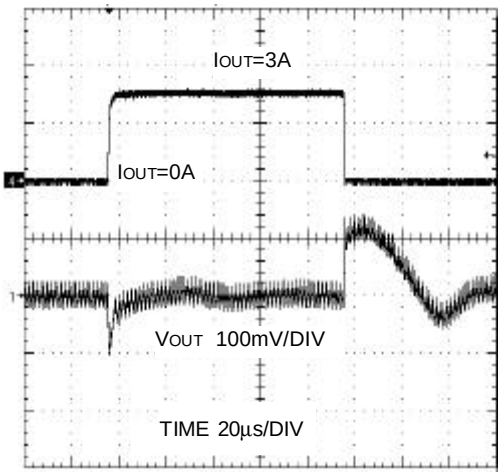


V_{IN}=3.3V, V_{OUT}=1.25V, R_{OUT}=0.4Ω

Typical Characteristics (Cont.)

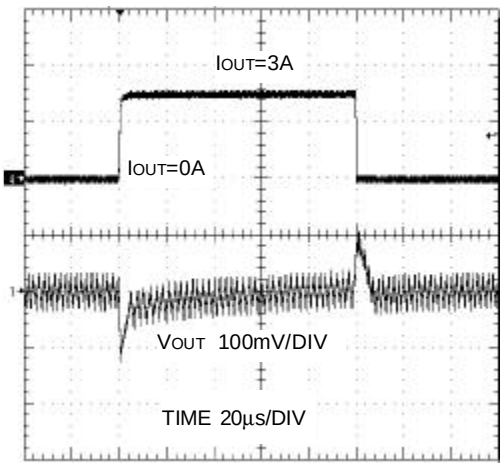
(Circuit of Figure2, V_{OUT}=1.25V, for V_{IN}=3.3V: L= 0.68µH, R_{TOFF}=68kΩ; for V_{IN}=5V: L=1µH, T_{OFF}=100kΩ. T_A=25°C if not specially)

Load Transient Response



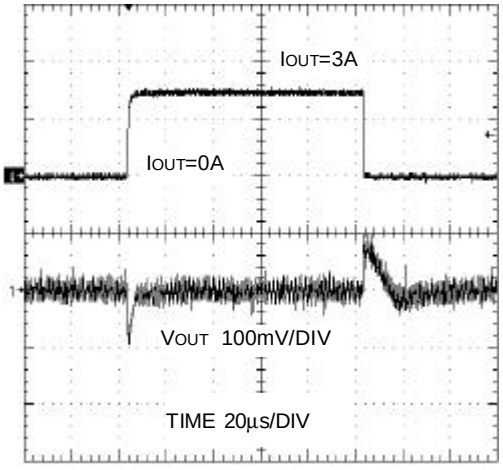
V_{IN}=5V, V_{OUT}=1.25V, $\frac{di}{dt}=\frac{3A}{ms}$

Load Transient Response



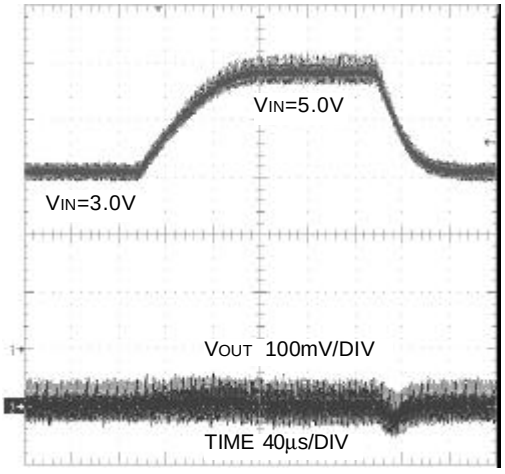
V_{IN}=5V, V_{OUT}=2.5V, $\frac{di}{dt}=\frac{3A}{ms}$

Load Transient Response



V_{IN}=3.3V, V_{OUT}=1.25V, $\frac{di}{dt}=\frac{3A}{ms}$

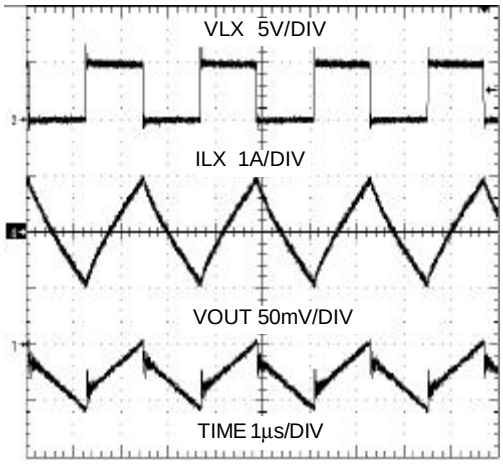
Line Transient Response



Typical Characteristics (Cont.)

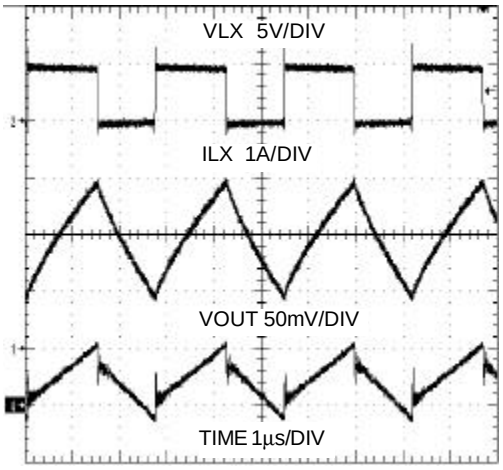
(Circuit of Figure2, V_{OUT}=1.25V, for V_{IN}=3.3V: L= 0.68µH, R_{TOFF}=68kΩ; for V_{IN}=5V: L=1µH, T_{OFF}=100kΩ. T_A=25°C if not specially)

Light Load Waveform



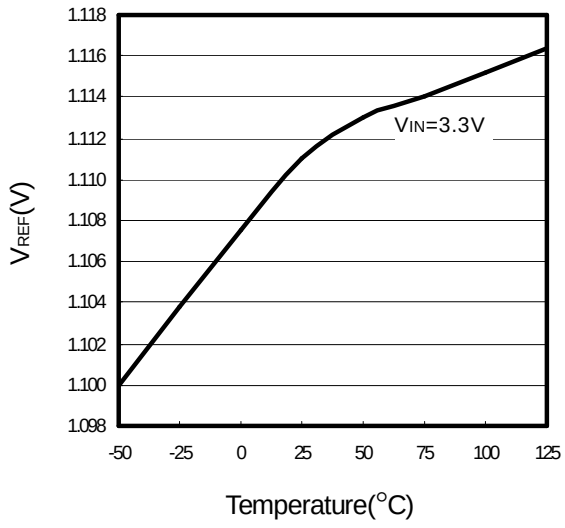
I_{OUT}=100mA

Heavy Load Waveform

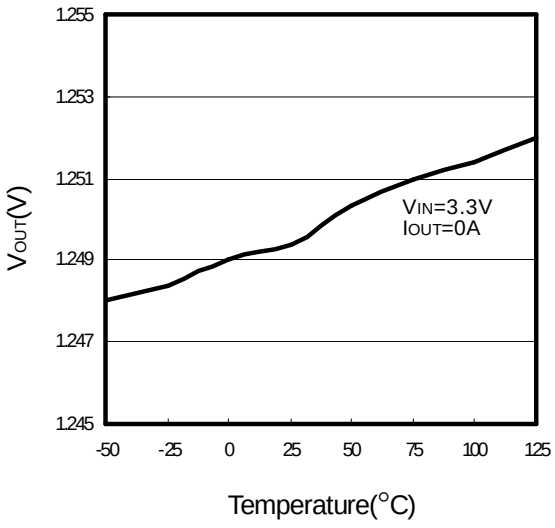


I_{OUT}=3A

V_{REF} vs. Temperature



Output Voltage vs. Temperature



Function Descriptions

The APW7093 synchronous, current-mode, constant off-time, PWM DC-DC converter steps down input voltages of 3V to 5.5V to an adjustable output voltage from 1.1V to VIN, as set by the voltage applied at EXTREF. It sources and sinks up to 3A of output current. Internal switches composed of a 90mΩ PMOS power switch and a 60m Ω NMOS synchronous-rectifier switch improve efficiency, reduce component count, and eliminate the need for an external Schottky diode across the synchronous switch.

The APW7093 operates in a constant-off-time mode under all loads. A single resistor-programmable constant- tradeoffs in efficiency, switching noise, component size, and cost. When power is drawn from a regulated supply, constant-off-time PWM architecture essentially provides constant-frequency operation. This architecture has the inherent advantage of quick response to line and load transients. The APW7093's current-mode, constant-off-time PWM architecture regulates the output voltage by changing the PMOS switch on-time relative to the constant off-time.

Constant-Off-Time Operation

In the constant-off-time architecture, the FB voltage comparator turns the PMOS switch on at the end of each off-time, keeping the device in continuous-conduction mode. The PMOS switch remains on until the feedback voltage exceeds the external reference voltage (V_{EXTREF}) or the positive current limit is reached. When the PMOS switch turns off, it remains off for the programmed off-time (T_{OFF}). To control the current under short-circuit conditions, the PMOS switch remains off for approximately 4 x T_{OFF} when V_{FB} < V_{EXTREF} / 4.

Synchronous Rectification

In a step-down regulator without synchronous rectification, an external Schottky diode provides a path for current to flow when the inductor is discharging. Replacing the Schottky diode with a low-resistance NMOS synchronous switch reduces conduction losses and improves efficiency. The NMOS synchronous-rectifier switch turns on following a short delay (typ. 20ns) after the PMOS power switch turns off, thus preventing cross-conduction or "shoot-through." In constant-off-time mode, the synchronous-rectifier switch turns off just prior to the PMOS power switch turning on. While both switches are off, inductor current flows through the internal body diode of the NMOS switch.

Current Sourcing and Sinking

By operating in a constant-off-time, pseudo-fixed-frequency mode, the APW7093 can both source and sink current. Depending on the output current requirement, the circuit operates in two modes. In the first mode the output draws current and the APW7093 behaves as a regular buck controller, sourcing current to the output from the input supply rail. However, when the output is supplied by another source, the APW7093 operates in a second mode as a synchronous boost, taking power from the output and returning it to the input.

Thermal Resistance

Junction-to-ambient thermal resistance, θ_{JA}, is highly dependent on the amount of copper area immediately surrounding the IC leads. The APW7093 QFN package has 1in square of copper area and a thermal resistance of 50°C/W with no forced airflow. The APW7093 16-pin SSOP evaluation kit has 0.5 in square of copper area and a thermal resistance of 80°C/W with no forced airflow. Airflow over the board significantly reduces the junction-to-ambient thermal resistance. For heat sinking purposes, it is essential to connect the exposed backside pad of the QFN package to a large analog ground plane.

Function Descriptions(Cont.)

Shutdown

Drive SHDN to a logic-level low to place the APW7093 in low-power shutdown mode and reduce supply current less than 1μA. In shutdown, all circuitry and internal MOSFETs turn off, so the LX node becomes high impedance. Drive $\overline{SHDN}$ to a logic-level high or connect to VCC for normal operation.

Power Dissipation

Power dissipation in the APW7093 is dominated by conduction losses in the two internal power switches. Power dissipation due to charging and discharging the gate capacitance of the internal switches (i.e., switching losses) is approximately:

$$P_{D(CAP)} = C \times V_{IN}^2 \times f_{SW}$$

where C = 500pF and fSW is the switching frequency. Resistive losses in the two power switches are approximated by:

$$P_{D(RES)} = I_{OUT}^2 \times R_{PMOS}$$

where RPMOS is the on-resistance of the PMOS switch. The junction-to-ambient thermal resistance required to dissipate this amount of power is calculated by:

$$\theta_{JA} = (T_{J,MAX} - T_{A,MAX}) / (P_{D(CAP)} + P_{D(RES)})$$

where:

θ_{JA} = junction-to-ambient thermal resistance

$T_{J,MAX}$ = maximum junction temperature

$T_{A,MAX}$ = maximum ambient temperature

Application Information

For typical applications, use the recommended component values in Figure 2. For other applications, take the following steps:

1. Select the desired PWM-mode switching frequency. See Figure 3 for maximum operating frequency.
2. Select the constant off-time as a function of input voltage, output voltage, and switching frequency.
3. Select RTOFF as a function of off-time.
4. Select the inductor as a function of output voltage, off-time, and peak-to-peak inductor current.

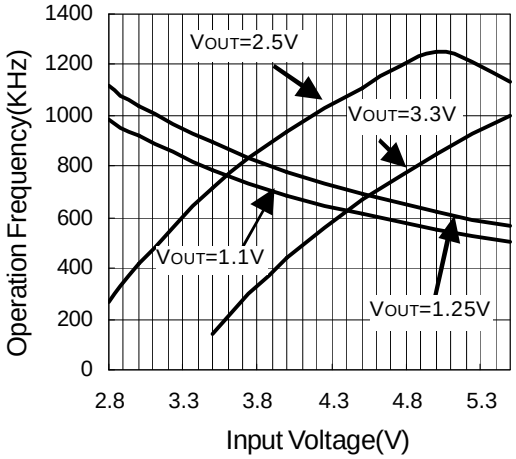


Fig 3. Maximum Recommended Operation Frequency

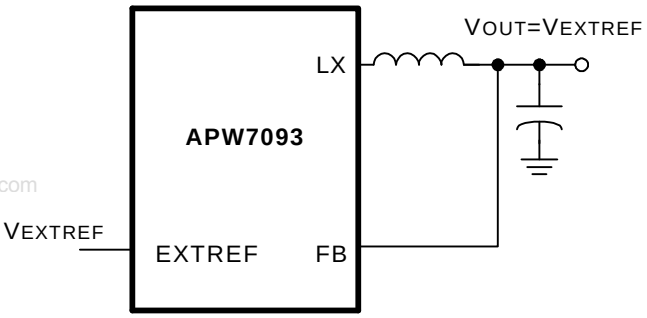
Setting the Output Voltage

An external voltage applied to the EXTREF pin sets the output voltage of the APW7093. This can come directly from another voltage source or external reference. When FB is directly tied to the output (Figure 4), the output voltage range is limited by the external reference's input voltage limits. VEXTREF should be limited to less than VIN-1.7V. Failure to comply can cause the part to operate abnormally and may cause part damage. Alternatively, the output can be adjusted up to VIN by connecting FB to a resistor-divider between the output voltage and ground (Figure 5). Use 50k Ω for R1. R2 is given by:

$$R2 = R1 \cdot \left(\frac{V_{OUT}}{V_{EXTREF}} - 1 \right)$$

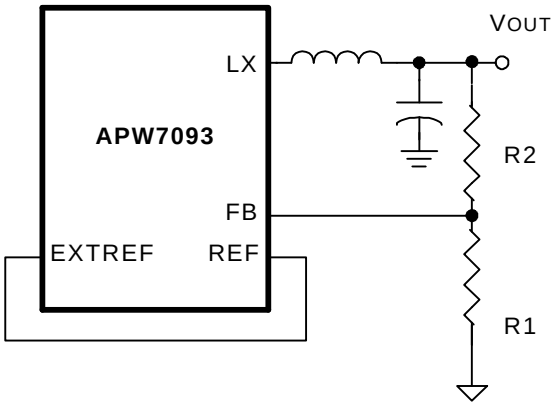
Application Information(Cont.)

Setting the Output Voltage (Cont.)



$1.1V \le V_{EXTREF} \le V_{IN} - 1.7V$

FIG.4 Adjsting the Output Voltage using EXTREF



$$R2 = R1 \cdot \left(\frac{V_{OUT}}{V_{EXTREF}} - 1 \right)$$

where $V_{EXTREF} = V_{REF} = 1.1V$

FIG.5 Adjsting the Output Voltage using FB

Programming the Switching Frequency and Off-Time and On-Time

The APW7093 features a programmable PWM-mode switching frequency, which is set by the input and output voltage and the value of RTOFF, connected from TOFF to GND. RTOFF sets the PMOS power switch off-time in PWM mode. Use the following equation to select the off-time while sourcing current according to the desired switching frequency in PWM mode:

$$T_{OFF} = \frac{(V_{IN} - V_{OUT} - V_{PMOS})}{f_{SW}(V_{IN} - V_{PMOS} + V_{NMOS})}$$

where:

TOFF = the programmed off-time

VIN = the input voltage

VOUT = the output voltage

VPMOS = the voltage drop across the internal PMOS power switch |IOUT x RPMOS|

VNMOS = the voltage drop across the internal NMOS synchronous-rectifier switch |IOUT x RNMOS|

fSW = switching frequency

Make sure that TON and TOFF are greater than 400ns when sourcing current. Select RTOFF according to the formula:

$$R_{TOFF} = (T_{OFF} - 0.18\,ms) \times (109k\,\Omega / 1.00\,ms)$$

Recommended values for RTOFF range from 24k Ω to 410k Ω for off-times of 0.4µs to 4µs. Often the switching frequency is set as high as possible, and the inductor value is reduced to minimize the energy transferred from inductor to capacitor during load-step recovery.

The operating frequency of the APW7093 is determined primarily by TOFF (set by RTOFF), VIN, and VOUT as shown in the following formula:

$$f_{SW} = \frac{(V_{IN} - V_{OUT} - V_{PMOS})}{T_{OFF}(V_{IN} - V_{PMOS} + V_{NMOS})}$$

However, as the output current increases, the voltage drop across the NMOS and PMOS switches increases and the voltage across the inductor decreases. This causes the frequency to drop. Assuming RPMOS = RNMOS, the change in frequency can be approximated with the following formula:

$$\Delta f_{SW} = \frac{-\Delta I_{OUT} \times R_{PMOS}}{V_{IN} \times T_{OFF}}$$

where RPMOS is the resistance of the internal MOSFETs (70m Ω typ).

Application Information(Cont.)

Programming the Switching Frequency and Off-Time and On-Time (Cont.)

When sinking current, the switching frequency increases due to the on-resistances of the internal switches adding to the voltage across the inductor, reducing the on-time. Calculate TON when sinking current using the equation:

$$T_{ON} = T_{OFF}\left(\frac{V_{OUT} - V_{NMOS}}{V_{IN} - V_{OUT} + V_{PMOS}}\right)$$

Inductor Selection

The key inductor parameters must be specified: inductor value (L) and peak current (IPEAK). A lower value of inductor allows smaller size but results in higher losses and ripple. A good compromise between size and losses is found at approximately a 25% ripple current to load current ratio ($\Delta I/I_{OUT} = 0.25$).

$$L = \frac{V_{OUT} \times T_{OFF}}{I_{OUT} \times 0.25}$$

The peak inductor current at full load is calculated by:

$$I_{PEAK} = I_{OUT} + \frac{V_{OUT} \times T_{OFF}}{2 \times L}$$

where IOUT is the maximum source or sink current. Choose an inductor with a saturation current at least as high as the peak inductor current. Additionally, verify the peak inductor current while sourcing output current (IOUT = ISOURCE) does not exceed the positive current limit. The inductor selected should exhibit low losses at the chosen operating frequency.

Input Capacitor Selection

The input filter capacitor reduces peak currents and noise at the voltage source. A 22µF to 47µF capacitor may be required for higher power and dynamic loads. Low-ESR and low-ESL Tantalum or ceramic capacitor should be suitable.

Output Capacitor Selection

The output filter capacitor affects the output voltage ripple, output load-transient response, and feedback loop stability. The output filter capacitor must have low enough ESR to meet output ripple and load transient requirements, yet have high enough ESR to satisfy stability requirements. Also, the capacitance value must be high enough to guarantee stability and absorb the inductor energy going from a full-load sourcing to full load sinking condition without exceeding the maximum output tolerance.

In applications where the output is subject to large load transients, the output capacitor's size typically depends on how much ESR is needed to prevent the output from dipping too low under a load transient.

$$R_{ESR} \leq \Delta V_{OUT} / \Delta I_{OUT(MAX)}$$

The actual microfarad capacitance value required is defined by the physical size needed to achieve low ESR, and by the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR, size and voltage rating rather than by capacitance value. When using low-capacity filter capacitors such as ceramic or polymer types, capacitor size is usually determined by the capacity needed to prevent overshoot and undershoot from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising-load edge is no longer a problem.

Application Information(Cont.)

Soft-Start

Soft-start allows a gradual increase of the internal current limit to reduce input surge currents at startup and at exit from shutdown. A timing capacitor, CSS, placed from SS to GND sets the rate at which the internal current limit is changed. Upon power-up, when the device comes out of under-voltage lockout (2.6V typ.) or after the SHDN pin is pulled high, a 4.7µA constant current source charges the soft-start capacitor and the voltage on SS increases. When the voltage on SS is less than approximately 0.7V, the current limit is set to zero. As the voltage increases from 0.7V to approximately VIN, the current limit is adjusted from 0V to the current-limit threshold. The voltage across the soft-start capacitor changes with time according to the equation:

$$V_{SS} = \frac{4.7\,mA \times t}{C_{SS}}$$

The output current limit during soft-start varies with the voltage on the soft-start pin, SS, according to the equation:

$$I_{LIIM(SS)} = \frac{(V_{SS} - 0.7V)}{1.1V} \times I_{LIMIT}, V_{SS} \le 1.8V$$

where ILIMIT is the current-limit threshold from the Electrical Characteristics. The constant-current source stops charging once the voltage across the soft-start capacitor reaches 1.8V.

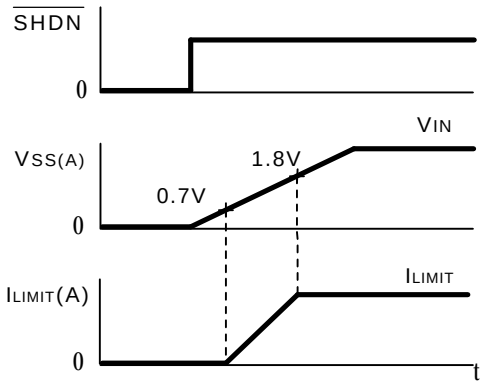


Fig6. Soft-Start Current Limit

Input Source

The output of the APW7093 can accept current due to the reversible properties of the buck and the boost converter. When voltage at the output of the APW7093 (low-voltage port) exceeds or equals the output set voltage the flow of energy reverses, going from the output to the input (high-voltage port). If the input (high voltage port) is not connected to a low-impedance source capable of absorbing energy, the voltage at the input will rise. This voltage can violate the absolute maximum voltage at the input of the APW7093 and destroy the part. This occurs when sinking current because the topology acts as a boost converter, pumping energy from the low-voltage side (the output), to the high-voltage side (the input). The input (high-voltage side) voltage is limited only by the clamping effect of the voltage source connected there. To avoid this problem, make sure the input to the APW7093 is connected to a low impedance, two quadrant supply or that the load (excluding the APW7093) connected to that supply consumes more power than the amount being transferred from the APW7093 output to the input.

Current Limit and Short Circuit Protection

The APW7093 monitors sourcing and sinking current, and limits the maximum output current to prevent damages during overload or short-circuit.

Circuit Layout and Grounding

Good layout is necessary to achieve the APW7093's intended output power level, high efficiency, and low noise. Good layout includes the use of ground planes, careful component placement, and correct routing of traces using appropriate trace widths. The following points are in order of decreasing importance:

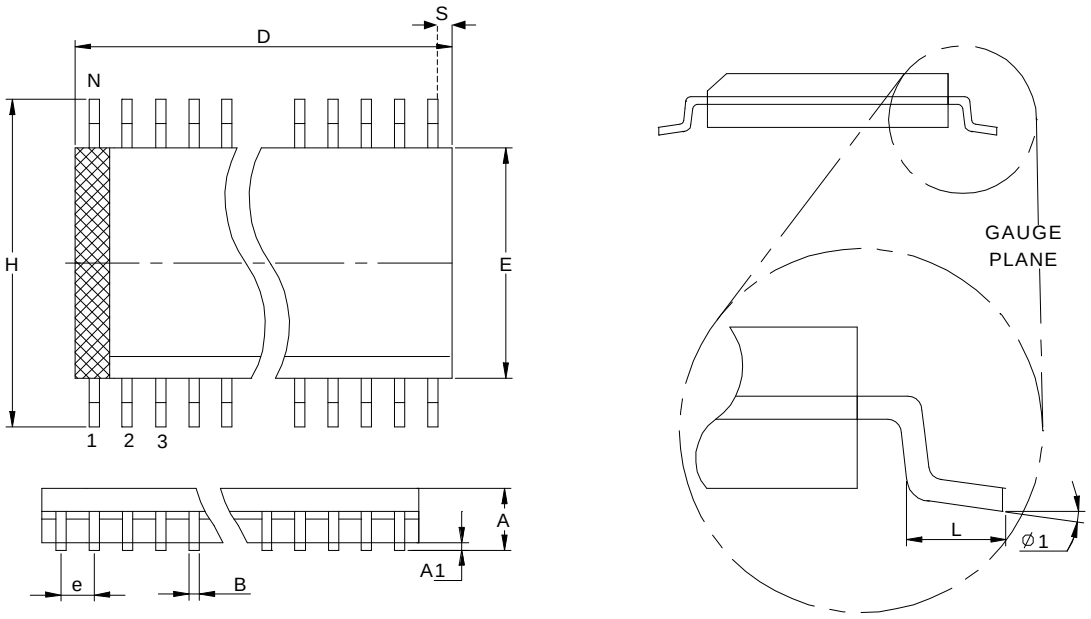
Application Information(Cont.)

Circuit Layout and Grounding (Cont.)

1. Minimize switched-current and high-current ground loops. Connect the input capacitor's ground, the output capacitor's ground, and PGND close together. Split the ground connections. Use separate traces or planes for the PGND and GND and tie them together at a single point.
2. The output capacitor should be placed close to the output terminals to obtain better smoothing effect on the output ripple.
3. Connect the input filter capacitor less than 5mm away from IN. The connecting copper trace carries large currents and must be at least 1mm wide, preferably 2.5mm.
4. Place the LX node components as close together and as near to the device as possible. This reduces resistive and switching losses as well as noise.
5. Ground planes are essential for optimum performance. In most applications, the circuit is located on a multilayer board and full use of the four or more layers is recommended. For heat dissipation, connect the exposed backside pad of the QFN package to a large analog ground plane, preferably on a surface of the board that receives good airflow. If the ground plane is located on the top layer, make use of the N.C. pins adjacent to GND to lower thermal resistance to the ground plane. If the ground is located elsewhere, use several vias to lower thermal resistance. Typical applications use multiple ground planes to minimize thermal resistance. Avoid large AC currents through the analog ground plane.

Packaging Information

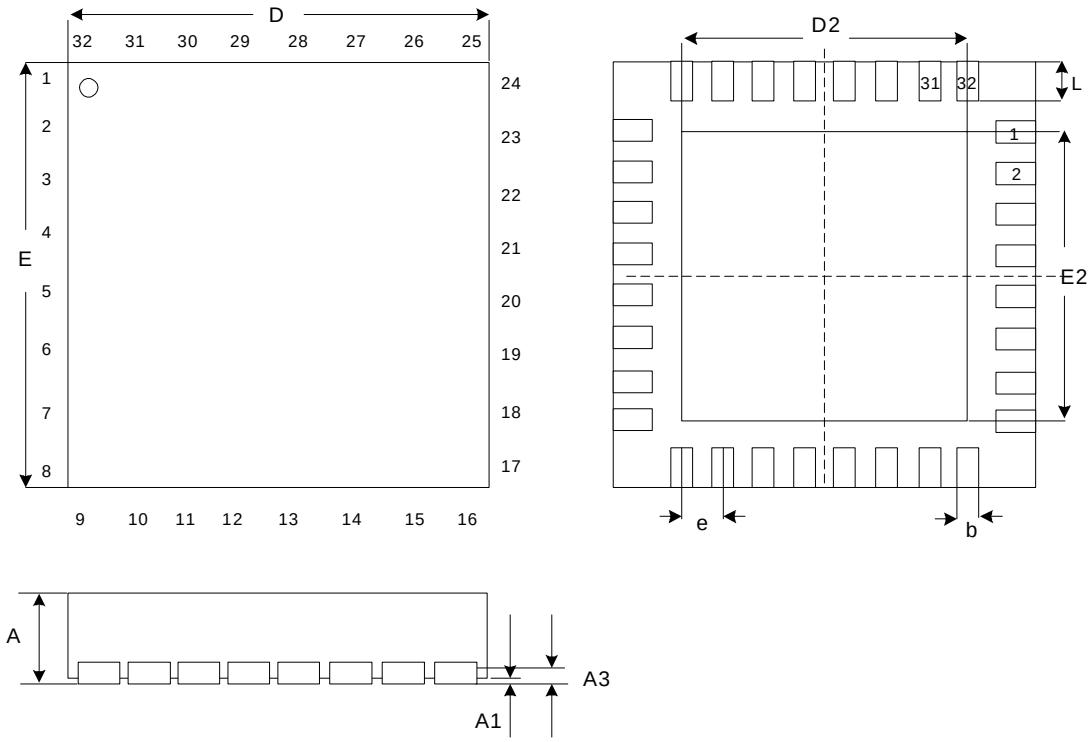
SSOP-16



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
B	0.20	0.30	0.008	0.012
D	4.75	5.05	0.187	0.199
E	3.75	4.05	0.147	0.160
e	0.625 TYP.		0.025 TYP.	
H	5.75	6.25	0.226	0.246
L	0.4	1.27	0.016	0.050
S	0.05	0.18	0.002	0.007
ϕ 1	0°	8°	0°	8°

Packaging Information

QFN-32

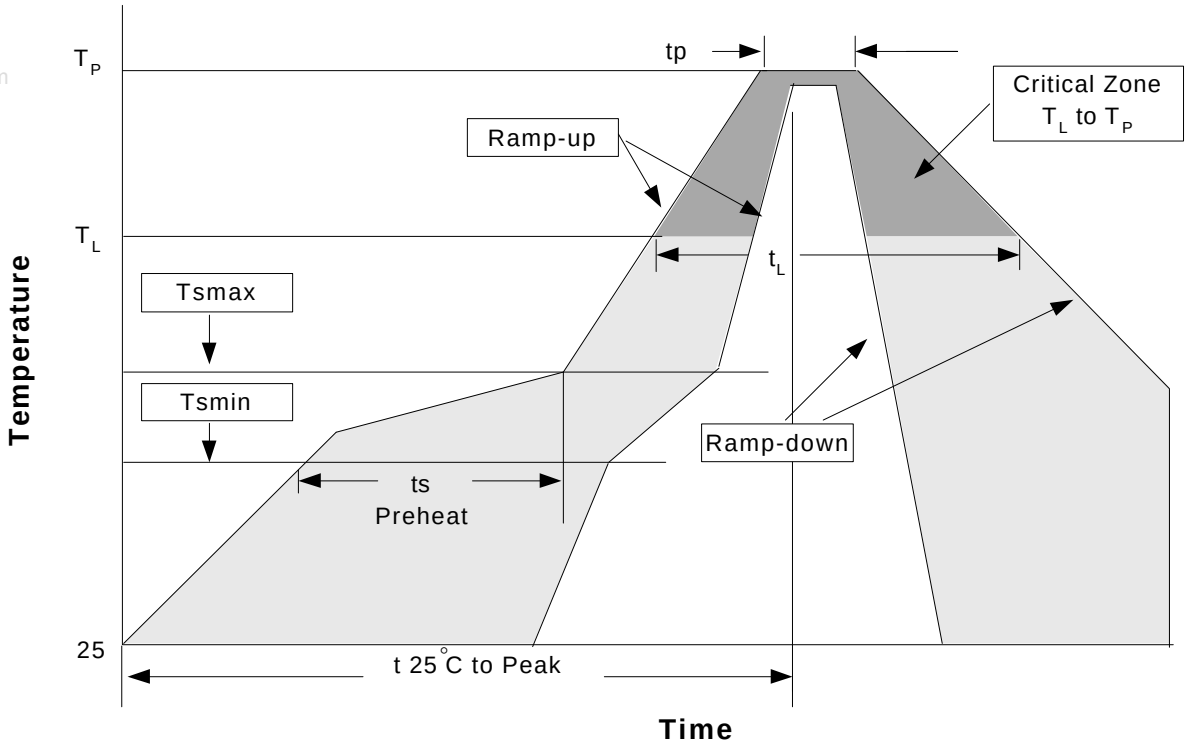


Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	-	0.84	-	0.033
A1	0.00	0.04	0.00	0.0015
A3	0.20 REF.		0.008 REF.	
D	4.90	5.10	0.192	0.200
E	4.90	5.10	0.192	0.200
b	0.18	0.28	0.007	0.011
D2	3.50	3.60	0.138	0.142
E2	3.50	3.60	0.138	0.142
e	0.500 BSC		0.020 BSC	
L	0.35	0.45	0.014	0.018

Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.
Packaging	2500 devices per reel

Reflow Condition (IR/Convection or VPR Reflow)



Classificatin Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classificatioon Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Notes: All temperatures refer to topside of the package .Measured on the body surface.

Classificatin Reflow Profiles(Cont.)

Table 1. SnPb Entectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

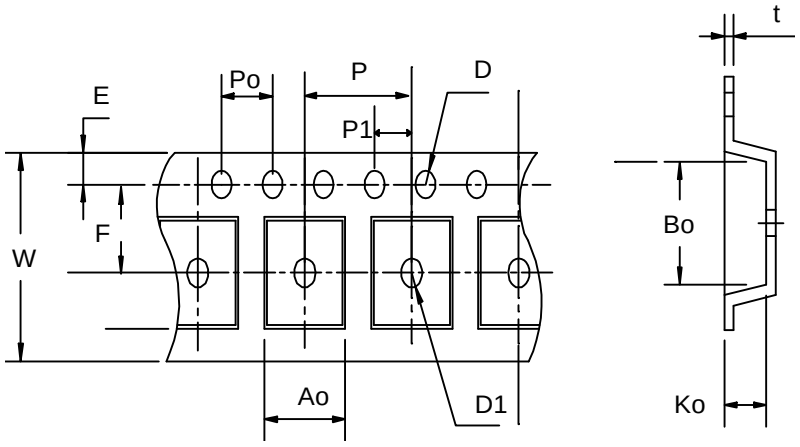
Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*
*Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.			

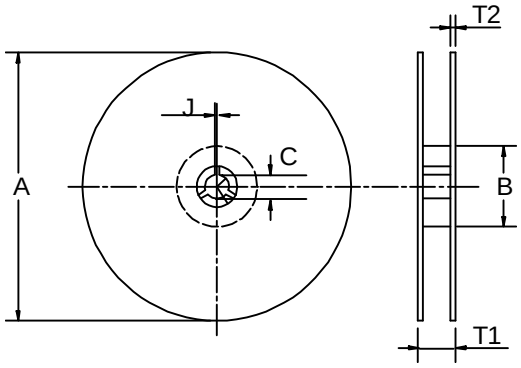
Reliability test program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C , 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @ 125 °C
PCT	JESD-22-B, A102	168 Hrs, 100 % RH , 121°C
TST	MIL-STD-883D-1011.9	-65°C ~ 150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms , I_{tr} > 100mA

Carrier Tape & Reel Dimension



Carrier Tape & Reel Dimension



Application	A	B	D0	D1	E	F	P0	P1	P2
SSOP-16	6.95	5.4	1.55±0.05	1.55±0.1	1.75±0.1	5.5±0.05	4.0±0.1	8.0±0.1	2.0±0.05
	T	T2	W	W1	C1	C2	T1	T2	C
	0.3±0.05	2.2	12.0±0.3	9.5	13±0.3	21±0.8	13.5±0.5	2.0±0.2	80±1

(mm)

Cover Tape Dimensions

Application	Carrier Width	Cover Tape Width	Devices Per Reel
SSOP- 16	16.8	12.3	2500

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