Dual Mobile-Friendly PWM Controller

Features

- **Adjustable Output Voltage up to 5.5V**
  - **0.9V Reference Voltage**
  - **±1% Accuracy Over Temperature**
- **Operates from an Input Battery Voltage Range of 5V to 24V or from 3.3V/5V System Rail**
- **Power-On-Reset Monitoring on VCC Pin**
- **Selectable Forced PWM or Automatic PFM/PWM Mode**
- **Constant-On-Time Control Scheme**
  - **Switching Frequency Compensation for PWM Mode**
  - **Constant Switching Frequency (CH1: 345kHz, CH2: 255KHz) in PWM Mode with DC Output Current**
- **Excellent Line and Load Transient Responses**
- **Adjustable Soft-Start and Soft-Stop**
- **Power-Good Outputs for both Channels**
- **Adjustable Current-Limit Protection**
  - **Using Sense Resistor or MOSFET's $R_{DS(ON)}$**
- **115% Over-Voltage Protection**
  - **No Negative Output Voltage Occurred**
- **70% Under-Voltage Protection**
- **Adaptive Dead-Time Control**
  - **Sensing G-to-S Voltage of Power MOSFETs**
- **Shutdown Control for both Channels**
- **28-pin SSOP (SSOP-28) and 4mmx4mm 24-lead QFN (QFN4x4-24) Packages**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **Note Book Computers**
  - **Chipset/RAM Supplies as low as 0.9V**
  - **1.8V and 2.5V Supplies**
- **Step-Down Converters Requiring High Efficiency**

General Description

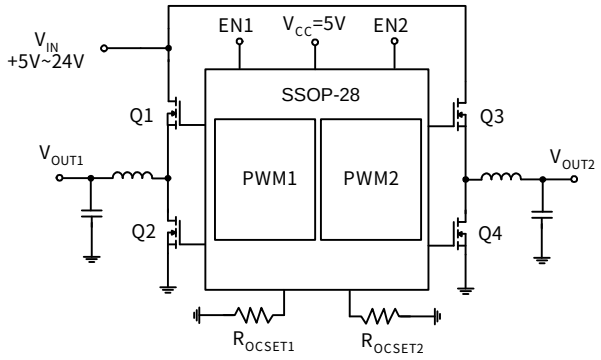
The APW7108 is a dual-channel, constant on-time, and synchronous PWM controller which drives dual N-channel MOSFETs for each channel. The APW7108 steps down high voltage of a battery to generate low-voltage chipset or RAM supplies in notebook computers.

The APW7108 provides excellent transient response and accurate DC voltage output in either PFM or PWM mode. In PFM mode, the APW7108 provides very high efficiency over light to heavy loads with loading-modulated switching frequencies. The Forced-PWM mode works nearly at constant frequency for low-noise requirements.

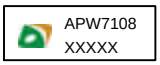
The APW7108 is equipped with accurate current-limit, output under-voltag, and output over-voltage protections, perfect for NB applications. A Power-On-Reset function monitors the voltage on V_{CC} to prevent wrong operation during power on. A soft-start ramps up the output voltage with programmable slew rate to reduce the start-up current. A soft-stop function actively discharges the output capacitors with controlled reverse inductor current. At the end of the soft-stop, the APW7108 forces LGATE high to prevent over-voltage in shutdown. The APW7108 has individual enable controls for each channel. Pulling both EN pin low shuts down the whole chip with low quiescent current close to zero.

The APW7108 is available in SSOP-28 and QFN4x4-24 packages.

Simplified Application Circuit

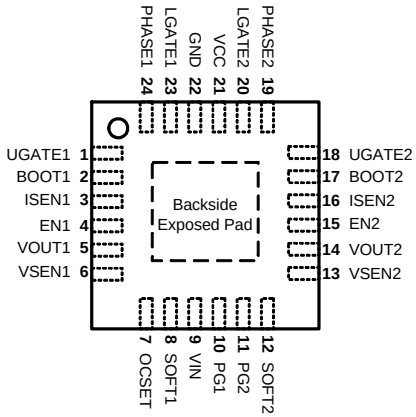


Ordering and Marking Information

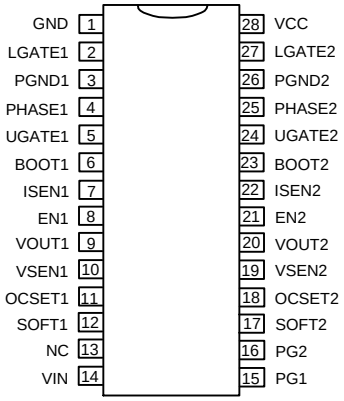
APW7108 □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code N : SSOP-28 QA: QFN4x4-24 Operating Ambient Temperature Range I : -40 to 85°C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW7108 N : 	XXXXX - Date Code
APW7108 QA : 	XXXXX - Date Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Pin Configuration



APW7108 (QFN4x4-24)
Top View



APW7108 (SSOP-28)
Top View

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{CC}	VCC Supply Voltage (VCC to GND)	-0.3 ~ 7	V
V_{IN}	Input Power Voltage (VIN to GND)	-0.3 ~ 28	V
V_{BOOT}	BOOT Supply Voltage (BOOT to PHASE)	-0.3 ~ 7	V
$V_{BOOT-GND}$	BOOT Supply Voltage (BOOT to GND)	-0.3 ~ 35	V
	UGATE Voltage (UGATE to PHASE) <400ns pulse width >400ns pulse width	 -5 ~ V_{BOOT}+0.3 -0.3 ~ V_{BOOT}+0.3	V
	LGATE Voltage (LGATE to GND) <400ns pulse width >400ns pulse width	 -5 ~ V_{CC}+0.3 -0.3 ~ V_{CC}+0.3	V

Absolute Maximum Ratings (Cont.) (Note 1)

Symbol	Parameter	Rating	Unit
V_{PHASE}	PHASE Voltage (PHASE to GND) <400ns pulse width >400ns pulse width	 -5 ~ 35 -2 ~ 28	V
	PGND to GND Voltage	-0.3 ~ 0.3	V
V_{ISEN}	ISEN Supply Voltage (ISEN to GND)	-0.3 ~ 28	V
V_{PG}	PG1, PG2 Supply Voltage (PG1, PG2 to GND)	-0.3 ~ 7	V
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance in Free Air (Note 2) SSOP-28 QFN4x4-24	 80 40	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions

Symbol	Parameter	Range	Unit
V_{CC}	VCC Supply Voltage	4.5 ~ 5.5	V
V_{OUT1} V_{OUT2}	Converter Output Voltages	0.9 ~ 5.5	V
V_{IN1} V_{IN2}	Converter Input Voltages	5 ~ 24	V
I_{OUT1} I_{OUT2}	Converter Output Currents	~ 20	A
R_{OCSET}	OCSET Resistance Range	39 ~ 200	kΩ
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Electrical Characteristics

Refer to the typical application circuits. These specifications apply over V_{CC}=5V, V_{IN}=5~24V and T_A= -40 ~ 85 °C, unless otherwise specified. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7108			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
I_{CC}	VCC Nominal Supply Current	UGATEx and LGATEx Open, VSENx forced above regulation point	-	1.2	3.0	mA
I_{CC_SHDN}	VCC Shutdown Supply Current		-	-	1.0	μA
POWER-ON-RESET (POR)						
V_{CCR}	Rising VCC Threshold Voltage		4.1	4.2	4.3	V
	VCC POR Hysteresis		0.1	0.2	0.3	V
VIN PIN						
I_{VIN}	VIN Pin Sink Current		-	-	35	μA
I_{VIN_SHDN}	VIN Shutdown Current		-	-	1.0	μA

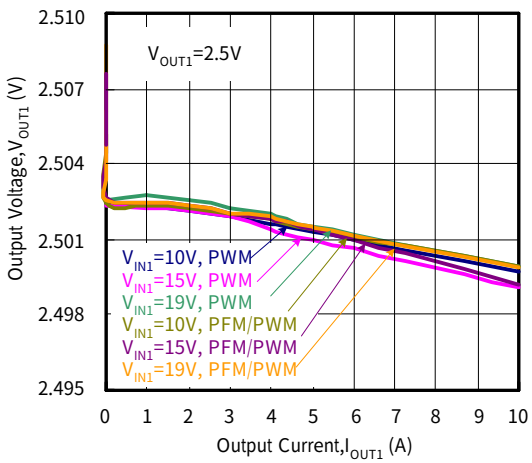
Electrical Characteristics (Cont.)

Refer to the typical application circuits. These specifications apply over V_{CC}=5V, V_{IN}=5~24V and T_A= -40 ~ 85 °C, unless otherwise specified. Typical values are at T_A=25°C.

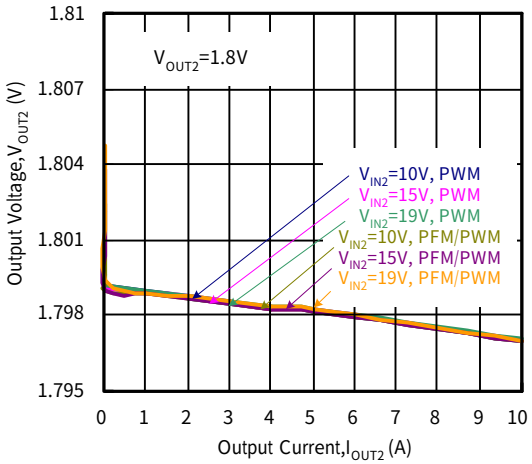
Symbol	Parameter	Test Conditions		APW7108			Unit
				Min.	Typ.	Max.	
REFERENCE VOLTAGE							
V_{REF}	Reference Voltage			-	0.9	-	
	Accuracy			-1.0	-	+1.0	%
	Line Regulation	V_{CC} = 4.5V to 5.5V, V_{IN} = 5~24V		-0.1	-	+0.1	%
	Load Regulation	0A < I_{OUT} < 5A; 5V < V_{IN} < 24V		-1.0	-	+1.0	%
PWM CONVERTERS							
I_{VSEN}	VSEN Pin Bias Current			-100	-	+100	nA
	Minimum off-time of UGATE			-	550	-	ns
	VOUT Pin Input Impedance	V_{OUT} = 5V		-	134	-	kΩ
V_{UV}	VSEN Under-Voltage Threshold	~ 2µs noise filter, VSEN Falling		65	70	75	%
V_{OV}	VSEN Over-Voltage Threshold	~ 2µs noise filter, VSEN Rising		110	115	120	%
SWITCHING FREQUENCY							
F_{SW}	Switching Frequency in PWM mode	DC output current	PWM1	294	345	396	kHz
			PWM2	217	255	293	
MOSFET GATE DRIVERS							
	UGATE Source Resistance	V_{BOOT} = 5V, I_{UGATE} = 0.1A		-	1	2	Ω
	UGATE Sink Resistance	V_{BOOT} = 5V, I_{UGATE} = 0.1A		-	0.9	1.8	Ω
	LGATE Source Resistance	V_{CC} = 5V, I_{LGATE}= 0.1A		-	1	2	Ω
	LGATE Sink Resistance	V_{CC} = 5V, I_{LGATE}= 0.1A		-	0.6	1.2	Ω
T_D	Dead-Time			-	25	-	ns
PGOOD AND CONTROL FUNCTIONS							
	PGOOD Threshold	POK is high：~ 3µs noise filter, VSEN is from low to target value		87	92	95	%
		POK is high：~ 3µs noise filter, VSEN is from high to target value		107	112	117	%
	POK Hysteresys			-	3	-	%
	PG1, PG2 Leakage Current	$V_{PG1,2}$ = 5.5V		-	-	1	µA
$V_{PG1, 2}$	PG1, PG2 Voltage Low	$I_{PG1,2}$ = -4mA		-	0.5	1	V
I_{SEN}	ISEN Sourcing Current	By Design		-	-	260	µA
	Continuous-Conduction-Mode (CCM) Enforced (PFM Operation Inhibited)	VOUTx pulled low		-	-	0.1	V
	Automatic CCM/PFM Operation Enabled	VOUTx connected to the output		0.9	-	-	V
SOFT-START, SOFT-STOP, AND ENABLE							
I_{START}	Soft-Start Current Source	Sourcing current		-	4.5	-	µA
I_{STOP}	Soft-Stop Current Sink	Sinking current		-	2.2	-	µA
	SOFTx Pull-Low Impedance			-	2	-	kΩ
V_{ST}	Soft-Start Complete Threshold			-	1.5	-	V
	Soft-Start Clamp Voltage	Voltage Threshold of SOFT Pin		-	2.4	-	V
	EN Voltage Low (OFF)			-	-	0.8	V
	EN Voltage High (ON)			2.0	-	-	V

Typical Operating Characteristics

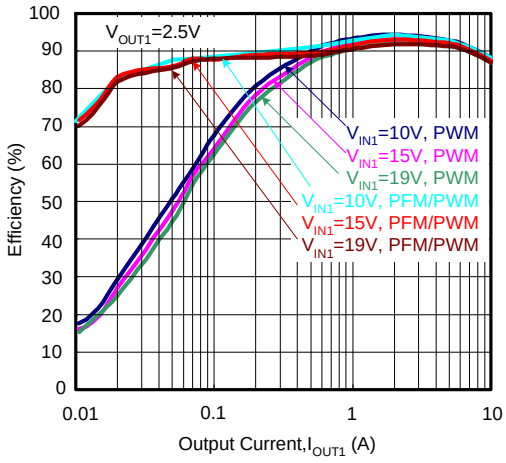
CH1 Output Voltage vs. Output Current



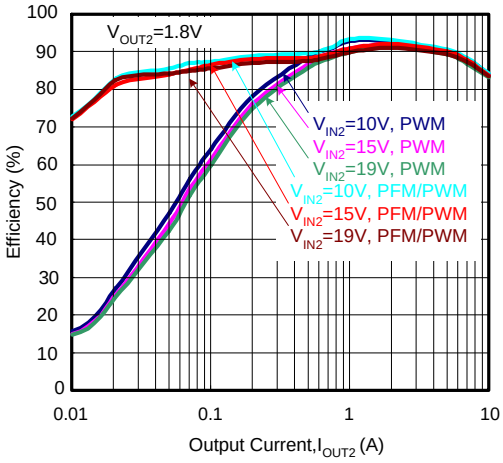
CH2 Output Voltage vs. Output Current



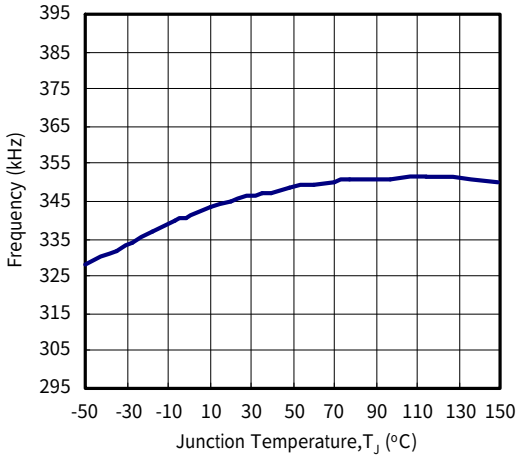
CH1 Efficiency vs. Output Current



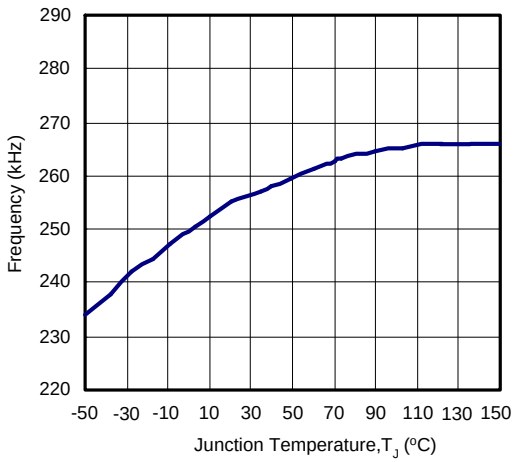
CH2 Efficiency vs. Output Current



CH1 Switching Frequency Over Temperature

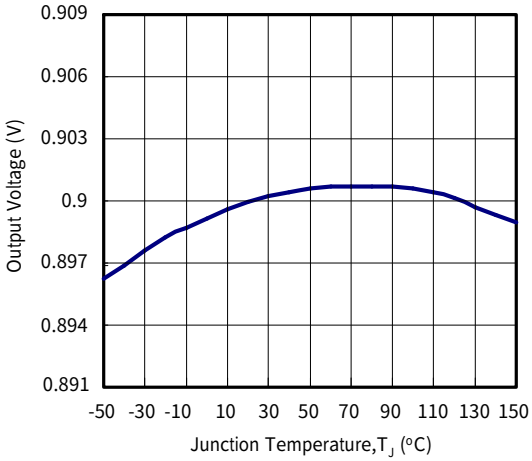


CH2 Switching Frequency Over Temperature

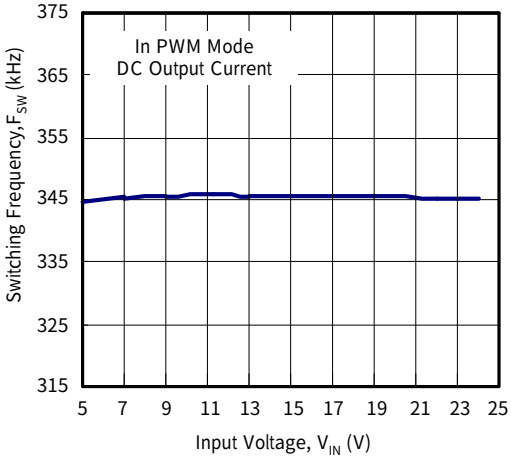


Typical Operating Characteristics (Cont.)

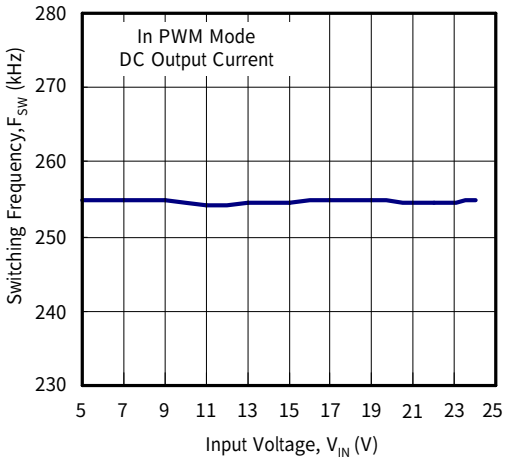
Reference Voltage Accuracy Over Temperature



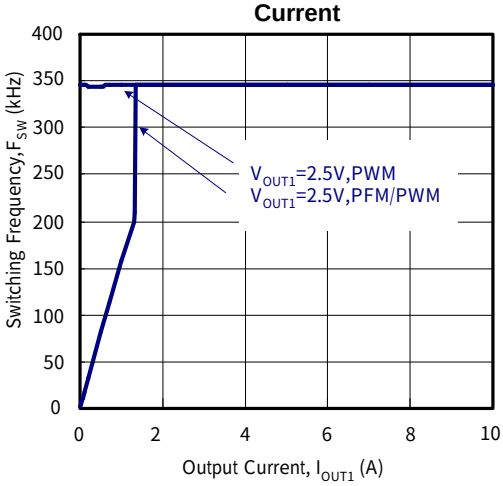
CH1 Switching Frequency vs. V_{IN}



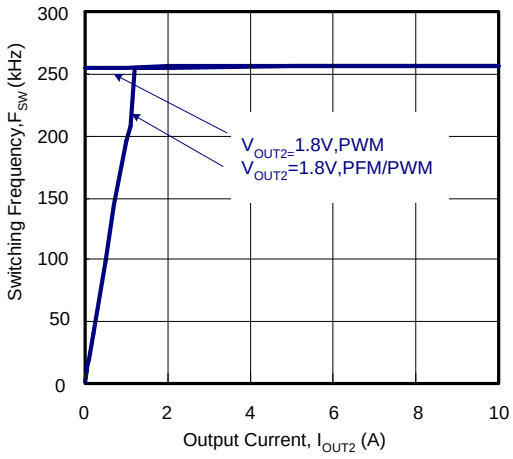
CH2 Switching Frequency vs. V_{IN}



CH1 Switching Frequency vs. Ouput Current

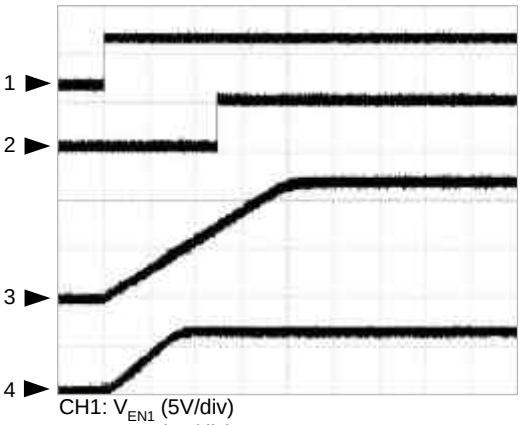


CH2 Switching Frequency vs. Ouput Current



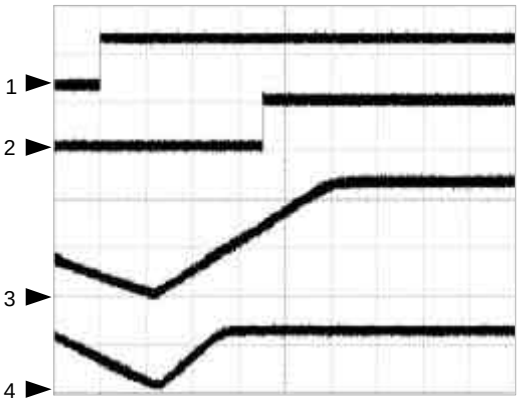
Operating Waveforms

Enable at Zero Initial Voltage of V_{OUT}



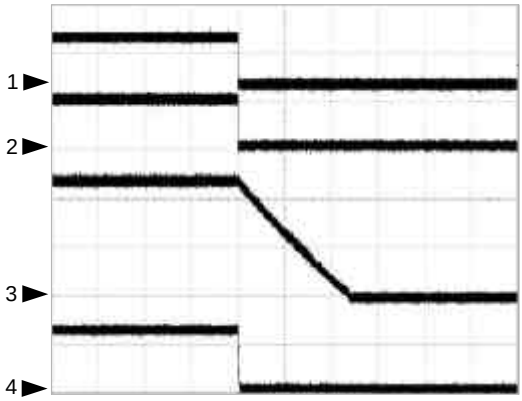
CH1: V_{EN1} (5V/div)
CH2: V_{PG1} (5V/div)
CH3: V_{SOFT1} (1V/div)
CH4: V_{OUT1} (2V/div)
Time: 2ms/div

Enable before End of Soft-Stop



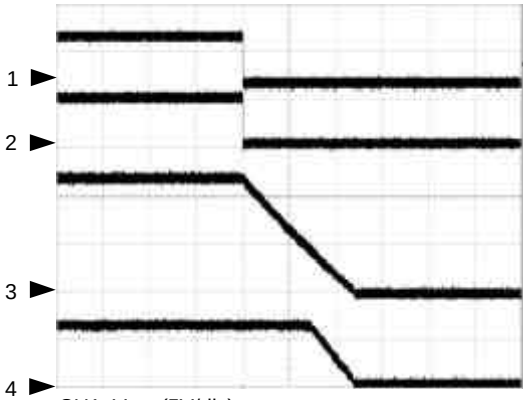
CH1: V_{EN1} (5V/div)
CH2: V_{PG1} (5V/div)
CH3: V_{SOFT1} (1V/div)
CH4: V_{OUT1} (2V/div)
Time: 2ms/div

Shutdown at I_{OUT1}=5A



CH1: V_{EN1} (5V/div)
CH2: V_{PG1} (5V/div)
CH3: V_{SOFT1} (1V/div)
CH4: V_{OUT1} (2V/div)
Time: 5ms/div

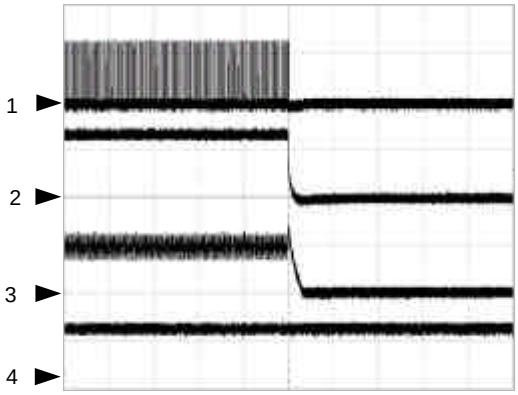
Shutdown with Soft-Stop at No Load



CH1: V_{EN1} (5V/div)
CH2: V_{PG1} (5V/div)
CH3: V_{SOFT1} (1V/div)
CH4: V_{OUT1} (2V/div)
Time: 5ms/div

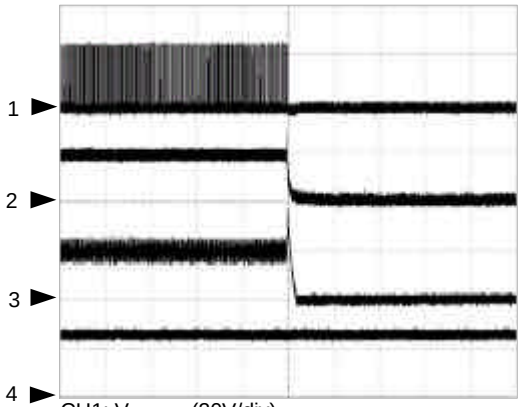
Operating Waveforms (Cont.)

UVP, PWM Mode (CH1)



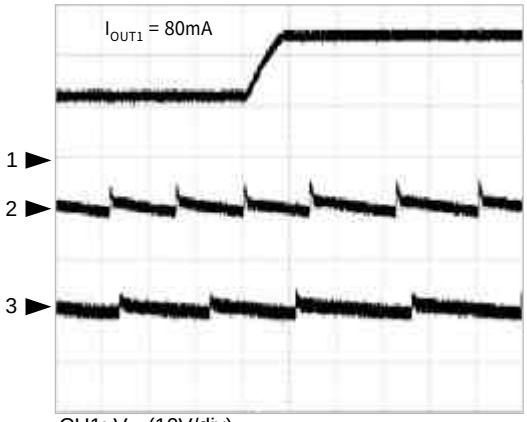
CH1: V_{PHASE1} (20V/div)
CH2: V_{OUT1} (2V/div)
CH3: I_{L1} (5A/div)
CH4: V_{OUT2} (2V/div)
Time: 100µs/div

UVP, PWM Mode (CH2)



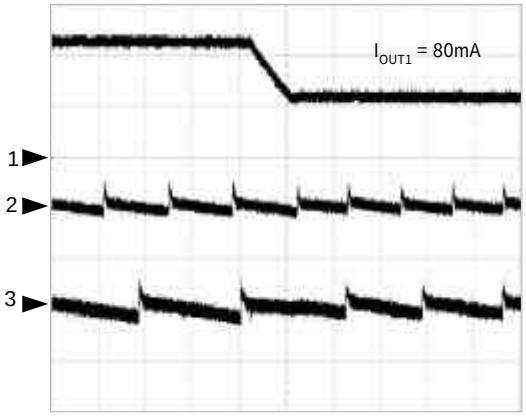
CH1: V_{PHASE2} (20V/div)
CH2: V_{OUT2} (2V/div)
CH3: I_{L2} (5A/div)
CH4: V_{OUT1} (2V/div)
Time: 200µs/div

Input Step-Up Transient at PFM Mode



CH1: V_{IN} (10V/div)
CH2: V_{OUT1} (AC, 100mV/div)
CH3: V_{OUT2} (AC, 100mV/div)
Time: 50µs/div

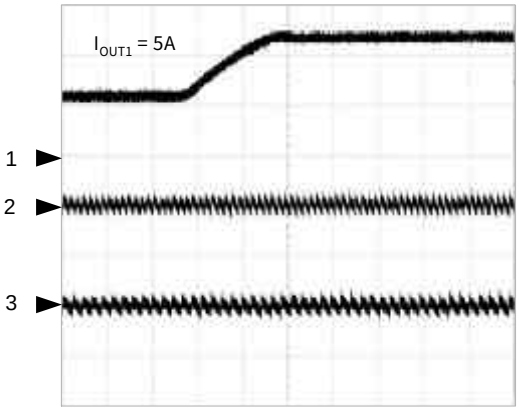
Input Step-Down Transient at PFM Mode



CH1: V_{IN} (10V/div)
CH2: V_{OUT1} (AC, 100mV/div)
CH3: V_{OUT2} (AC, 50mV/div)
Time: 50µs/div

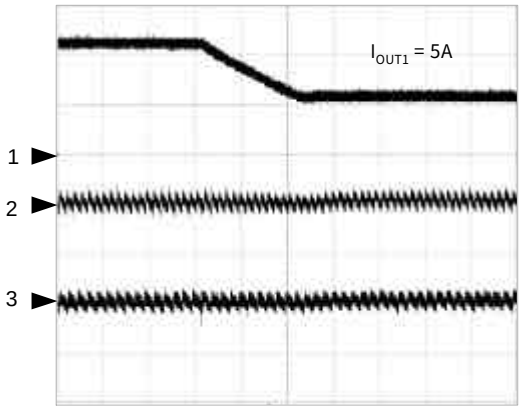
Operating Waveforms (Cont.)

Input Step-Up Transient at PWM Mode



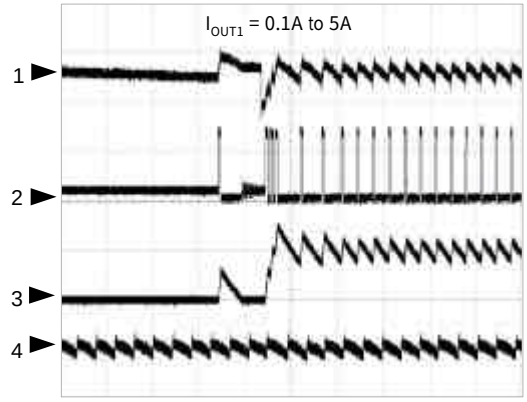
CH1: V_{IN} (10V/div)
CH2: V_{OUT1} (AC, 100mV/div)
CH3: V_{OUT2} (AC, 100mV/div)
Time: 20µs/div

Input Step-Down Transient at PWM Mode



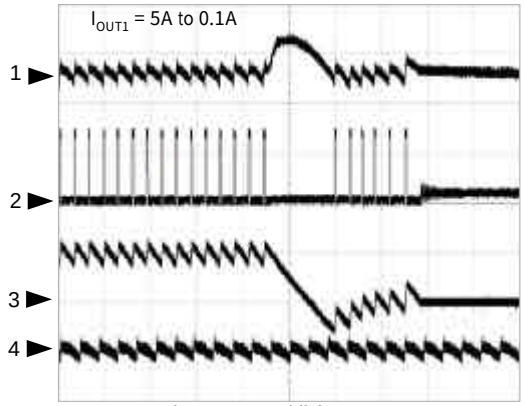
CH1: V_{IN} (10V/div)
CH2: V_{OUT1} (AC, 100mV/div)
CH3: V_{OUT2} (AC, 100mV/div)
Time: 20µs/div

Mode Transient of PFM to PWM



CH1: V_{OUT1} (AC, 100mV/div)
CH2: V_{PHASE1} (20V/div)
CH3: I_{L1} (5A/div)
CH4: V_{OUT2} (AC, 100mV/div)
Time: 10µs/div

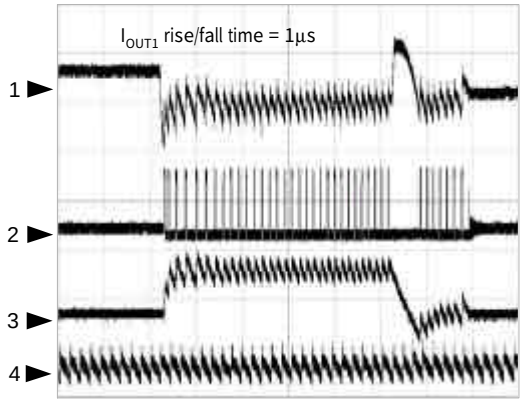
Mode Transient of PWM to PFM



CH1: V_{OUT1} (AC, 100mV/div)
CH2: V_{PHASE1} (20V/div)
CH3: I_{L1} (5A/div)
CH4: V_{OUT2} (AC, 100mV/div)
Time: 10µs/div

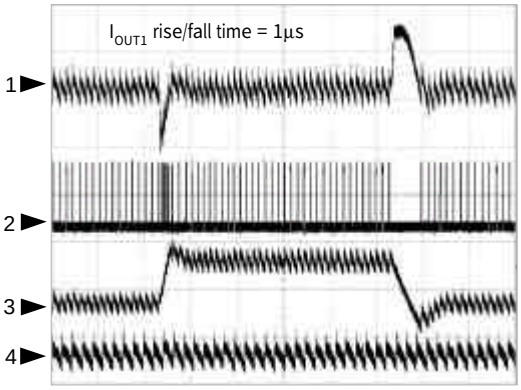
Operating Waveforms (Cont.)

Load Transient at PFM Mode
0A->5A->0A (CH1)



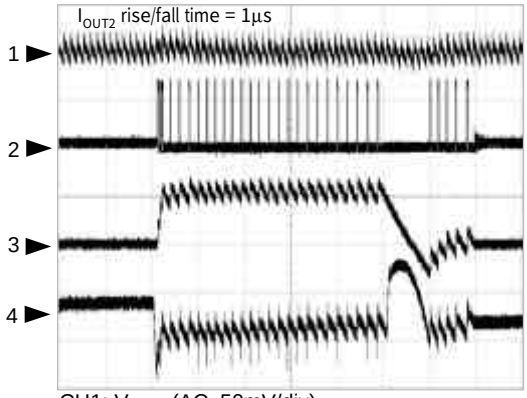
CH1: V_{OUT1} (AC, 50mV/div)
CH2: V_{PHASE1} (20V/div)
CH3: I_{L1} (5A/div)
CH4: V_{OUT2} (AC, 50mV/div)
Time: 20µs/div

Load Transient at PWM Mode
0A->5A->0A (CH1)



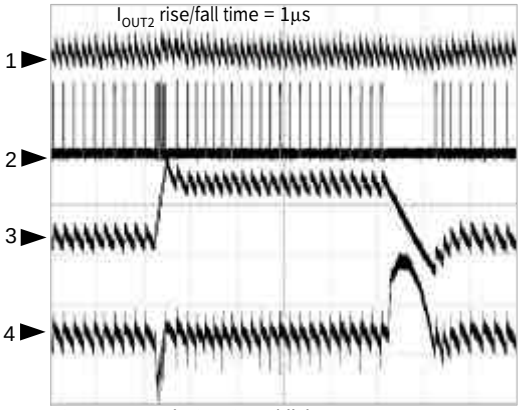
CH1: V_{OUT1} (AC, 50mV/div)
CH2: V_{PHASE1} (20V/div)
CH3: I_{L1} (5A/div)
CH4: V_{OUT2} (AC, 50mV/div)
Time: 20µs/div

Load Transient at PFM Mode
0A->5A->0A (CH2)



CH1: V_{OUT1} (AC, 50mV/div)
CH2: V_{PHASE1} (20V/div)
CH3: I_{L1} (5A/div)
CH4: V_{OUT2} (AC, 50mV/div)
Time: 20µs/div

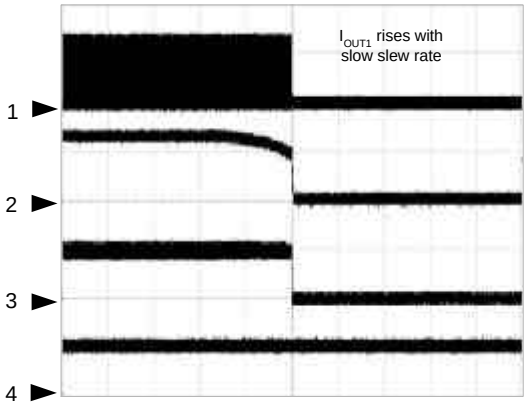
Load Transient at PWM Mode
0A->5A->0A (CH2)



CH1: V_{OUT1} (AC, 50mV/div)
CH2: V_{PHASE1} (20V/div)
CH3: I_{L1} (5A/div)
CH4: V_{OUT2} (AC, 50mV/div)
Time: 20µs/div

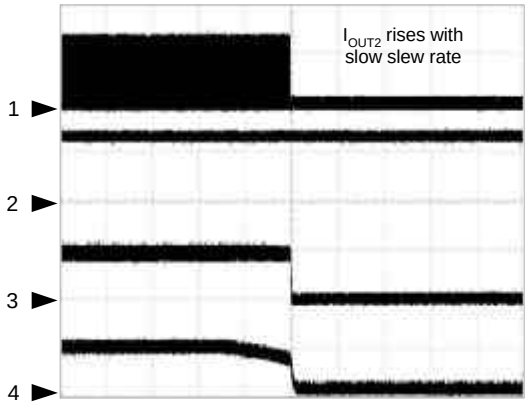
Operating Waveforms (Cont.)

Current-Limit and UV Protections (CH1)



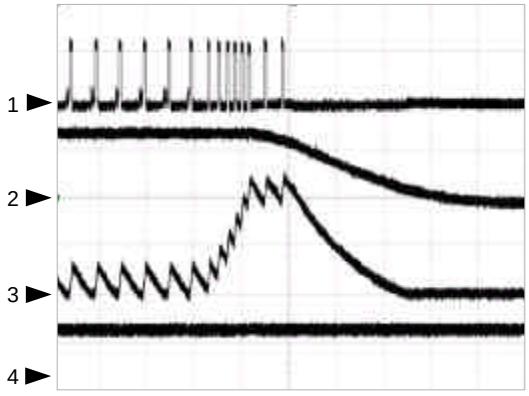
CH1: V_{PHASE1} (20V/div)
CH2: V_{OUT1} (2V/div)
CH3: I_{L1} (10A/div)
CH4: V_{OUT2} (2V/div)
Time: 2ms/div

Current-Limit and UV Protections (CH2)



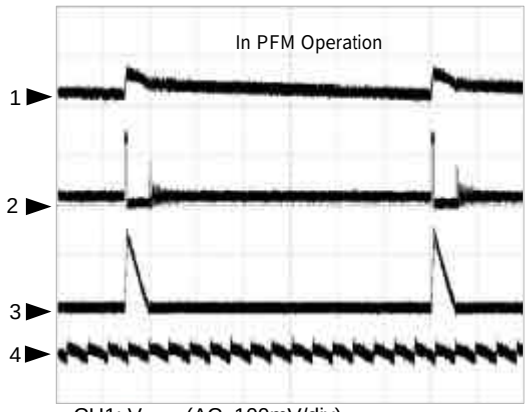
CH1: V_{PHASE2} (20V/div)
CH2: V_{OUT1} (2V/div)
CH3: I_{L2} (10A/div)
CH4: V_{OUT2} (2V/div)
Time: 1ms/div

Short Circuit Test



CH1: V_{PHASE1} (20V/div)
CH2: V_{OUT1} (2V/div)
CH3: I_{L1} (5A/div)
CH4: V_{OUT2} (2V/div)
Time: 10µs/div

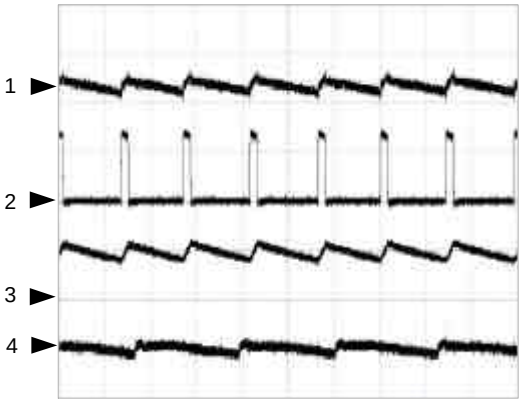
Operating at Light Load of 100mA (CH1)



CH1: V_{OUT1} (AC, 100mV/div)
CH2: V_{PHASE1} (20V/div)
CH3: I_{L1} (2A/div)
CH4: V_{OUT2} (AC, 100mV/div)
Time: 10µs/div

Operating Waveforms (Cont.)

Operating at Heavy Load of 5A (CH1)



CH1: V_{OUT1} (AC, 100mV/div)
CH2: V_{PHASE1} (20V/div)
CH3: I_{L1} (2A/div)
CH4: V_{OUT2} (AC, 100mV/div)
Time: 2μs/div

Pin Description

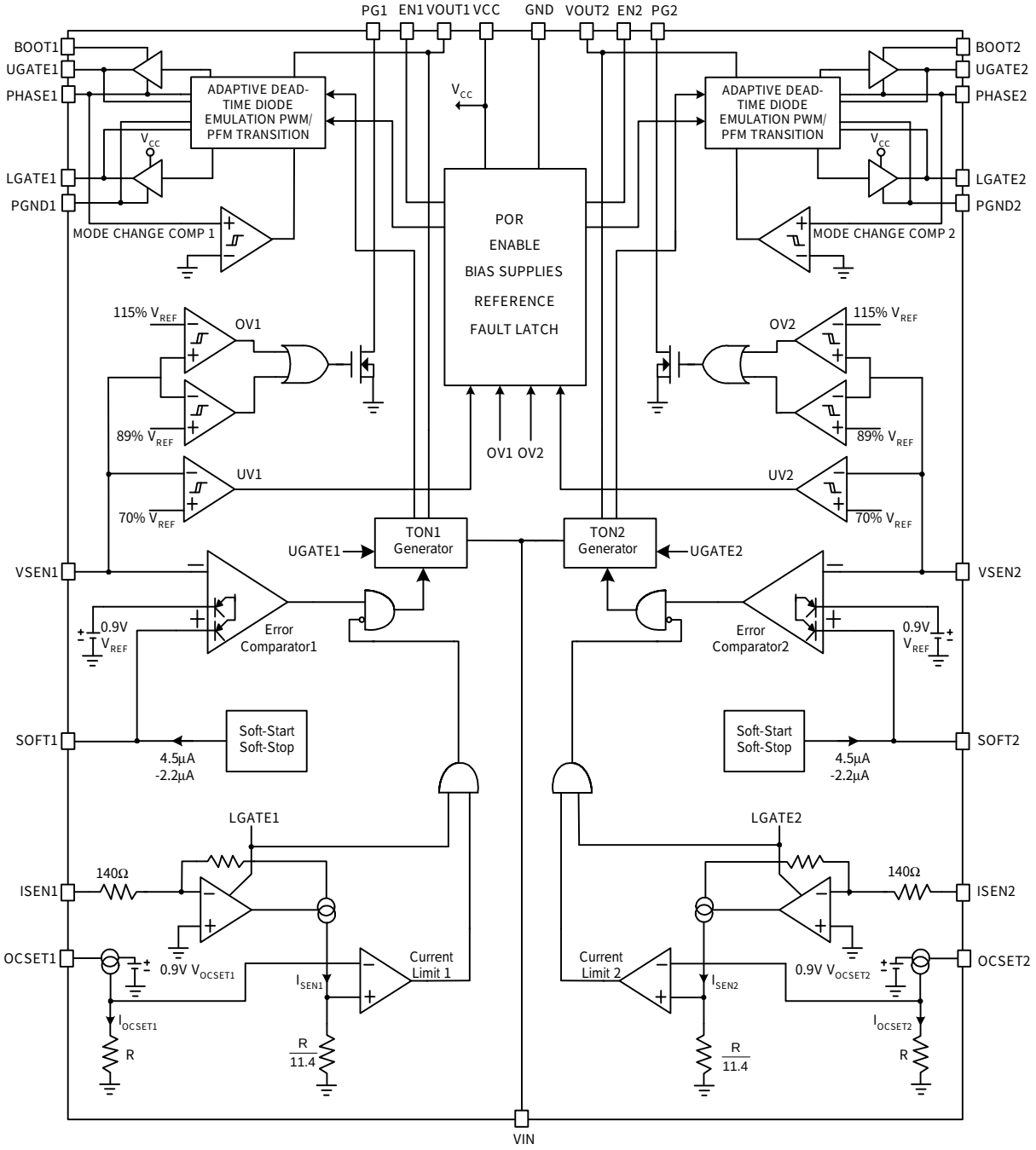
PIN		NAME	FUNCTION
QFN-24	SSOP-28		
22	1	GND	Signal ground for the IC.
23	2	LGATE1	Output of the low-side MOSFET driver (PWM 1). Connect this pin to Gate of the low-side MOSFET. Swings from PGND1 or PGND to VCC.
-	3	PGND1	Power ground of the LGATE1 low-side MOSFET driver. Connect the pin to the Source of the low-side MOSFET.
24	4	PHASE1	Junction point of the high-side MOSFET Source, output filter inductor and the low-side MOSFET Drain. Connect this pin to the Source of the high-side MOSFET. PHASE1 serves as the lower supply rail for the UGATE1 high-side gate driver.
1	5	UGATE1	Output of the high-side MOSFET driver (PWM 1). Connect this pin to Gate of the high-side MOSFET.
2	6	BOOT1	Supply Input for the UGATE1 Gate Driver and an internal level-shift circuit. Connect to an external capacitor and diode to create a boosted voltage suitable to drive a logic-level N-channel MOSFET.
3	7	ISEN1	Current sense pin (PWM 1). This pin is used to monitor the voltage drop across the Drain and Source of the low-side MOSFET for current limit. For precise current detection, this input can be connected to the optional current sense resistor placed in series with the Source of the low-side MOSFET.
4	8	EN1	Enable pin of the PWM 1 controller. The PWM 1 is enabled when EN1=1. When both EN1 and EN2 are low, the chip is disabled and only low leakage current is taken from V_{CC} and V_{IN}.
5	9	VOUT1	Selection pin for PWM 1 controller to operate in either forced PWM or automatic PFM/PWM mode.
6	10	VSEN1	Output voltage feedback pin (PWM1). This pin is connected to the resistive divider that set the desired output voltage for PWM 1. The PGOOD, UVP, and OVP circuits detect this signal to report output voltage status.

Pin Description (Cont.)

PIN		NAME	FUNCTION
QFN-24	SSOP-28		
-	11	OCSET1	Current-limit threshold setting pin (PWM1). This pin is a buffered 0.9V internal reference voltage. A resistor from this pin to the ground sets the current limit threshold for the converter.
8	12	SOFT1	Soft-start and soft-stop interval setting pin. The SOFT1 pin can source 4.5μA in soft-start process or sink 2.2μA in soft-stop process. The SOFT1 current charges or discharges the capacitor connected from the pin to the GND. The output voltage of the converter follows the ramping-up/down voltage on the SOFT1 pin in the soft-start/soft-stop process with the SOFT1 pin voltage as reference. When the SOFT1 pin voltage is higher than internal reference 0.9V, the error amplifier will use the reference to regulate output voltage. In the event of under-voltage, or EN1 shutdown, the SOFT1 is used by the soft-stop function and then pulled down though a 2K resistor to the ground after the falling SOFT1 voltage reaches about 50mV threshold. In soft-stop process, the converter only has sinking capability even though the output voltage is below the regulated voltage.
-	13	NC	No comment
9	14	VIN	Battery voltage input pin.
10	15	PG1	Power-good output pin of PWM 1. PGOOD1 is an open drain output used to indicate the status of the output voltage. This pin is pulled low when the PWM 1 Converter output is out of -11% ~ +15% of the set value.
11	16	PG2	Power-good output pin of PWM 2. The function is same as the PG1 pin.
12	17	SOFT2	Soft-start and soft-stop interval setting pin. The function is the same as the SOFT1 pin.
-	18	OCSET2	Current-limit threshold setting pin (PWM 2). This pin is a buffered 0.9V internal reference voltage. A resistor from this pin to ground sets the current-limit threshold for the converter.
13	19	VSEN2	Output voltage feedback pin. This pin is connected to the resistive divider that set the desired output voltage for PWM 2. The PGOOD, UVP, and OVP circuits use this signal to report output voltage status.
14	20	VOUT2	Selection pin for PWM 2 controller to operate in either forced PWM or automatic PFM/PWM mode.
15	21	EN2	Enable pin of the PWM 2 controller. The PWM 2 is enabled when EN2 = 1. When both EN1 and EN2 are low, the chip is disabled and only low leakage current is taken from V_{CC} and V_{IN}.
16	22	ISEN2	Current sense pin (PWM 2). This pin has the same function as ISEN1.
17	23	BOOT2	Supply Input for the UGATE2 Gate Driver and an internal level-shift circuit. Its function is same as BOOT1.
18	24	UGATE2	Output of the high-side MOSFET driver (PWM 2). Connect this pin to Gate of the high-side MOSFET.
19	25	PHASE2	Junction point of the high-side MOSFET source, output filter inductor and the low-side MOSFET Drain. Connect this pin to the Source of the high-side MOSFET. PHASE2 serves as the lower supply rail for the UGATE2 high-side gate driver.
-	26	PGND2	Power ground of the LGATE2 low-side MOSFET driver. Connect the pin to the Source of the low-side MOSFET.
20	27	LGATE2	Output of the low-side MOSFET driver (PWM 2). Connect this pin to Gate of the low-side MOSFET. Swings from PGND2 or PGND to VCC.
21	28	VCC	Supply voltage input pin for control circuitry and both low-side MOSFET drivers.
7	-	OCSET	Current limit threshold setting pin for PWM1 and PWM 2. This pin is a buffered 0.9V internal reference voltage. A resistor from this pin to the ground sets the current-limit threshold for the converter.
Thermal Pad	-	PGND	Power ground of the both channels' low-side MOSFET drivers. Connect the Sources of the both channels' low-side MOSFETs to the IC thermal pad as close as possible.

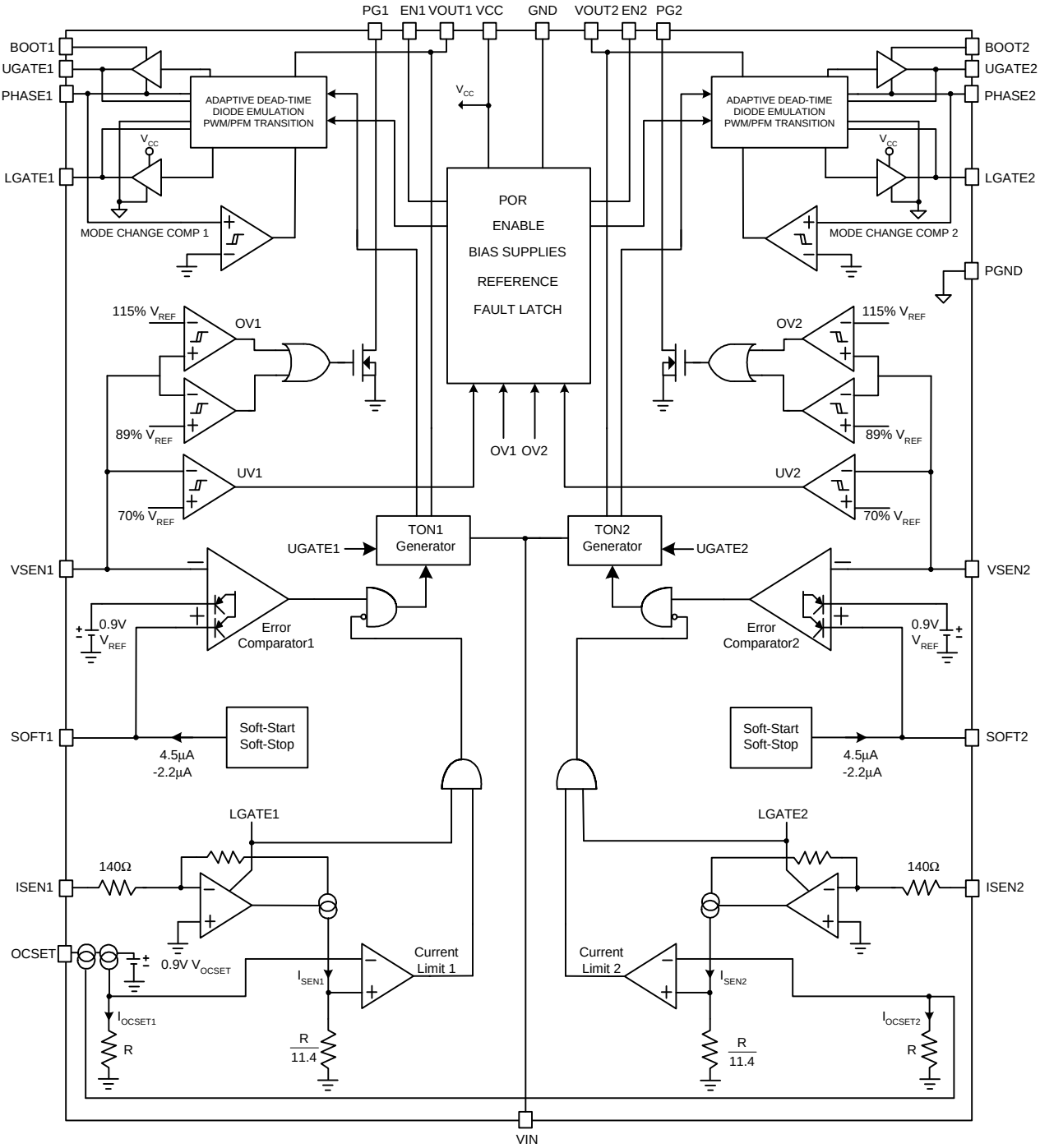
Block Diagram

1. SSOP-28



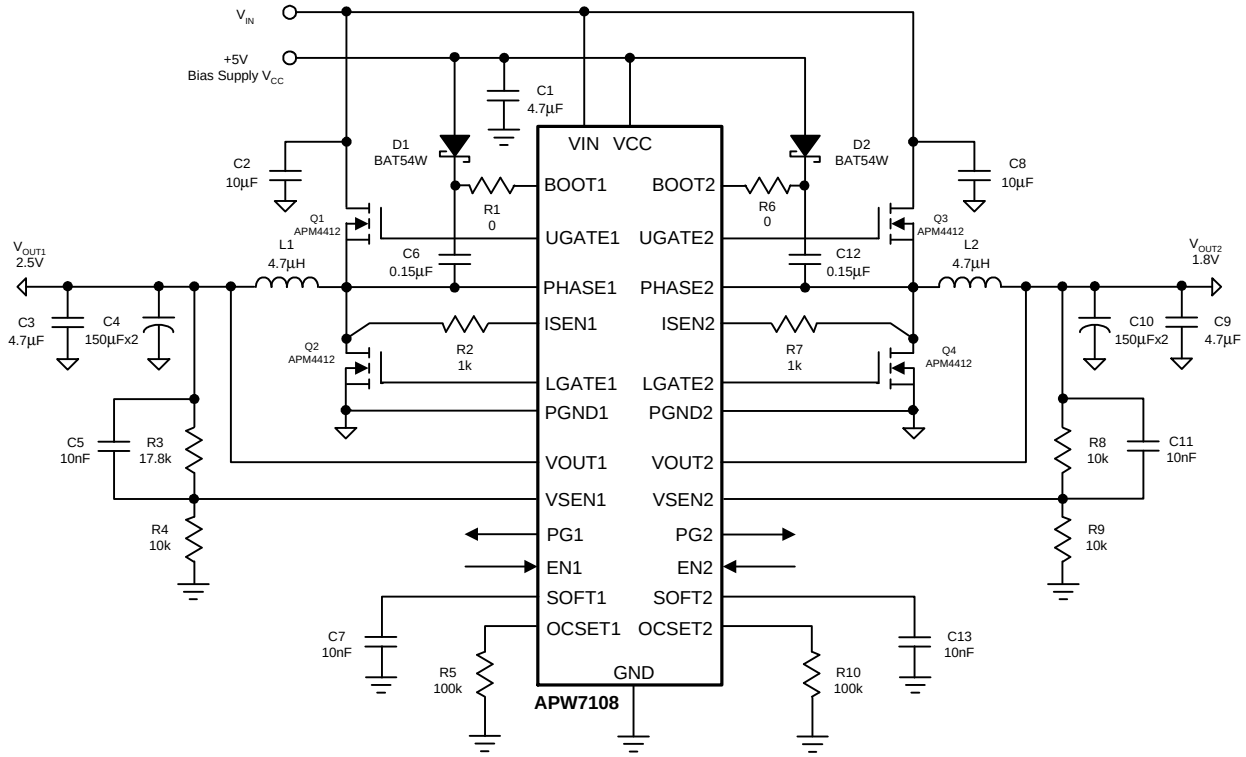
Block Diagram

2. QFN4x4-24

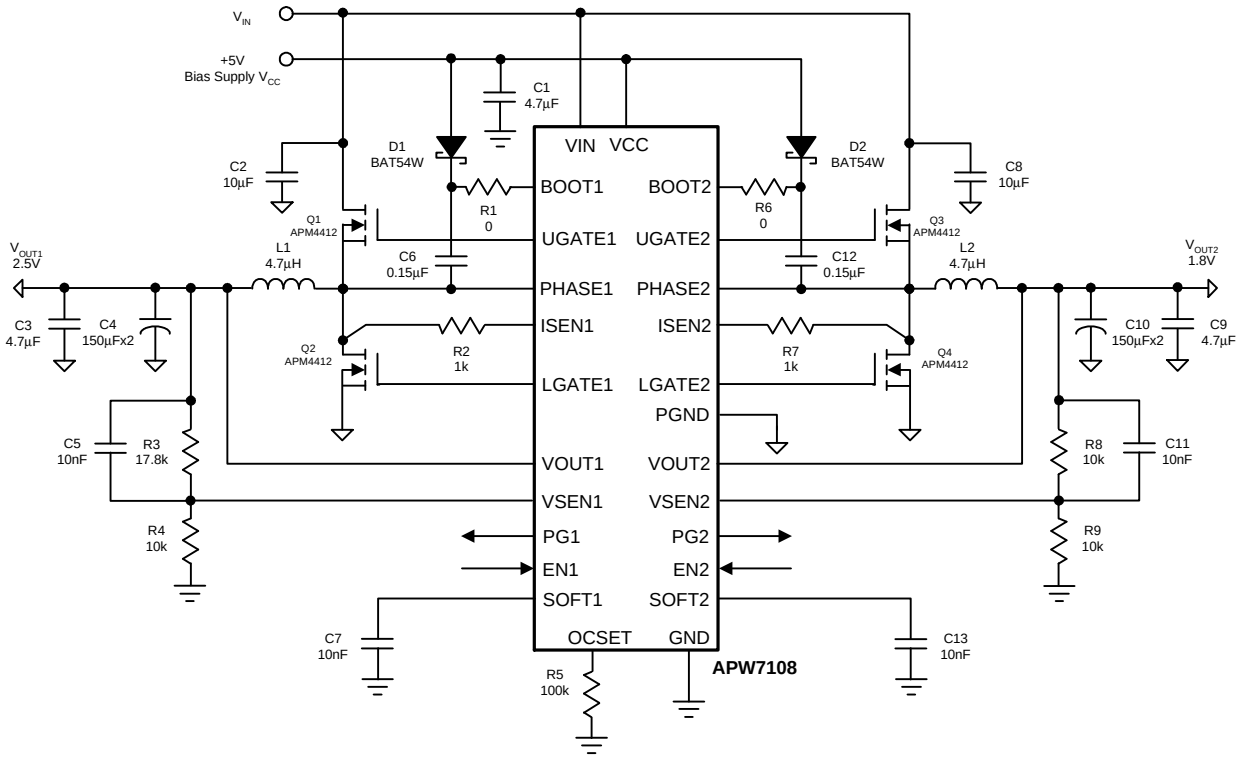


Typical Application Circuit

1. SSOP-28



2. QFN4x4-24



Function Description

Constant-On-Time PWM Controller with Input Feed-Forward

The constant-on-time control architecture is a pseudo-fixed frequency with input voltage feed-forward. This architecture relies on the output filter capacitor's effective series resistance (ESR) to act as a current-sense resistor, therefore, the output ripple voltage provides the PWM ramp signal. In PFM operation, the high-side switch on-time controlled by the on-time generator is determined solely by a one-shot whose pulse width is inversely proportional to input voltage and directly proportional to output voltage. In PWM operation, the high-side switch on-time is determined by a switching frequency control circuit in the on-time generator block for each channel. The switching frequency control circuit senses the switching frequency of the high-side switch and keeps regulating it at a constant frequency in PWM mode. The design improves the frequency variation and is more outstanding than a conventional constant-on-time controller which has large switching frequency variation over input voltage, output current and temperature. Both in PFM and PWM, the on-time generator, which senses input voltage on VIN pin, provides very fast on-time response to input line transients.

The on-times for channel 2 are set 35% higher than the on-times for channel 1. This is done to prevent audio-frequency "beating" between the two sides, which switch asynchronously for each side.

Another one-shot sets a minimum off-time (typical: 550ns). The on-time one-shot is triggered if the error comparator is high, the low-side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

PFM Mode

In PFM mode, an automatic switchover to pulse-frequency modulation (PFM) takes place at light loads. This switchover is effected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. This mechanism causes the threshold between PFM and PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the critical conduction point). The on-time of PFM mode is designed at 1.5 time of the nominal on-time of PWM mode. The on-time of PFM is given by:

$$T_{ON\text{ - }PFM} = \frac{1.5}{F_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

Where F_{SW} is the nominal switching frequency of the converter in PWM mode.

This design provides a hysteresis of converter's output current to prevent wrong or repeatedly PFM/PWM handoff with constant output current. The load current at handoff from PFM to PWM mode is given by:

$$I_{LOAD(PFM\ to\ PWM)} = \frac{1}{2} \times \frac{V_{IN} - V_{OUT}}{L} \times T_{ON\ -\ PFM} = \frac{V_{IN} - V_{OUT}}{2L} \times \frac{1.5}{F_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

The load current at handoff from PWM to PFM mode is given by:

$$I_{LOAD(PWM\ to\ PFM)} = \frac{1}{2} \times \frac{V_{IN} - V_{OUT}}{L} \times T_{ON\ -\ PWM} = \frac{V_{IN} - V_{OUT}}{2L} \times \frac{1}{F_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

Therefore, the $I_{LOAD(PFM\ to\ PWM)}$ is 1.5 time of the $I_{LOAD(PWM\ to\ PFM)}$.

Forced PWM Mode

The forced-PWM mode disables the zero-crossing comparator, which controls the low-side switch on time. This causes the low-side gate-drive waveform to become the complement of the high-side gate-drive waveform. This in turn causes the inductor current to reverse at light loads while UGATE maintains a duty factor of V_{OUT}/V_{IN}. The benefit of forced-PWM mode is to keep the switching frequency fairly constant. Forced-PWM mode is the most useful for reducing audio frequency noise, improving load-transient response, and providing sink-current capability for dynamic output voltage adjustment.

Power-On-Reset

A Power-On-Reset (POR) function is designed to prevent wrong logic controls when the V_{CC} voltage is low. The POR function continually monitors the bias supply voltage on the VCC pin if at least one of the enable pins is

Function Description (Cont.)

Power-On-Reset

set high. When the rising V_{CC} voltage reaches the rising POR voltage threshold (4.2V typical), the POR signal goes high and the chip initiates soft-start operations for the enabled channels. This voltage should drop lower than 4V (typical), the POR disables the chip.

Soft-Start/Soft-Stop

When soft-start is initiated, the voltage on the SOFT pin of the enabled channel starts to ramp up gradually with the internal 4.5μA current charging the soft-start capacitor. The output voltage follows the soft-start voltage with the converter operating in PWM mode. When the SOFT pin voltage reaches 0.9V, the output voltage comes into regulation. When the SOFT voltage reaches 1.5V, the power-good (PGOOD) is enabled. Even though the SOFT pin voltage continues to rise after reaching 1.5V, this voltage does not affect the output voltage. The maximum SOFT voltage is clamped about 2.4V.

The soft-start time (the time from the moment when EN becomes high to the moment when PGOOD is reported) is determined by the following equation:

$$T_{SOFT} = \frac{1.5V \times C_{SOFT}}{4.5\mu A}$$

The time that takes the output voltage to come into regulation can be obtained from the following equation:

$$T_{RISE} = 0.6 \times T_{SOFT}$$

During the soft-start stage before the PGOOD pin is ready, the under-voltage protection is prohibited. The over-voltage and current-limit protection functions are enabled. If the output capacitor has residue voltage before start-up, both low-side and high-side MOSFETs are in off-state until the soft-start capacitor charges equal to the VSEN pin voltage. This will ensure the output voltage starts from its existing voltage level.

In the event of under-voltage or shutdown, the SOFT pin is used by the soft-stop function. The soft-stop function discharges the voltage on SOFT pin with the internal 2.2μA current sink. The channel with soft-stop enabled gradually ramps down the output voltage, following the SOFT voltage, by controlling the low-side MOSFET working as a sinking linear regulator. The soft-stop process is completed when the falling SOFT voltage reaches about 50mV (typical) threshold. At this moment, the LGATE goes high level with latch and SOFT pulls low by using the internal 2kΩ resistor to the ground. The latch can be reset by cycling both of the EN signals or VCC power-on-reset signal.

Under-Voltage Protection (UVP)

In the operational process, if a short-circuit occurs, the output voltage will drop quickly. When load current is bigger than current-limit threshold value, the output voltage will fall out of the required regulation range. The under-voltage continually monitors the V_{SEN} voltage after soft-start is completed. If a load step is strong enough to pull the output voltage lower than the under-voltage threshold, the offending channel pulls low the PGOOD immediately and starts a soft-stop process to shut down the output gradually. The offending channel is latched off when the soft-stop process is completed.

The under-voltage threshold is 70% of the nominal output voltage. The under voltage comparator has a built-in 2μs noise filter to prevent the chip from wrong UVP shutdown caused by noise. Toggling both enable pins to low, or recycling V_{CC}, will clear the latch and bring the chip back to operation.

Over-Voltage Protection (OVP)

The over-voltage function monitors the output voltage by VSEN pin. The V_{SEN} voltage should increase over 115% of the reference voltage due to the high-side MOSFET failure or for other reasons, and the over-voltage protection comparator designed with a 2μs noise filter will force the low-side MOSFET gate driver to be high. This action actively pulls down the output voltage and eventually attempts to blow the battery fuse. As soon as the output voltage is within regulation, the OVP comparator is disengaged. The chip will restore its normal operation. When the OVP occurs, the PGOOD will drop to low as well.

This OVP scheme only clamps the voltage overshoot and does not invert the output voltage when otherwise activated with a continuously high output from low-side MOSFET driver-a common problem for OVP schemes with a latch.

Function Description (Cont.)

Power Good Indicator

In the soft-start process, the PGOOD is an open-drain and established after the soft pin voltage is above 1.5V. In normal operation, the PGOOD window is from 89% to 115% of the converter's reference voltage. The VSEN pin has to stay within this window for PGOOD to be high. Since the VSEN pin is used for both feedback and monitoring purposes, the output voltage deviation can be coupled directly to the VSEN pin by the capacitor in parallel with the voltage divider as shown in the typical applications. In order to prevent false PGOOD drop, capacitors need to parallel at the output to confine the voltage deviation with severe load step transient. The PGOOD comparator has a built-in 3µs noise filter.

When POR=0, EN= 0, or after UVP, the PGOOD is pulled low regardless of the output voltage.

Enable Control

When the EN pin is high (EN=1), the PWM is enabled and the soft-start is initiated. When both EN1 and EN2 are low (EN=0), the chip is in the shutdown and only low leakage current is taken from V_{CC} and V_{IN}. In shutdown mode, LGATE will be pulled high.

Current-Limit

The current-limit circuit employs an unique "valley" current sensing algorithm (Figure 1). If the magnitude of the current-sense signal at ISEN pin is above the current-limit threshold, the PWM is not allowed to initiate a new cycle. The actual peak current is greater than the current-limit threshold by an amount equals to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are the function of the sense resistance, inductor value, and battery voltage.

The current sensing pin can source up to 260µA. The current sense resistor R_{ISEN} and OCSET resistor R_{OCSET} can be adjusted simultaneously for the same current-limit threshold level. The relationship between the sampled current and MOSFET current is given by:

$$I_{SEN}(R_{ISEN}+140)=R_{DS(ON)}\cdot I_D$$

Which means the current sensing pin will source current to make the voltage drop on the MOSFET equals to the voltage generated on the sensing resistor, plus the internal resistor, along the ISEN pin current flowing path.

Both PWM controllers use the low-side MOSFETs on-resistance $R_{DS(ON)}$, to monitor the current for protection against shortened outputs. The sensed current from the ISEN pin is compared with a current set by a resistor connected from the OCSET pin to the ground:

$$R_{OCSET}=\frac{10.3}{\frac{I_{OC}\cdot R_{DS(ON)}}{R_{ISEN}+140\Omega}+8\mu A}$$

where, I_{OC} is a desired current-limit threshold and R_{ISEN} is the value of the current sense resistor connected to the ISEN pin. The 8µA is the offset current added on top of the sensed current from the ISEN pin for internal circuit biasing.

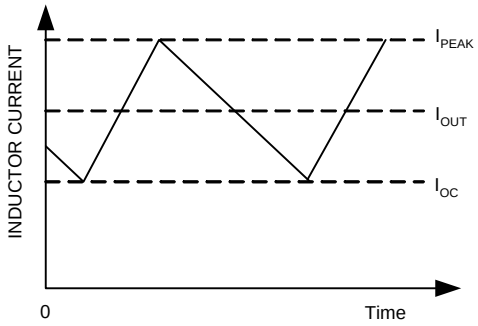


Figure 1. Current Limit Algorithm

Application Information

Output Voltage Selection

The output voltage can be adjustable from 0.9V to 5.5V with a resistor-divider. Using 1% or better resistors for the resistive divider is recommended. The VSEN pin is the inverter input of the error amplifier, and the reference voltage is 0.9V. Take APW7108 as the example, the output voltage is determined by:

$$V_{OUTX} = 0.9 \times \left(1 + \frac{R1}{R_{GND}}\right)$$

Where R1 is the resistor connected from V_{OUTX} to VSENx and R_{GND} is the resistor connected from VSENx to the GND.

Output Inductor Selection

The duty cycle of a buck converter is the function of the input voltage and output voltage. Once an output voltage is fixed, it can be written as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

The inductor value determises the inductor ripple current and affects the load transient reponse. Higher inductor value reduces the inductor's ripple current and induces lower output ripple voltage. The ripple current and ripple voltage can be approxminated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{F_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Where F_{SW} is the switching frequency of the regulator. Although increase the inductor value and frequency would reduce the ripple current and voltage, there is a tradeoff between the inductor's ripple current and the regulator load transient response time.

A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current. Increasing the switching frequency (F_{SW}) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFETs and the power dissipation of the converter. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current. Once the inductance value has been chosen, select an inductor that is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This will result in a larger output ripple voltage.

Output Capacitor Selection

Output voltage ripple and the transient voltage deviation are factors that have to be taken into consideration when selecting an output capacitor. Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, it's important to select high performance low ESR capacitors that are intended for switching regulator applications. In addition to high frequency noise related MOSFET turn-on and turn-off, the output voltage ripple includes the capacitance voltage drop and ESR voltage drop caused by the AC peak-to-peak current. These two voltages can be represented by:

$$\Delta V_{COUT} = \frac{I_{RIPPLE}}{8 C_{OUT} F_{SW}}$$

$$\Delta V_{ESR} = I_{RIPPLE} \times R_{ESR}$$

These two components constitute a large portion of the total output voltage ripple. In some applications, multiple capacitors have to be paralleled to achieve the desired ESR value. If the output of the converter has to support another load with high pulsating current, more capacitors are needed in order to reduce the equivalent ESR and suppress the voltage ripple to a tolerable level. A small decoupling capacitor in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors are also must be considered.

To support a load transient that is faster than the switching frequency, more capacitors have to be used to reduce the voltage excursion during load step change. Another aspect of the capacitor selection is that the total AC current going through the capacitors has to be less than the rated RMS current specified on the capacitors to prevent the capacitor from over-heating.

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation,

Application Information (Cont.)

Input Capacitor Selection

select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage. The maximum RMS current rating requirement is approximately $I_{OUT}/2$, where I_{OUT} is the load current. During power up, the input capacitors have to handle large amount of surge current. In low-duty notebook appliactions, ceramic capacitors are recommended. The capacitors must be connected between the drain of high-side MOSFET and the source of low-side MOSFET with very low-impeadance PCB layout.

MOSFET Selection

The application for a notebook battery with a maximum voltage of 24V, at least a minimum 30V MOSFETs should be used. The design has to trade off the gate charge with the $R_{DS(ON)}$ of the MOSFET:

- For the low-side MOSFET, before it is turned on, the body diode has been conducted. The low-side MOSFET driver will not charge the miller capacitor of this MOSFET.
- In the turning-off process of the low-side MOSFET, the load current will shift to the body diode first. The high dv/dt of the phase node voltage will charge the miller capacitor through the low-side MOSFET driver sinking current path. This results in much less switching loss of the low-side MOSFETs.The duty cycle is often very small in high battery voltage applications, and the low-side MOSFET will conduct most of the switching cycle; therefore, the less the $R_{DS(ON)}$ of the low-side MOSFET loss, the less the power loss. The gate charge for this MOSFET is usually of secondary consideration. The high-side MOSFET does not have the zero voltage switching condition, and because it conducts for less time compared to the low-side MOSFET, the switching loss tends to be dominant. Priority should be given to the MOSFETs with less gate charge, so that both the gate driver loss and switching loss will be minimized.

The selection of the N-channel power MOSFETs are determined by the $R_{DS(ON)}$, reversing transfer capacitance (C_{RSS}) and maximum output current requirement. The losses in the MOSFETs have two components: conduction loss and transition loss. For the high-side and low-side MOSFETs, the losses are approximately given by the following equations:

$$P_{high\text{-}side} = I_{OUT}^{2}(1+TC)(R_{DS(ON)})D + (0.5)(I_{OUT})(V_{IN})(t_{SW})F_{SW}$$

$$P_{low\text{-}side} = I_{OUT}^{2}(1+TC)(R_{DS(ON)})(1-D)$$

Where

I_{OUT} is the load current
TC is the temperature dependency of $R_{DS(ON)}$
F_{SW} is the switching frequency
t_{SW} is the switching interval
D is the duty cycle

Note that both MOSFETs have conduction losses while the high-side MOSFET includes an additional transition loss. The switching internal, t_{SW}, is the function of the reverse transfer capacitance C_{RSS}. The (1+TC) term is to factor in the temperature dependency of the $R_{DS(ON)}$ and can be extracted from the "$R_{DS(ON)}$ vs Temperature" curve of the power MOSFET.

Layout Consideration

In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator. With power devices switching at higher frequency, the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic circuit elements. As an example, consider the turn-off transition of the PWM MOSFET. Before turn-off condition, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is freewheeling by the low-side MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short and wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike. Signal and power grounds are to be kept separating and finally combined using ground plane construction or single point grounding. The best tie-point between the signal ground and the power ground is at the negative side of the output capacitor on each channel, where there is less noise. Noisy traces beneath the IC are not recommended. Below is a checklist for your layout:

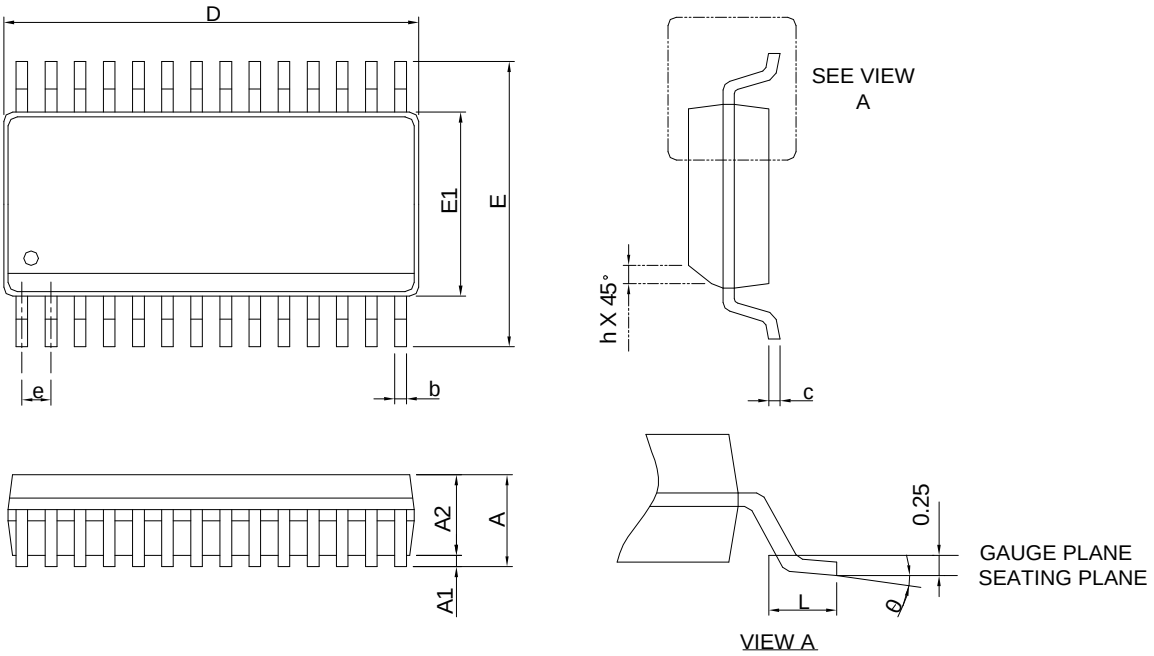
Application Information (Cont.)

Layout Consideration (Cont.)

- Keep the switching nodes (UGATEx, LGATEx, BOOTx, PHASEx, and ISENx) away from sensitive small signal nodes since these nodes are fast moving signals. Therefore, keep traces to these nodes as short as possible and there should be no other weak signal traces in parallel with theses traces on any layer.
- The signals going through theses traces have both high dv/dt and high di/dt, with high peak charging and discharging current. The traces from the gate drivers to the MOSFETs (UGATEx and LGATEx) should be short and wide.
- Place the source of the high-side MOSFET and the drain of the low-side MOSFET as close as possible. Minimizing the impedance with wide layout plane between the two pads reduces the voltage bounce of the node.
- The ISENx trace should be a separate trace, and independently go to the drain terminal of the low-side MOSFET. The current sense resistor should be close to ISENx pin. The loop formed by the bottom MOSFET, output inductor, and output capacitor, should be very small. The source of the bottom MOSFET should tie to the negative side of the output capacitor in order for the ISENx pin to get the voltage drop on the $R_{DS(ON)}$.
- Decoupling capacitor, compensation component, the resistor dividers, boot capacitors, and soft-start capacitors should be close their pins. (For example, place the decoupling ceramic capacitor near the drain of the high-side MOSFET as close as possible. The bulk capacitors are also placed near the drain).
- The input capacitor should be near the drain of the high-side MOSFET; the high quality ceramic decoupling capacitor can be put close to the VCC and GND pins; the output capacitor should be near the loads. The input capacitor GND should be close to the output capacitor GND and the low-side MOSFET GND.
- The drain of the MOSFETs (V_{IN} and PHASEx nodes) should be a large plane for heat sinking. And PHASEx pin traces are also the return path for UGATEx. Connect these pins to the respective converter's high-side MOSFET source.
- The APW7108 uses ripple mode control. Build the resistor divider close to the VSENx pin so that the high impedance trace is shorter. The VSENx pin traces can't be closed to the switching signal traces (UGATEx, LGATEx, BOOTx, PHASEx, and ISENx).
- The PGNDx trace should be a seperate trace, and inpendently go to the source of the low-side MOSFET.
- For QFN4x4-24 package only, the thermal pad is the PGND of the dual channels. The sources of the both channels' low-side MOSFETs should be near the PGND respectively.

Package Information

SSOP-28

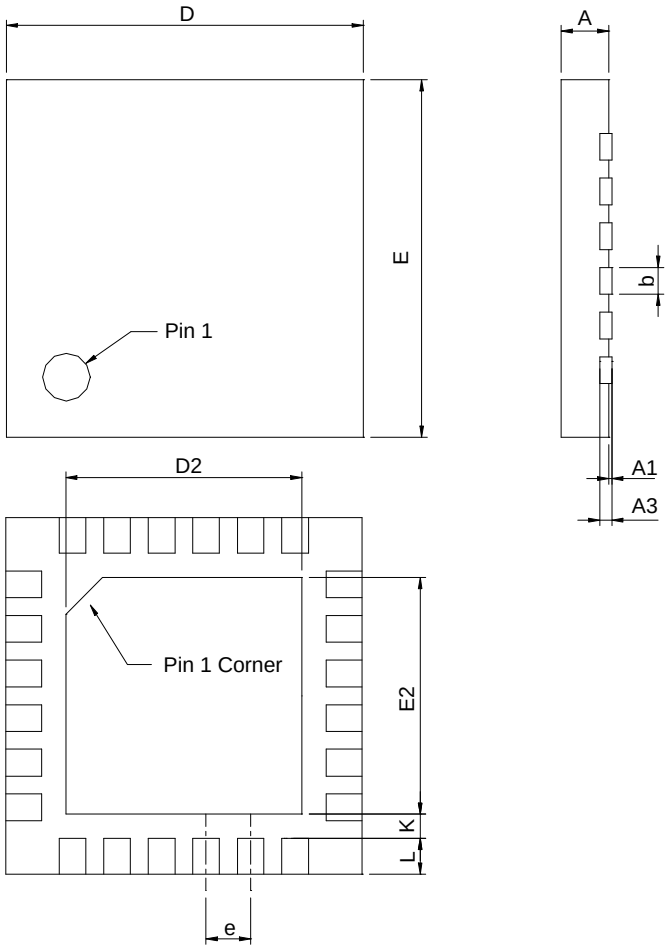


SYMBOL	SSOP-28			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.24		0.049	
b	0.20	0.30	0.008	0.012
c	0.15	0.25	0.006	0.010
D	9.80	10.00	0.386	0.394
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	0.635 BSC		0.025 BSC	
L	0.40	1.27	0.016	0.050
h	0.25	0.50	0.010	0.020
θ	0 °	8 °	0 °	8 °

Note : 1. Followed from JEDEC MO-137 AF.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Package Information

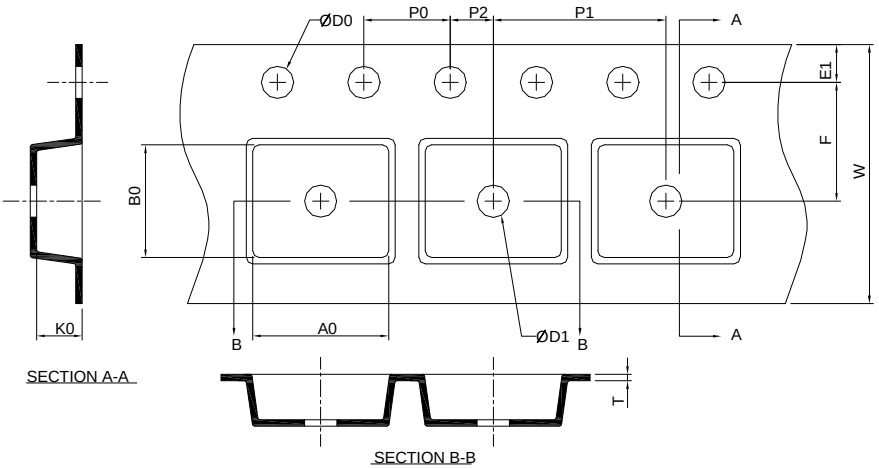
QFN4x4-24

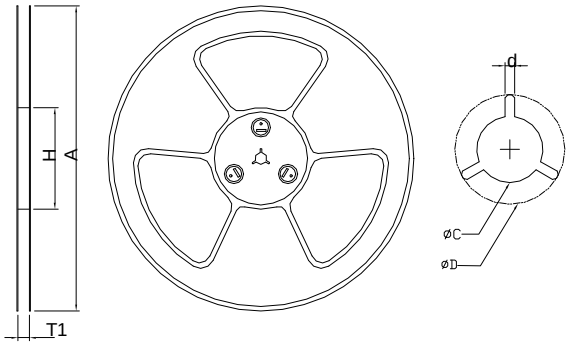


SYMBOL	QFN4x4-24			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.008	0.012
D	3.90	4.10	0.154	0.161
D2	2.50	2.80	0.098	0.110
E	3.90	4.10	0.154	0.161
E2	2.50	2.80	0.098	0.110
e	0.50 BSC		0.020 BSC	
L	0.35	0.45	0.014	0.018
K	0.20		0.008	

Note : 1. Followed from JEDEC MO-220 WGGD-6.

Carrier Tape & Reel Dimensions





Application	A	H	T1	C	d	D	W	E1	F
SSOP-28	330.0±2.00	50 MIN.	16.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	16.0±0.30	1.75±0.10	7.5±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.4±0.20	10.2±0.20	2.1±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
QFN4x4-24	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	4.30±0.20	4.30±0.20	1.30±0.20

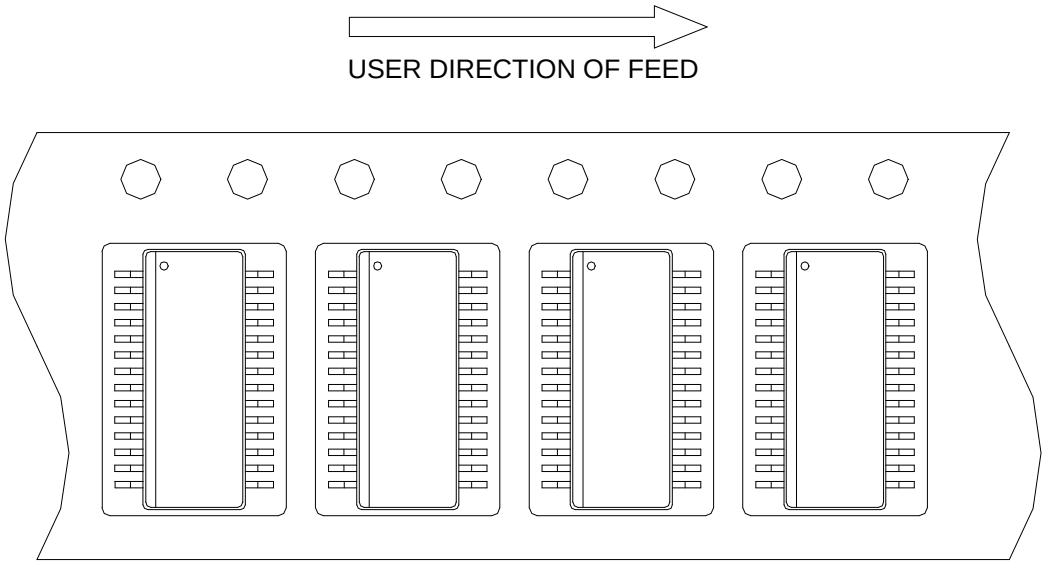
(mm)

Devices Per Unit

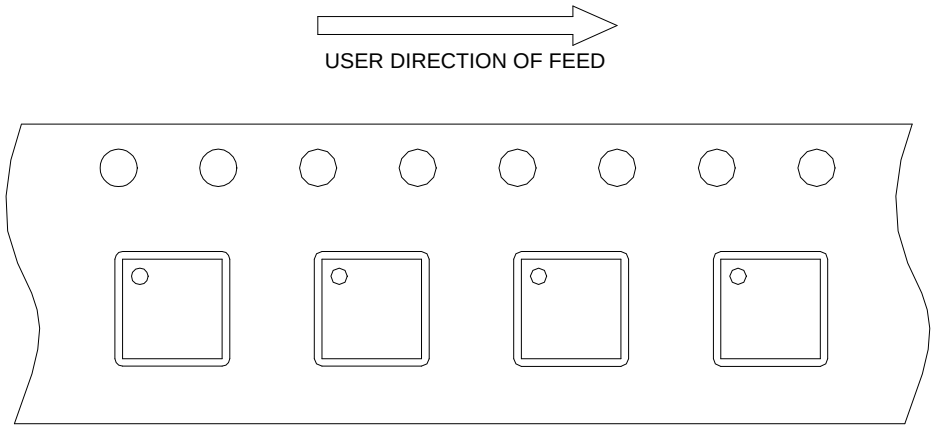
Package Type	Unit	Quantity
SSOP-28	Tape & Reel	2500
QFN4x4-24	Tape & Reel	3000

Taping Direction Information

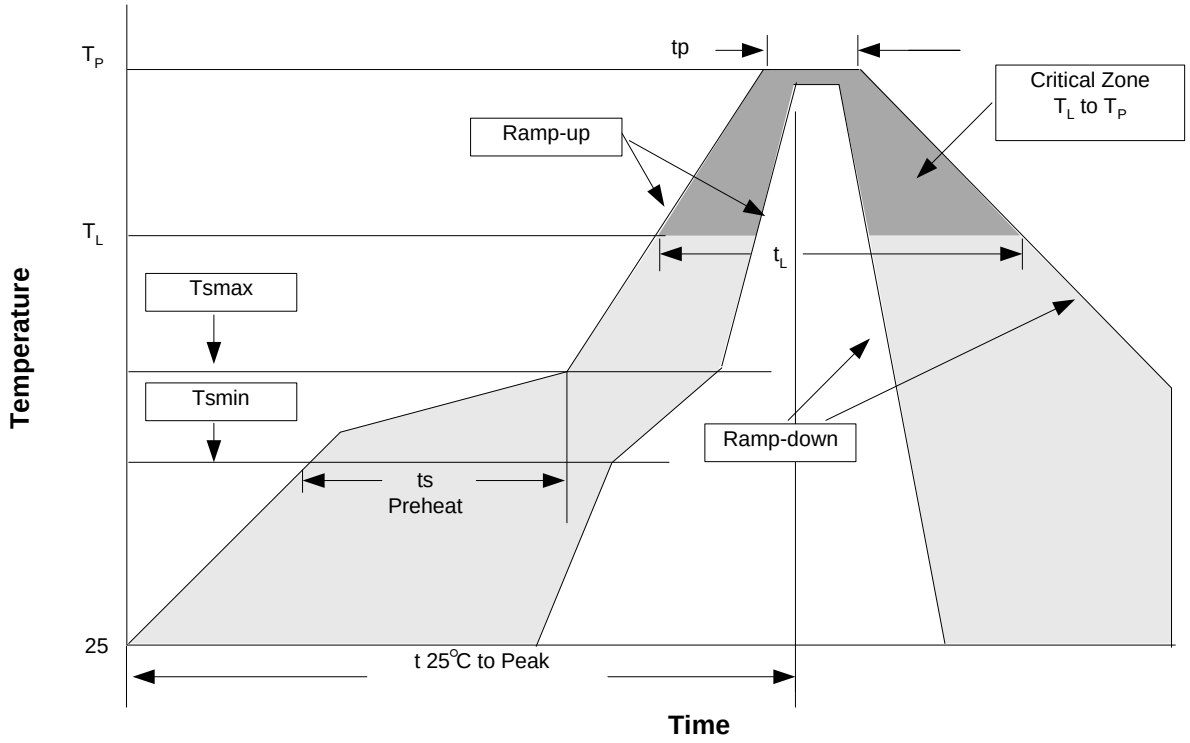
SSOP-28



QFN4x4



Reflow Condition (IR/Convection or VPR Reflow)



Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 sec
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B, A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1_{tr} > 100mA

Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classification Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Notes: All temperatures refer to topside of the package. Measured on the body surface.

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*

* Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.

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