3A 5V 2MHz Synchronous Buck Converter

Features

- **High Efficiency up to 95%**
  - PFM/PWM Mode Operation
- **Adjustable Output Voltage from 0.8V to VIN**
- **Integrated 110mΩ High/Low Side MOSFET**
- **Programmable Switching Frequency: 300kHz to 2MHz**
- **Low Dropout Operation: 100% Duty Cycle**
- **Stable with Low ESR Capacitors**
- **Power-On-Reset Detection on VDD and PVDD**
- **Integrate Soft-Start and Soft-Off**
- **Over-Temperature Protection**
- **Over-Voltage Protection**
- **Under-Voltage Protection**
- **High/Low Side Current-Limit**
- **Power Good Indicator (APW7153A/B)**
- **Enable/Shutdown Function**
- **Small TDFN3x3-10 and SOP-8P Packages**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **LCD Minitor/TV**
- **Set-Top Box**
- **DSL, Switch HUB**
- **Notebook Computer**
- **Portable Instrument**

General Description

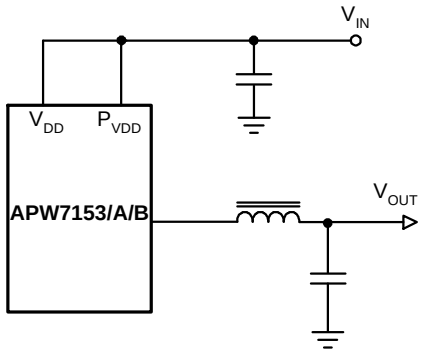
APW7153/A/B is a 3A synchronous buck converter with integrated 110mΩ power MOSFETs. The APW7153/A/B is designed with a current-mode control scheme; it can convert wide input voltage of 2.6V to 5.5V to the output voltage adjustable from 0.8V to 5.5V to provide excellent output voltage regulation.

The APW7153/A/B is equipped with an PFM/PWM mode operation. At light load, the IC operates in the PFM mode to reduce the switching losses. At heavy load, the IC works in PWM. At PWM mode, the switching frequency is set by the external resistor.

The APW7153/A/B is also equipped with Power-on-reset, soft-start, soft-stop, and whole protections (under-voltage, over-voltage, over-temperature and current-limit) into a single package.

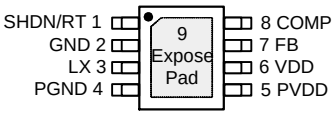
This device, available TDFN3x3-10 and SOP-8P provides a very compact system solution external components and PCB area.

Simplified Application Circuit



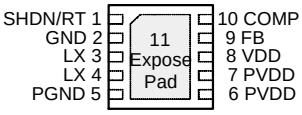
Pin Configuration

APW7153



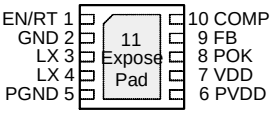
SOP-8P
(Top View)

APW7153



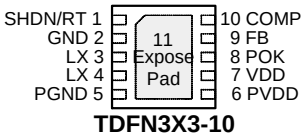
TDFN3X3-10
(Top View)

APW7153A



TDFN3X3-10
(Top View)

APW7153B



TDFN3X3-10
(Top View)

9 The pin 2 and 4 must be connected to the pin 9 (Exposed Pad)

11 The pin 2 and 5 must be connected to the pin 11 (Exposed Pad)

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Rev. A.6 - Aug., 2012

Ordering and Marking Information

APW7153/A/B □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QB : TDFN3x3-10 KA : SOP-8P Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW7153/A/B QB: APW 7153 XXXXX / APW 7153A XXXXX / APW 7153B XXXXX	XXXXX - Date Code
APW7153 KA: APW7153 XXXXX	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter		Rating	Unit
V_{VDD}, V_{PVDD}	Input Supply Voltage		-0.3 ~ 6	V
V_{LX}	LX to GND Voltage	>20ns pulse width	-1 ~V_{PVDD}+0.3	V
		<20ns pulse width	-3 ~V_{PVDD}+3	V
	SHDN/RT, FB, COMP, POK to GND Voltage		-0.3 ~ 6	V
PGND	PGND to GND Voltage		-0.3 ~ +0.3	V
P_D	Power Dissipation		Internally Limited	W
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature		-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds		260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air (Note 2) TDFN3x3-10 SOP-8P	 50 80	°C/W
θ_{JC}	Junction-to-Case Resistance in Free Air (Note 3) TDFN3x3-10 SOP-8P	 10 20	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of TDFN3x3-10 and SOP-8P is soldered directly on the PCB.

Note 3: The case temperature is measured at the center of the exposed pad on the underside of the TDFN3x3-10 and SOP-8P packages.

Recommended Operating Conditions (Note 4)

Symbol	Parameter	Range	Unit
V_{VDD}	Control and Driver Supply Voltage	2.6~ 5.5	V
V_{PVDD}	Input Supply Voltage	1. 5~5.5	V
V_{OUT}	Converter Output Voltage	0.8~5.5	V
I_{OUT}	Converter Output Current	0~3	A
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 4: Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{VDD}=V_{PVDD}=3.3V, T_A= -40 ~ 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions		APW7153/A/B			Unit
				Min.	Typ.	Max.	
SUPPLY CURRENT							
I_{VDD}	VDD Supply Current	V_{FB}=1V		-	460	-	µA
I_{VDD_SDH}	VDD Shutdown Supply Current	SHDN/RT=VDD		-	-	1	µA
I_{VDD_SDL}	VDD Shutdown Supply Current	SHDN/RT=GND		-	-	10	µA
POWER-ON-RESET (POR)							
	VDD POR Voltage Threshold	V_{IN} Rising		2.3	2.4	2.5	V
	VDD Debounce Time			-	100	-	µs
	VDD POR Hysteresis			0.1	0.2	0.3	V
	PVDD POR Voltage Threshold			1.5	1.6	1.7	V
	PVDD POR Debounce			-	10	-	µs
	PVDD POR Hysteresis			-	50	-	mV
REFERENCE VOLTAGE							
V_{REF}	Reference Voltage	Regulated on FB pin	APW7153/B	-	0.8	-	V
			APW7153A	-	0.5	-	
	Output Voltage Accuracy	T_J=25°C, I_{OUT}=10mA, V_{DD}=5V		-0.5	-	+0.5	%
		I_{OUT}=10mA~3A, V_{DD}=2.6~5V		-0.8	-	+0.8	%
OSCILLATOR AND DUTY CYCLE							
F_{OSC}	Oscillator Frequency			0.3	-	2	MHz
	Oscillator Frequency	R_T=332kΩ		0.8	1	1.2	MHz
	Maximum Converter's Duty			-	100	-	%
	Minimum on Time			-	90	-	ns
POWER MOSFET							
	High Side P-MOSFET Resistance	I_{LX}=0.5A, T_A=25°C		-	110	160	mΩ
	Low Side N-MOSFET Resistance	I_{LX}=0.5A, T_A=25°C		-	110	160	mΩ
	High/Low Side MOSFET Leakage Current			-	-	10	µA

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{VDD}=V_{PVDD}=3.3V, T_A= -40 ~ 85 °C. Typical values are at T_A=25°C.

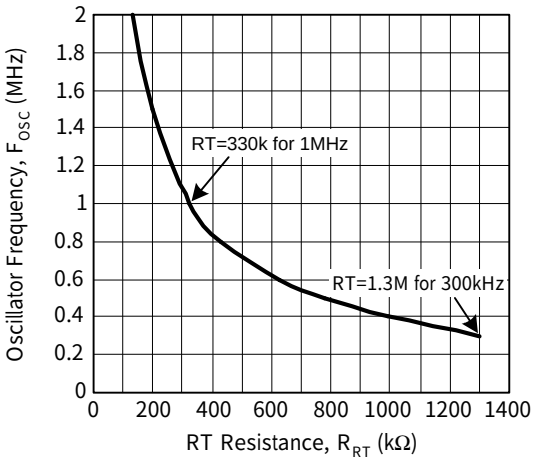
Symbol	Parameter	Test Conditions	APW7153/A/B			Unit
			Min.	Typ.	Max.	
CURRENT-MODE PWM CONVERTER						
Gm	Error Amplifier Transconductance		-	550	-	μA/V
	Error Amplifier DC Gain	COMP=NC	-	80	-	dB
	Current Sense Transresistance		-	500	-	mΩ
T_D	Dead Time (Note 5)		-	20	-	ns
PROTECTIONS						
I_{LIM}	High Side MOSFET Current-Limit	Peak Current	4.0	4.5	5.0	A
T_{OTP}	Over-Temperature Trip Point (Note 5)		-	160	-	°C
	Over-Temperature Hysteresis		-	50	-	°C
	Over-Voltage Protection Threshold		119	125	131	%V_{OUT}
	Under-Voltage Protection Threshold		44	50	56	%
	Low Side MOSFET Current-Limit	From Drain to Source	0.7	-	1.6	A
SOFT-START, ENABLE AND INPUT CURRENTS						
	Soft-Start Time		1	1.5	2	ms
V_{SHDN}	SHDN Shutdown Threshold	V_{SHDN} > SHDN shutdown Threshold, IC shutdown	-	V_{VDD}-0.9	V_{VDD} -0.4	V
	POK Threshold	POK in from Lower (POK Goes High)	85	87.5	90	%V_{OUT}
		POK Low Hysteresis (POK Goes High)	-	5	-	%V_{OUT}
		POK in from Higher (POK Goes High)	110	112.5	115	%V_{OUT}
		POK High Hysteresis (POK Goes Low)	-	5	-	%V_{OUT}
	Power Good Pull Low Resistance		-	100	-	Ω
	Power Good Debounce		-	0.5	-	ms

Note 5: Guarantee by design.

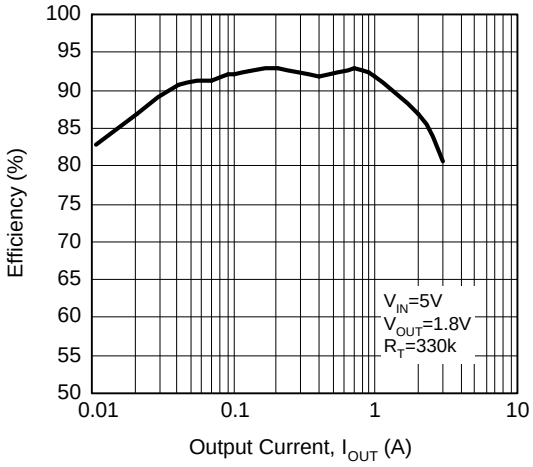
Typical Operating Characteristics

Refer to the application circuit in the section "Typical Application Circuits", V_{IN}=5V, T_A=25°C, unless otherwise specified.

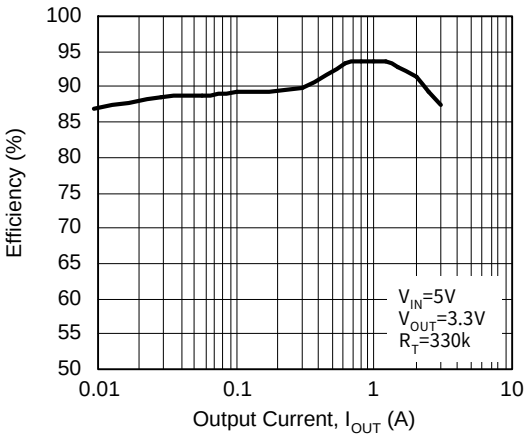
Oscillator Frequency vs. RT Resistance



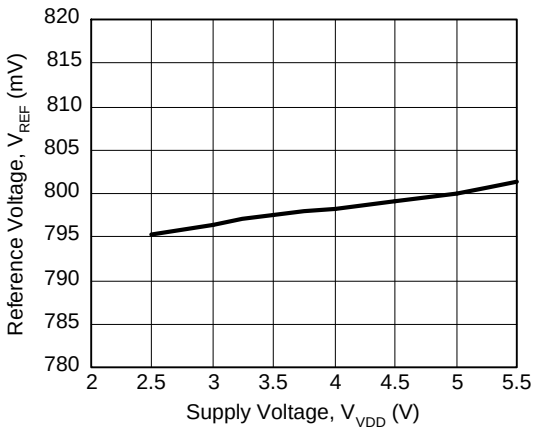
Efficiency vs. Output Current



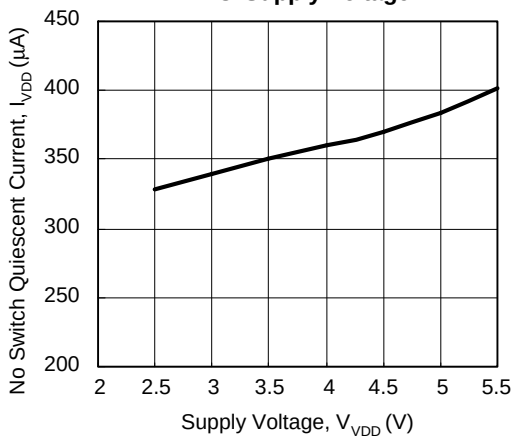
Efficiency vs. Output Current



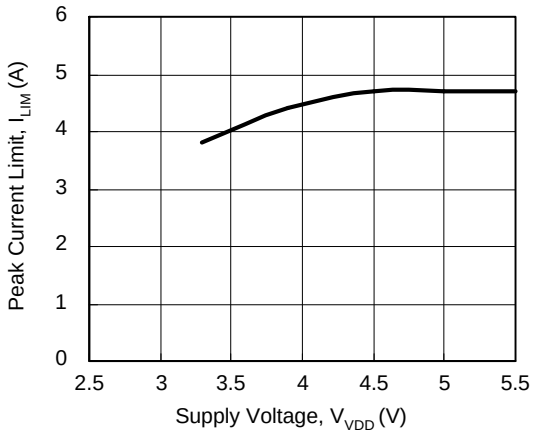
Reference Voltage vs. Supply Voltage



No Switch Quiescent Current vs. Supply Voltage

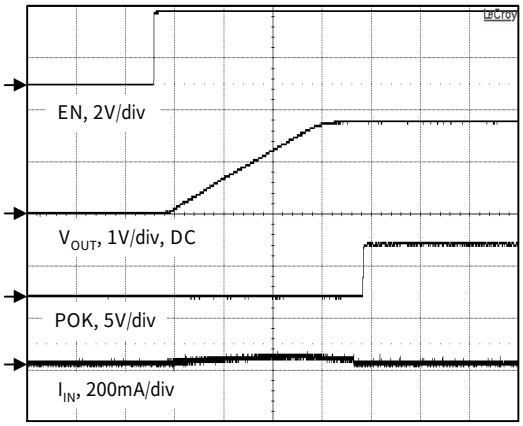


Peak Current-Limit vs. Supply Voltage

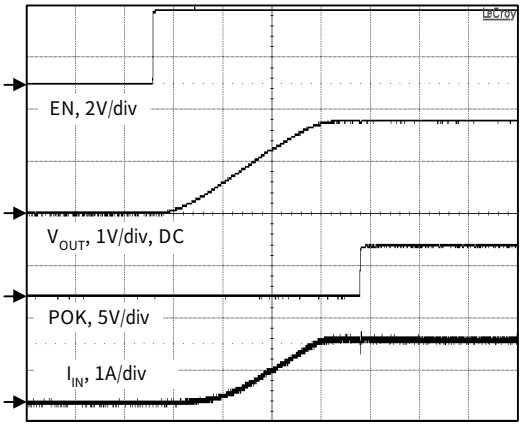


Operating Waveforms

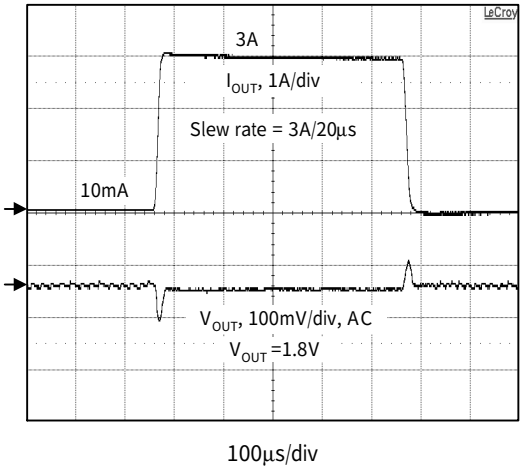
Start-up with No Load



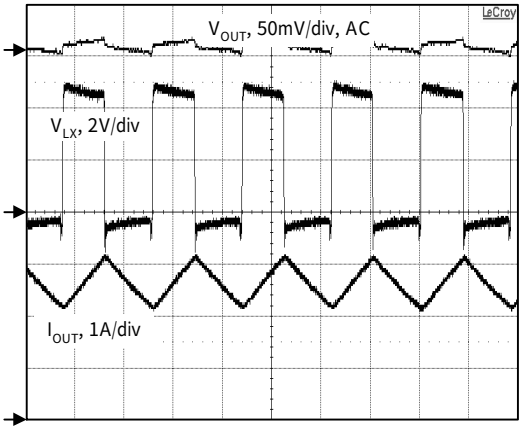
Start-up with 3A Load



Load Transient Response



Normal Operating

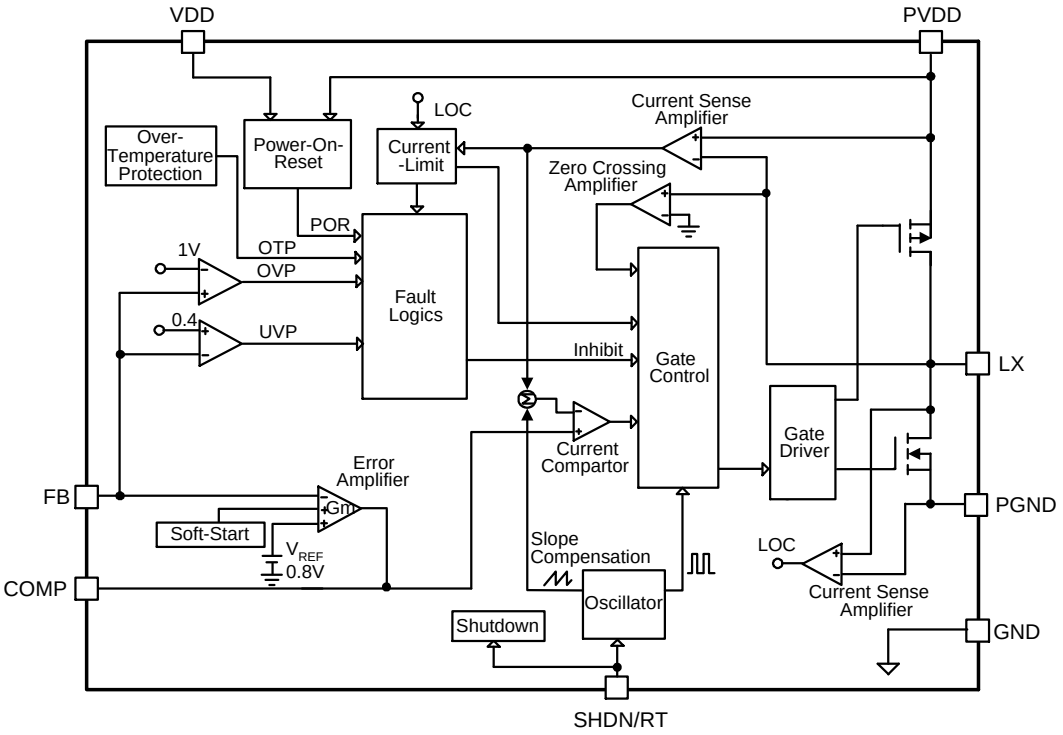


Pin Description

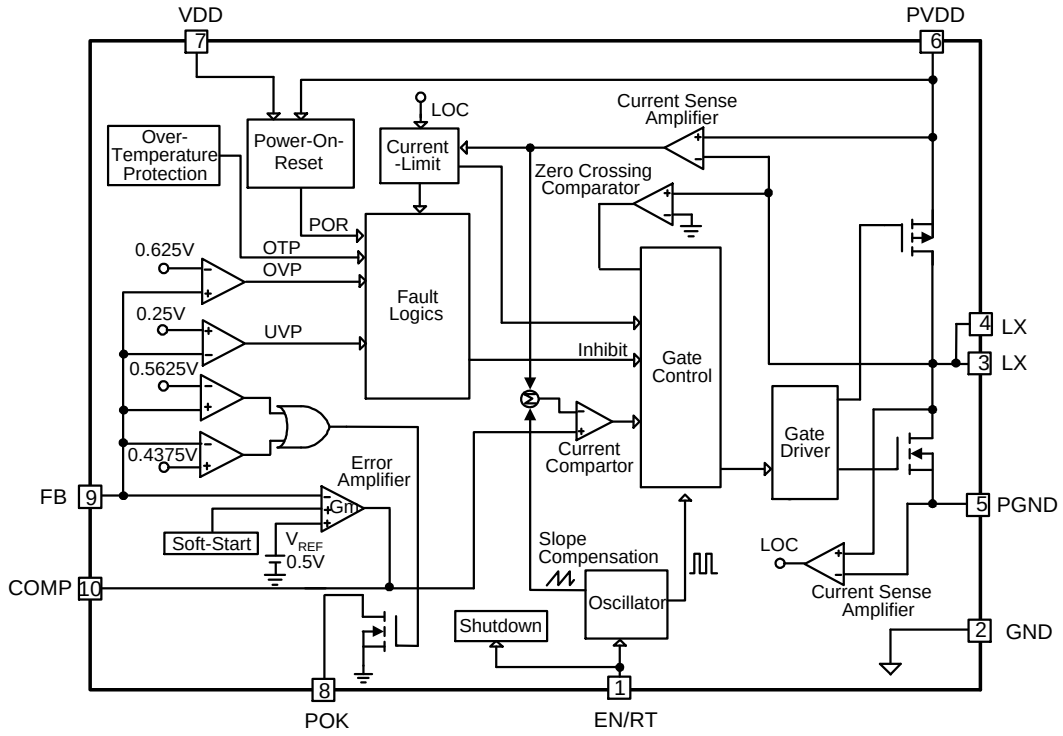
PIN				NAME	FUNCTION
TDFN3x3-10			SOP-8P		
APW7153	APW7153A	APW7153B	APW7153		
1	-	1	1	SHDN/RT	Shutdown/Enable and Oscillator Input. Connecting a resistor to GND sets the switching Frequency. Pull the pin to VDD to shut down the device. Do leave the pin floating.
-	1	-	-	EN/RT	Shutdown/Enable and Oscillator Input. Connecting a resistor to VDD sets the switching Frequency. Pull the pin to GND to shut down the device. Do leave the pin floating.
2	2	2	2	GND	Signal Ground. Ground of MOSFET Gate Drivers and Control Circuitry.
3, 4	3, 4	3, 4	3	LX	Power Switching Output. LX is the Junction of the high-side and low-side Power MOSFETs to supply power to the output LC filter.
5	5	5	4	PGND	Power Ground. The Source of the N-channel power MOSFET. Connect this pin to the system ground with lowest impedance.
6, 7	6	6	5	PVDD	Power Input. PVDD supplies the step-down converter switches. Connecting a ceramic bypass capacitor from PVDD to PGND to eliminate switching noise and voltage ripple on the input to the IC.
8	7	7	6	VDD	Control circuitry supply Input. VDD supplies the control circuitry, gate drivers. Connecting a ceramic bypass capacitor from VDD to GND to eliminate switching noise and voltage ripple on the input to the IC.
-	8	8	-	POK	Power Good Output. This pin is open-drain logic output that is pulled to ground when the output voltage is not within ±12.5% of regulation point.
9	9	9	7	FB	Output Feedback Input. The APW7153/A senses the feedback voltage via FB and regulates the voltage at 0.8V. Connecting FB with a resistor-divider from the converter's output sets the output voltage.
10	10	10	8	COMP	Output of the error amplifier. Connect a series RC network from COMP to GND to compensate the regulation control loop. In some cases, an additional capacitor from COMP to GND is required.
11	11	11	9	Exposed Pad	Connect the exposed pad to the system ground plan with large copper area for dissipating heat into the ambient air.

Block Diagram

APW7153

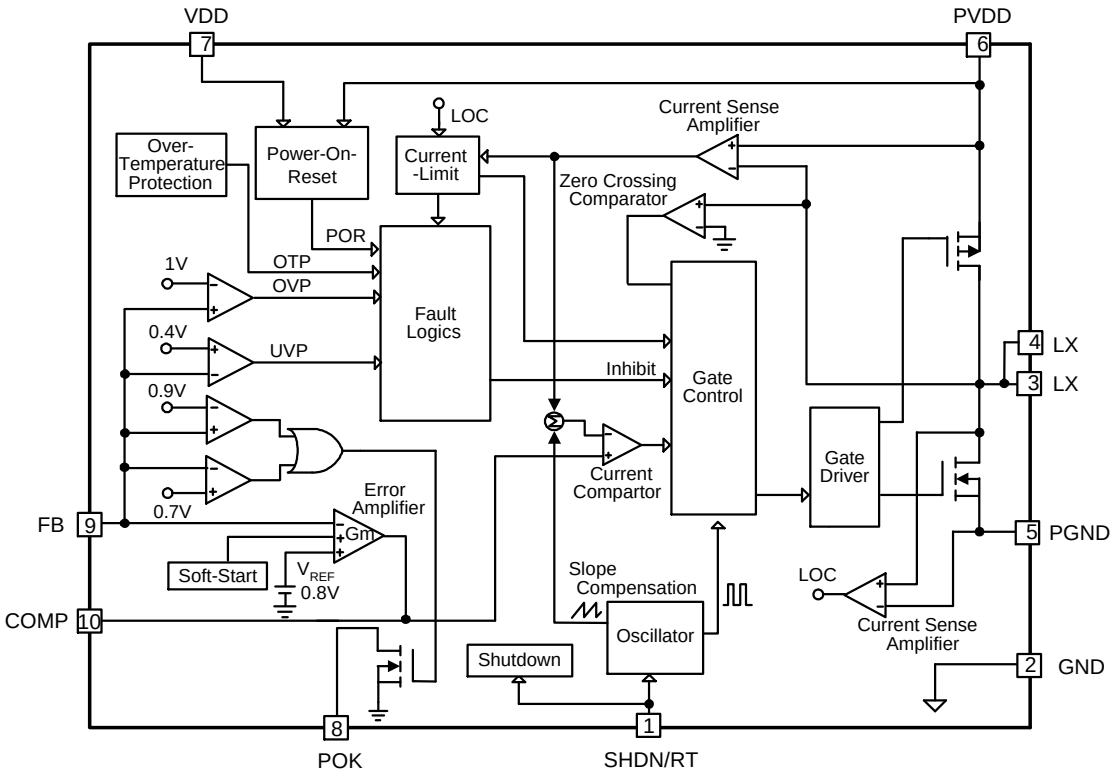


APW7153A

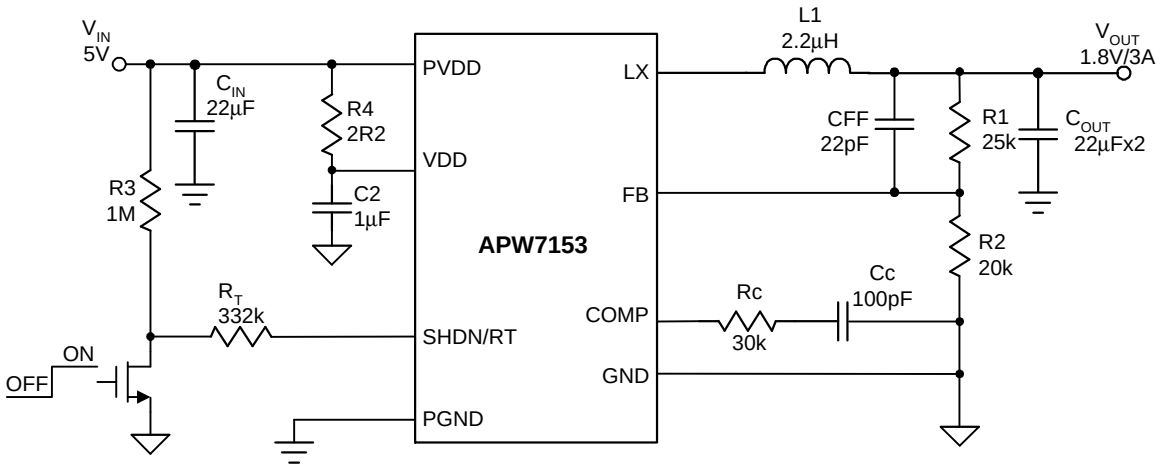


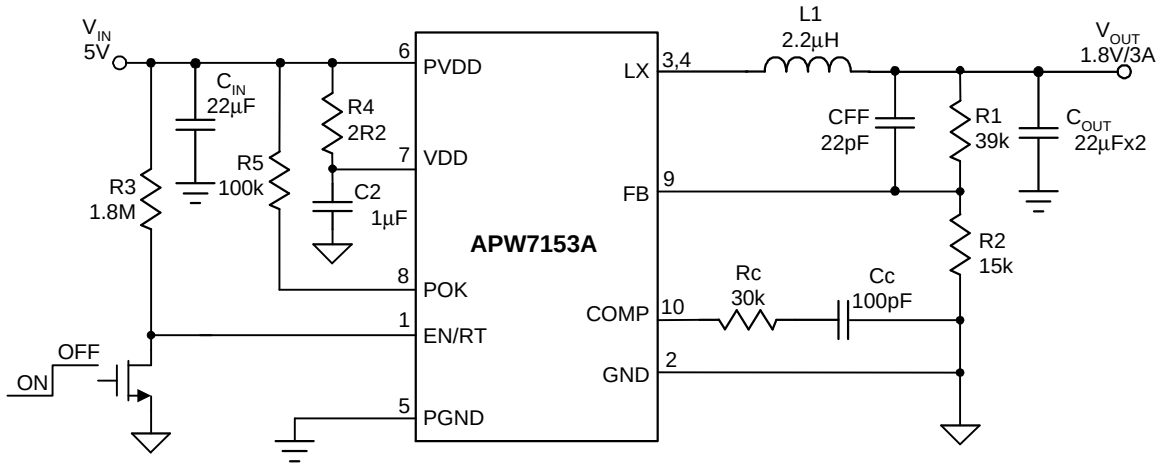
Block Diagram

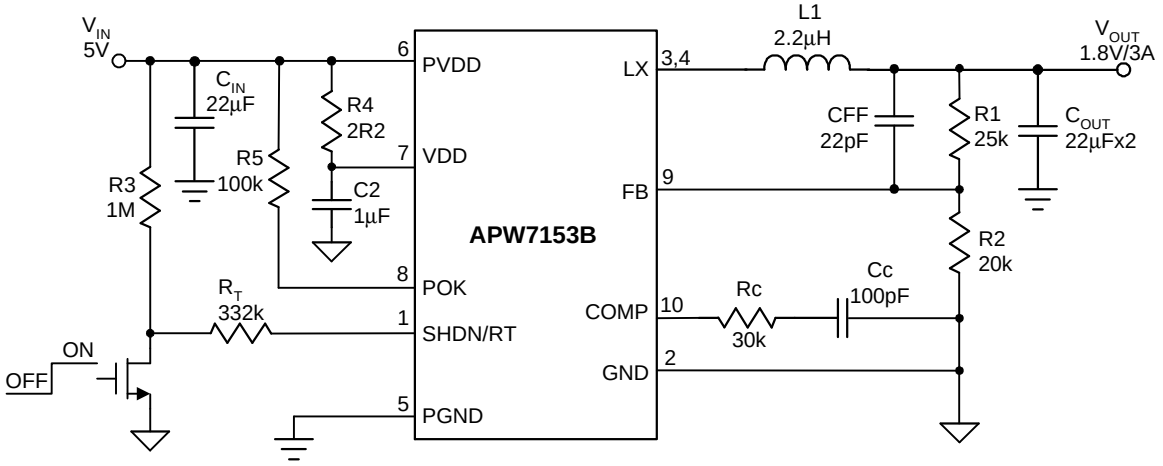
APW7153B



Typical Application Circuit







Function Description

VDD and PVDD Power-On-Reset (POR)

The APW7153/A/B keeps monitoring the voltage on VDD and PVDD pins to prevent wrong logic operations which may occur when VDD or PVDD voltage is not high enough for internal control circuitry to operate. The VDD POR rising threshold is 2.4V (typical) with 0.2V hysteresis and PVDD POR rising threshold is 1.7V with 0.05V hysteresis. During start-up, the VDD and PVDD voltage must exceed the enable voltage threshold. Then, the IC starts a start-up process and ramps up the output voltage to the voltage target.

Output Under-Voltage Protection (UVP)

In the operational process, if a short-circuit occurs, the output voltage will drop quickly. Before the current-limit circuit responds, the output voltage will fall out of the required regulation range. The under-voltage continually monitors the FB voltage after soft-start is completed. If a load step is strong enough to pull the output voltage lower than the under-voltage threshold, the IC shuts down converter's output.

The under-voltage threshold is 50% of the nominal output voltage. The under-voltage comparator has a built-in 3µs noise filter to prevent the chips from wrong UVP shutdown being caused by noise. APW7153/A/B will be latched after under-voltage protection.

Over-Voltage Protection (OVP)

The over-voltage function monitors the output voltage by FB pin. When the FB voltage increases over 125% of the reference voltage due to the high-side MOSFET failure or for other reasons, the over-voltage protection comparator will force the low-side MOSFET gate driver to be high. This action actively pulls down the output voltage and eventually attempts to blow the internal bonding wires. As soon as the output voltage is within regulation, the OVP comparator is disengaged. The chip will restore its normal operation.

Over-Temperature Protection (OTP)

The over-temperature circuit limits the junction temperature of the APW7153/A/B. When the junction temperature exceeds T_J=+160°C, a thermal sensor turns off the both power MOSFETs, allowing the devices to cool. The thermal sensor allows the converters to start a start-up process and to regulate the output voltage again after the junction temperature cools by 50°C. The OTP is designed with a 50°C hysteresis to lower the average T_J during continuous thermal overload conditions, increasing lifetime of the APW7153/A/B.

Current-Limit Protection

The APW7153/A/B monitors the output current, flows through the high-side and low-side power MOSFETs, and limits the current peak at current-limit level to prevent the IC from damaging during overload, short-circuit, and over-voltage conditions. Typical high side power MOSFET current-limit is 4.5A, and low side MOSFET current-limit is 1.6A maximum.

Soft-Start

The APW7153/A/B has a built-in soft-start to control the rise rate of the output voltage and limit the input current surge during start-up. During soft-start, an internal voltage ramp connected to one of the positive inputs of the error amplifier, rises up from 0V to 0.95V to replace the reference voltage, V_{REF} until the voltage ramp reaches the reference voltage. During soft-start without output over-voltage, the APW7153/A/B converter's sinking capability is disabled until the output voltage reaches the voltage target.

Soft-Off

At the moment of shutdown controlled by SHDN/RT signal, under-voltage event or over-temperature protection, the APW7153/A/B initiates a soft-stop process to discharge the output voltage in the output capacitors. Certainly, the load current also discharges the output voltage. During soft-stop, the internal voltage ramp (V_{RAMP}) falls down rises from 0.95V to 0V to replace the reference voltage. Therefore, the output voltage falls down slowly at the light load. After the soft-stop interval elapses, the soft-stop process ends and the IC turns on the low-side power MOSFET.

Function Description (Cont.)

Switching Frequency and Shutdown/Enable

The SHDN/RT pin is a multi-function pin that is used to control the switching frequency and Shutdown/Enable function of APW7153/A/B. The switching frequency is set by the external resistor that is connected between SHDN/RT and GND. The value of the resistor sets the ramp current that is used to charge and discharge an internal timing capacitor within the oscillator.

The SHDN/RT pin also provides Shutdown/Enable function. Pulling the pin to VDD or GND, APW7153/A/B initiates a soft-stop process and shutdown the IC.

Power Good Indicator (APW7153A/B)

POK is actively held low in shutdown and soft-start status. In the soft-start process, the POK is an open-drain. When the soft-start is finished, the POK is released. In normal operation, the POK window is from 87.5% to 112.5% of the converter reference voltage. When the output voltage has to stay within this window, POK signal will become high after 0.5ms internal delay. When the output voltage outruns 85% or 115% of the target voltage, POK signal will be pulled low immediately. In order to prevent false POK drop, capacitors need to parallel at the output to confine the voltage deviation with severe load step transient.

Application Information

Input Capacitor Selection

Because buck converters have a pulsating input current, a low ESR input capacitor is required. This results in the best input voltage filtering, minimizing the interference with other circuits caused by high input voltage spikes. Also, the input capacitor must be sufficiently large to stabilize the input voltage during heavy load transients. For good input voltage filtering, usually a 22µF input capacitor is sufficient. It can be increased without any limit for better input voltage filtering. Ceramic capacitors show better performance because of the low ESR value, and they are less sensitive against voltage transients and spikes compared to tantalum capacitors. Place the input capacitor as close as possible to the input and GND pin of the device for better performance.

Inductor Selection

For high efficiencies, the inductor should have a low dc resistance to minimize conduction losses. Especially at high-switching frequencies the core material has a higher impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. A reasonable starting point for setting ripple current, $\Delta I_{L,}$ is 40% of maximum output current. The recommended inductor value can be calculated as below:

$$L \geq \frac{V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right)}{F_{SW}\cdot \Delta I_L}$$

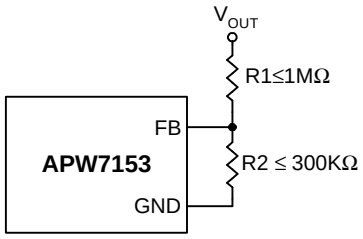
$$I_{L(MAX)} = I_{OUT(MAX)} + 1/2 \times \Delta I_L$$

To avoid saturation of the inductor, the inductor should be rated at least for the maximum output current of the converter plus the inductor ripple current.

Output Voltage Setting

In the adjustable version, the output voltage is set by a resistive divider. The external resistive divider is connected to the output, allowing remote voltage sensing as shown in "Typical Application Circuits". A suggestion of maximum value of R2 is 300kΩ to keep the minimum current that provides enough noise rejection ability through the resistor divider. The output voltage can be calculated as below:

$$V_{OUT} = V_{REF}\cdot\left(1+\frac{R1}{R2}\right)$$

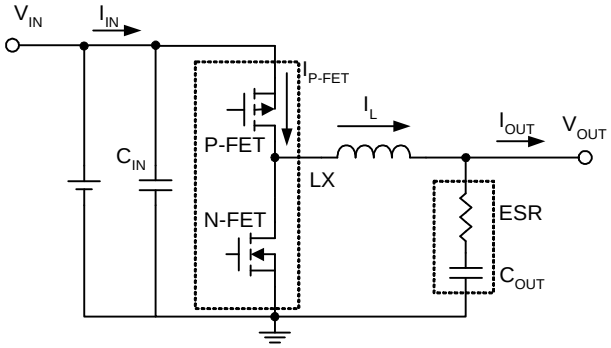


Output Capacitor Selection

The current-mode control scheme of the APW7153 allows the use of tiny ceramic capacitors. The higher capacitor value provides the good load transients response. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. If required, tantalum capacitors may be used as well. The output ripple is the sum of the voltages across the ESR and the ideal output capacitor.

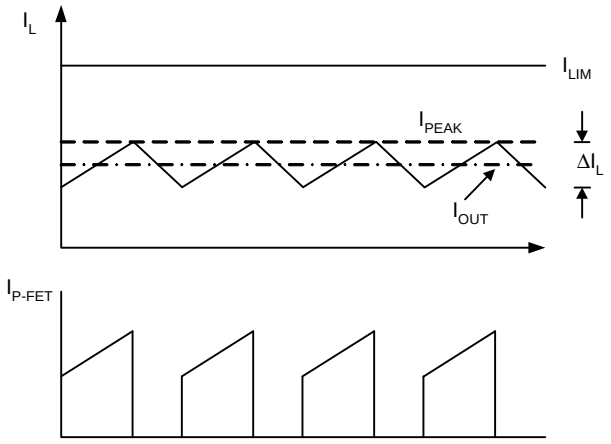
$$\Delta V_{OUT} \cong \frac{V_{OUT}\cdot\left(1-\frac{V_{OUT}}{V_{IN}}\right)}{F_{SW}\cdot L}\cdot\left(ESR+\frac{1}{8\cdot F_{SW}\cdot C_{OUT}}\right)$$

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.



Application Information (Cont.)

Output Capacitor Selection (Cont.)



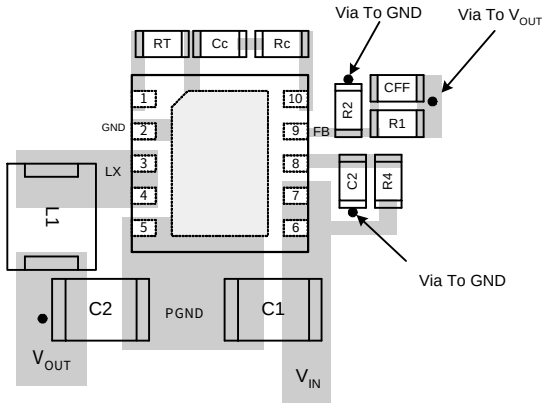


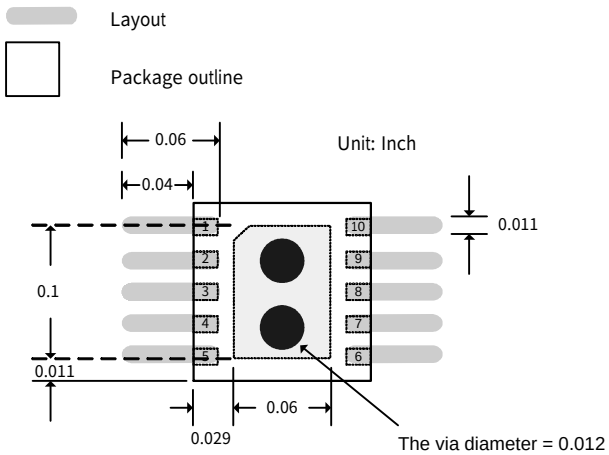
Figure 1. APW7153/A/B Layout Suggestion

Layout Considerations

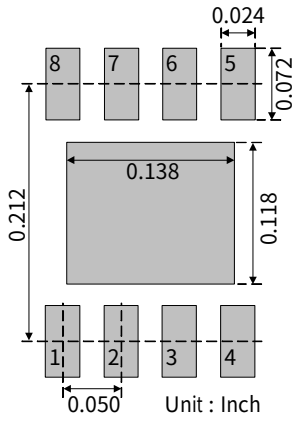
For all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

1. The input capacitor should be placed close to the PVDD and GND. Connect the capacitor and PVDD/GND with short and wide trace without any via holes for good input voltage filtering. The distance between PVDD/GND to capacitor less than 2mm respectively is recommended.
2. To minimize copper trace connections that can inject noise into the system, the inductor should be placed as close as possible to the LX pin to minimize the noise coupling into other circuits.
3. The output capacitor should be place closed to VOUT and GND.
4. Keep the sensitive small signal nodes (FB, COMP) away from switching nodes (LX) on the PCB. Therefore place the feedback divider and the feedback compensation network close to the IC to avoid switching noise. Connect the ground of feedback divider directly to the GND pin of the IC using a dedicated ground trace.
5. A star ground connection or ground plane minimizes ground shifts and noise is recommended.

Recommended Minimum Footprint



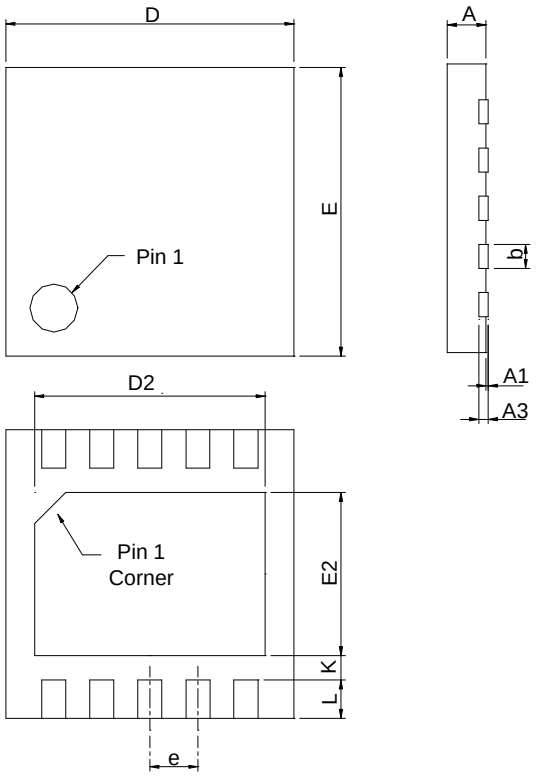
TDFN3x3-10



SOP-8P

Package Information

TDFN3x3-10

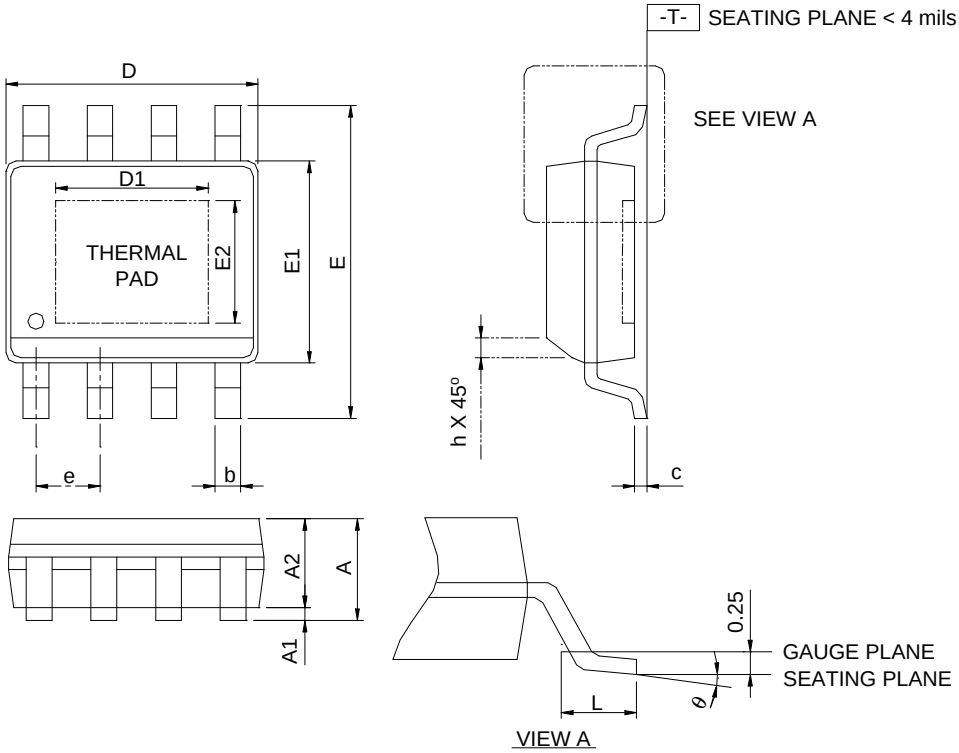


SYMBOL	TDFN3x3-10			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
D2	2.20	2.70	0.087	0.106
E	2.90	3.10	0.114	0.122
E2	1.40	1.75	0.055	0.069
e	0.50 BSC		0.020 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	

Note : 1. Followed from JEDEC MO-229 VEED-5.

Package Information

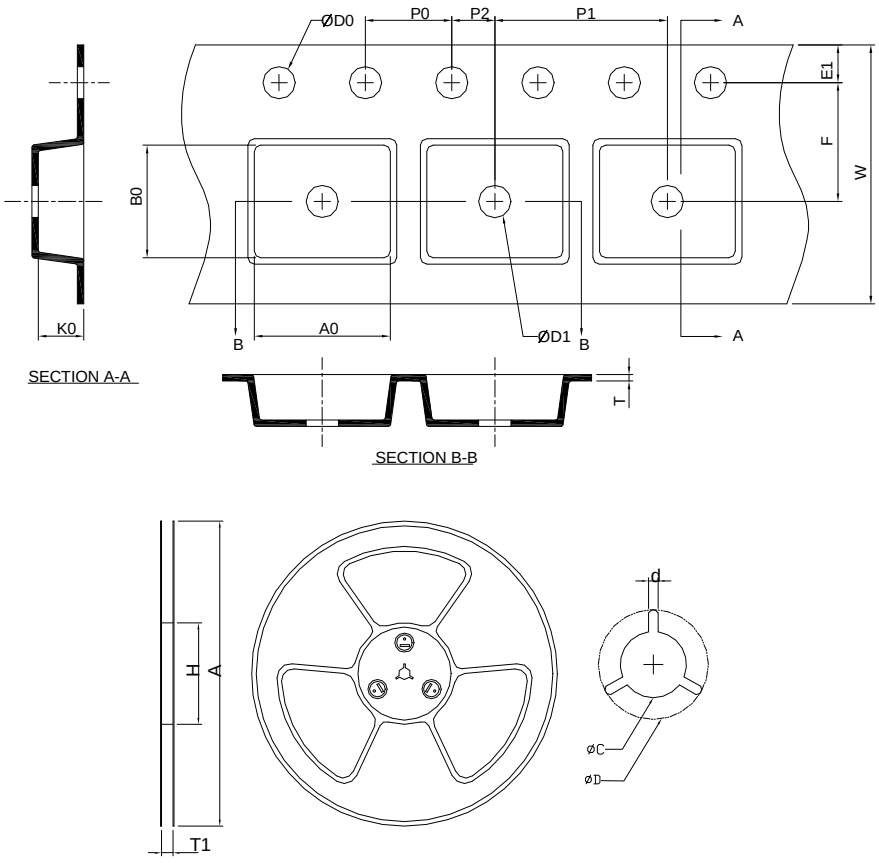
SOP-8P



SYMBOL	SOP-8P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.60		0.063
A1	0.00	0.15	0.000	0.006
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
D1	2.50	3.50	0.098	0.138
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
E2	2.00	3.00	0.079	0.118
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°C	8°C	0°C	8°C

Note : 1. Followed from JEDEC MS-012 BA.
2. Dimension "D" does not include mold flash, protrusions or gate burrs.
Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
3. Dimension "E" does not include inter-lead flash or protrusions.
Inter-lead flash and protrusions shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TDFN3x3-10	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.30±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
SOP-8P	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20

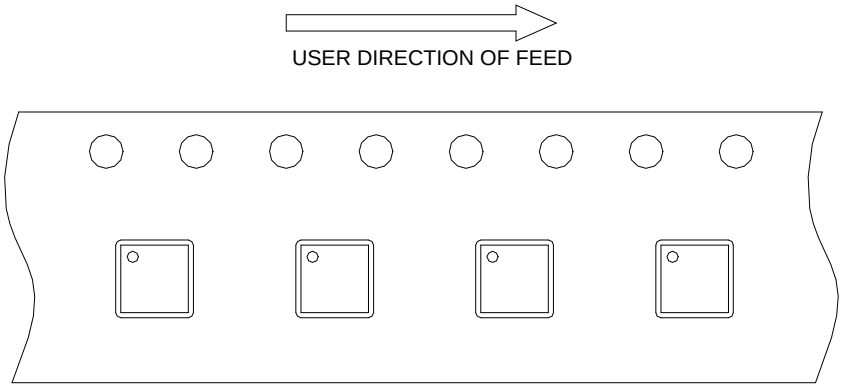
(mm)

Devices Per Unit

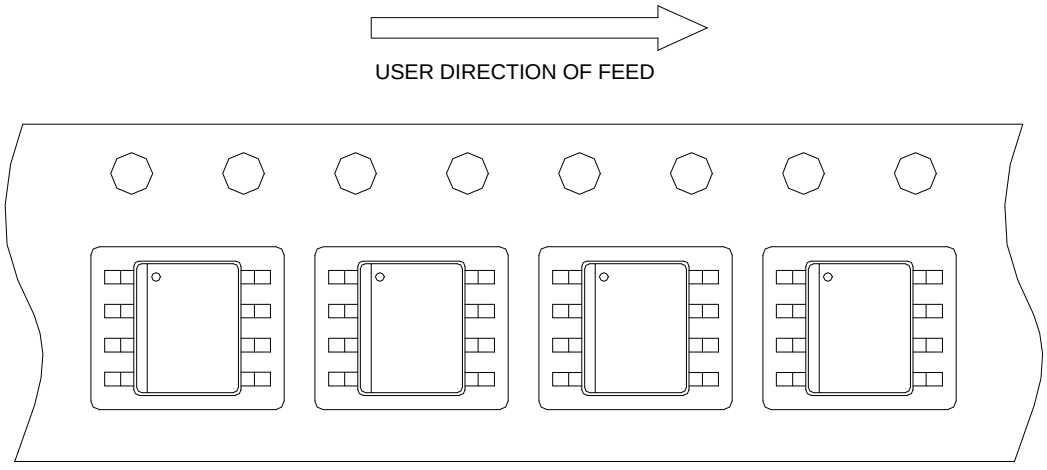
Package Type	Unit	Quantity
TDFN3x3-10	Tape & Reel	3000
SOP-8P	Tape & Reel	2500

Taping Direction Information

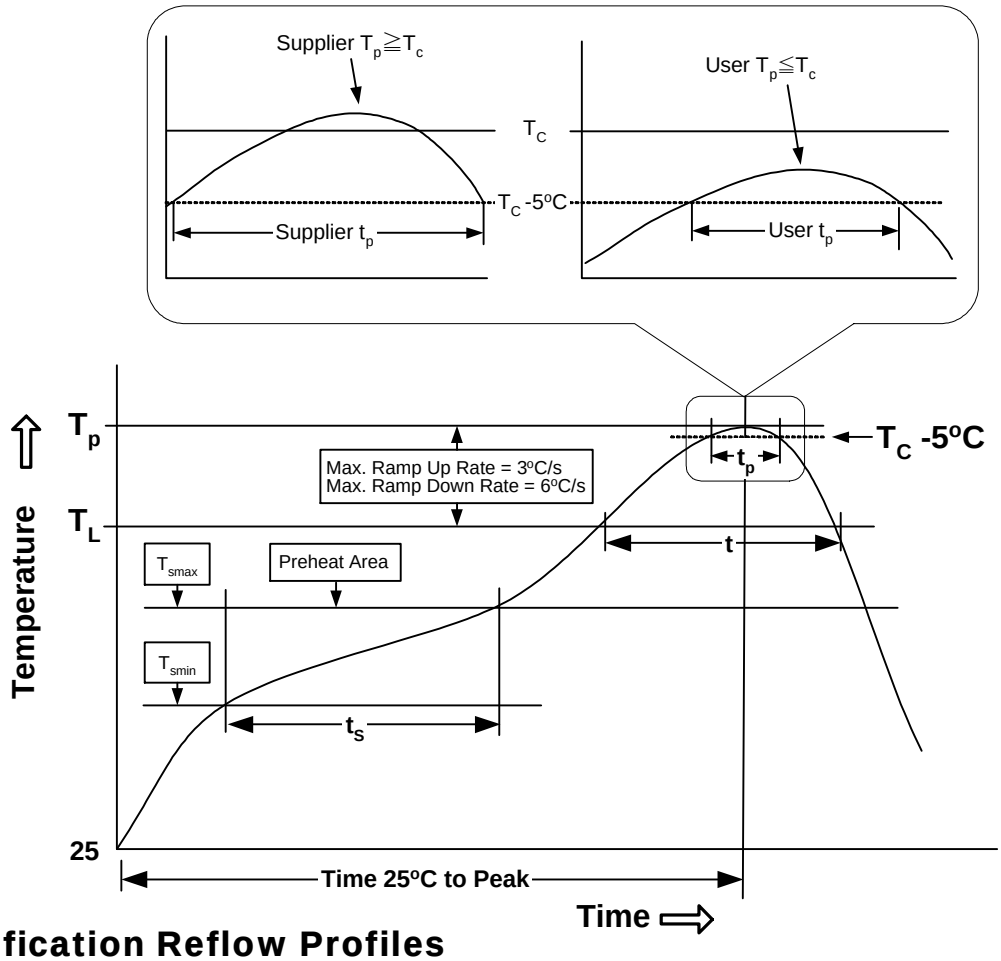
TDFN3x3-10



SOP-8P



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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