5V to 12V Single Synchronous Buck PWM and Linear Controller

Features

- **Provides Two Regulated Voltages**
  - **Synchronous Buck Converter**
  - **Linear Controller**
- **Wide 5V to 12V Supply Voltage**
  Excellent Output Voltage Regulations
  - **0.8V Internal Reference**
  - **±1% Over Line Voltage and Temperature**
- **Integrated Soft-Start for PWM and Linear Outputs**
- **Selectable Forced PWM and PSM/PWM Modes**
- **Programmable Frequency Range from 150kHz to 600kHz**
- **Voltage Mode PWM Operation with Up to 75% (Typ.) Duty Cycle**
- **Under-Voltage Protections for PWM and Linear Regulator Outputs**
- **Adjustable Over-Current Protection Threshold for PWM Converter**
  - **Using the $R_{DS(ON)}$ of Low-Side MOSFET**
- **Over-Voltage Protection for PWM Output**
- **SOP-14 Package**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **Graphic Cards**

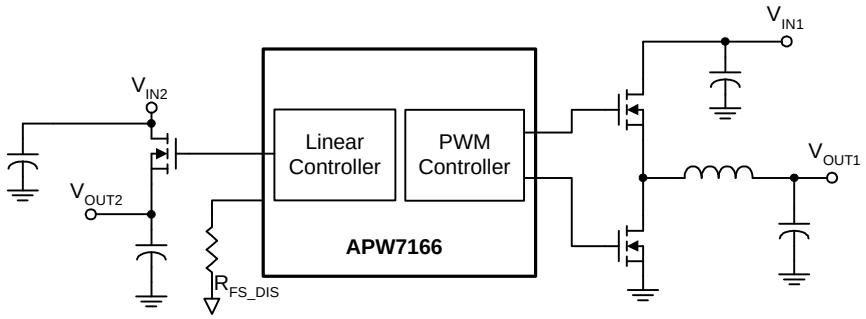
General Description

The APW7166 integrates a synchronous buck PWM and linear controller, as well as monitoring and protection functions into a single package.

The APW7166 allows wide input voltage that is either a single 5~12V or two supply voltage(s) for various applications. A power-on-reset (POR) circuit monitors the VCC supply voltage to prevent wrong logic controls. A built-in digital soft-start circuit prevents the output voltages from overshoot as well as limits the input current. An internal 0.8V temperature-compensated reference voltage with high accuracy is designed to meet the requirement of low output voltage applications. The APW7166 provides excellent output voltage regulations against load current variation. An adjustable oscillator with frequency range from 150kHz to 600kHz provides more flexibility in choosing external components that balance cost and efficiency. The PWM controller's over-current protection monitors the output current by using the voltage drop across the $R_{DS(ON)}$ of low-side MOSFET, eliminating the need for a current sensing resistor that features high efficiency and low cost. The APW7166 also integrates an Over-Voltage Protection (OVP) circuit which monitors the FB voltage to prevent the PWM output from over voltage.

The APW7166 is available in a SOP-14 package.

Simplified Application Circuit

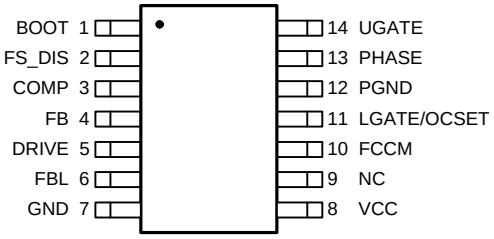


Ordering and Marking Information

APW7166 □□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code K : SOP-14 Operating Ambient Temperature Range E : -20 to 70°C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW7166 K : 	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Pin Configuration



SOP-14
(Top View)

Absolute Maximum Ratings (Note 1)

Symbol	Parameter		Rating	Unit
V_{VCC}	VCC Supply Voltage (VCC to GND)		-0.3 ~ 16	V
V_{BOOT}	BOOT to PHASE Voltage		-0.3 ~ 16	V
V_{UGATE}	UGATE to PHASE Voltage	> 400ns	-0.3 ~ V_{BOOT}+0.3	V
		< 400ns	-5 ~ V_{BOOT}+5	V
V_{LGATE}	LGATE to PGND Voltage	> 400ns	-0.3 ~ V_{VCC}+0.3	V
		< 400ns	-5 ~ V_{VCC}+5	V
V_{PHASE}	PHASE to GND Voltage	> 200ns	-0.3 ~ 16	V
		< 200ns	-10 ~ 30	V
V_{DRIVE}	DRIVE to GND Voltage		-0.3 ~ V_{VCC}	V
	FB, FBL, COMP, FS_DIS and FCCM to GND (< V_{VCC} + 0.3V)		-0.3 ~ 7	V
	PGND to GND Voltage		-0.3 ~ 0.3	V
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature		-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds		260	°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Thermal Resistance -Junction to Ambient (Note 2) SOP-14	90	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{VCC}	VCC Supply Voltage (VCC to GND)	4.5 ~ 13.2	V
V_{OUT}	Buck Converter Output Voltage	0.9 ~ 5	V
V_{IN}	Buck Converter Input Voltage	2.9 ~ V_{VCC}	V
F_{OSC}	Oscillator Frequency	150 ~ 600	kHz
I_{OUT}	Buck Converter Output Current	0 ~ 30	A
T_A	Ambient Temperature	-20 ~ 70	°C
T_J	Junction Temperature	-20 ~ 125	°C

Note 3: Refer to the application circuit for further information

Electrical Characteristics

Refer to the typical application circuit. These specifications apply over V_{VCC} = 12V, T_A = -20°C to 70°C unless otherwise noted. Typical values are at T_A = 25°C.

Symbol	Parameter	Test Conditions	APW7166			Unit
			Min.	Typ.	Max.	
INPUT SUPPLY VOLTAGE AND CURRENT						
I_{VCC}	VCC Supply Current (Shutdown Mode)	UGATE, LGATE and DRIVE open; FS_DIS=GND	-	4	6	mA
	VCC Supply Current	UGATE, LGATE and DRIVE open; F_{OSC}=600kHz	-	6	-	mA
POWER-ON-RESET						
	Rising VCC Threshold		3.8	4.1	4.4	V
	Hysteresis		0.3	0.45	0.6	V
OSCILLATOR						
	Accuracy		-15	-	15	%
F_{OSC}	Oscillator Frequency	R_{FS_DIS} = 110 kΩ	255	300	345	kHz
ΔV_{OSC}	Oscillator Sawtooth Amplitude	(1.2V~2.7V typical)	-	1.5	-	V
	Shutdown Threshold of R_{FS_DIS}		-	-	1	kΩ
D_{MAX}	Maximum Duty Cycle		-	75	-	%
REFERENCE						
V_{REF}	Reference Voltage	T_A = -20 ~ 70°C	0.792	0.8	0.808	V
	PWM Controller Load Regulation (Note 4)	I_{OUT1} = 0 ~ 10A	-	-	0.2	%
	Linear Controller Load Regulation (Note 4)	I_{OUT2} = 0 ~ 3A	-	-	0.2	%

Electrical Characteristics (Cont.)

Refer to the typical application circuit. These specifications apply over V_{VCC} = 12V, T_A = -20°C to 70°C unless otherwise noted. Typical values are at T_A = 25°C.

Symbol	Parameter	Test Conditions	APW7166			Unit
			Min.	Typ.	Max.	
PWM ERROR AMPLIFIER 1						
gm	Transconductance		-	667	-	µA/V
	FB Input Leakage Current	V_{FB} = 0.8V	-	0.1	1	µA
V_{COMP}	COMP High Voltage	R_L = 10kΩ to GND	-	3	-	V
	COMP Low Voltage	R_L = 10kΩ to GND	-	0.3	-	
I_{COMP}	Maximum COMP Source Current	V_{COMP} = 2V	-	120	-	µA
	Maximum COMP Sink Current	V_{COMP} = 2V	-	120	-	
PWM ERROR AMPLIFIER 2						
	Open-Loop Gain (Note 4)	R_L = 10kΩ, C_L =10pF	-	93	-	dB
	Open-Loop Bandwidth (Note 4)	R_L = 10kΩ, C_L = 10pF	-	20	-	MHz
	Slew Rate (Note 4)	R_L = 10kΩ, C_L = 10pF	-	8	-	V/µs
	FB Input Leakage Current	V_{FB} = 0.8V	-	0.1	1	µA
V_{COMP}	COMP High Voltage	R_L = 10kΩ to GND	-	3	-	V
	COMP Low Voltage	R_L = 10kΩ to GND	-	0.3	-	
I_{COMP}	Maximum COMP Source Current	V_{COMP} = 2V	-	12	-	mA
	Maximum COMP Sink Current	V_{COMP} = 2V	-	12	-	
GATE DRIVERS						
I_{UGATE}	High-side Gate Driver Source Current	V_{BOOT}= 12V, $V_{UGATE-PHASE}$ = 2V	-	2.0	-	A
	High-side Gate Driver Sink Current	V_{BOOT}= 12V, $V_{UGATE-PHASE}$ = 2V	-	0.8	-	
I_{LGATE}	Low-side Gate Driver Source Current	V_{VCC} = 12V, V_{LGATE} = 2V	-	2.0	-	A
	Low-side Gate Driver Sink Current	V_{VCC} = 12V, V_{LGATE} = 2V	-	1.6	-	
T_D	Dead-time (Note 4)		20	30	-	ns
LINEAR-REGUALTOR CONTROLLER						
	Open-Loop Gain (Note 4)	R_L = 10kΩ, C_L =10pF	-	70	-	dB
	Open-Loop Bandwidth (Note 4)	R_L = 10kΩ, C_L =10pF	-	2	-	MHz
	Slew Rate (Note 4)	R_L = 10kΩ, C_L =10pF	-	6	-	V/µs
	FBL Input Current	V_{FBL} = 0.8V	-	0.1	1	µA
	DRIVE High Voltage	R_L = 10kΩ to GND	-	V_{VCC} - 0.3	-	V
	DRIVE Low Voltage	R_L = 10kΩ to GND	-	0	-	V
	Maximum DRIVE Source Current	V_{DRIVE} = 5V	-	4	-	mA
	Maximum DRIVE Sink Current	V_{DRIVE} = 5V	-	3	-	mA
PROTECTIONS						
V_{FB_UV}	FB Under-Voltage Protection Trip Point	Percentage of V_{REF}	-	50	-	%
V_{FBL_UV}	FBL Under-Voltage Protection Trip Point	Percentage of V_{REF}	-	50	-	%
V_{FB_OV}	FB Over-Voltage Protection Trip Point	V_{FB} rising	-	120	-	%
	FB Over-Voltage Protection Hysteresis		-	5	-	%

Electrical Characteristics (Cont.)

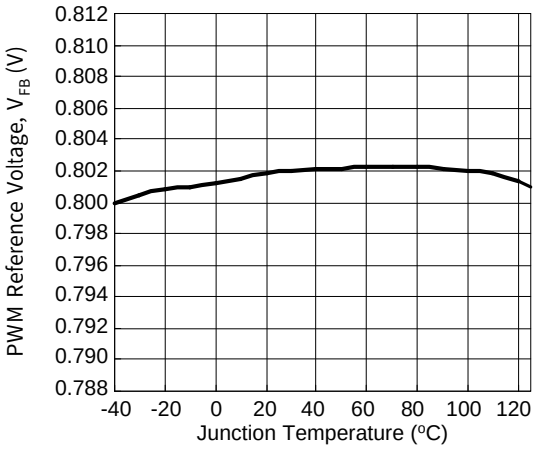
Refer to the typical application circuit. These specifications apply over V_{VCC} = 12V, T_A = -20°C to 70°C unless otherwise noted. Typical values are at T_A = 25°C.

Symbol	Parameter	Test Conditions	APW7166			Unit
			Min.	Typ.	Max.	
PROTECTIONS (CONT.)						
V_{OCP_MAX}	Built-in Maximum OCP Voltage		300	-	-	mV
I_{OCSET}	OCSET Current Source		19.5	21.5	23.5	µA
FORCED-PWM CONTROL PIN INPUT						
$V_{FCCMTHR}$	FCCM High-Level Input Voltage		2	-	-	V
$V_{FCCMTHF}$	FCCM Low-Level Input Voltage		-	-	0.8	V
SOFT-START						
T_{SS}	Internal Soft-Start Interval (Note 4)	F_{OSC} = 600kHz	-	1.05	-	ms
		F_{OSC} = 300kHz	-	2.1	-	ms

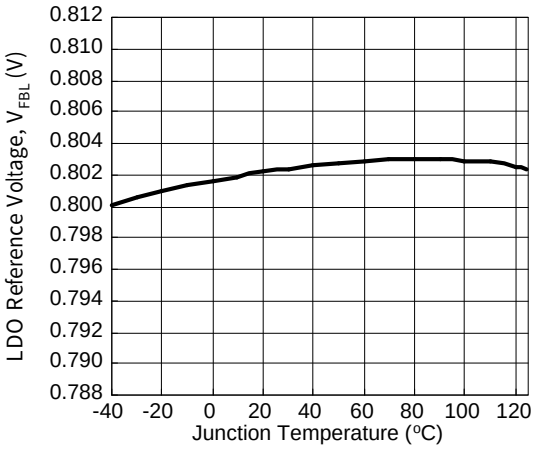
Note 4: Guaranteed by design, not production tested.

Typical Operating Characteristics

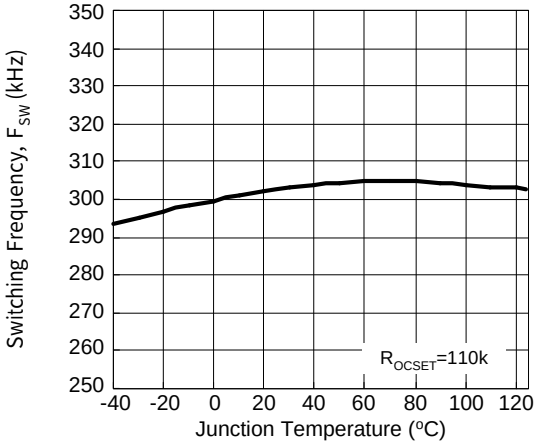
PWM Reference Voltage vs. Junction Temperature



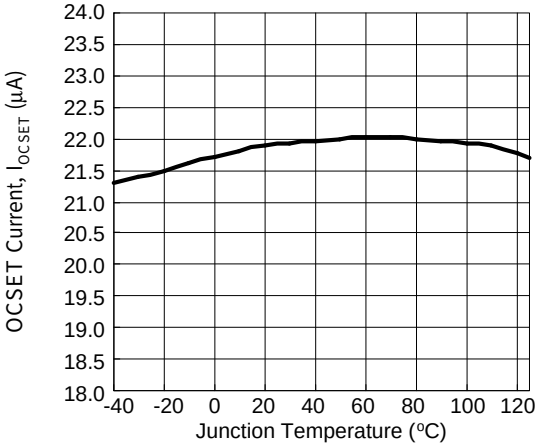
LDO Reference Voltage vs. Junction Temperature



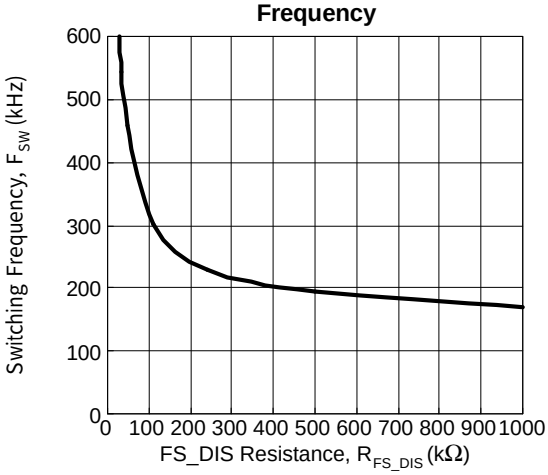
Switching Frequency vs. Junction Temperature



OCSET Current vs. Junction Temperature

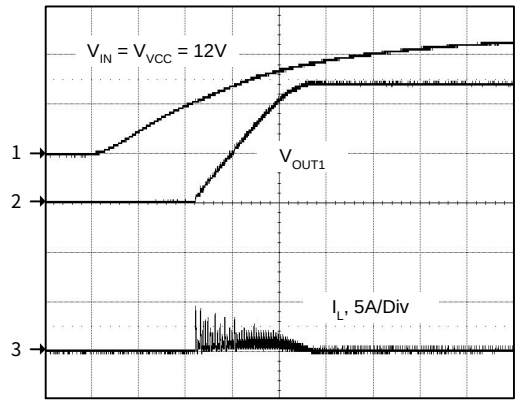


FS_DIS Resistance vs. Switching Frequency



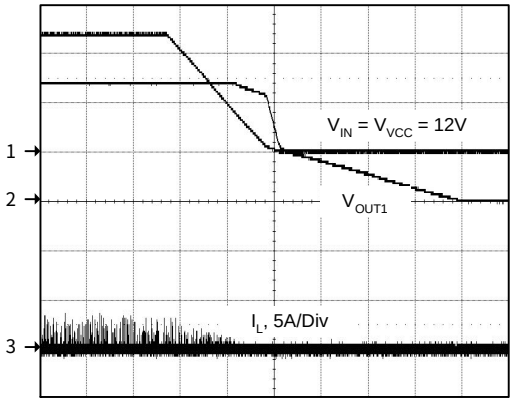
Operating Waveforms

Power On



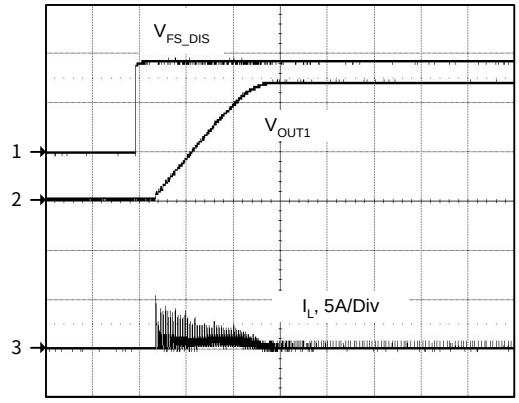
CH1: V_{IN}, 5V/Div, DC
CH2: V_{OUT1}, 0.5V/Div, DC
CH3: I_L, 5A/Div, DC
Time: 1ms/Div

Power Off



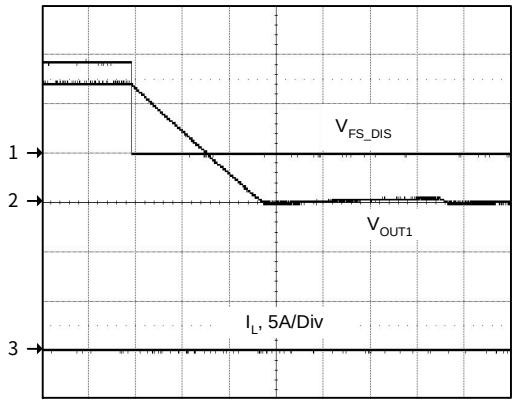
CH1: V_{IN}, 5V/Div, DC
CH2: V_{OUT1}, 0.5V/Div, DC
CH3: I_L, 5A/Div, DC
Time: 50ms/Div

Enable



CH1: V_{FS_DIS}, 0.5V/Div, DC
CH2: V_{OUT1}, 0.5V/Div, DC
CH3: I_L, 5A/Div, DC
Time: 1ms/Div

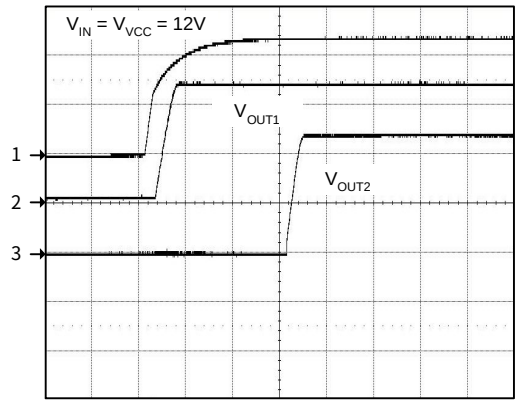
Shutdown



CH1: V_{FS_DIS}, 0.5V/Div, DC
CH2: V_{OUT1}, 0.5V/Div, DC
CH3: I_L, 5A/Div, DC
Time: 50ms/Div

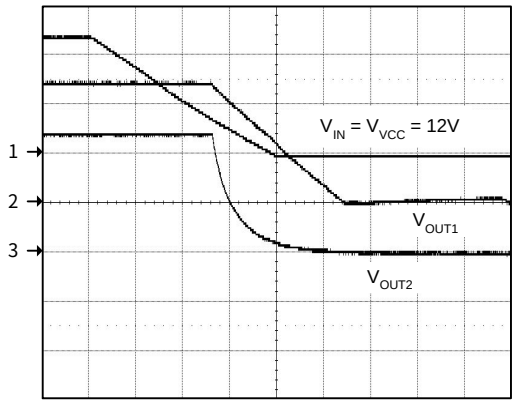
Operating Waveforms (Cont.)

Power Sequence



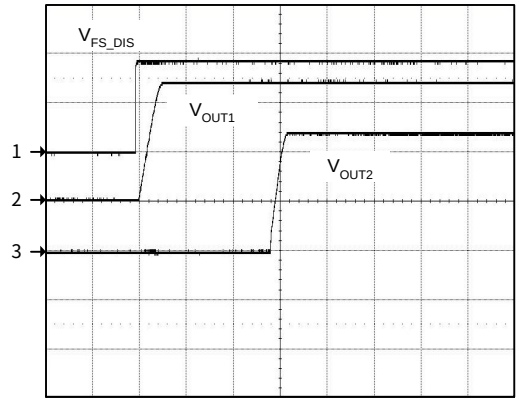
CH1: V_{IN}, 5V/Div, DC
CH2: V_{OUT1}, 0.5V/Div, DC
CH3: V_{OUT2}, 0.5V/Div, DC
Time: 5ms/Div

Power Sequence



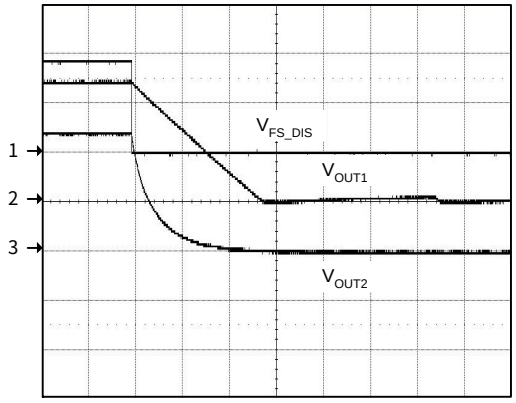
CH1: V_{IN}, 5V/Div, DC
CH2: V_{OUT1}, 0.5V/Div, DC
CH3: V_{OUT2}, 0.5V/Div, DC
Time: 50ms/Div

Enable



CH1: V_{IN}, 5V/Div, DC
CH2: V_{OUT1}, 0.5V/Div, DC
CH3: V_{OUT2}, 0.5V/Div, DC
Time: 5ms/Div

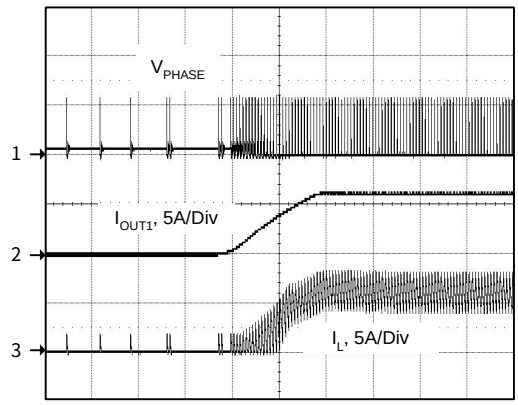
Shutdown



CH1: V_{IN}, 5V/Div, DC
CH2: V_{OUT1}, 0.5V/Div, DC
CH3: I_L, 5A/Div, DC
Time: 50ms/Div

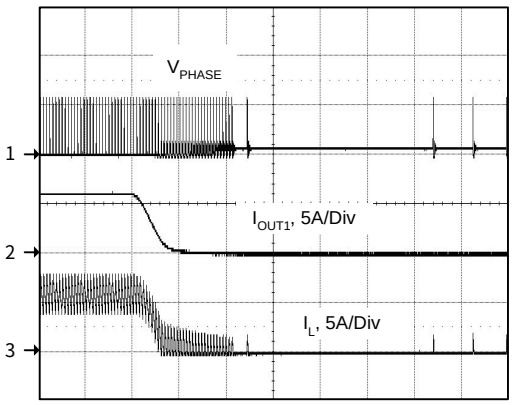
Operating Waveforms (Cont.)

PSM to PWM



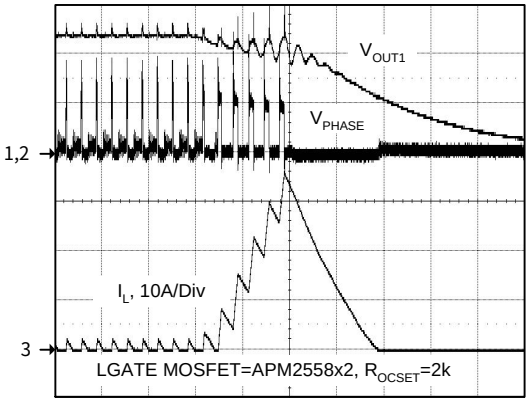
CH1: V_{PHASE}, 10V/Div, DC
CH2: I_{OUT1}, 5A/Div, DC
CH3: I_L, 5A/Div, DC
Time: 50µs/Div

PWM to PSM



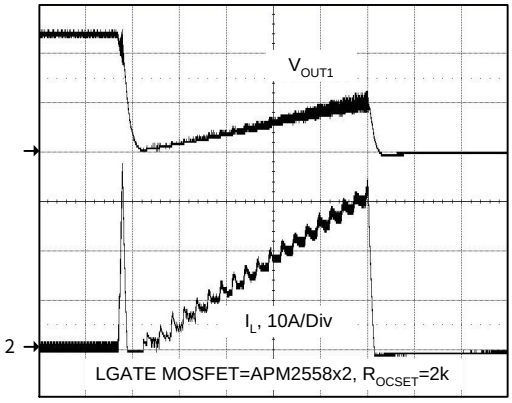
CH1: V_{PHASE}, 10V/Div, DC
CH2: I_{OUT1}, 5A/Div, DC
CH3: I_L, 5A/Div, DC
Time: 50µs/Div

OCP



CH1: V_{PHASE}, 10V/Div, DC
CH2: V_{OUT1}, 0.5V/Div, DC
CH3: I_L, 10A/Div, DC
Time: 10µs/Div

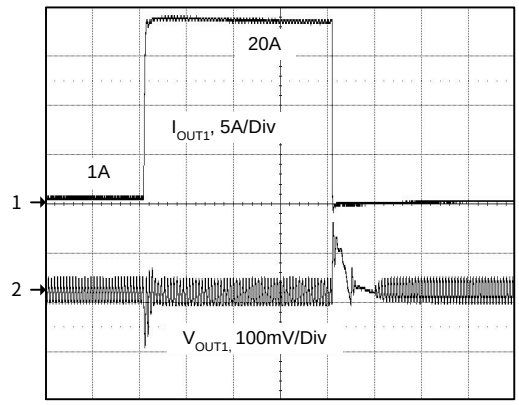
OCP



CH1: V_{OUT1}, 0.5V/Div, DC
CH2: I_L, 10A/Div, DC
Time: 0.2ms/Div

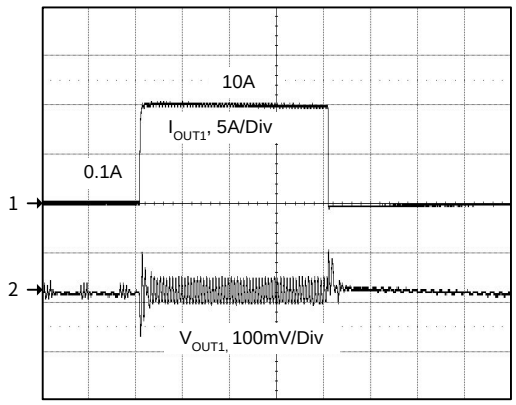
Operating Waveforms (Cont.)

Load Transient Response



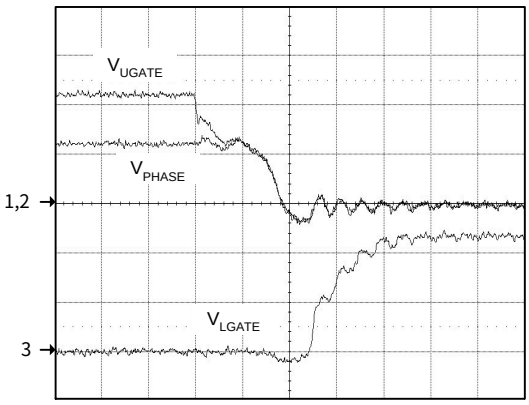
CH1: I_{OUT1}, 5A/Div, DC
CH2: V_{OUT1}, 100mV/Div, AC
Time: 20µs/Div

Load Transient Response



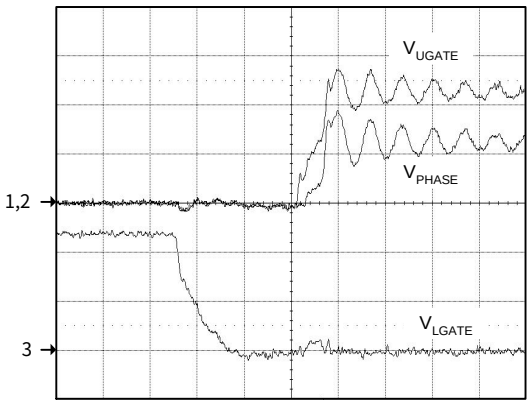
CH1: I_{OUT1}, 5A/Div, DC
CH2: V_{OUT1}, 100mV/Div, AC
Time: 20µs/Div

UGATE Falling



CH1: V_{UGATE}, 10V/Div, DC
CH2: V_{PHASE}, 10V/Div, DC
CH3: V_{LGATE}, 5V/Div, DC
Time: 20ns/Div

UGATE Rising

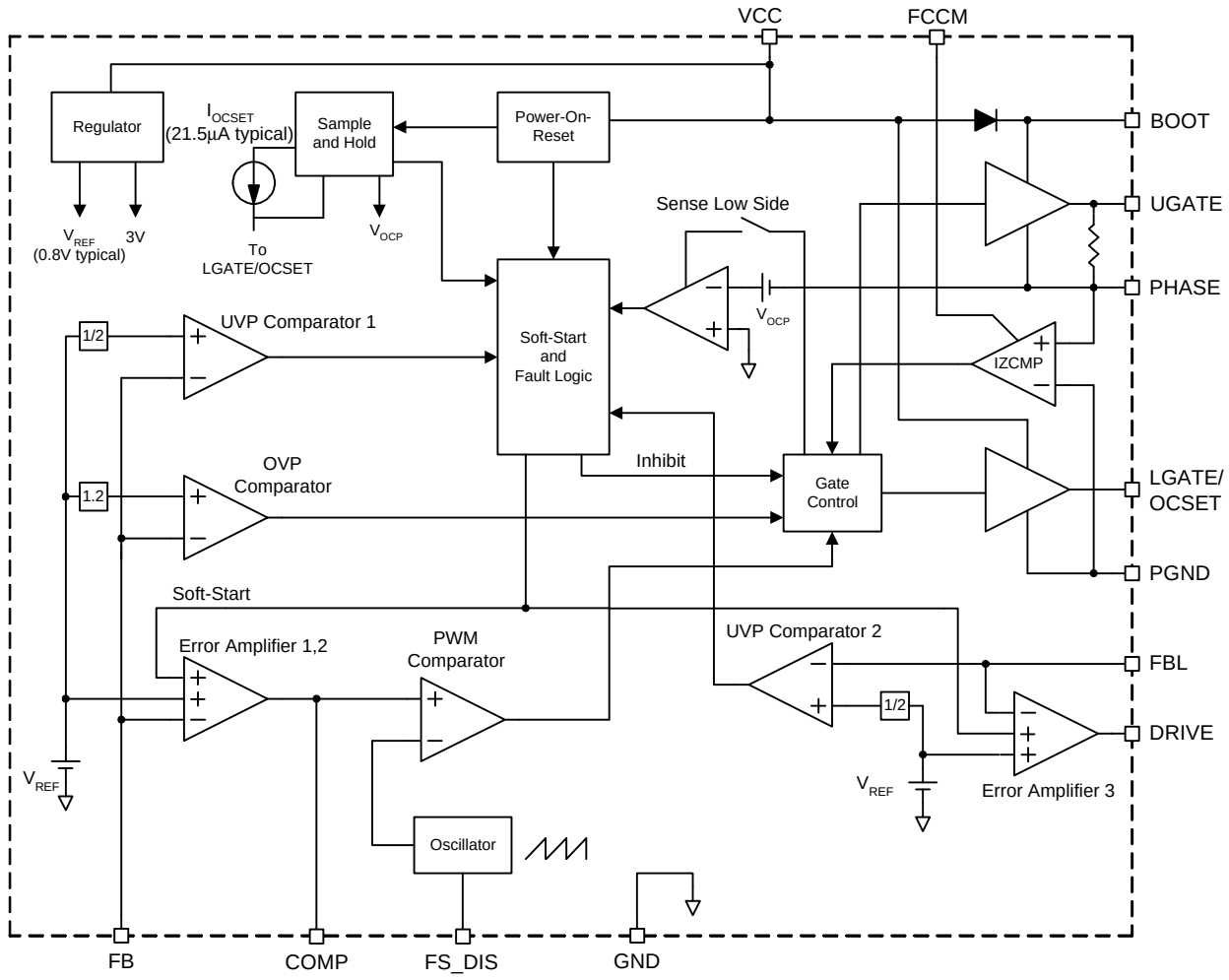


CH1: V_{UGATE}, 10V/Div, DC
CH2: V_{PHASE}, 10V/Div, DC
CH3: V_{LGATE}, 5V/Div, DC
Time: 20ns/Div

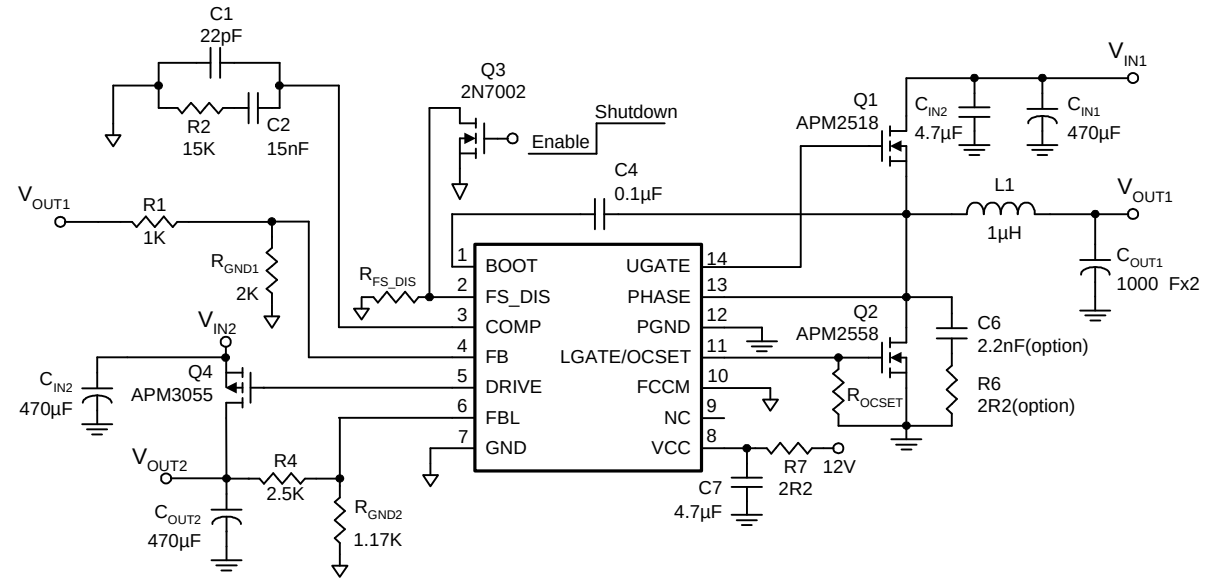
Pin Description

PIN		FUNCTION
NO.	NAME	
1	BOOT	This pin provides the bootstrap voltage to the high-side gate driver for driving the N-channel MOSFET. An external capacitor from PHASE to BOOT, an internal diode, and the power supply voltage VCC, generates the bootstrap voltage for the high-side gate driver (UGATE).
2	FS_DIS	This is a multiplexed pin. Connect a resistor from FS_DIS to GND to adjust the switching frequency range from 150kHz to 600kHz. This pin also provides shutdown function: use an open drain logic signal to pull this pin low to disable both outputs; Left FS_DIS floating enable both PWM and LDO. The switching frequency is 150kHz typical at floating.
3	COMP	Output of Error Amplifier 1 for the Buck Converter. It is used to compensate the regulation control loop. Refer to the section “Application Information” for details.
4	FB	Feedback Input of Buck Converter. The Buck converter senses feedback voltage via FB and regulates the FB voltage at 0.8V. Connecting FB with a resistor-divider from the output sets the output voltage of the Buck converter.
5	DRIVE	Output of Error Amplifier 2 for the linear controller. This pin drives the gate of an external N-channel MOSFET for linear regulator. It is also used to set the compensation for some specific applications, for example, with low values of output capacitance and ESR.
6	FBL	Feedback Input of Liner Controller. The linear controller senses feedback voltage via FBL and regulates the FBL voltage at 0.8V. Connecting FBL with a resistor-divider from the output sets the output voltage of the linear regulator.
7	GND	Signal ground. Connecting this pin to system ground.
8	VCC	Power Supply Input. Connect a nominal 5V to 12V power supply voltage to this pin. A power-on-reset function monitors the input voltage at this pin. It is recommended that a decoupling capacitor (1 to 10μF) be connected to the GND for noise decoupling.
9	NC	No Internal Connection.
10	FCCM	Forced PWM Mode Selection Input. Internal pull high. Pulling this pin to logic high forces Buck converter to enter the forced PWM mode. Pulling it low sets automatic mode, which switches the operation mode to be either PSM (Pulse Skipping Mode) or PWM mode by depending on the load current.
11	LGATE/OCSET	Low-side Gate Driver Output and Over-Current Setting Input for the Buck converter. This pin is the gate driver for low-side MOSFET of buck converter. It also used to set the maximum inductor current. Refer to the section in “Function Description” for detail.
12	PGND	Power Ground of the Low-Side Gate Driver. Use a separate track to connect this pin to Source of the low-side MOSFET. The Source of the low-side MOSFET must be connected to system ground with very low impedance.
13	PHASE	This pin is the return path for the high-side gate driver. Connecting this pin to the high-side MOSFET source and connect a capacitor to BOOT for the bootstrap voltage. This pin is also used to monitor the voltage drop across the low-side MOSFET for over-current protection.
14	UGATE	High-side Gate Driver Output. This pin is the gate driver for high-side MOSFET of buck converter.

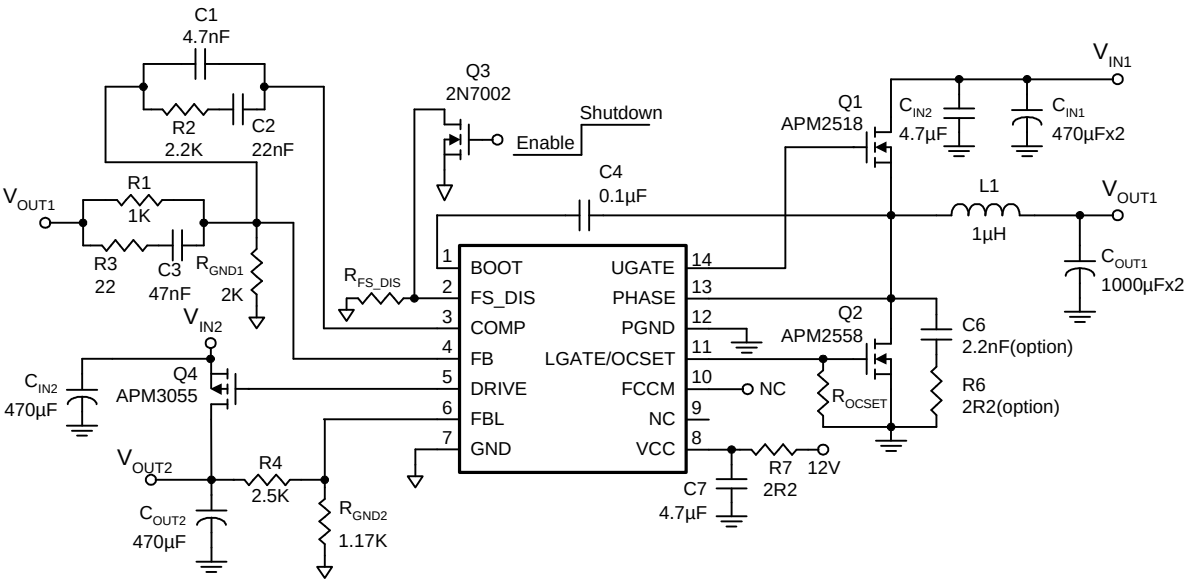
Block Diagram



Typical Application Circuits



APW7166 Operates at PSM/PWM



APW7166 Operates at Force PWM

Function Description

Power-On-Reset (POR)

The Power-On-Reset (POR) function of APW7166 continually monitors the input supply voltage (VCC) and ensures that the IC has sufficient supply voltage and can work well. The POR function initiates a soft-start process while the VCC voltage exceeds the POR threshold; the POR function also inhibits the operations of the IC while the VCC voltage falls below the POR threshold.

Soft-Start

The APW7166 builds in, 40-step, and digital soft-start to control the output voltage rise as well as limit the current surge at the start-up. During soft-start, an internal ramp voltage connected to the one of the positive inputs of the error amplifier replaces the reference voltage (0.8V typical) until the ramp voltage reaches the reference voltage. The digital soft-start circuit interval (shown as figure 1) depends on the switching frequency.

$$T_{SS} = (t_3 - t_2) = \frac{1}{F_{OSC}} \cdot 630$$

The linear regulator initiates a soft-start process, which lags behind the Buck converters for 6 period of a soft-start process.

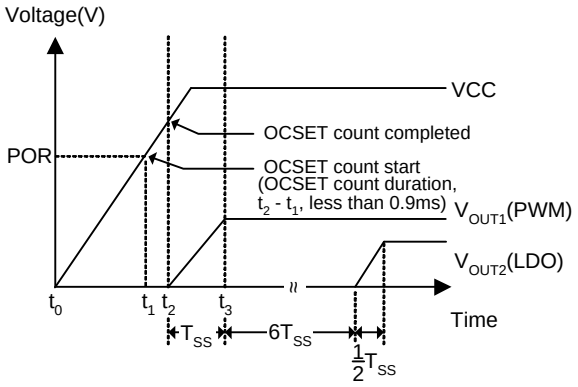


Figure 1. Soft-Start Interval

Over-Current Protection of the PWM Converter

The over-current function protects the switching converter against over-current or short-circuit conditions. The controller senses the inductor current by detecting the drain-to-source voltage which is the product of the inductor's current and the on-resistance of the low-side MOSFET during on-state.

A resistor (R_{OCSET}), connected from the LGATE to the GND, programs the over-current trip level. Before the IC initiates a soft-start process, an internal current source, I_{OCSET} (21.5µA typical), flowing through the R_{OCSET} develops a voltage (V_{ROCSET}) across the R_{OCSET}. During the normal operation, the device holds V_{ROCSET} and stops the current source, I_{OCSET}. When the voltage across the low-side MOSFET exceeds the double V_{ROCSET} (2 x V_{ROCSET}), the IC shuts off the converter and then initiates a new soft-start process. After 2 over-current events are counted, the device is shut down and all the gate drivers (UGATE, LGATE, and DRIVE) are off. Both the output of the PWM converter and linear controller are latched to be floating.

The APW7166 has an internal OCP voltage, V_{OCP_MAX}, and the value is 0.3V minimum. When the R_{OCSET} x I_{OCSET} exceeds 0.3V or the R_{OCSET} is floating or not connected, the V_{ROCSET} will be the default value 0.3V. The over current threshold would be 0.3V across low-side MOSFET. The threshold of the valley inductor current-limit is therefore given by:

$$I_{LIMIT} = \frac{2 \times I_{OCSET} \times R_{OCSET}}{R_{DS(ON)}(low-side)}$$

For the over-current is never occurred in the normal operating load range; the variation of all parameters in the above equation should be considered:

- The $R_{DS(ON)}$ of low-side MOSFET is varied by temperature and gates to source voltage. Users should determine the maximum $R_{DS(ON)}$ by using the manufacturer's datasheet.
- The minimum I_{OCSET} (19.5µA) and minimum R_{OCSET} should be used in the above equation.
- Note that the I_{LIMIT} is the current flow through the low-side MOSFET; I_{LIMIT} must be greater than valley inductor current which is output current minus the half of inductor ripple current.

$$I_{LIMIT} > I_{OUT(MAX)} - \frac{\Delta I}{2}$$

Where ΔI = output inductor ripple current

- The overshoot and transient peak current also should be considered.

Function Description (Cont.)

Under-Voltage Protection

The under-voltage function monitors the voltage on FB (V_{FB}) and FBL (V_{FBL}) by their own Under-Voltage (UV) comparator to protect the PWM converter and linear controller against short-circuit conditions. When either the V_{FB} or V_{FBL} falls below the falling UVP threshold (50% V_{REF}), a fault signal is internally generated and the device turns off high-side and low-side MOSFET and linear regulator. The buck converter's output is latched to be floating and linear regulator is shutdown.

Over-Voltage Protection (OVP) of the PWM Converter

The over-voltage protection monitors the FB voltage to prevent the output from over-voltage condition. When the output voltage rises above 120% of the nominal output voltage, the APW7166 turns off the high-side MOSFET and turns on the low-side MOSFET until the output voltage falls below the falling OVP threshold, regulating the output voltage around the OVP threshold.

Shutdown and Enable

Pulling the FS_DIS voltage low by an open drain transistor (R_{FS_DIS} <1kΩ), shown in typical application circuit, shuts down the device. In shutdown mode, the UGATE and LGATE are pulled to PHASE- and GND respectively. Both the outputs of linear regulator and PWM controller are latched to be floating. When the pull-down device is released, the APW7166 initiate a new soft-start process.

PSM (Pulse Skipping Mode) of the PWM Converter

At light loads, the inductor current may reach zero or reverse on each pulse. The low-side MOSFET is turned off by the current reversal comparator, IZCMP, to block the negative inductor current. In this condition, the converter enters discontinuous current mode operation.

The APW7166 is designed with a minimum on-time control for the PSM operation. At very light loads, the APW7166 will automatically skip pulses in pulse skipping mode operation to reduce switching losses as well as maintain output regulation for efficient applications.

Adaptive Shoot-Through Protection of the PWM Converter

The gate drivers incorporate an adaptive shoot-through protection to prevent high-side and low-side MOSFETs from conducting simultaneously and shorting the input supply. This is accomplished by ensuring the falling gate has turned off one MOSFET before the other is allowed to rise.

During turn-off the low-side MOSFET, the LGATE voltage is monitored until it is below 1.5V threshold, at which time the UGATE is released to rise after a constant delay. During turn-off of the high-side OCSFET, the UGATE-to-PHASE voltage is also monitored until it is below 1.5V threshold, at which time the LGATE is released to rise after a constant delay.

Application Information

Output Voltage Selection

The output voltage of PWM converter can be programmed with a resistive divider. Use 1% or better resistors for the resistive divider is recommended. The FB pin is the inverter input of the error amplifier, and the reference voltage is 0.8V. The output voltage is determined by:

$$V_{OUT1} = 0.8 \times \left(1 + \frac{R1}{R_{GND1}}\right)$$

Where R1 is the resistor connected from V_{OUT1} to FB and RGND1 is the resistor connected from FB to GND.
The linear regulator output voltage V_{OUT2} is also set by means of an external resistor divider. The FBL pin is the inverter input of the error amplifier, and the reference voltage is 0.8V. The output voltage is determined by:

$$V_{OUT2} = 0.8 \times \left(1 + \frac{R4}{R_{GND2}}\right)$$

Where R4 is the resistor connected from V_{OUT2} to FBL and R_{GND2} is the resistor connected from FBL to GND.

Output Capacitor Selection

The selection of C_{OUT} is determined by the required effective series resistance (ESR) and voltage rating rather than the actual capacitance requirement. Therefore, selecting high performance low ESR capacitors is intended for switching regulator applications. In some applications, multiple capacitors have to be paralleled to achieve the desired ESR value. If tantalum capacitors are used, make sure they are surge tested by the manufactures. If in doubt, consult the capacitors manufacturer.

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage. The maximum RMS current rating requirement is approximately $I_{OUT}/2$ where I_{OUT} is the load current. During power up, the input capacitors have to handle large amount of surge current. If tantalum capacitors are used, make sure they are surge tested by the manufactures. If in doubt, consult the capacitors manufacturer.
For high frequency decoupling, a ceramic capacitor between 0.1µF to 1µF can connect between VCC and ground pin.

Inductor Selection

The inductance of the inductor is determined by the output voltage requirement. The larger the inductance, the lower the inductor's current ripple. This will translate into lower output ripple voltage. The ripple current and ripple voltage can be approximated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{F_{SW} \cdot L} \cdot \frac{V_{OUT}}{V_{IN}}$$

where Fs is the switching frequency of the regulator.

$$\Delta V_{OUT} \cong I_{RIPPLE} \times ESR$$

A tradeoff exists between the inductor's ripple current and the regulator load transient response time. A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current and vice versa. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current.
Once the inductance value has been chosen, selecting an inductor is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is make of ferrite, the ripple current will increase abruptly when it saturates. This will result in a larger output ripple voltage.

MOSFET Section

The selection of the N-channel power MOSFETs is determined by the $R_{DS(ON)}$, reverse transfer capacitance (C_{RSS}), and maximum output current requirement.The losses in the MOSFETs have two components: conduction loss and transition loss. For the upper and lower MOSFET, the losses are approximately given by the following equations:

$$P_{UPPER} = I_{out}\,(1+TC)(R_{DS(ON)})D + (0.5)(I_{out})(V_{IN})(t_{sw})F_{SW}$$
$$P_{LOWER} = I_{out}\,(1+TC)(R_{DS(ON)})(1-D)$$

where I_{OUT} is the load current
TC is the temperature dependency of $R_{DS(ON)}$
F_{SW} is the switching frequency
t_{sw} is the switching interval
D is the duty cycle

Application Information (Cont.)

MOSFET Section (Cont.)

Note that both MOSFETs have conduction losses while the upper MOSFET includes an additional transition loss. The switching internal, t_{sw}, is the function of the reverse transfer capacitance C_{RSS}. Figure 2 illustrates the switching waveform internal of the MOSFET.

The (1+TC) term factors in the temperature dependency of the $R_{DS(ON)}$ and can be extracted from the "$R_{DS(ON)}$ vs Temperature" curve of the power MOSFET.

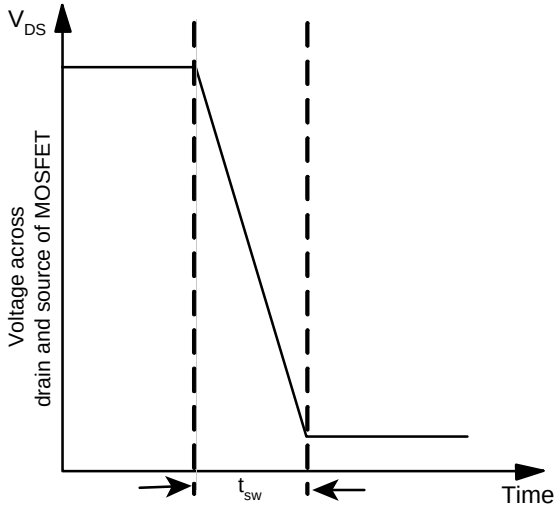


Figure 2. Switching waveform across MOSFET

Compensation

The APW7166 builds in two error amplifiers. When FCCM was pulled low, the device operates at PSM or PWM mode by depending on the load current. The FB internal connected to error amplifier 1 which transconductance, gm, is 667uA/V typical. When FCCM was pull high or floating, the device operates at force PWM mode. The FB internal connected to error amplifier 2.

FCCM=L (EA1)

The output LC filter of a step down converter introduces a double pole, which contributes with -40dB/decade gain slope and 180 degrees phase shift in the control loop. A compensation network between COMP pin and ground should be added. The simplest loop compensation network is shown in Figure 6.

The output LC filter consists of the output inductor and output capacitors. The transfer function of the LC filter is given by:

$$GAIN_{LC} = \frac{1 + s \times ESR \times C_{OUT}}{s^2 \times L \times C_{OUT} + s \times ESR \times C_{OUT} + 1}$$

The poles and zero of this transfer function are:

$$F_{LC} = \frac{1}{2 \times \pi \times \sqrt{L \times C_{OUT}}}$$

$$F_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}}$$

The FLC is the double poles of the LC filter, and FESR is the zero introduced by the ESR of the output capacitor.

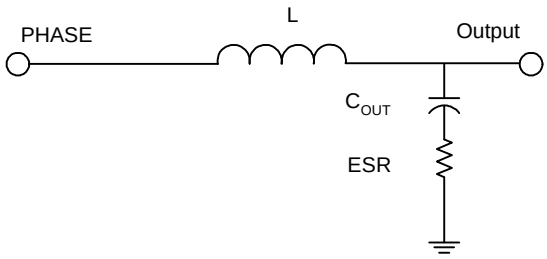


Figure 3. The Output LC Filter

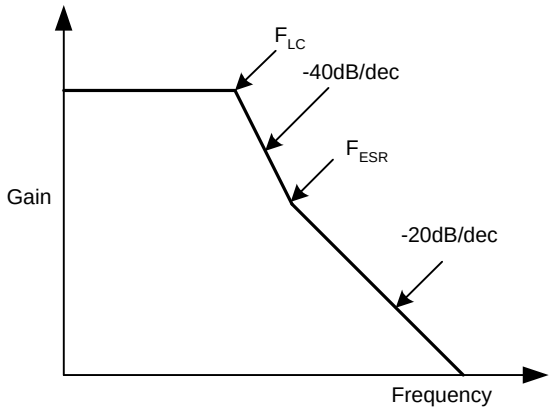


Figure 4. The LC Filter Gain & Frequency

The PWM modulator is shown in Figure 5. The input is the output of the error amplifier and the output is the PHASE node. The transfer function of the PWM modulator is given by:

$$GAIN_{PWM} = \frac{V_{IN}}{\Delta V_{OSC}}$$

Application Information (Cont.)

FCCM=L (EA1) (Cont.)

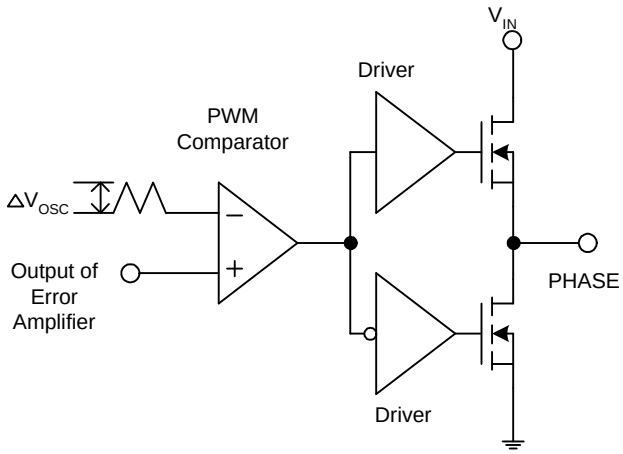


Figure 5. The PWM Modulator

The compensation circuit is shown in Figure 6. R3 and C1 introduce a zero and C2 introduces a pole to reduce the switching noise. The transfer function of error amplifier is given by:

$$GAIN_{AMP} = gm \times Z_O = gm \times \left[\left(R3 + \frac{1}{sC1}\right) // \frac{1}{sC2}\right]$$

$$= gm \times \frac{\left(s + \frac{1}{R3 \times C1}\right)}{s \times \left(s + \frac{C1 + C2}{R3 \times C1 \times C2}\right) \times C2}$$

The pole and zero of the compensation network are:

$$F_P = \frac{1}{2 \times \pi \times R3 \times \frac{C1 \times C2}{C1 + C2}}$$

$$F_Z = \frac{1}{2 \times \pi \times R3 \times C1}$$

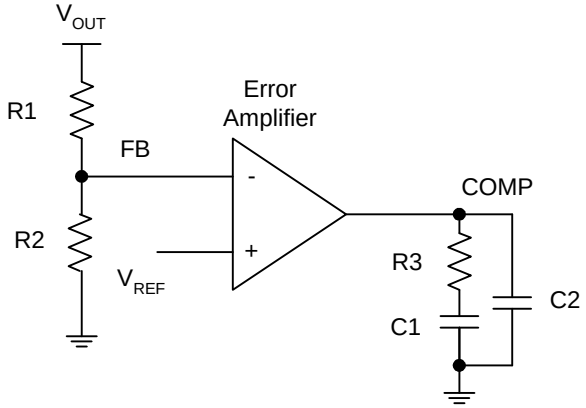


Figure 6. Compensation Network

The closed loop gain of the converter can be written as:

$$GAIN_{LC} \times GAIN_{PWM} \times \frac{R2}{R1 + R2} \times GAIN_{AMP}$$

Figure 7 shows the converter gain and the following guidelines will help to design the compensation network.

1.Select the desired zero crossover frequency F_O:

$(1/5 \sim 1/10) \times F_{SW} > F_O > F_Z$

Use the following equation to calculate R3:

$$R3 = \frac{\Delta V_{OSC}}{V_{IN}} \times \frac{F_{ESR}}{F_{LC}^2} \times \frac{R1 + R2}{R2} \times \frac{F_O}{gm}$$

Where:

gm = 667μA/V

2.Place the zero F_Z before the LC filter double poles F_{LC}:

$F_Z = 0.75 \times F_{LC}$

Calculate the C1 by the equation:

$$C1 = \frac{1}{2 \times \pi \times R1 \times 0.75 \times F_{LC}}$$

3. Set the pole at the half the switching frequency:

$F_P = 0.5 \times F_{SW}$

Calculate the C2 by the equation:

$$C2 = \frac{C1}{\pi \times R3 \times C1 \times F_{SW} - 1}$$

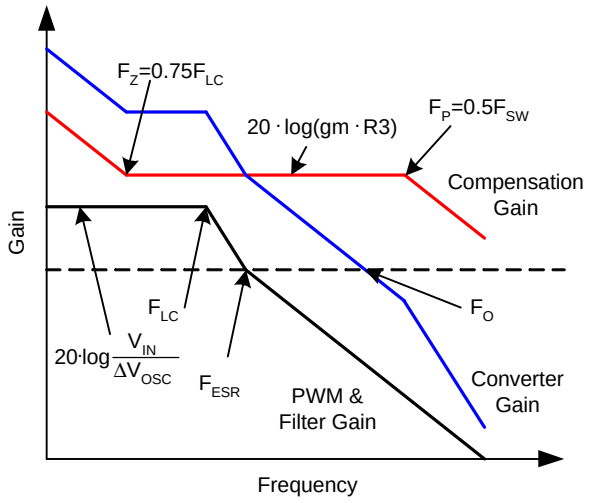


Figure 7. Converter Gain & Frequency

Application Information (Cont.)

FCCM=H or floating (EA2)

The output LC filter of a step down converter introduces a double pole, which contributes with -40dB/decade gain slope and 180 degrees phase shift in the control loop. A compensation network among COMP, FB and V_{OUT1} should be added. The compensation network is shown in Figure 11. The output LC filter consists of the output inductor and output capacitors. The transfer function of the LC filter is given by:

$$GAIN_{LC} = \frac{1+s\times ESR\times C_{OUT1}}{s^2\times L\times C_{OUT1}+s\times ESR\times C_{OUT1}+1}$$

The poles and zero of this transfer functions are:

$$F_{LC} = \frac{1}{2\times\pi\times\sqrt{L\times C_{OUT1}}}$$

$$F_{ESR} = \frac{1}{2\times\pi\times ESR\times C_{OUT1}}$$

The F_{LC} is the double poles of the LC filter, and F_{ESR} is the zero introduced by the ESR of the output capacitor.

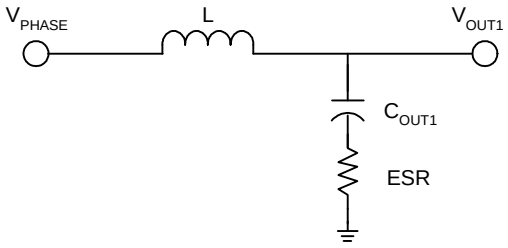


Figure 8. The Output LC Filter

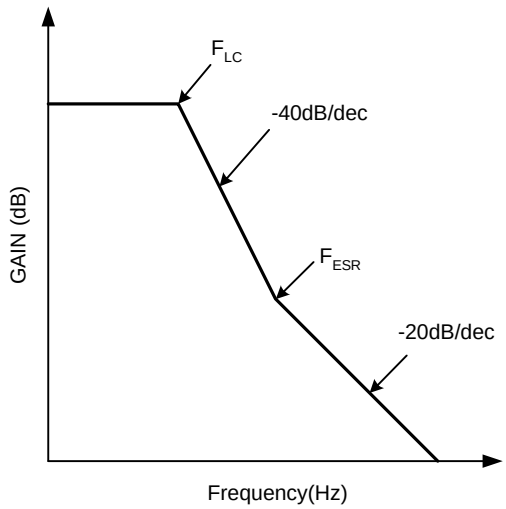


Figure 9. The LC Filter GAIN and Frequency

The PWM modulator is shown in Figure 10. The input is the output of the error amplifier and the output is the PHASE node. The transfer function of the PWM modulator is given by:

$$GAIN_{PWM} = \frac{V_{IN}}{\Delta V_{OSC}}$$

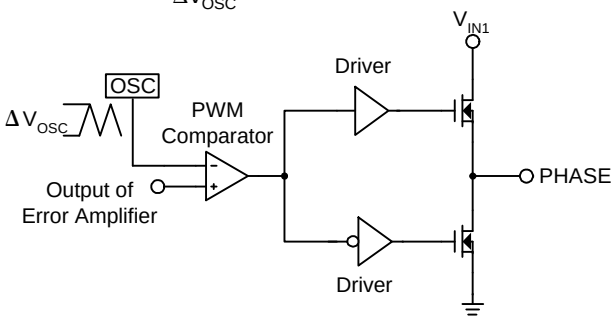


Figure 10. The PWM Modulator

The compensation network is shown in Figure 11. It provides a close loop transfer function with the highest zero crossover frequency and sufficient phase margin.

The transfer function of error amplifier is given by:

$$GAIN_{AMP} = \frac{V_{COMP}}{V_{OUT1}} = \frac{\frac{1}{sC1}//\left(R2+\frac{1}{sC2}\right)}{R1//\left(R3+\frac{1}{sC3}\right)}$$

$$= \frac{R1+R3}{R1\times R3\times C1}\times\frac{\left(s+\frac{1}{R2\times C2}\right)\times\left(s+\frac{1}{(R1+R3)\times C3}\right)}{s\left(s+\frac{C1+C2}{R2\times C1\times C2}\right)\times\left(s+\frac{1}{R3\times C3}\right)}$$

The poles and zeros of the transfer function are:

$$F_{Z1} = \frac{1}{2\times\pi\times R2\times C2}$$

$$F_{Z2} = \frac{1}{2\times\pi\times(R1+R3)\times C3}$$

$$F_{P1} = \frac{1}{2\times\pi\times R2\times\left(\frac{C1\times C2}{C1+C2}\right)}$$

$$F_{P2} = \frac{1}{2\times\pi\times R3\times C3}$$

Application Information (Cont.)

FCCM=H or floating (EA2) (Cont.)

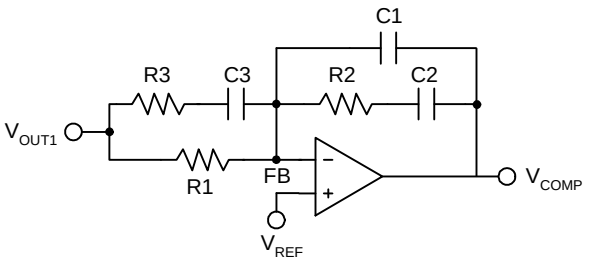


Figure 11. Compensation Network

The closed loop gain of the converter can be written as:

$GAIN_{LC}$ X $GAIN_{PWM}$ X $GAIN_{AMP}$

Figure 12. shows the asymptotic plot of the closed loop converter gain, and the following guidelines will help to design the compensation network. Using the below guidelines should give a compensation similar to the curve plotted. A stable closed loop has a -20dB/ decade slope and a phase margin greater than 45 degree.

1. Choose a value for R1, usually between 1K and 5K.
2. Select the desired zero crossover frequency

F_O: (1/5 ~ 1/10) X F_S > F_O > F_{ESR}

Use the following equation to calculate R2:

$$R2 = \frac{\Delta V_{OSC}}{V_{IN}} \times \frac{F_O}{F_{LC}} \times R1$$

3. Place the first zero F_{Z1} before the output LC filter double pole frequency F_{LC}.

F_{Z1} = 0.75 X F_{LC}

Calculate the C2 by the equation:

$$C2 = \frac{1}{2 \times \pi \times R2 \times F_{LC} \times 0.75}$$

4. Set the pole at the ESR zero frequency F_{ESR}:

F_{P1} = F_{ESR}

Calculate the C1 by the equation:

$$C1 = \frac{C2}{2 \times \pi \times R2 \times C2 \times F_{ESR} - 1}$$

5. Set the second pole F_{P2} at the half of the switching frequency and also set the second zero F_{Z2} at the output LC filter double pole F_{LC}. The compensation gain should not exceed the error amplifier open loop gain, check the compensation gain at F_{P2} with the capabilities of the error amplifier.

F_{P2} = 0.5 X F_S

F_{Z2} = F_{LC}

Combine the two equations will get the following component calculations:

$$R3 = \frac{R1}{\frac{F_S}{2 \times F_{LC}} - 1}$$

$$C3 = \frac{1}{\pi \times R3 \times F_S}$$

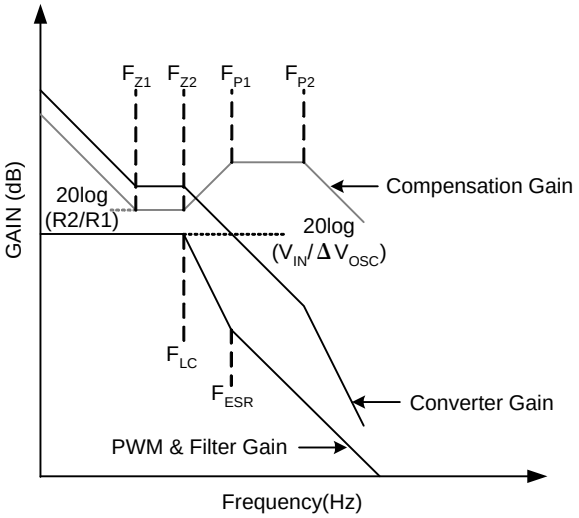


Figure 12. Converter Gain and Frequency

Layout Consideration

In any high switching frequency converter, a correct lay-out is important to ensure proper operation of the regulator. With power devices switching at 300kHz,the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic circuit elements. As an example, consider the turn-off transition of the PWM MOSFET. Before turn-off, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is free-wheeling by the lower MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short and wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike. And signal and power grounds are to be kept separate till combined using ground plane construction or single point grounding. Figure 13. illustrates the layout, with bold lines indicating high current paths; these traces must be short and wide. Components along the bold lines should be

Application Information (Cont.)

Layout Consideration (Cont.)

placed lose together. Below is a checklist for your layout:

- Keep the switching nodes (UGATE, LGATE, and PHASE) away from sensitive small signal nodes since these nodes are fast moving signals. Therefore, keep traces to these nodes as short as possible.
- The traces from the gate drivers to the MOSFETs (UG and LG) should be short and wide.
- Place the source of the high-side MOSFET and the drain of the low-side MOSFET as close as possible. Minimizing the impedance with wide layout plane between the two pads reduces the voltage bounce of the node.
- Decoupling capacitor, compensation component, the resistor dividers, and boot capacitors should be close their pins. (For example, place the decoupling ceramic capacitor near the drain of the high-side MOSFET as close as possible. The bulk capacitors are also placed near the drain).
- The input capacitor should be near the drain of the upper MOSFET; the output capacitor should be near the loads. The input capacitor GND should be close to the output capacitor GND and the lower MOSFET GND.
- The drain of the MOSFETs (V_{IN} and PHASE nodes) should be a large plane for heat sinking.
- The R_{OCSET} resistance should be placed near the IC as close as possible.

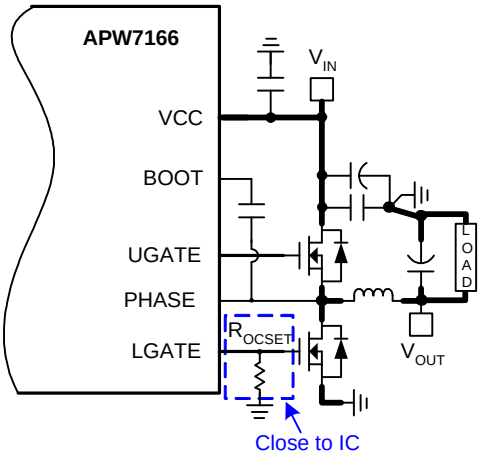
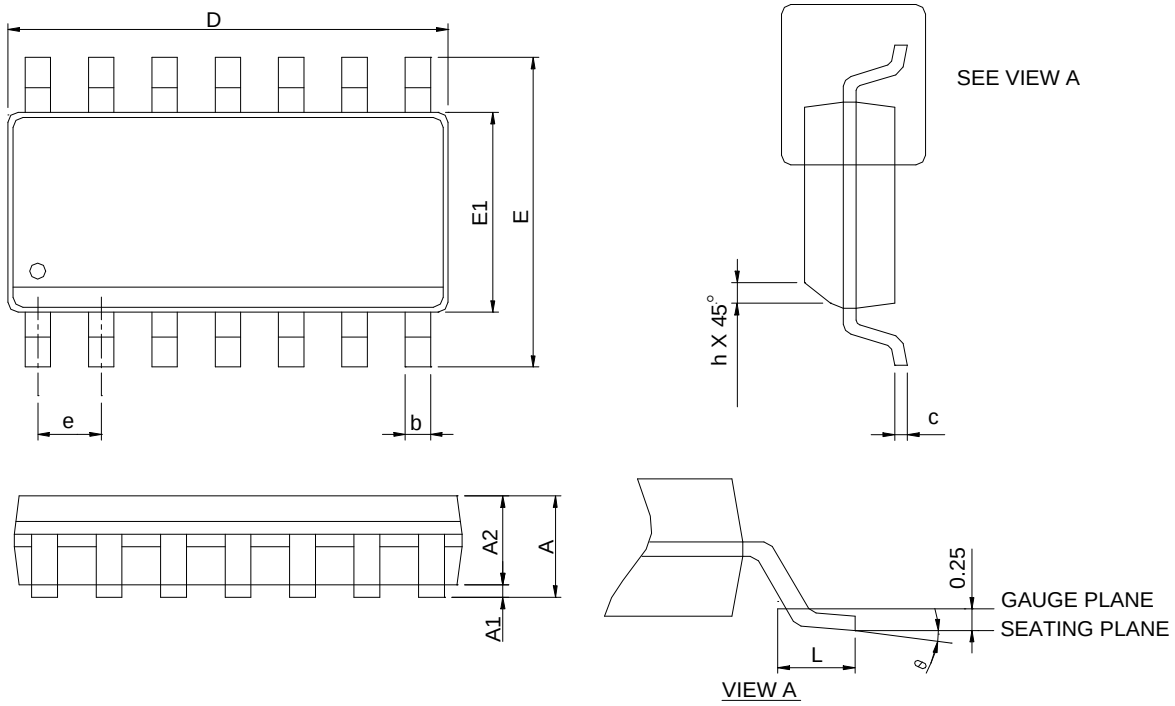


Figure 13. Layout Guidelines

Package Information

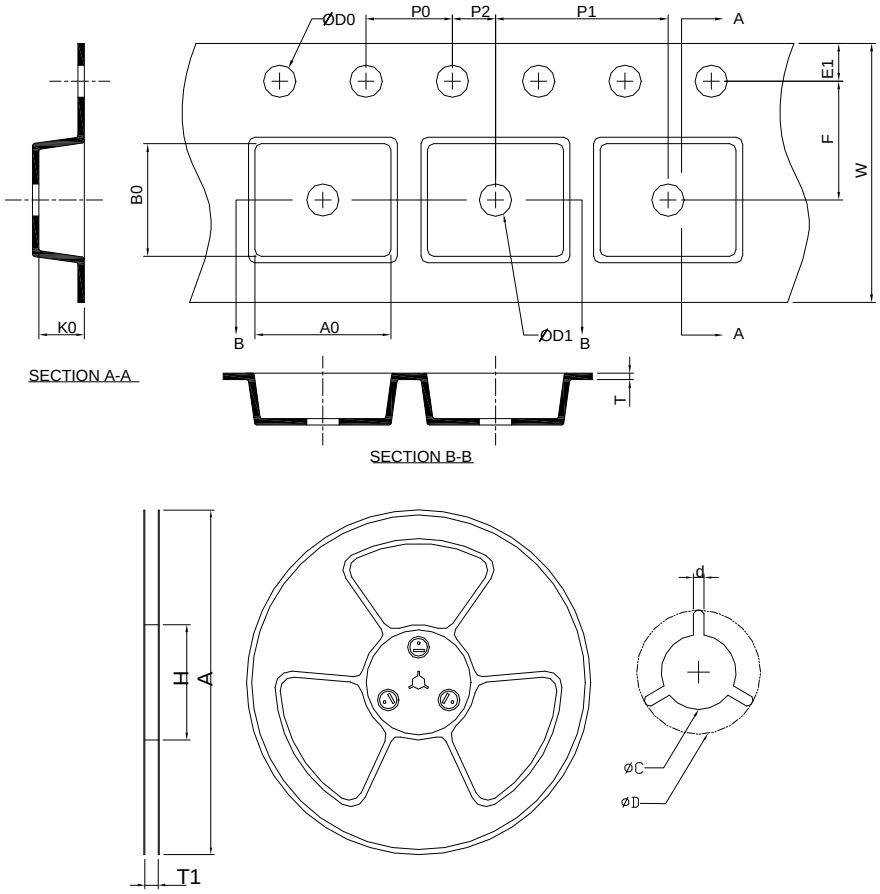
SOP-14



SYMBOL	SOP-14			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	8.55	8.75	0.337	0.344
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MS-012 AB.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension “E” does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOP-14	330.0±2.00	50 MIN.	16.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	16.0±0.30	1.75±0.10	7.50±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	9.00±0.20	2.10±0.20

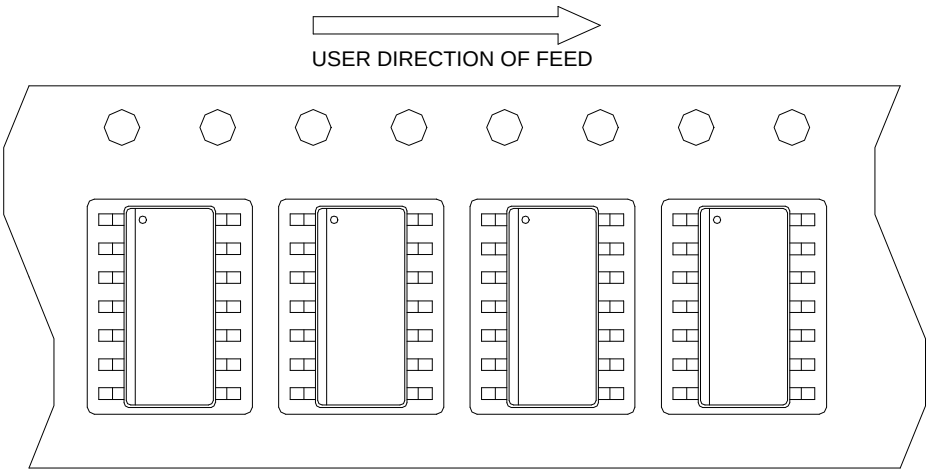
(mm)

Devices Per Unit

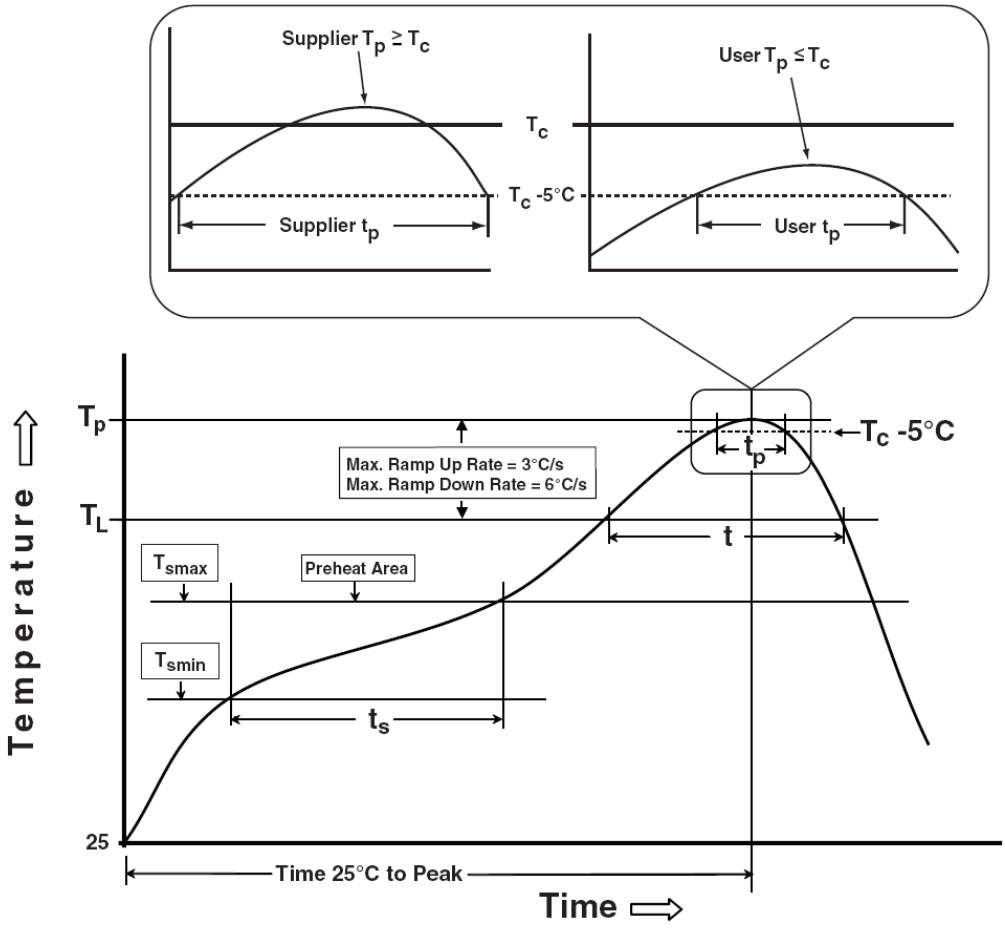
Package Type	Unit	Quantity
SOP-14	Tape & Reel	2500

Taping Direction Information

SOP-14



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ 125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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