Full-Bridge Inverter Gate Driver

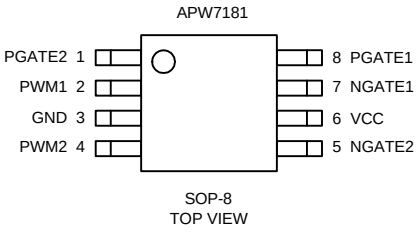
Features

- **Wide Input Voltage Range: 4.5V to 13.2V**
- **Drives a Full-Bridge Inverter(High-Side P-Channel MOSFETs and Low-Side N-Channel MOSFETs)**
- **Thermal Shutdown Protection**
- **VCC Power-On-Reset**
- **SOP-8 Package**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **LCD Monitor and LCD TV**

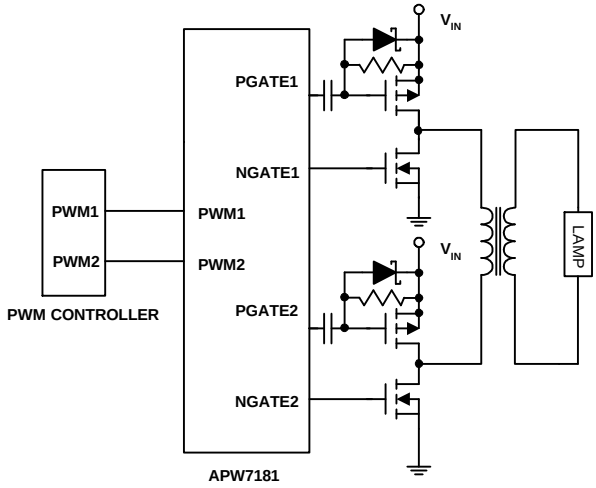
Pin Configuration



General Description

The APW7181 is designed to drive two high-side P-channel MOSFETs and two low-side N-channel MOSFETs in a full-bridge configuration. The outputs are independently controlled by PWM1 and PWM2 input signals.
The other features include VCC power-on-reset and thermal shutdown.

Simplified Application Circuit



Ordering and Marking Information

APW7181 □□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code K: SOP-8 Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW7181 K : APW7181 XXXXX ●	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{CC}	VCC Pin to GND	-0.3 to 16	V
	PGATEs, NGATEs Pins to GND	-0.3 to V_{CC}+0.3	V
	PWM1, PWM2 Pins to GND	-0.3 to 16	V
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 to 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note 1 : Stresses beyond the absolute maximum rating may damage the device and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics (Note 2)

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction to Ambient Thermal Resistance SOP-8	150	°C/W

Note 2 :θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions

Symbol	Parameter	Range	Unit
V_{CC}	VCC to GND	4.5 to 13.2	V
V_{PWM1}, V_{PWM2}	PWM1, PWM2 Pins to GND	0 to 13.2	V
C_{VCC}	VCC Pin Input Capacitor (MLCC)	1 to 10	µF
T_J	Junction Temperature	-40 to 125	°C
T_A	Ambient Temperature	-40 to 85	°C

Electrical Characteristics

Refer to the typical application circuit. These specifications apply over V_{CC}=12V, T_A= -40~85°C, unless otherwise specified. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7181			Unit
			Min.	Typ.	Max.	
POWER SUPPLY						
I_Q	VCC Quiescent Current	V_{PWM1}=V_{PWM2}=0V	-	400	600	µA
		V_{PWM1}=V_{PWM2}=V_{CC}	-	550	750	µA
	VCC POR Threshold	V_{CC} rising	2	3	4.1	V
LOGIC INPUT						
V_{IH}	PWMs Logic High Threshold	V_{CC}=4.5V to 13.2V	3.2	-	-	V
V_{IL}	PWMs Logic Low Threshold	V_{CC}=4.5V to 13.2V	-	-	1.2	V
I_{PWMs}	PWMs Input Current	V_{PWMs}=13.2V	-	13.2	-	µA

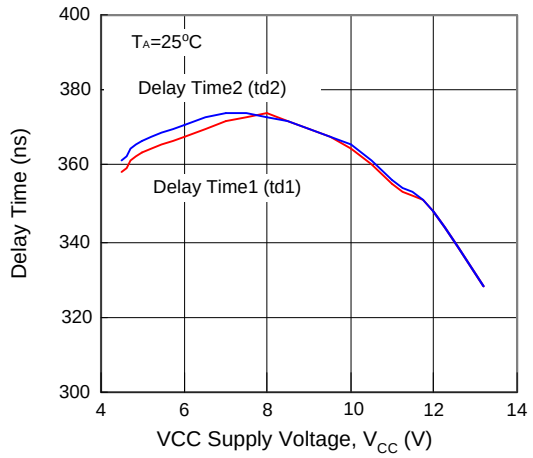
Electrical Characteristics (Cont.)

Refer to the typical application circuit. These specifications apply over V_{CC}=12V, T_A= -40~85°C, unless otherwise specified. Typical values are at T_A=25°C.

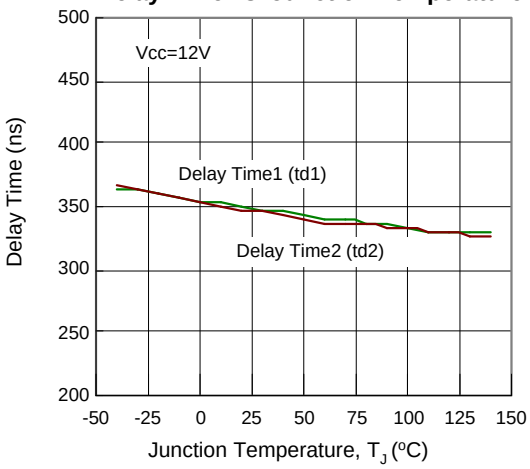
Symbol	Parameter	Test Conditions	APW7181			Unit
			Min.	Typ.	Max.	
TOP DRIVER						
	Gate Source Resistance	Source Current=0.1A, V_{CC}=12V	-	3.1	4.9	Ω
		Source Current =0.1A, V_{CC}=5V	-	5	8	
	Gate Sink Resistance	Sink Current=0.1A, V_{CC}=12V	-	5.3	9.1	
		Sink Current =0.1A, V_{CC}=5V	-	8.5	14.6	
BOTTOM DRIVER						
	Gate Source Resistance	Source Current =0.1A, V_{CC} =12V	-	6.2	10	Ω
		Source Current =0.1A, V_{CC} =5V	-	10	16	
	Gate Sink Resistance	Sink Current =0.1A, V_{CC} =12V	-	2.4	4	
		Sink Current =0.1A, V_{cc} =5V	-	3.9	7	
TIMING						
tp	Propagation Delay	PWMs rising to PGATEs rising, V_{CC}=5~12V	-	50	100	ns
		PWMs falling to NGATEs falling, V_{CC}=5~12V	-	50	100	
td1_12V	Delay Time1	PGATEs rising to NGATEs rising, V_{CC}=12V, T_A= -40°C ~85°C	250	350	450	ns
td1_5V		PGATEs rising to NGATEs rising, V_{CC}=5V, T_A= -40°C ~85°C	225	375	525	
td2_12V	Delay Time2	NGATEs falling to PGATEs falling, V_{CC}=12V, T_A=-40°C ~85°C	250	350	450	ns
td2_5V		NGATEs falling to PGATEs falling, V_{CC}=5V, T_A=-40°C ~85°C	225	375	525	
THERMAL SHUTDOWN						
	Thermal Shutdown Threshold	T_J rising	-	150	-	°C
	Thermal Shutdown Hysteresis		-	40	-	°C

Typical Operating Characteristics

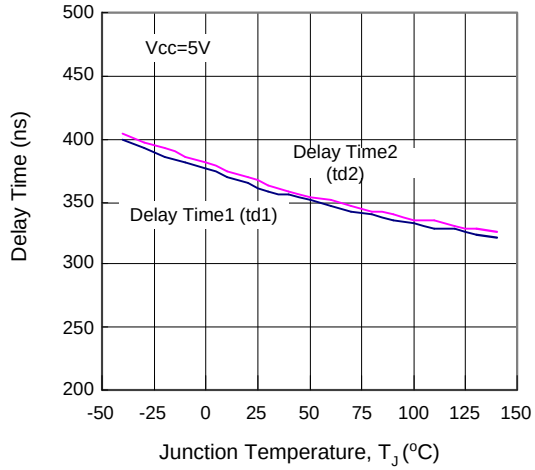
Delay Time vs. VCC Supply Voltage



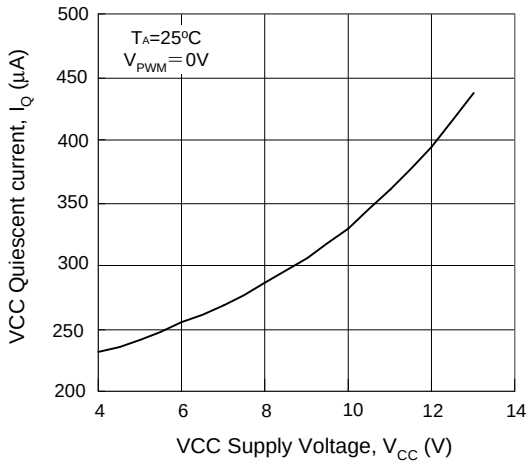
Delay Time vs. Junction Temperature



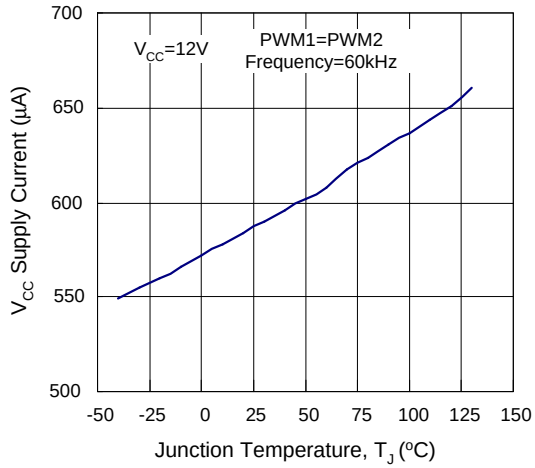
Delay Time vs. Junction Temperature



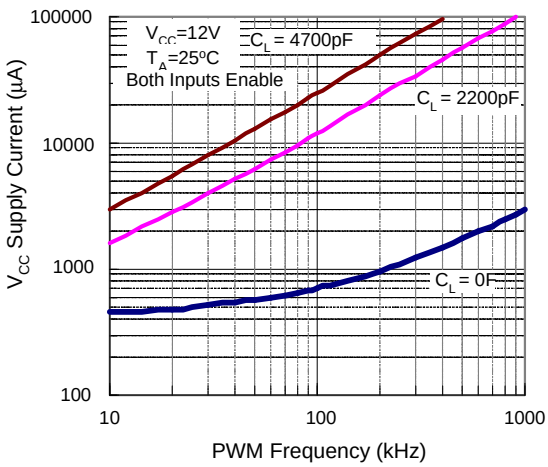
VCC Quiescent Current vs. VCC Supply Voltage



VCC Supply Current vs. Junction Temperature

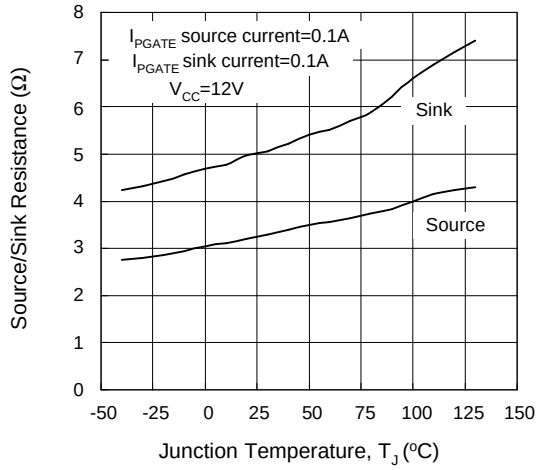


VCC Supply Current vs. PWM Frequency

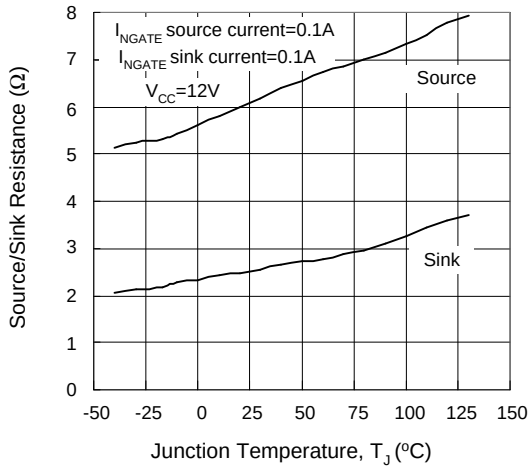


Typical Operating Characteristics (Cont.)

PGATE Source/Sink Resistance vs. Junction Temperature



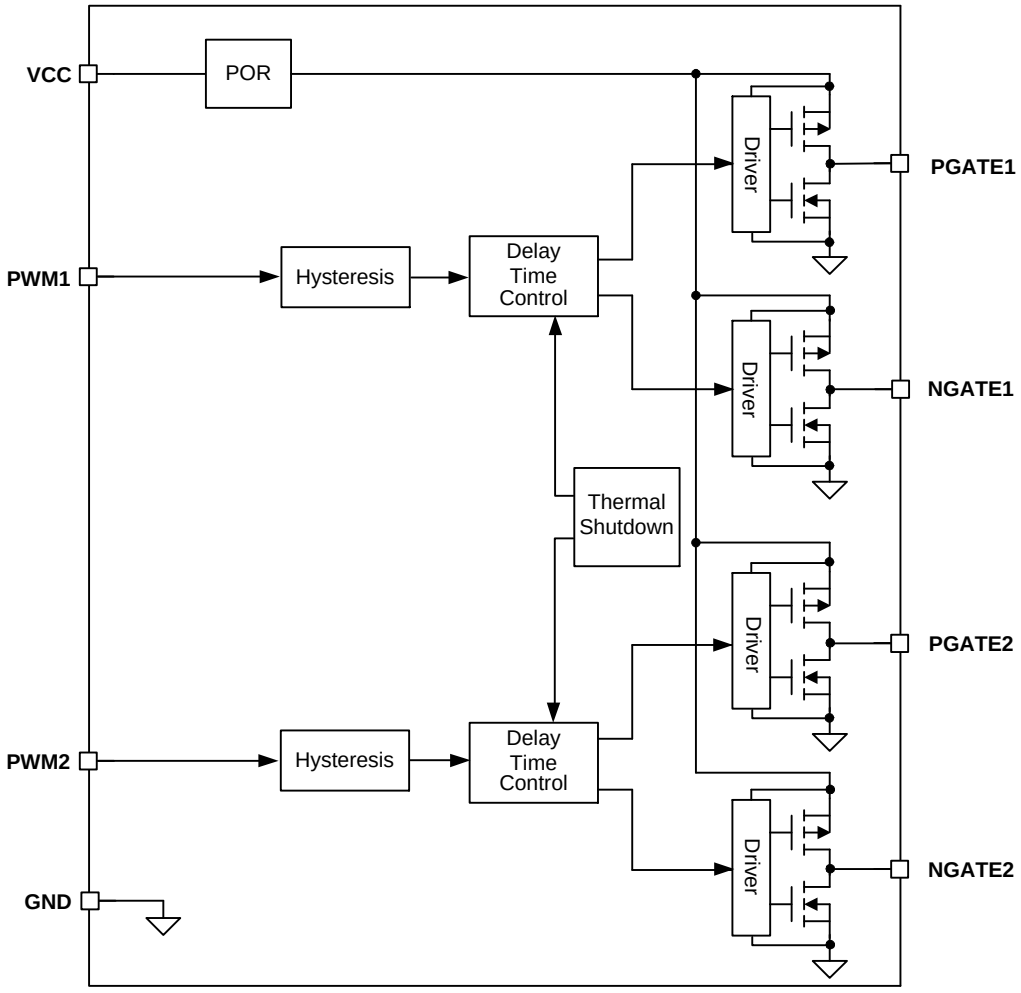
NGATE Source/Sink Resistance vs. Junction Temperature



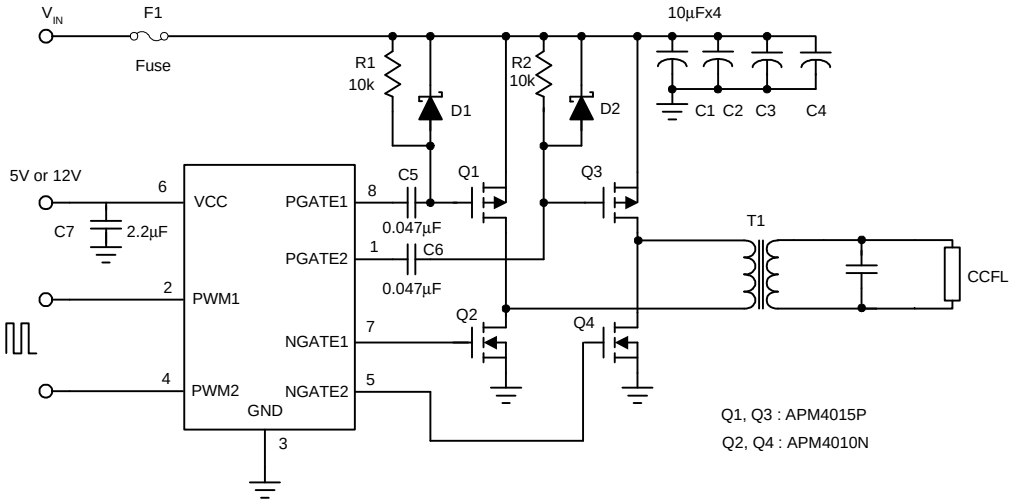
Pin Description

PIN		FUNCTION
NO.	NAME	
1	PGATE2	High-Side Gate Driver Output for P-channel MOSFET of Channel 2.
2	PWM1	Input PWM Signal for Channel 1.
3	GND	Ground.
4	PWM2	Input PWM Signal for Channel 2.
5	NGATE2	Low-Side Gate Driver Output for N-channel MOSFET of Channel 2.
6	VCC	Power Supply Input.
7	NGATE1	Low-Side Gate Driver Output for N-channel MOSFET of Channel 1.
8	PGATE1	High-Side Gate Driver Output for P-channel MOSFET of Channel 1.

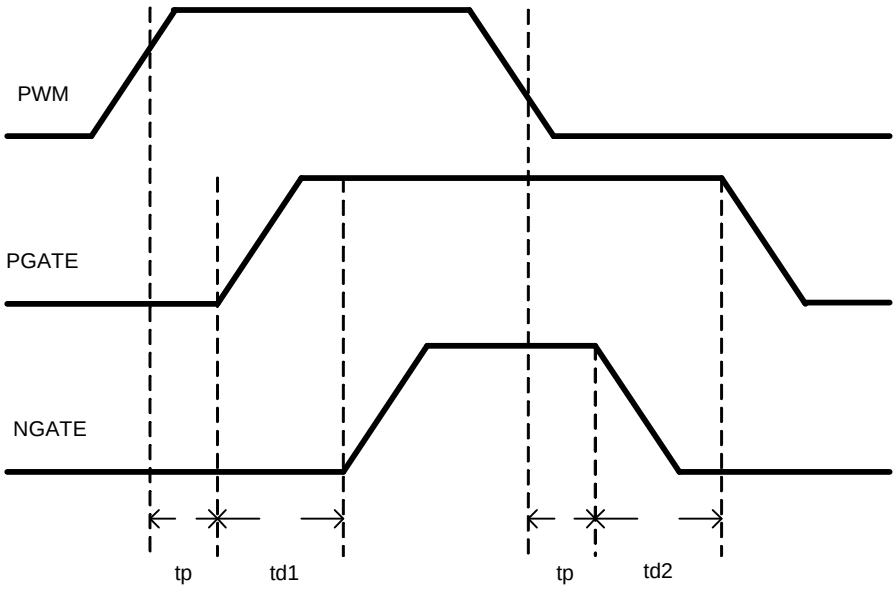
Block Diagram



Typical Application Circuit



Timing Diagram



Function Description

Thermal Shutdown

If the junction temperature exceeds 150°C, the thermal shutdown circuit will pull PGATE outputs high and NGATE outputs low thus turning high-side and low-side MOSFET off. When the driver cools down below 110°C after a thermal shutdown, it resumes normal operation and follows the PWM input signals.

Power-On-Reset (POR)

The APW7181 provides the power-on-reset function that keeps the driver disable when the VCC voltage is insufficient to driver external MOSFETs reliably. The PGATE outputs remain high and the NGATE outputs remain low until the VCC voltage exceeds POR threshold. Once the POR threshold is reached, the condition of gate driver outputs is defined by the PWM signals.

State		PGATE	NGATE
PWM Signal	L	L	L
	H	H	H
Thermal Shutdown		H	L

Table 1. Truth Table

Application Information

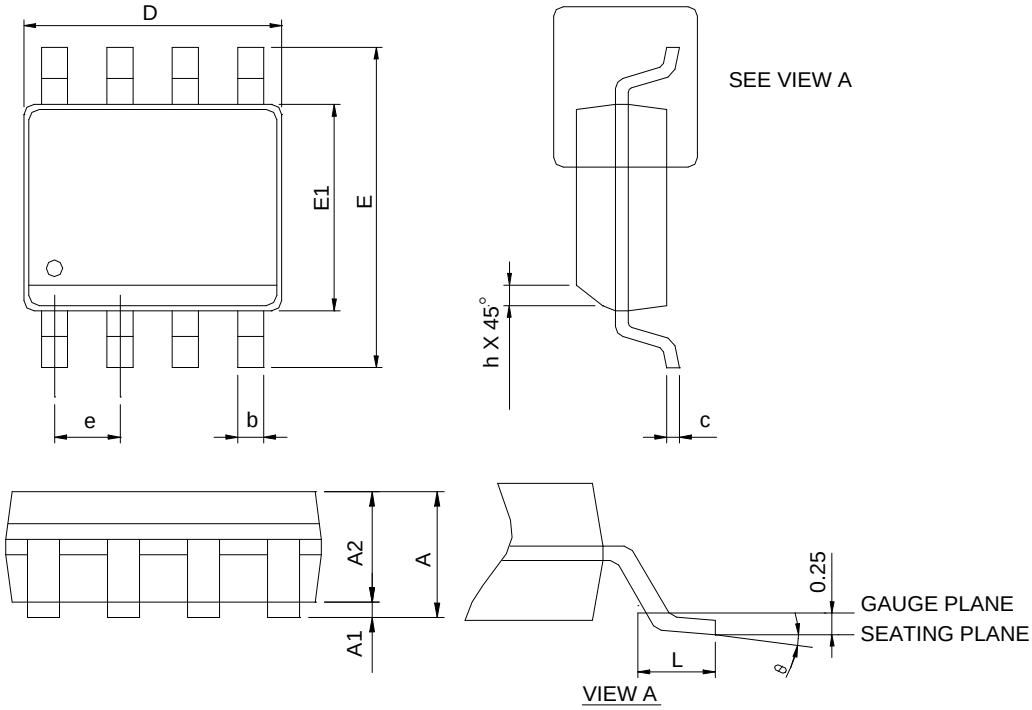
Layout Consideration

In any high switching frequency application, a correct layout is important to ensure proper operation of the device. With power devices switching at high frequency, the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic circuit elements. As an example, consider the turn-off transition of the PWM MOSFET. Before turn-off, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is free-wheeling by the lower MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short and wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike. Below is a checklist for your layout :

- Keep the switching nodes (PGATE, NGATE and the drain of the MOSFETs) away from sensitive small signal nodes (PWM1, PWM2, MS, and DTC) since these nodes are fast moving signals. Therefore, keep traces to these nodes as short as possible.
- Place the drain of the P-MOSFET and the drain of the N-MOSFET as close as possible to minimize the imped ance with wide layout plane between the two pads and reduce the voltage bounce of the node.
- The traces from the gate drivers to the MOSFETs (PGATE and NGATE) should be short and wide.
- The VCC decoupling capacitor (C7), C5, C6, and R_{DTC} should be close to their pins.
- The input capacitor should be near the source of the P-MOSFET.
- The drain of the MOSFETs should be a large plane for heat sinking.

Package Information

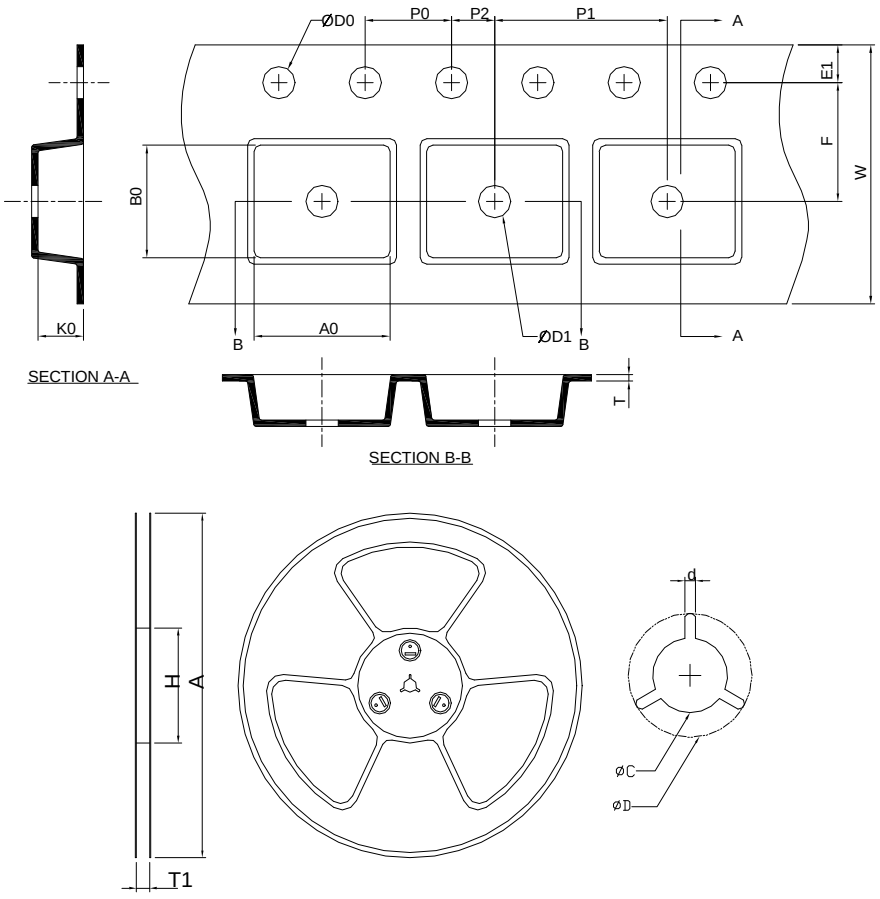
SOP-8



SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MS-012 AA.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension “E” does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOP-8	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20

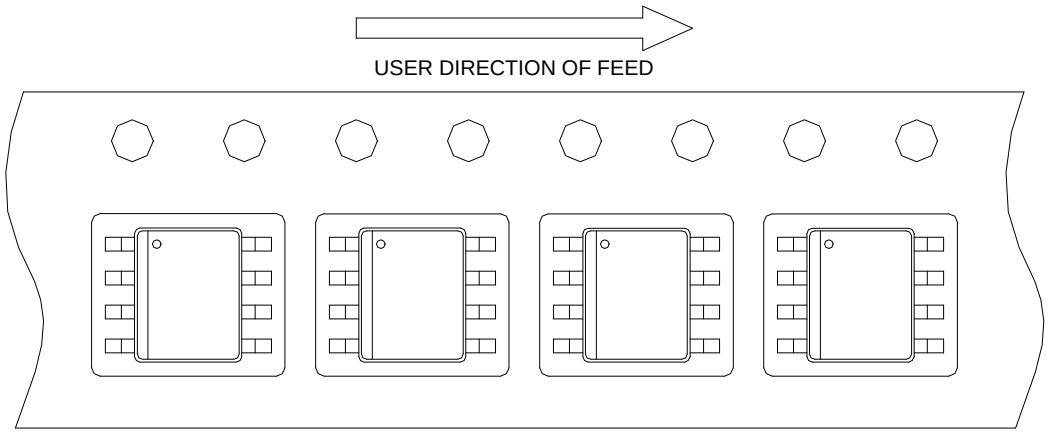
(mm)

Devices Per Unit

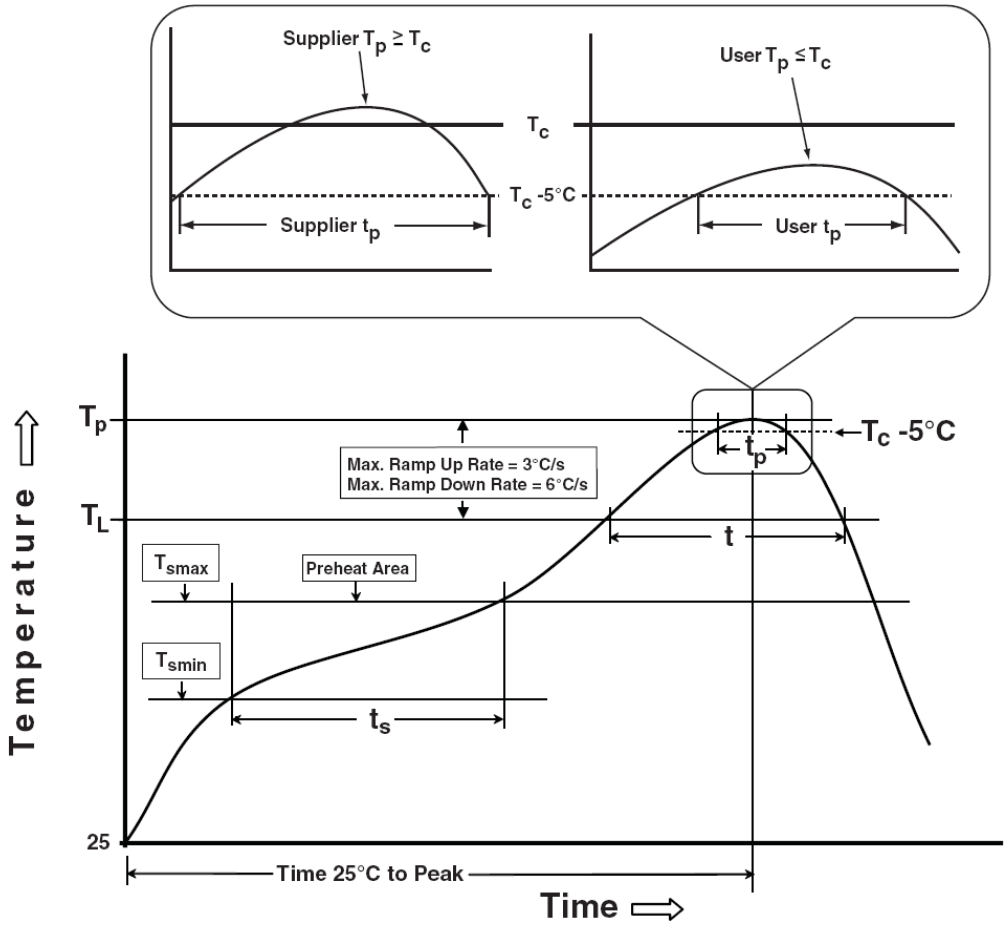
Package Type	Unit	Quantity
SOP-8	Tape & Reel	2500

Taping Direction Information

SOP-8



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ 125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
ESD	JESD-22, A114; A115	VHBM≧2KV, VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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