High-Performance Step-Down PWM Controller with PFM

Features

- Operates from An Input Battery Voltage Range of +3V to +25V
- ±0.6% 0.5V Reference
  - Over Line, Load Regulation, and Operating Temp.
- Drive Dual Low Cost N-Channel MOSFETs
  - Adaptive Shoot-Through Protection
- Power-On-Reset Monitoring on VCC Pin
- PFM Mode for Increasing Light Load Efficiency
- Constant-On-Time Control Scheme
  - Switching Frequency Compensation for PWM Operation
- 300kHz Constant Switching Frequency
- Integrated MOSFET Drivers and Bootstrap Diode
- Internal Soft-Start and Soft-Stop
- Power Good Monitoring
- 70% Under-Voltage Protection
- 125% Over-Voltage Protection
  - Using Low-Side MOSFETs $R_{DS(ON)}$
- Over-Temperature Protection
- TDFN-10 3mmx3mm Package
- Lead Free and Green Devices Available (RoHS Compliant)

Applications

- Notebook
- Low Cost PC
- Wide Input DC/DC Regulators

General Description

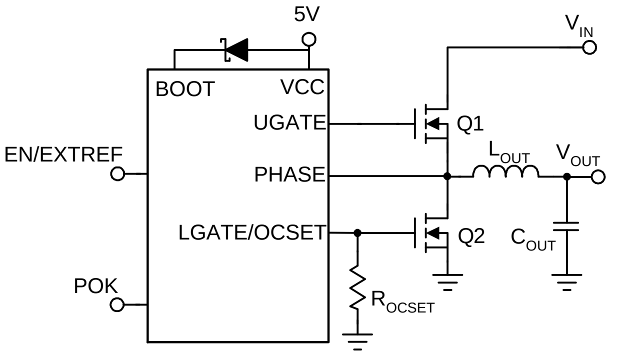
The APW7199 is a single-phase, constant-on-time, and synchronous PWM controller, which drives N-channel MOSFETs. An internal 0.5V temperature-compensated reference voltage with high accuracy is designed to meet the requirement of low output voltage applications. The APW7199 steps down high voltage to generate low-voltage chipset or RAM supplies in notebook computers.

The PWM controller operates fixed 300kHz pseudo-constant frequency PWM with an adaptive constant-on-time control. The device provides excellent transient response and accurate DC voltage output in either PFM or PWM Mode. In Pulse Frequency Mode (PFM), the APW7199 provides very high efficiency over light to heavy loads with loading-modulated switching frequencies. The device works in ultrasonic mode with PFM at no load. The unique ultrasonic mode maintains the switching frequency above 20kHz, which eliminates noise in audio applications.

The APW7199 is equipped with accurate over-current, output under-voltage, and output over-voltage protections. A Power-On-Reset function monitors the voltage on VCC to prevent wrong operation during power-on. The APW7199 has a 1.5ms digital soft-start to ramp up the output voltage to reduce the start-up current. A soft-stop function actively discharges the output capacitors with controlled reverse inductor current.

The APW7199 is available in TDFN3x3-10 package.

Simplified Application Circuit

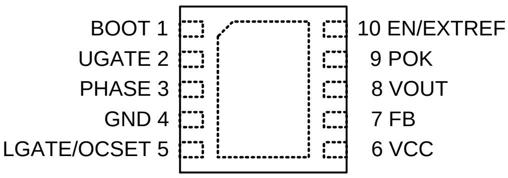


Ordering and Marking Information

APW7199 □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QB : TDFN3x3-10 Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW7199 QB : APW 7199 XXXXX	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Pin Configuration



TDFN3x3-10
(Top View)

= Thermal Pad (connected to GND plane for better heat dissipation)

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{CC}	VCC Supply Voltage (VCC to GND)	-0.3 ~ 7	V
$V_{BOOT-GND}$	BOOT Supply Voltage (BOOT to GND)	-0.3 ~ 32	V
V_{BOOT}	BOOT Supply Voltage (BOOT to PHASE)	-0.3 ~ 7	V
	All Other Pins (FB, VOUT, POK, and EN/EXTREF to GND)	-0.3 ~ V_{CC}+0.3	V
	UGATE Voltage (UGATE to PHASE) <400ns Pulse Width >400ns Pulse Width	 -5 ~ V_{BOOT}+0.3 -0.3 ~ V_{BOOT}+0.3	V
	LGATE/OCSET Voltage (LGATE to GND) <400ns Pulse Width >400ns Pulse Width	 -5 ~ V_{CC}+0.3 -0.3 ~ V_{CC}+0.3	V
V_{PHASE}	PHASE Voltage (PHASE to GND) <400ns Pulse Width >400ns Pulse Width	 -5 ~ 32 -1 ~ 25	V
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Thermal Resistance -Junction to Ambient (Note 2) TDFN3x3-10	55	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective the thermal conductivity test board in free air. The exposed pad of package is soldered directly on the PCB.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN}	Converter Input Voltage	3 ~ 25	V
V_{CC}	VCC Supply Voltage	4.5 ~ 5.5	V
V_{OUT}	Converter Output Voltage	0.5 ~ 3.3	V
I_{OUT}	Converter Output Current	0 ~ 25	A
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3 : Refer to the typical application circuit.

Electrical Characteristics

Refer to the typical application circuits. These specifications apply over V_{CC} = 5V, and T_A = -40 ~ 85°C, unless otherwise specified. Typical values are at T_A = 25°C.

Symbol	Parameter	Test Conditions	APW7199			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
$I_{VCC-PWM}$	VCC Input Bias Current	UGATE and LGATE Open	-	400	500	µA
$I_{VCC-PFM}$	VCC Input Bias Current	UGATE and LGATE Open	-	350	450	µA
I_{VCC_SHDN}	VCC Shutdown Current	$V_{EN/EXTREF}$ = 0V	-	-	7	µA
REFERENCE VOLTAGE						
V_{REF}	Reference Voltage		-	0.5	-	V
	Regulation Accuracy	T_A = -40°C ~ 85°C, I_{OUT} = 0 ~ 20A	-0.6	-	+0.6	%
	Line and Load Regulation	0A < I_{OUT} < 20A; 4V < V_{CC} < 5.5V	-0.2	-	+0.2	%
I_{FB}	FB Input Bias Current	V_{FB} = 0.5V	-0.5	-	0.5	µA
PWM CONTROLLER						
$T_{ON(MIN)}$	Minimum On Time of UGATE	Over-Temperature and V_{CC}	-	100	-	ns
$T_{OFF(MIN)}$	Minimum Off Time of UGATE	Over-Temperature and V_{CC}	-	300	-	ns
T_{SS}	Internal Soft-Start Time		1	1.5	2	ms
	VOUT Pin Input Impedance		-	130	-	kΩ
	VOUT Discharge Resistance		-	20	32	Ω
	Zero Crossing Voltage Threshold		-3	0	+3	mV
	PWM to PFM Debounce Time		-	20	-	µs
	PFM to PWM Debounce Time		-	20	-	µs

Electrical Characteristics (Cont.)

Refer to the typical application circuits. These specifications apply over V_{CC} = 5V, and T_A = -40 ~ 85°C, unless otherwise specified. Typical values are at T_A = 25°C.

Symbol	Parameter	Test Conditions	APW7199			Unit
			Min.	Typ.	Max.	
GATE DRIVER						
	UGATE Source Resistance	V_{BOOT} = 5V, V_{BOOT} - V_{UGATE} = 0.5V	-	1.5	3	Ω
	UGATE Sink Resistance	V_{BOOT} = 5V, V_{UGATE} - V_{PHASE} = 0.5V	-	1	2	Ω
	LGATE Source Resistance	V_{CC} = 5V, V_{CC} - V_{LGATE} = 0.5V	-	1.5	3	Ω
	LGATE Sink Resistance	V_{CC} = 5V, V_{LGATE} - V_{GND} = 0.5V	-	0.8	1.5	Ω
	Dead Time	(Note 4)	20	25	40	ns
BOOTSTRAP DIODE						
V_F	Forward Voltage	V_{CC} - $V_{BOOT-GND}$, I_F = 5mA	-	0.8	1	V
I_R	Reverse Leakage	$V_{BOOT-GND}$ = 30V, V_{PHASE} = 25V, V_{CC} = 5V	-	-	0.5	μA
VCC POWER-ON-RESET (POR) THRESHOLD						
V_{VCC_THR}	Rising VCC POR Threshold Voltage		4.05	4.2	4.35	V
	VCC POR Hysteresis		0.1	0.2	0.3	V
OSCILLATOR						
F_{SW}	Switching Frequency in PWM Mode	DC Output Current, V_{CC} = 4.5V ~ 5.5V	270	300	330	kHz
	Minimum Ultrasonic Operating Frequency	V_{CC} = 4.5V ~ 5.5V	20	25	-	kHz
CONTROL INPUTS						
	PWM Converter Shutdown Threshold	$V_{EN/EXTREF}$ Falling	-	-	0.4	V
	External Reference Voltage Input Range	V_{REF} = $V_{EN/EXTREF}$	0.5	-	2.5	V
	Internal Reference Enable Threshold	V_{REF} = 0.5V (typical), $V_{EN/EXTREF}$ Rising	2.75	-	-	V
	EN/EXTREF Leakage Current	$V_{EN/EXTREF}$ = 0V	-0.1	-	0.1	μA
	Maximum Voltage Slew Rate of V_{REF}	External reference voltage used, V_{REF} = $V_{EN/EXTREF}$	8	-	-	mV/μs
POWER OK INDICATOR (POK)						
V_{POK}	POK Threshold	V_{FB} is from low to target value (POK Goes High)	91	95	99	%
		~3μs noise filter, V_{FB} Falling (POK Goes Low)	65	70	75	%
		~3μs noise filter, V_{FB} Rising (POK Goes Low)	120	125	130	%
I_{POK}	POK Leakage Current	V_{POK} = 5V	-	0.1	1.0	μA
V_{POK}	POK Output Low Voltage	I_{POK} = -4mA	-	0.5	1	V
PROTECTIONS						
I_{OCSET}	I_{OCSET} Source Current	I_{OCSET} Sourcing	9	10	11	μA
V_{OCP_MAX}	Built-in Maximum OCP Voltage		230	250	270	mV

Electrical Characteristics (Cont.)

Refer to the typical application circuits. These specifications apply over V_{CC} = 5V, and T_A = -40 ~ 85°C, unless otherwise specified. Typical values are at T_A = 25°C.

Symbol	Parameter	Test Conditions	APW7199			Unit
			Min.	Typ.	Max.	
PROTECTIONS (CONT.)						
V_{UV}	Under-Voltage Protection Threshold		65	70	75	%
	Under-Voltage Protection Debounce Interval		-	2	-	µs
V_{OVR}	Over-Voltage Protection Rising Threshold		120	125	133	%
	Over-Voltage Protection Falling Threshold		100	105	110	%
	Over-Voltage Protection Debounce Interval		-	2	-	µs
T_{OTR}	Over-Temperature Protection Rising Threshold (Note 4)		-	150	-	°C
	Over-Temperature Protection Hysteresis (Note 4)		-	20	-	°C

Note4: Guaranteed by design.

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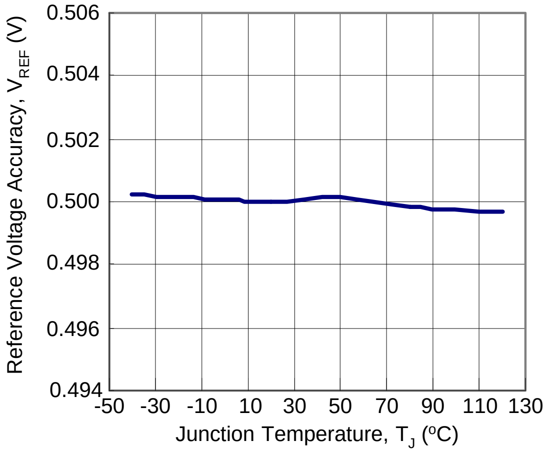
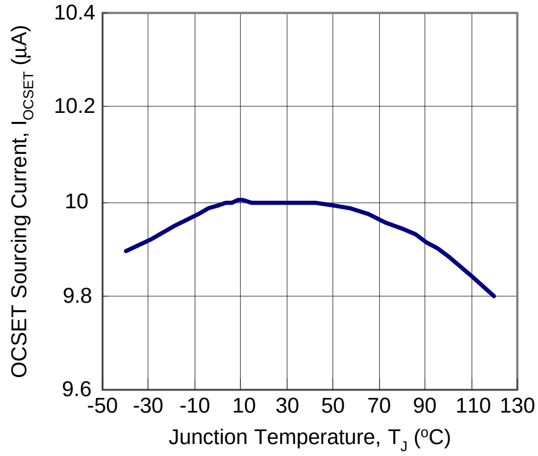
Typical Operating Characteristics

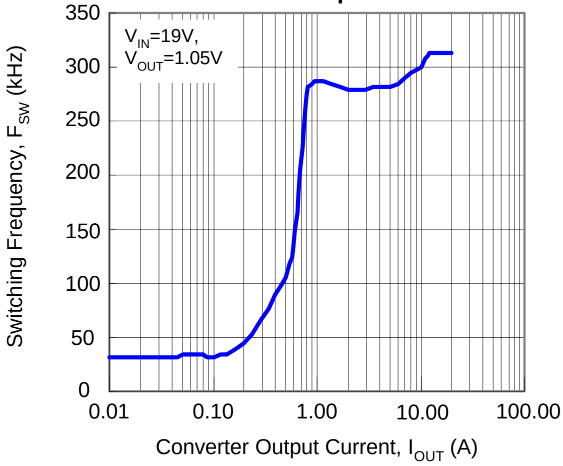
Reference Voltage Accuracy vs. Junction Temperature



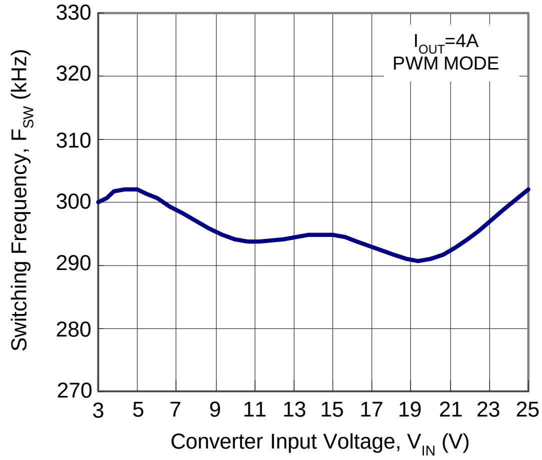
OCSET Sourcing Current vs. Junction Temperature



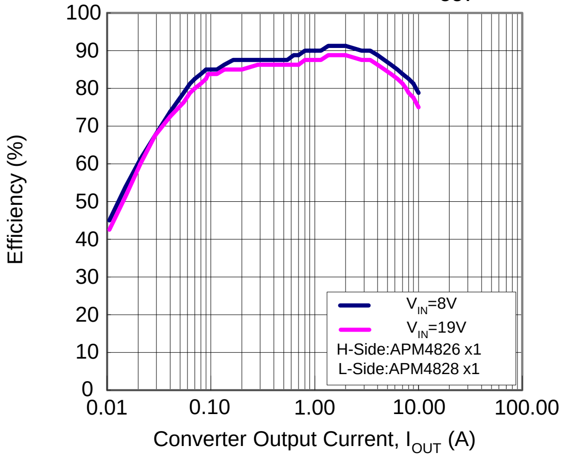
Switching Frequency vs. Converter Output Current



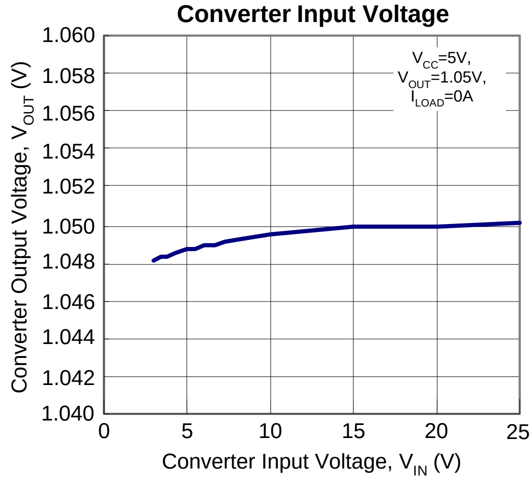
Switching Frequency vs. Converter Input Voltage



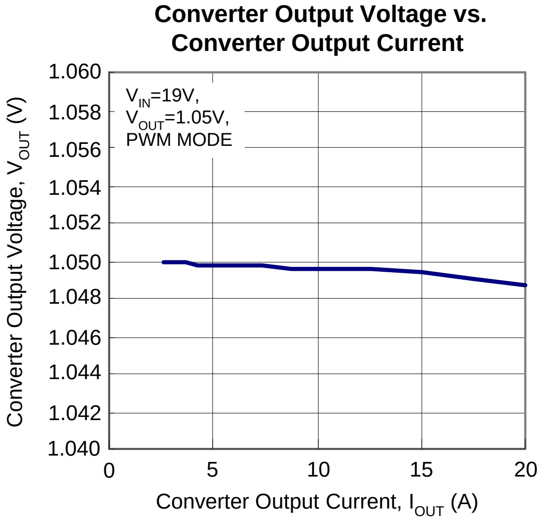
Efficiency vs. Load Current , V_{OUT}=1.05V



Converter Output Voltage vs. Converter Input Voltage



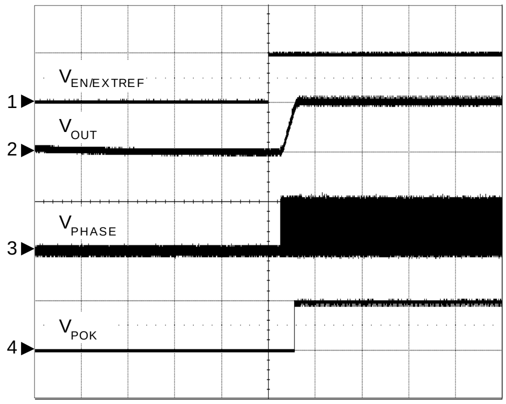
Typical Operating Characteristics (Cont.)



Operating Waveforms

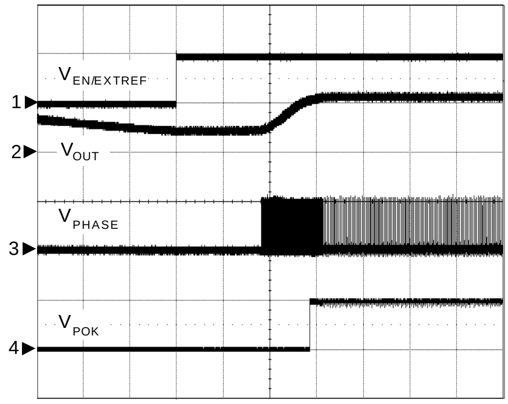
Refer to the typical application circuit. The test condition is V_{IN}=19V, T_A=25^{o}C unless otherwise specified.

Enable at Zero Initial Voltage of V_{OUT}



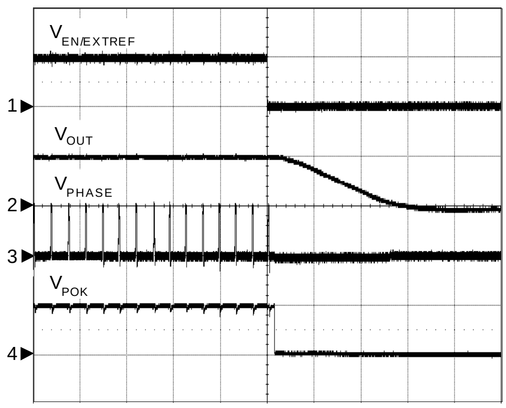
CH1: $V_{EN/EXTREF}$, 5V/Div, DC
CH2: V_{OUT}, 1V/Div, DC
CH3: V_{PHASE}, 20V/Div, DC
CH4: V_{POK}, 5V/Div, DC
TIME: 5ms/Div

Enable Before End of Soft-Stop



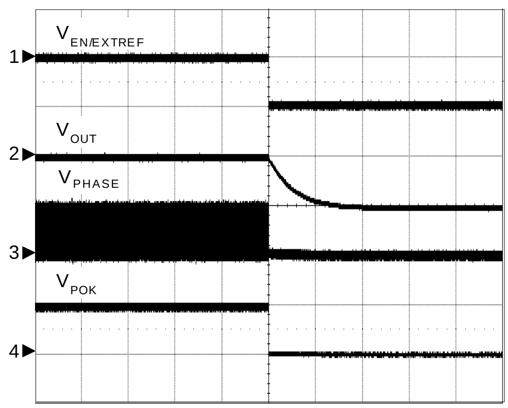
CH1: $V_{EN/EXTREF}$, 5V/Div, DC
CH2: V_{OUT}, 1V/Div, DC
CH3: V_{PHASE}, 20V/Div, DC
CH4: V_{POK}, 5V/Div, DC
TIME: 1ms/Div

Shutdown at I_{OUT}=20A



CH1: $V_{EN/EXTREF}$, 5V/Div, DC
CH2: V_{OUT}, 1V/Div, DC
CH3: V_{PHASE}, 20V/Div, DC
CH4: V_{POK}, 5V/Div, DC
TIME: 10μs/Div

Shutdown with Soft-Stop at No Load

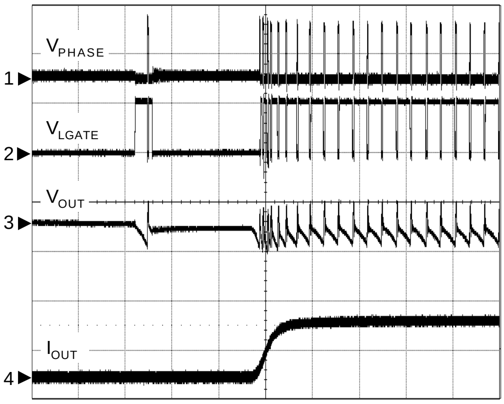


CH1: $V_{EN/EXTREF}$, 5V/Div, DC
CH2: V_{OUT}, 1V/Div, DC
CH3: V_{PHASE}, 20V/Div, DC
CH4: V_{POK}, 5V/Div, DC
TIME: 20ms/Div

Operating Waveforms (Cont.)

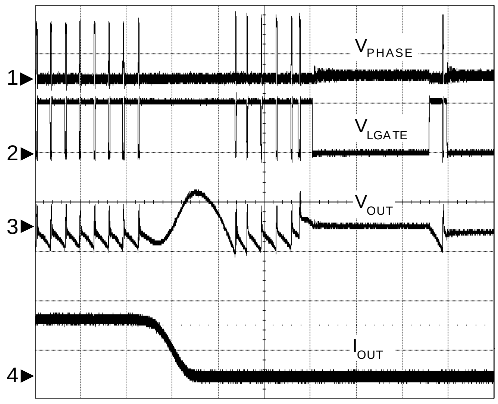
Refer to the typical application circuit. The test condition is V_{IN}=19V, T_A=25°C unless otherwise specified.

Load Transient
0A->10A



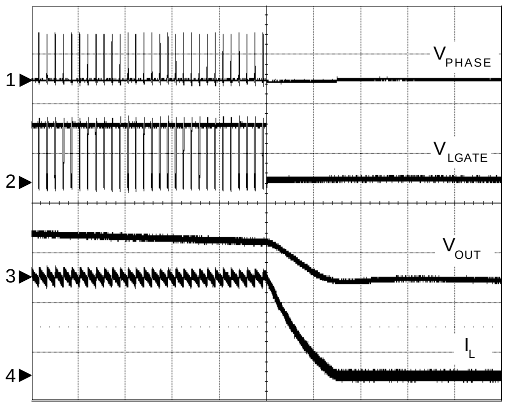
CH1: V_{PHASE}, 20V/Div, DC
CH2: V_{LGATE}, 5V/Div, DC
CH3: V_{OUT}, 50mV/Div, AC
CH4: I_{OUT}, 10A/Div, DC
TIME: 10μs/Div

Load Transient
10A->0A



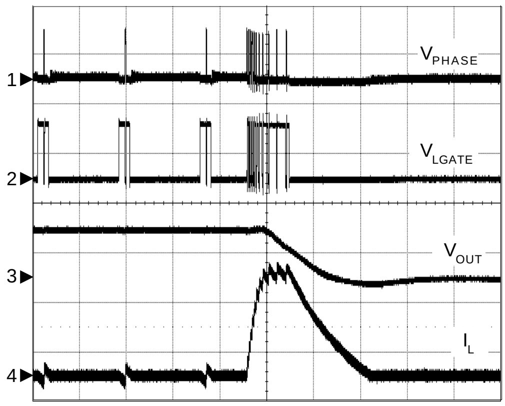
CH1: V_{PHASE}, 20V/Div, DC
CH2: V_{LGATE}, 5V/Div, DC
CH3: V_{OUT}, 50mV/Div, AC
CH4: I_{OUT}, 10A/Div, DC
TIME: 10μs/Div

Current-Limit and UV Protections



CH1: V_{PHASE}, 20V/Div, DC
CH2: V_{LGATE}, 5V/Div, DC
CH3: V_{OUT}, 1V/Div, DC
CH4: I_L, 10A/Div, DC
TIME: 20μs/Div

Short Circuit Test

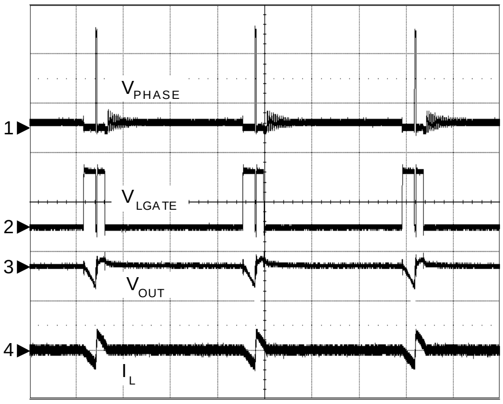


CH1: V_{PHASE}, 20V/Div, DC
CH2: V_{LGATE}, 5V/Div, DC
CH3: V_{OUT}, 1V/Div, DC
CH4: I_L, 10A/Div, DC
TIME: 20μs/Div

Operating Waveforms (Cont.)

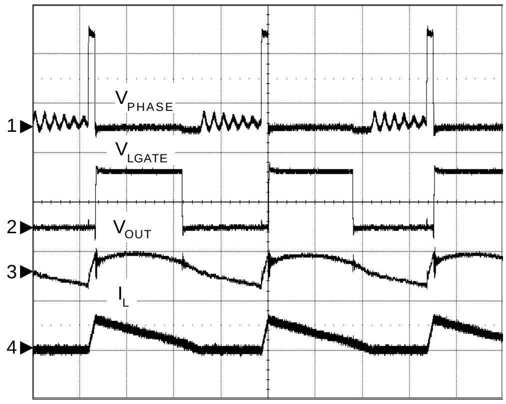
Refer to the typical application circuit. The test condition is V_{IN}=19V, T_A=25°C unless otherwise specified.

Operating at ULTRASONIC Mode



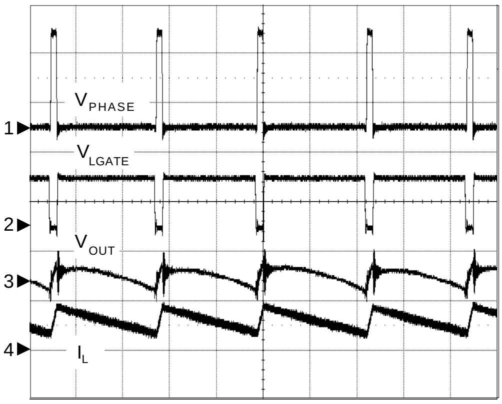
CH1: V_{PHASE}, 10V/Div, DC
CH2: V_{LGATE}, 5V/Div, DC
CH3: V_{OUT}, 50mV/Div, AC
CH4: I_L, 5A/Div, DC
TIME: 10μs/Div

Operating at PFM Mode



CH1: V_{PHASE}, 10V/Div, DC
CH2: V_{LGATE}, 5V/Div, DC
CH3: V_{OUT}, 50mV/Div, AC
CH4: I_L, 5A/Div, DC
TIME: 2μs/Div

Operating at PWM Mode

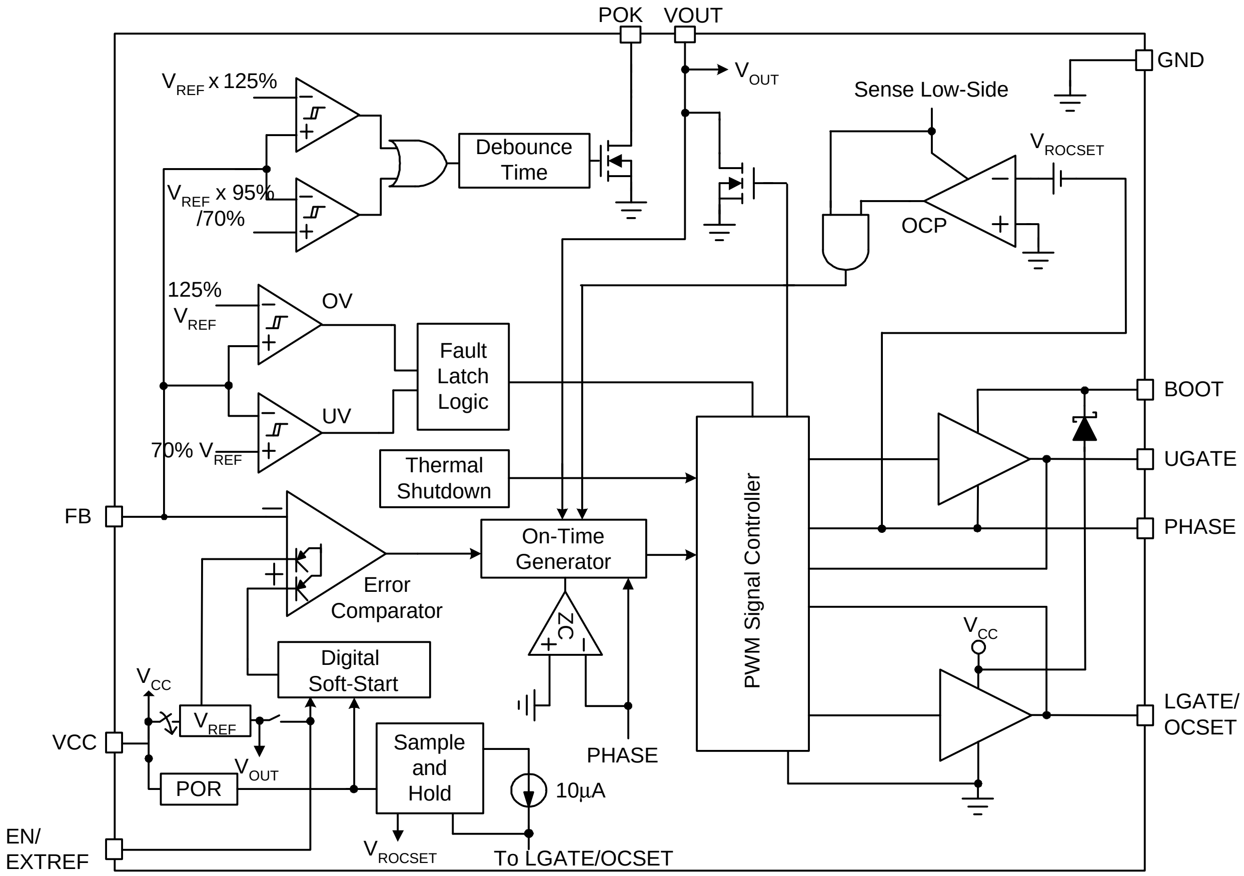


CH1: V_{PHASE}, 10V/Div, DC
CH2: V_{LGATE}, 5V/Div, DC
CH3: V_{OUT}, 50mV/Div, AC
CH4: I_L, 5A/Div, DC
TIME: 2μs/Div

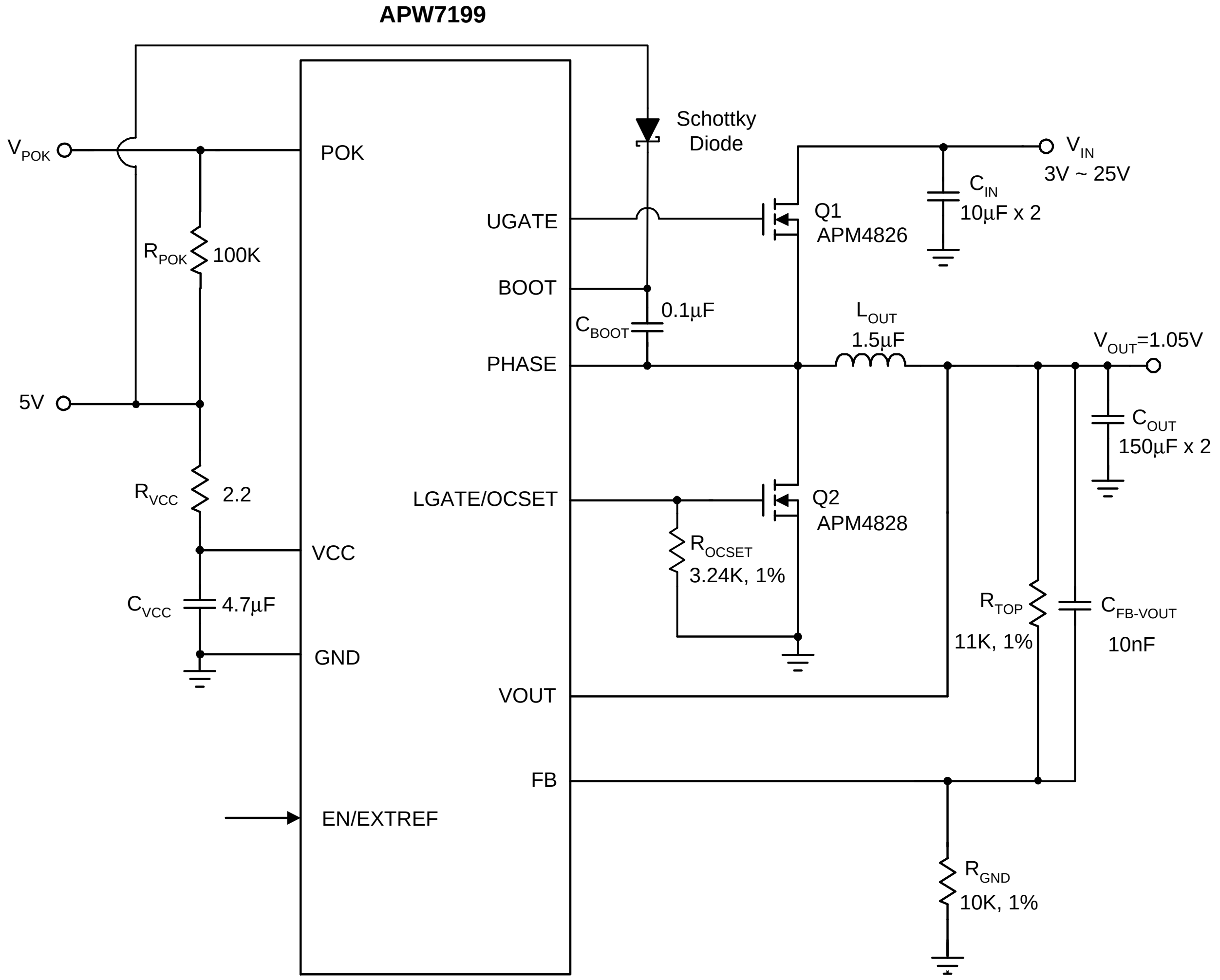
Pin Description

PIN		FUNCTION
NO.	NAME	
1	BOOT	This pin provides ground referenced bias voltage to the high-side MOSFET driver. A bootstrap circuit with a diode connected to 5V is used to create a voltage suitable to drive a logic-level N-channel MOSFET.
2	UGATE	Connect this pin to the high-side N-channel MOSFET's gate. This pin provides gate drive for the high-side MOSFET.
3	PHASE	The pin provides return path for the high-side MOSFET driver's pull-low current. Connect this pin to the high-side MOSFET's source.
4	GND	The GND terminal provides return path for the IC's bias current and the low-side MOSFET driver's pull-low current. Connect the pin to the system ground via very low impedance layout on PCBs.
5	LGATE/OCSET	Low-side Gate Driver Output and Over-Current Setting Input. This pin is the gate driver for low-side MOSFET.
6	VCC	Connect this pin to a 5V supply voltage. This pin provides bias supply for the control circuitry and the low-side MOSFET driver. The voltage at this pin is monitored for the Power-On-Reset (POR) purpose. Decoupling capacitor (4.7µF) be connected to GND for noise decoupling.
7	FB	Output Voltage Feedback pin. This pin is connected to the resistive divider that set the desired output voltage. The POK, UVP, and OVP circuits detect this signal to report output voltage status.
8	VOUT	The VOUT pin makes a direct measurement of the converter output voltage. The VOUT pin should be connected to the top feedback resistor at the converter output.
9	POK	POK is an open drain output used to indicate the status of the output voltage. Connect the POK pin to +5V through a pull-high resistor.
10	EN/EXTREF	Enable/Shutdown Pin or External Reference Selection of The PWM Controller.

Block Diagram



Typical Application Circuit



Function Description

Constant-On-Time PWM Controller with Input Feed-Forward

The constant-on-time control architecture is a pseudo-fixed frequency with input voltage feed-forward. This architecture relies on the output filter capacitor 's effective series resistance (ESR) to act as a current-sense resistor so the output ripple voltage provides the P WM ramp signal. In PFM operation, the high-side switch on-time controlled by the on-time generator is determined solely by a one-shot whose pulse width is inversely proportional to the input voltage and directly proportional to the output voltage. In P WM operation, the high-side switch on-time is determined by a switching frequency control circuit in the on-time generator block.

The switching frequency control circuit senses the switching frequency of the high-side switch and keeps regulating it at a constant frequency in PWM mode. The design improves the frequency variation and is more outstanding than a conventional constant-on-time controller, which has large switching frequency variation over input voltage, output current, and temperature. Both in PFM and PWM, the on-time generator, which senses input voltage on PHASE pin, provides very fast on-time response to input line transients.

Another one-shot sets a minimum off-time (typical: 300ns). The on-time one-shot is triggered if the error comparator is high, the low-side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

Pulse-Frequency Modulation (PFM)

In PFM mode, an automatic switchover to pulse-frequency modulation (PFM) takes place at light loads. This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current zero crossing. This mechanism causes the threshold between PFM and PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the critical conduction point). The on-time of PFM is given by:

$$T_{ON-PFM} = \frac{1}{F_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

Where F_{SW} is the nominal switching frequency of the converter in PWM mode.

The load current at handoff from PFM to P WM mode is given by:

$$I_{LOAD(PFMtoPWM)} = \frac{1}{2} \times \frac{V_{IN} - V_{OUT}}{L} \times T_{ON-PFM} = \frac{V_{IN} - V_{OUT}}{L} \times \frac{1}{F_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

In this case, APW7199 operates in ultrasonic mode with PFM when the load is zero. The ultrasonic mode is illustrated as below description.

Ultrasonic Mode

The ultrasonic mode activates an unique PFM mode with a minimum switching frequency of 20kHz. The minimum frequency 20kHz of ultrasonic mode eliminates audio-frequency interference in light load condition. It will transit to unique PFM mode when output loading makes the frequency bigger than ultrasonic frequency.

In ultrasonic mode, the controller automatically transits to fixed-frequency PWM operation when the load reaches the same critical conduction point ($I_{LOAD(PFM\ to\ PWM)}$).

When the controller detects that no switching has occurred within about 40 μs (Typical), an ultrasonic pulse will be occurred. The ultrasonic controller turns on the low-side MOSFET firstly to reduce the output voltage. After feedback voltage drops below the internal reference voltage, the controller turns off the low-side MOSFET and triggers a constant-on-time. When the constant-on-time has expired, the controller turns on the low-side MOSFET again until the inductor current is below the zero-crossing threshold. The behavior is the same as PFM mode.

Power-On-Reset (POR)

A Power-On-Reset (POR) function is designed to prevent wrong logic controls when the VCC voltage is low. The POR function continually monitors the bias supply voltage on the VCC pin if at least one of the enable pins is set high. When the rising VCC voltage reaches the rising POR voltage threshold (4.2V, typical), the POR signal goes high and the chip initiates soft-start operations. When this voltage drops lower than 4.0V (typical), the POR disables the chip.

Function Description (Cont.)

EN/EXTREF Pin Control

The voltage ($V_{EN/EXTREF}$) applied to EN/EXTREF pin selects either enable-shutdown or adjustable external reference. When $V_{EN/EXTREF}$ is above the EN high threshold (2.75V, typical), the PWM is enabled. When $V_{EN/EXTREF}$ is from 0.5V to 2.5V, the output voltage can be programmed as same as $V_{EN/EXTREF}$ voltage. When $V_{EN/EXTREF}$ is below the EN low threshold (0.4V, typical), the chip is in the shutdown and only low leakage current is taken from VCC. The slew rate of $V_{EN/EXTREF}$ must be faster than 0.5V/μs to avoid wrong output voltage.

Digital Soft-Start

The APW7199 integrates digital soft-start circuits to ramp up the output voltage of the converter to the programmed regulation setpoint at a predictable slew rate. The slew rate of output voltage is internally controlled to limit the inrush current through the output capacitors during soft-start process. The figure 1 shows soft-start sequence. When the EN/EXTREF pin is pulled above the rising EN threshold voltage, the V_{OCSET} voltage is equal to 10 μA x R_{OCSET}. When VCC rising POR threshold is triggered, the device starts to sample and hold the current-limit setting threshold. The sample time is as below:

$[I_{OCSET}(\mu A) \times R_{OCSET}(k\Omega) \times 4.0 + 70]\ \mu s.$

When current-limit setting action has finished, the device initiates a soft-start process to ramp up the output voltage. The soft-start interval, T_{SS}, is about 1.5ms (typical value).

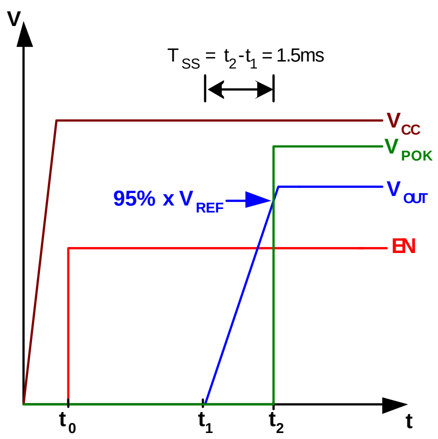


Figure 1. Soft-Start Sequence

During soft-start stage before the POK pin is ready, the under-voltage protection is prohibited. The over-voltage and over-current protection functions are enabled. If the output capacitor has residue voltage before start-up, both low-side and high-side MOSFETs are in off-state until the internal digital soft-start voltage is equal to the V_{FB} voltage. This will ensure that the output voltage starts from its existing voltage level.

In the event of under-voltage or shutdown, the chip enables the soft-stop function. The soft-stop function discharges the output voltages to the GND through an internal 20Ω switch. Cycling the EN/EXTREF enable signal or VCC power-on-reset signal can reset the latch.

Power OK Indicator

The APW7199 features an open-drain POK pin to indicate output regulation status. In normal operation, when the output voltage rises 95% of its target value, the POK goes high. When the output voltage outruns 70% or 125% of the target voltage, POK signal will be pulled low immediately.

Since the FB pin is used for both feedback and monitoring purposes, the output voltage deviation can be coupled directly to the FB pin by the capacitor in parallel with the voltage divider as shown in the typical applications. In order to prevent false POK from dropping, capacitors need to parallel at the output to confine the voltage deviation with severe load step transient and the POK comparator has a built-in 3 μs noise filter.

Under-Voltage Protection (UVP)

In the operational process, if a short-circuit occurs, the output voltage will drop quickly. When load current is bigger than current-limit threshold value, the output voltage will fall out of the required regulation range. The under-voltage protection circuit continually monitors the V_{FB} after soft-start is completed. If a load step is strong enough to pull the output voltage lower than the under-voltage threshold, the device starts to soft-stop process to shut down the output gradually. The under-voltage threshold is 70% of the normal output voltage. The under-voltage comparator has a built-in 2μs noise filter to prevent the chip from wrong UVP shutdown caused by noise. Cycling the EN/EXTREF enable signal or VCC power-on-reset signal can reset the latch.

Function Description (Cont.)

Over-Voltage Protection (OVP)

The over-voltage function monitors the output voltage by the FB pin. When the FB voltage increases over 125% of the reference voltage due to the high-side MOSFET failure or for other reasons, the over-voltage protection comparator designed with a 2μs noise filter will force the low-side MOSFET gate driver fully turn on. This action actively pulls down the output voltage. When the FB voltage decreases below 105%, the OVP comparator is disengaged and both high-side and low-side drivers turn off.
This OVP scheme only clamps the voltage overshoot, and does not invert the output voltage when otherwise activated with a continuously high output from low-side MOSFET driver. Its a common problem for OVP schemes with a latch. Once an over-voltage fault condition is set, it can only be reset by toggling EN/EXTREF or VCC power-on-reset signal.

Current-Limit

The current-limit circuit employs a "valley" current-sensing algorithm (See Figure 2). The APW7199 uses the low-side MOSFET $R_{DS(ON)}$ of the synchronous rectifier as a current-sensing element. If the magnitude of the current-sense signal at PHASE pin is above the current-limit threshold, the PWM is not allowed to initiate a new cycle. The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are the functions of the sense resistance, inductor value, and input voltage.

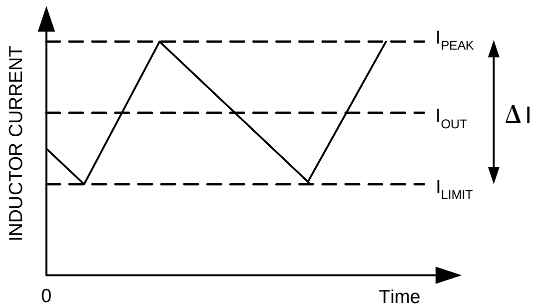


Figure 2. Current-Limit Algorithm

A resistor (R_{OCSET}), connected from the LGATE/OCSET to GND, programs the current-limit threshold. Before the IC initiates a soft-start process, an internal current source, I_{OCSET} (10μA typical), flowing through the R_{OCSET} develops a voltage (V_{OCSET}) across the R_{OCSET}. The device holds V_{OCSET} and stops the current source, I_{OCSET}, during normal operation. The relationship between the sampled voltage V_{OCSET} and the current-limit threshold I_{LIMIT} is given by:

$$10\mu A \times R_{OCSET} = I_{LIMIT} \times R_{DS(ON)}$$

I_{LIMIT} can be expressed as I_{OUT} minus half of peak-to-peak inductor current.
The APW7199 has an internal current-limit voltage (V_{OCSET_MAX}), and the value is 0.25V typicalWhen the R_{OCSET} x I_{OCSET} exceeds 0.25V or the R_{OCSET} is floating or not connected, the over current threshold will be the internal default value 0.25V.
The PCB layout guidelines should ensure that noise and DC errors do not corrupt the current-sense signals at PHASE. Place the hottest power MOSEF Ts as close to the IC as possible for best thermal coupling. When combined with the under-voltage protection circuit, this current-limit method is effective in almost every circumstance.

Over-Temperature Protection (OTP)

When the junction temperature increases above the rising threshold temperature TOTR, the IC will enter the over-temperature protection state that suspends the PWM, which forces the UG ATE and LGATE gate drivers output low. The thermal sensor allows the converters to start a start-up process and regulate the output voltage again after the junction temperature cools by 20°C. The OTP is designed with a 20°C hysteresis to lower the average T_J during continuous thermal overload conditions, which increases lifetime of the APW7199.

Application Information

Output Voltage Setting

The output voltage is adjustable from 0.5V to 3.3V with a resistor-divider connected with FB, GND, and converter's output. The voltage ($V_{EN/EXTREF}$) applied to EN/EXTREF pin selects adjustable external reference from 0.5V to 2.5V. Using 1% or better resistors for the resistor-divider is recommended. The output voltage is determined by:

$$V_{OUT} = 0.5 \times \left(1 + \frac{R_{TOP}}{R_{GND}}\right)$$

Where 0.5 is the reference voltage, R_{TOP} is the resistor connected from converter's output to FB, and R_{GND} is the resistor connected from FB to GND. Suggested R_{GND} is in the range from 1K to 20k Ω. To prevent stray pickup, locate resistors R_{TOP} and R_{GND} close to APW7199. Similarly, when $V_{EN/EXTREF}$ is from 0.5V to 2.5V, the output voltage can be programmed as same as $V_{EN/EXTREF}$ voltage.

Output Inductor Selection

The duty cycle (D) of a buck converter is the function of the input voltage and output voltage. Once an output voltage is fixed, it can be written as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

The inductor value (L) determines the inductor ripple current, I_{RIPPLE}, and affects the load transient response. Higher inductor value reduces the inductor's ripple current and induces lower output ripple voltage. The ripple current and ripple voltage can be approximated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{F_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Where F_{SW} is the switching frequency of the regulator. Although the inductor value and frequency are increased and the ripple current and voltage are reduced, a tradeoff exists between the inductor's ripple current and the regulator load transient response time.
A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current. Increasing the switching frequency (F_{SW}) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFETs and the power dissipation of the converter. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current. Once the inductance value has been chosen, selecting an inductor which is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This results in a larger output ripple voltage. Besides, the inductor needs to have low DCR to reduce the loss of efficiency.

Output Capacitor Selection

Output voltage ripple, the transient voltage deviation and the stability issue are factors which have to be taken into consideration when selecting an output capacitor. Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Generally, selecting high performance low ESR capacitors is recommended for switching regulator applications. In addition to high frequency noise related to MOSFET turn-on and turn-off, the output voltage ripple includes the capacitance voltage drop ΔV_{COUT} and ESR voltage drop ΔV_{ESR} caused by the AC peak-to-peak inductor's current. These two voltages can be represented by:

$$\Delta V_{COUT} = \frac{I_{RIPPLE}}{8 C_{OUT} F_{SW}}$$

$$\Delta V_{ESR} = I_{RIPPLE} \times R_{ESR}$$

These two components constitute a large portion of the total output voltage ripple. In some applications, multiple capacitors have to be paralleled to achieve the desired ESR value. If the output of the converter has to support another load with high pulsating current, more capacitors are needed in order to reduce the equivalent ESR and suppress the voltage ripple to a tolerable level.
Nevertheless, the constant-on-time (COT) control architecture relies on the output capacitor's ESR to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal. For stability issue, the output ripple also need to be considered. By stability experiment result, we suggest the feedback ripple is above 25mV when operated in the internal mode and above 40mV when operated in the external mode.
To support a load transient that is faster than the switching frequency, more capacitors are needed for reducing

Application Information (Cont.)

Output Capacitor Selection (Cont.)

the voltage excursion during load step change. Another aspect of the capacitor selection is that the total AC current going through the capacitors has to be less than the rated RMS current specified on the capacitors in order to prevent the capacitor from over-heating.

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, selecting the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage. The maximum RMS current rating requirement is approximately $I_{OUT}/2$, where I_{OUT} is the load current. During power-up, the input capacitors have to handle great amount of surge current. For low-duty notebook appliactions, ceramic capacitor is recommended. The capacitors must be connected between the drain of high-side MOSFET and the source of low-side MOSFET with very low-impeadance PCB layout.

MOSFET Selection

The selection of the N-channel power MOSFETs are determined by the $R_{DS(ON)}$, reversing transfer capacitance (C_{RSS}) and maximum output current requirement. The losses in the MOSFETs have two components: conduction loss and transition loss. For the high-side and low-side MOSFETs, the losses are approximately given by the following equations:

$$P_{high\text{-}side} = I_{OUT}^2(1+TC)(R_{DS(ON)})D + (0.5)(I_{OUT})(V_{IN})(t_{SW})F_{SW}$$
$$P_{low\text{-}side} = I_{OUT}^2(1+TC)(R_{DS(ON)})(1-D)$$

Where

I_{OUT} is the load current
TC is the temperature dependency of $R_{DS(ON)}$
F_{SW} is the switching frequency
t_{SW} is the switching interval
D is the duty cycle

Note that both MOSFE Ts have conduction losses while the high-side MOSFET includes an additional transition loss. The switching interval, t_{SW}, is the function of the reverse transfer capacitance C_{RSS}. The (1+TC) term is a factor in the temperature dependency of the $R_{DS(ON)}$ and can be extracted from the "$R_{DS(ON)}$ vs. Temperature" curve of the power MOSFET.

Layout Consideration

In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator. With power devices switching at higher frequency, the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic circuit elements. As an example, consider the turn-off transition of the P WM MOSFET. Before turn-off condition, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is freewheeling by the low side MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short and wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike. Besides, signal and power grounds are to be kept separating and finally combined using ground plane construction or single point grounding. Figure 3 illustrates the layout, with bold lines indicating high current paths; these traces must be short and wide. Components along the bold lines should be placed lose together. Below is a checklist for your layout:

- Keep the switching nodes (UGATE, LGATE/OCSET, BOOT, and PHASE) away from sensitive small signal nodes since these nodes are fast moving signals. Therefore, keep traces to these nodes as short as possible and there should be no other weak signal traces in parallel with theses traces on any layer.
- The signals going through theses traces have both high dv/dt and high di/dt with high peak charging and discharging current. The traces from the gate drivers to the MOSFETs (UGATE and LGATE/OCSET) should be short and wide.
- Place the source of the high-side MOSFET and the drain of the low-side MOSFET as close as possible. Minimizing the impedance with wide layout plane between the two pads reduces the voltage bounce of the node. In addition, the large layout plane between the drain of the MOSFETs (V_{IN} and PHASE nodes) can get better heat sinking.
- Decoupling capacitors, the resistor-divider, and boot capacitor should be close to their pins. (For example, place the decoupling ceramic capacitor close to the drain of the high-side MOSFET as close as possible.)

Application Information (Cont.)

Layout Consideration (Cont.)

- The input bulk capacitors should be close to the drain of the high-side MOSFET, and the output bulk capacitors should be close to the loads. The input capacitor's ground should be close to the grounds of the output capacitors and low-side MOSFET.
- Locate the resistor-divider close to the FB pin to minimize the high impedance trace. In addition, FB pin traces can't be close to the switching signal traces (UG ATE, LGATE/OCSET, BOOT, and PHASE).
- The R_{OCSET} resistance should be placed near the IC as close as possible.

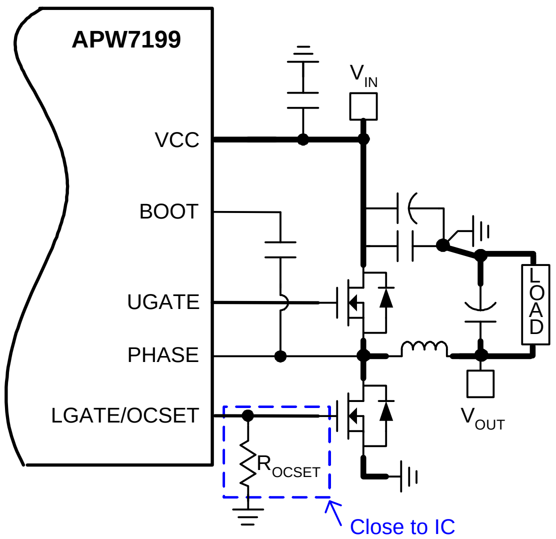
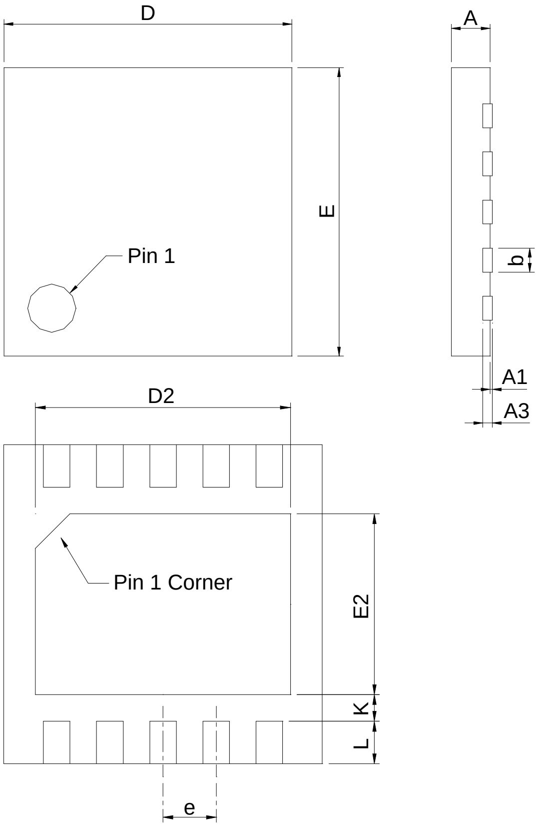


Figure 3.

Package Information

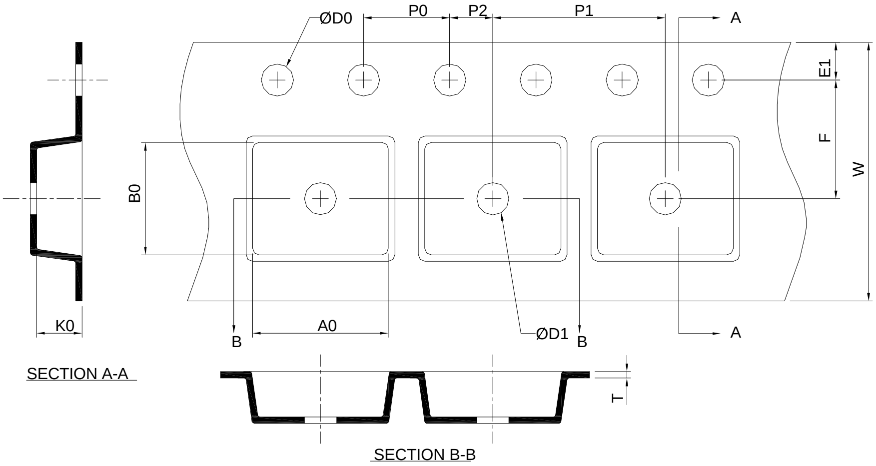
TDFN3x3-10

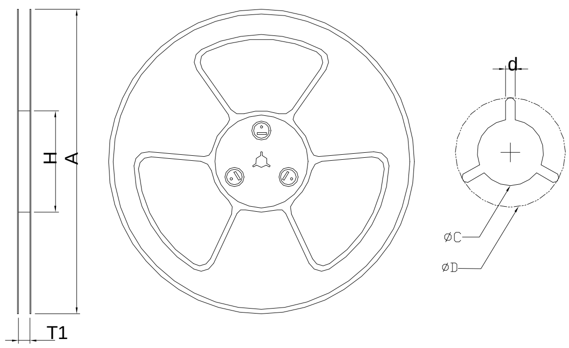


SYMBOL	TDFN3x3-10			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
D2	2.20	2.70	0.087	0.106
E	2.90	3.10	0.114	0.122
E2	1.40	1.75	0.055	0.069
e	0.50 BSC		0.020 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	

Note : 1. Followed from JEDEC MO-229 VEED-5.

Carrier Tape & Reel Dimensions





Application	A	H	T1	C	d	D	W	E1	F
TDFN3x3-10	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.20	1.75±0.10	3.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.35±0.20	3.35±0.20	1.30±0.20

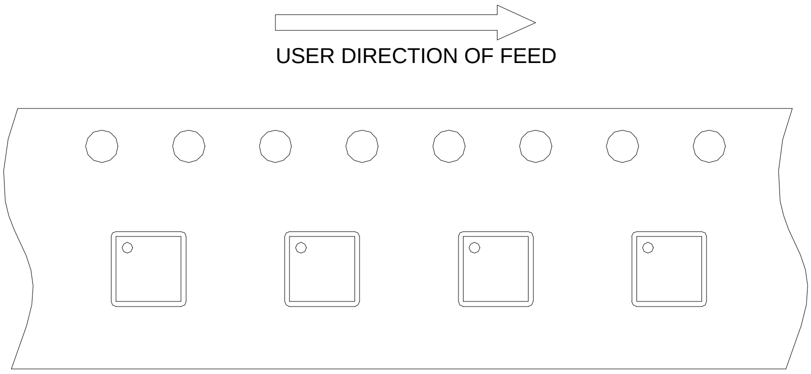
(mm)

Devices Per Unit

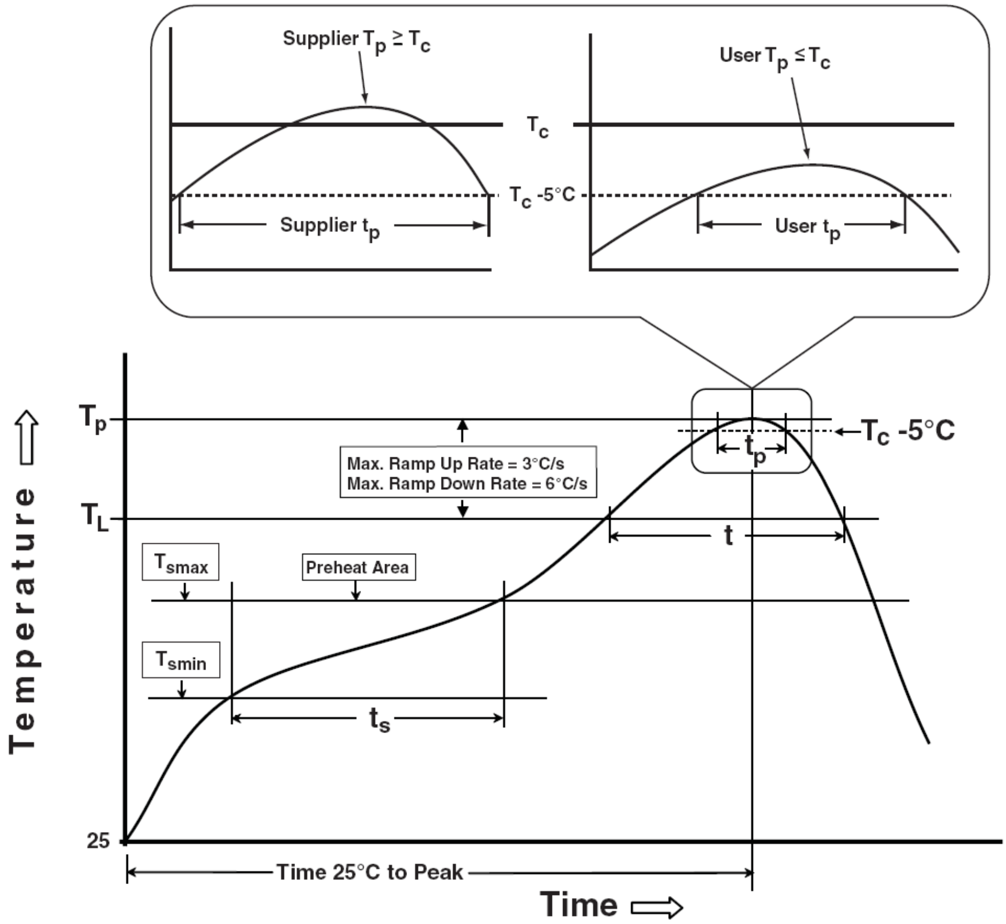
Package Type	Unit	Quantity
TDFN3x3-10	Tape & Reel	3000

Taping Direction Information

TDFN3x3-10



Classification Profile



Classification Reflow Profiles (Cont.)

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.

* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum.
** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ^{3}350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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