Two Channel Regulators and Three Channel Buck Converters PMIC

Features

- **Wide Input Operating Range: 2.9V~5.5V**
- **Three Synchronous Buck Regulators for SoC**
  - **-Adjustable Output with 1500mA Output for Core Power**
  - **-Adjustable Output with 1000mA Output for Memory Power**
  - **-Adjustable Output with 1000mA Output for System Power**
  - **-1.5MHz Switching Frequency**
  - **-High Efficient up to 93%**
- **Tow Low-Dropout Linear Regulators for Sensor:**
  - **-Adjustable 300mA Output High PSRR, Low Noise**
  - **-Adjustable 300mA Output High PSRR, Low Noise**
- **Thermal-Overload Protection**
- **Power-OK Indicator after CH2 Ready**
- **TQFN3x3-20 Package**
- **Lead Free Green Devices Available (RoHS Compliant)**

General Description

The APW7255 is a two P-channel low dropout linear regulator and three synchronous buck converter which needs input voltage from 2.9 to 5.5V.

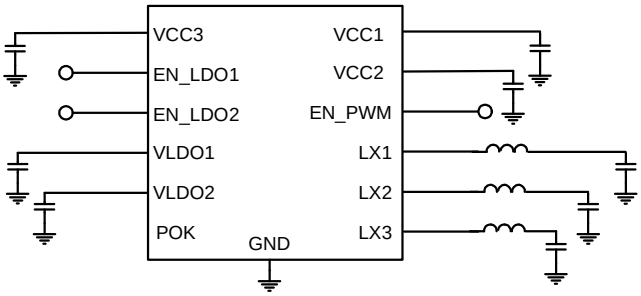
Synchronous buck converter with integrated high side and low side power MOSFET. It is equipped with an automatic PSM/PWM mode operation. At light load , the IC operates in the PSM mode to reduce the switching losses. At heavy load, the IC works in PWM mode.

Low dropout linear regulator delivers current up to 300mA to set output voltage, and it also can work with low ESR ceramic capacitors. Typical dropout voltage is only 240mV at 300mA loading.

The APW7255 is equipped with Power-on-reset, shutdown control, soft start, over-temperature and current-limit into a single package to protect the device against wrong logic control and over-temperature and current over-loads.

The APW7255 available TQFN3x3-20 provides a very compact system solution external components and PCB area.

Simplified Application Circuit

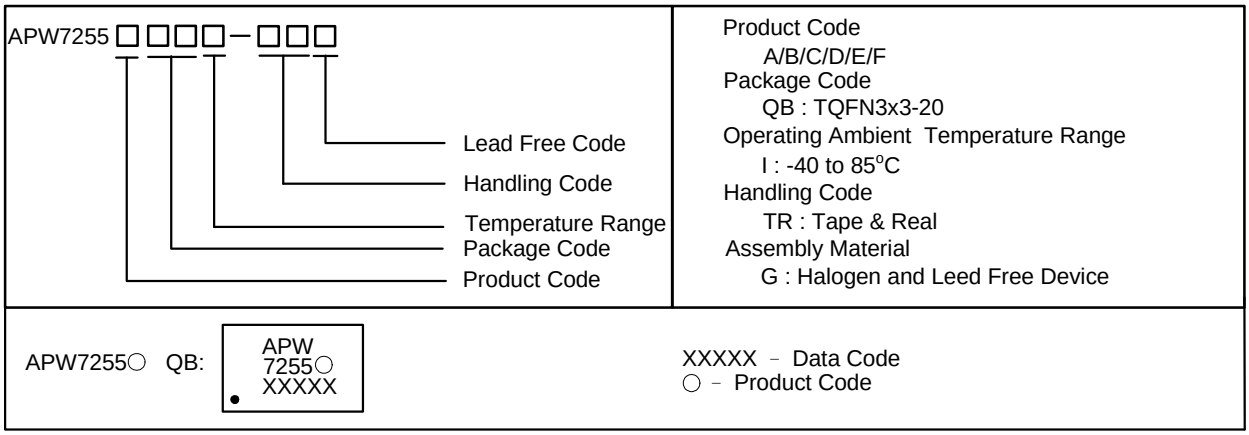


Applications

- **IP-Cam**
- **Car Recorder**
- **Security**

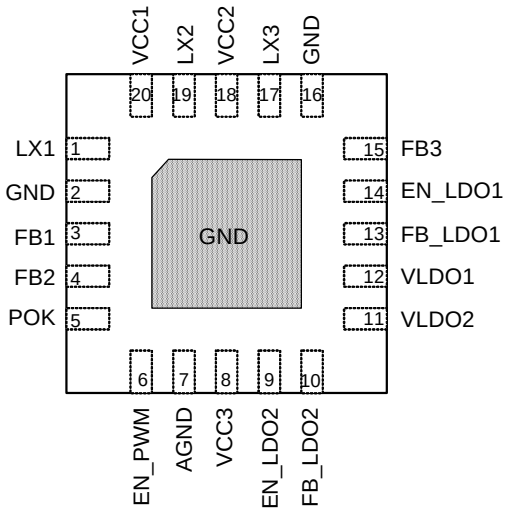
ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information



Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Pin Configuration



Absolute Maximum Ratings (Note 1)

Symbol	Parameter		Rating	Unit
	VCC1, VCC2, VCC3, VLDO1, VLDO2 to GND Voltage		-0.3 ~ 7	V
	LX1 LX2 LX3 to GND Voltage	>20ns	-1 ~ (V_{CC1}, V_{CC2}, V_{CC3})+0.3	V
		<20ns	-3 ~ (V_{CC1}, V_{CC2}, V_{CC3})+3	V
	All other pins		-0.3 ~7	V
	Power Dissipation		Internally Limited	W
T_J	Maximum Junction Temperature		-40 ~ 150	°C
T_{STG}	Storage Temperature		-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)		260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Thermal Characteristics (Note 2, 3)

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	50	°C/W
θ_{JC}	Junction-to-Case Resistance in free air (Note 3)	12	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad is soldered directly on the PCB.
Note 3: The case temperature is measured at the center of the exposed pad on the underside.

Recommended Operating Conditions (Note 4)

Symbol	Parameter	Range	Unit
V_{CCX}	VCC1, VCC2, VCC3 Supply Voltage	2.9 ~ 5.5	V
I_{OUTX}	Converter Output Current	0 ~ 2	A
I_{LDOX}	VLDO1, VLDO2 Output Current	0 ~ 0.3	A
L	Inductor	0.47~2.2	µH
C_{OUTX}	VOUT1, VOUT2, VOUT3 Output Capacitor	4.7~22	µF
C_{LDOX}	VLDO1, VLDO2 Output Capacitor	1~22	µF
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 4: Refer to the typical application circuit.

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Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{CC1}, V_{CC2}, V_{CC3}=5V, V_{EN_LDO1}=V_{EN_LDO2}=V_{EN_PWM}=5V. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7255			Unit
			Min	Typ	Max	
VCC3 SUPPLY CURRENT						
I_{VCC3}	Quiescent Current	T_A=25°C	-	300	550	uA
I_{VCC3_SD}	Shutdown Input Current	EN_PWM = EN_LDO1 = EN_LOD2 = GND			1	uA
POWER-ON-RESET (PWM/LDO)						
	POR Threshold		2.3	2.6	2.85	V
	POR Hysteresis		-	0.25	-	V
REFERENCE VOLTAGE(PWM, LDO)						
	Reference Voltage		-	0.6	-	V
		T_A=-40~85 °C	-2	-	2	%
OUTPUT VOLTAGE (PWM)						
	Output Voltage Accuracy	I_{OUT1}= I_{OUT2}=0mA~0.8A, I_{OUT3}= 0mA~1.5A, V_{CC1}, V_{CC2} =2.9~5.5V, T_A=-40~85 °C	-2.5	-	2.5	%
OUTPUT VOLTAGE (LDO)						
	Output Voltage Accuracy	I_{LDO1}= I_{LDO2}= 1mA~0.3A, V_{CC3} =2.9~5.5V, T_A=-40~85 °C	-3		3	%
	Line Regulation	I_{LDO1}= I_{LDO2}=1mA, V_{CC3}=(V_{LDO1}, V_{LDO2})+1V to 5.5V	-	-	0.2	%/V
	Load Regulation	I_{LDO1}= I_{LDO2}=1mA to 300mA, V_{CC3}=(V_{LDO1}, V_{LDO2})+1V	-	-	0.6	%
V_{DROP}	Dropout Voltage	I_{LDOX}=300mA	-	240	330	mV
PSRR	Power Supply Rejection Ratio	I_{LDOX}=50mA, C_{LDOX}=2.2µF, f=100Hz	-	70	-	dB
		f=1kHz	-	70	-	
		f=10kHz	-	60	-	
		f=100kHz	-	35	-	
	Output Noise	I_{LDOX}=1mA, BW=10 to 100kHz, C_{LDOX}=10µF	-	100	-	μV_{RMS}
	V_{LDO1}, V_{LDO2} Discharge Resistance	V_{EN_LDO1}=V_{EN_LDO2}=0V	-	3	-	kΩ
POWER MOSFETS(PWM)						
R_{P-FET}	CH1, 2 High Side P-MOS $R_{DS(ON)}$	I_{LX1}= I_{LX2}=200mA	-	0.35	0.4	Ω
	CH3 High Side P-MOS $R_{DS(ON)}$	I_{LX3}=200mA	-	0.3		Ω
R_{N-FET}	CH1, 2 low Side N-MOS $R_{DS(ON)}$	I_{LX1}= I_{LX2}=200mA	-	0.35	0.4	Ω
	CH3 low Side N-MOS $R_{DS(ON)}$	I_{LX3}=200mA	-	0.3	-	Ω

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Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{CC1}, V_{CC2}, V_{CC3}=5V, V_{EN_LDO1}=V_{EN_LDO2}=V_{EN_PWM}=5V. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7255			Unit
			Min	Typ	Max	
POWER MOSFETS(PWM)						
	High Side MOSFET Leakage Current	V_{EN_PWM}=0V, V_{LX1}=V_{LX2}=V_{LX3}=0V, V_{CC1}= V_{CC2}=5V	-	-	1	μA
	Low Side MOSFET Leakage Current	V_{EN_PWM}=0V, V_{LX1}=V_{LX2}=V_{LX3}=5V, V_{CC1}= V_{CC2}=5V	-	-	1	μA
CURRENT-MODE CONVERTER(PWM)						
	Switch Current to COMP Voltage Transconductance		-	5.2	-	A/V
T_D	Dead Time			10		ns
ENABLE AND INPUT CURRENTS(PWM, LDO)						
	EN Input High Threshold	V_{CC1}, V_{CC2}, V_{CC3}=2.9V~5.5V	1	-	-	V
	EN Input Low Threshold	V_{CC1}, V_{CC2}, V_{CC3}=2.9V~5.5V	-	-	0.4	V
	EN Leakage Current	V_{EN_LDOX}= V_{EN_PWM}=5V	-1	-	1	μA
POWER-OK AND DELAY(PWM)						
	POK Threshold(POK goes high)	V_{FB2} rising	-	87.8	-	%V_{REF}
	POK Threshold Hysteresis	V_{FB2} Falling	-	3	-	%V_{REF}
	POK Delay Time	The time from V_{FB}=90%*V_{FB} to POK goes high	-	Version different	-	us
	POK Pull Low Resistance	V_{POK}=0.1V	-	100	-	Ω
	POK Leakage Current	EN=0V, V_{PG} =5V	-100	-	+100	nA
PROTECTIONS(PWM)						
	CH1,2 Maximum Inductor Current-Limit		1.5	1.6	-	A
	CH3 Maximum Inductor Current-Limit		2.0	2.2	-	A
	Low Side Switch Current-Limit	From Drain to Source, EN shutdown to turn on low side MOSFET to discharge Vout till current limit.	-	0.3	-	A
	Soft-Start Time		-	0.7	-	ms
F_{SW}	Switching Frequency	V_{FBX} =0.6V	1.2	1.5	1.8	MHz
	Foldback Frequency		-	210	-	kHz
	Minimum On Time		-	-	100	ns
	Maximum Duty Cycle		-	-	100	%
	UVP Threshold		25	30	35	%V_{REF}
PROTECTIONS(LDO)						
	Current Limit		330	450	-	mA
	Soft-Start Time		-	60	-	μs

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Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{CC1}, V_{CC2}, V_{CC3}=5V, V_{EN_LDO1}=V_{EN_LDO2}=V_{EN_PWM}=5V. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7255			Unit
			Min	Typ	Max	
PROTECTIONS(PWM, LDO)						
T_{OTP}	Over-Temperature Protection	T_J Rising	-	150	-	°C
	Over-Temperature Protection Hysteresis	T_J Falling	-	30	-	°C

Pin Description

PIN		Function
NO.	Name	
1	LX1	Power Switching Output. The LX1 is the junction of the high-side and low-side power MOSFET to supply power to the output LC filter.
2, 16	GND	Connect this pin with large copper area to negative terminals of the input and output capacitors.
3	FB1	Output Feedback Input. The APW7255 senses the feedback voltage via FB1 and regulates the voltage at 0.600V. Connecting FB with a resistor-divider from the converter's output sets the output voltage.
4	FB2	Output Feedback Input. The APW7255 senses the feedback voltage via FB2 and regulates the voltage at 0.600V. Connecting FB with a resistor-divider from the converter's output sets the output voltage.
5	POK	Power Good Output
6	EN_PWM	Enable pin of the PWM converter. When the EN_PWM is above high logic level, the device is in operation mode. When the EN_PWM is below low logic level, the device is in shutdown mode. This pin can not be left open.
7	AGND	Connect this pin with large copper area to negative terminals of the input and output capacitors.
8	VCC3	Power Input. Connect a ceramic bypass capacitor from VCC3 to GND.
9	EN_LDO2	Enable pin of the LDO2. When the EN_LDO2 is above high logic level, the device is in operation mode. When the EN_LDO2 is below low logic level, the device is in shutdown mode. This pin can not be left open.
10	FB_LDO2	Output Feedback Input. The APW7255 senses the feedback voltage via FB_LDO2 and regulates the voltage at 0.600V. Connecting FB_LDO2 with a resistor-divider from the VLDO2 sets the output voltage.
11	VLDO2	Regulator Output Pin
12	VLDO1	Regulator Output Pin
13	FB_LDO1	Output Feedback Input. The APW7255 senses the feedback voltage via FB_LDO1 and regulates the voltage at 0.600V. Connecting FB_LDO1 with a resistor-divider from the VLDO1 sets the output voltage.
14	EN_LDO1	Enable pin of the LDO1. When the EN_LDO1 is above high logic level, the device is in operation mode. When the EN_LDO1 is below low logic level, the device is in shutdown mode. This pin can not be left open.
15	FB3	Output Feedback Input. The APW7255 senses the feedback voltage via FB3 and regulates the voltage at 0.600V. Connecting FB with a resistor-divider from the converter's output sets the output voltage.
17	LX3	Power Switching Output. The LX3 is the junction of the high-side and low-side power MOSFET to supply power to the output LC filter.
18	VCC2	Power Input. Connect a ceramic bypass capacitor from VCC2 to GND.
19	LX2	Power Switching Output. The LX2 is the junction of the high-side and low-side power MOSFET to supply power to the output LC filter.
20	VCC1	Power Input. Connect a ceramic bypass capacitor from VCC1 to GND.

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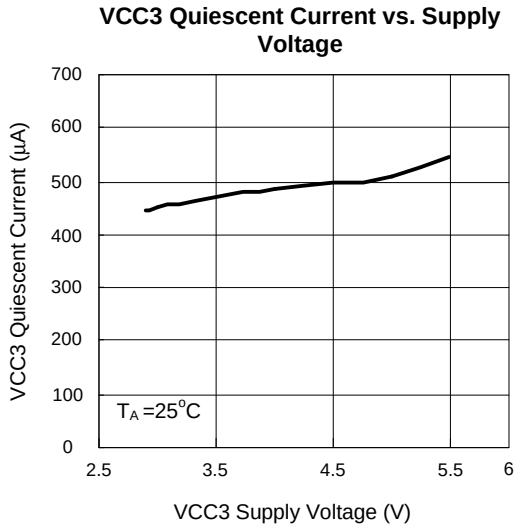
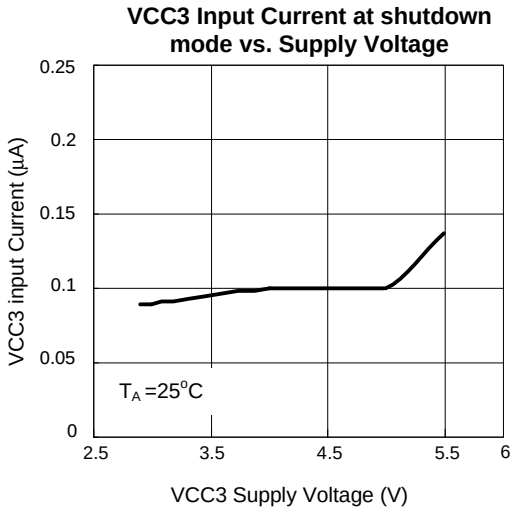
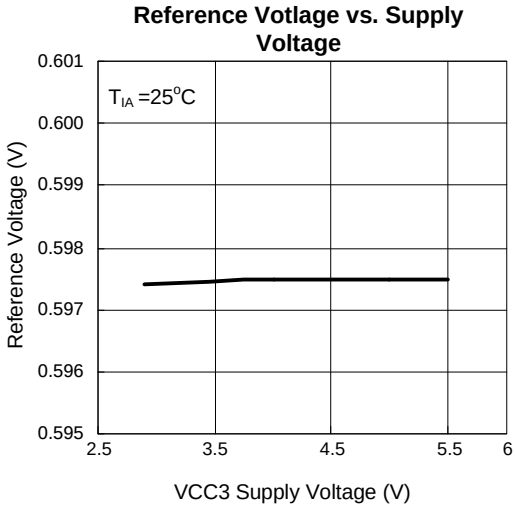
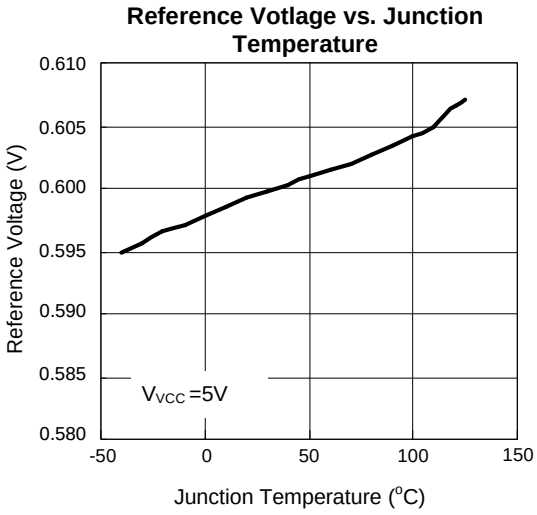
Typical Operating Characteristics





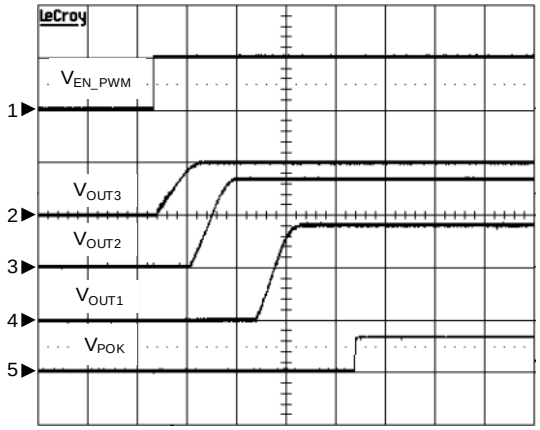




Operating Waveforms

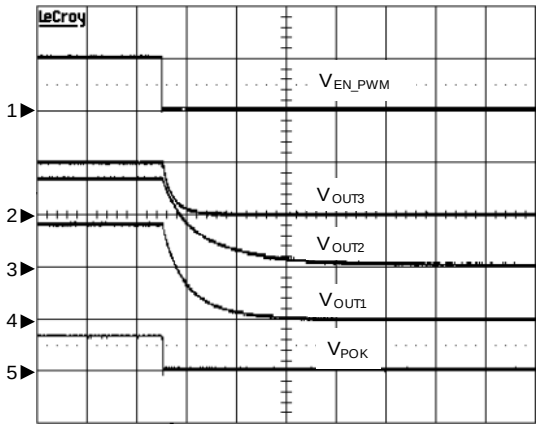
Please Refer to Typical Application Circuit, Test Condition is at T_A= 25°C unless otherwise specified.

Turn On Response -PWM Converter



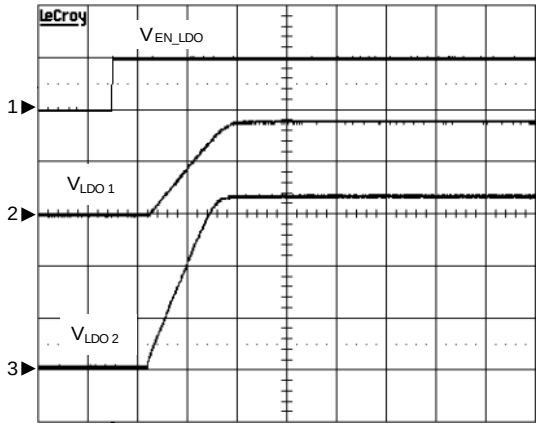
APW7255A, V_{VCC1} =V_{VCC2}=V_{VCC3}=5V,
R_{VOUT1} =2.5Ω, R_{VOUT2} =3.9Ω, R_{VOUT3} =1Ω,
EN power on
CH1: V_{EN_PWM}, 5V/Div, DC
CH2: V_{OUT3}, 1V/Div, DC
CH3: V_{VOUT2}, 2/Div, DC
CH4: V_{VOUT1}, 1/Div, DC
CH5: V_{POK}, 5/Div, DC
TIME:1ms/Div

Turn Off Response-PWM Converter



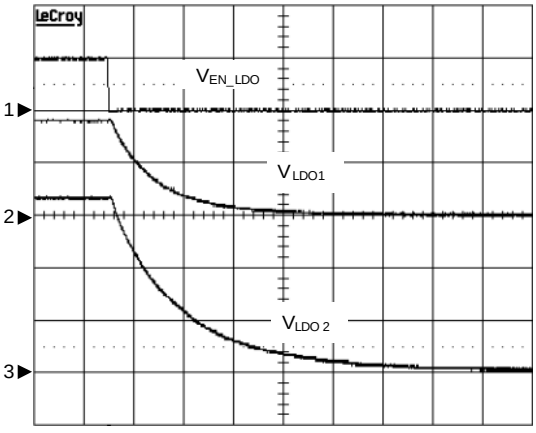
APW7255A, V_{VCC1} =V_{VCC2}=V_{VCC3}=5V,
R_{VOUT1} =2.5Ω, R_{VOUT2} =3.9Ω, R_{VOUT3} =1Ω,
EN power off
CH1: V_{EN_PWM}, 5V/Div, DC
CH2: V_{OUT3}, 1V/Div, DC
CH3: V_{VOUT2}, 2/Div, DC
CH4: V_{VOUT1}, 1/Div, DC
CH5: V_{POK}, 5/Div, DC
TIME:50µs/Div

Turn On Response -LDO



APW7255A, V_{VCC1} =V_{VCC2}=V_{VCC3}=5V, EN_LDO
tied with EN_PWM, R_{LDO1} =8Ω, R_{LDO2} =12Ω,
EN power on
CH1: V_{EN_LDO}, 5V/Div, DC
CH2: V_{LDO1}, 1V/Div, DC
CH3: V_{LDO2}, 1/Div, DC
TIME:100µs/Div

Turn Off Response-LDO



APW7255A, V_{VCC1} =V_{VCC2}=V_{VCC3}=5V, EN_LDO
tied with EN_PWM, R_{LDO1} =8Ω, R_{LDO2} =12Ω,
EN power off
CH1: V_{EN_LDO}, 5V/Div, DC
CH2: V_{LDO1}, 1V/Div, DC
CH3: V_{LDO2}, 1/Div, DC
TIME:20µs/Div

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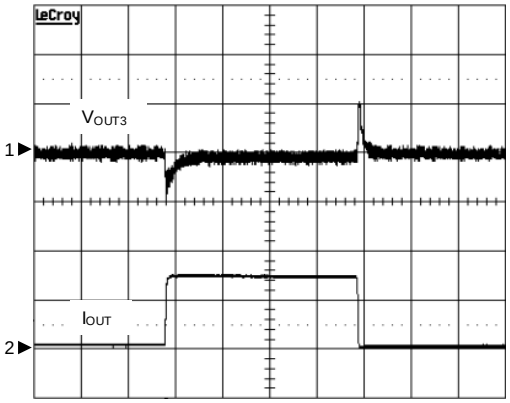
Operating Waveforms (Cont.)

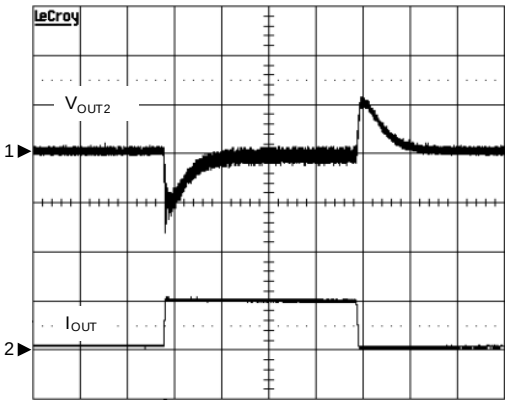
Please Refer to Typical Application Circuit, Test Condition is at T_A= 25°C unless otherwise specified.

Load Transient Response- PWM3 Converter



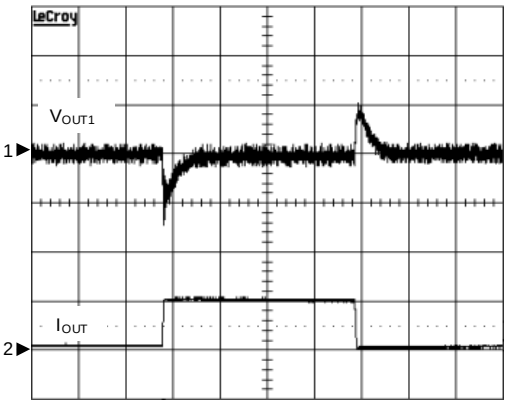
APW7255A, V_{OUT3}=1V, L=2.2µH, C_{OUT}=22µF, C8=47pF, R6=100kΩ, R7=150kΩ
I_{OUT}=0.1A-1.5A-0.1A,
CH1: V_{OUT3}, 50mV/Div, offset=1V
CH2: I_{OUT}, 1A/Div, DC
TIME:100µs/Div

Load Transient Response- PWM2 Converter



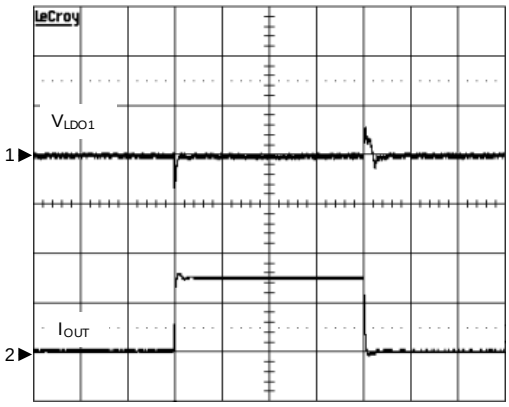
APW7255A, V_{OUT2}=3.3V, L=2.2µH, C_{OUT}=10µF, C5=47pF, R2=680kΩ, R4=150kΩ
I_{OUT}=0.1A-1A-0.1A,
CH1: V_{OUT2}, 50mV/Div, offset=3.3V
CH2: I_{OUT}, 1A/Div, DC
TIME:100µs/Div

Load Transient Response- PWM1 Converter



APW7255A, V_{OUT1}=1.8V, L=2.2µH, C_{OUT}=10µF, C4=47pF, R1=300kΩ, R3=150kΩ
I_{OUT}=0.1A-1A-0.1A,
CH1: V_{OUT1}, 50mV/Div, offset=1.8V
CH2: I_{OUT}, 1A/Div, DC
TIME:100µs/Div

Load Transient Response- LDO1

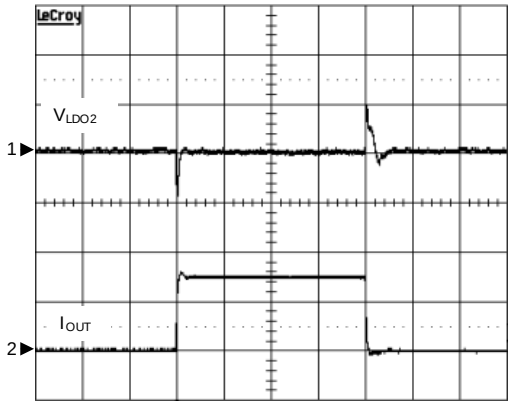


APW7255A, V_{LDO1}=1.8V, C_{OUT}=2.2µF, R11=30kΩ, R10=15kΩ
I_{OUT}=10mA-300mA-10mA,
CH1: V_{LDO1}, 50mV/Div, offset=1.8V
CH2: I_{OUT}, 200mA/Div, DC
TIME:50µs/Div

Operating Waveforms (Cont.)

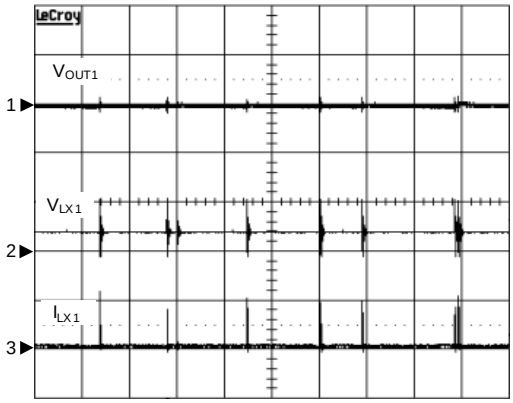
Please Refer to Typical Application Circuit, Test Condition is at T_A= 25°C unless otherwise specified.

Load Transient Response- LDO2



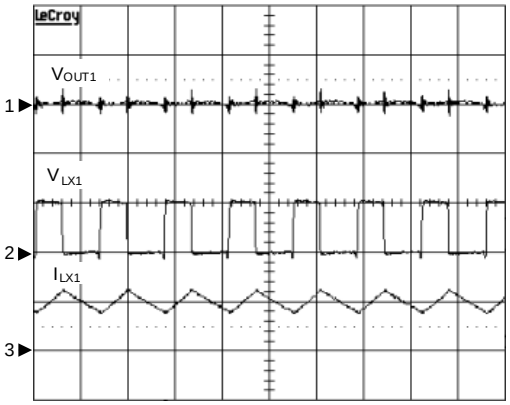
APW7255A, V_{LDO2}=3.3V,
C_{OUT}=2.2µF, R9=68kΩ, R8=15kΩ
I_{OUT}=10mA-300mA-10mA,
CH1: V_{LDO2}, 50mV/Div, offset=3.3V
CH2: I_{OUT}, 200mA/Div, DC
TIME:50µs/Div

PWM Converter at Light Load



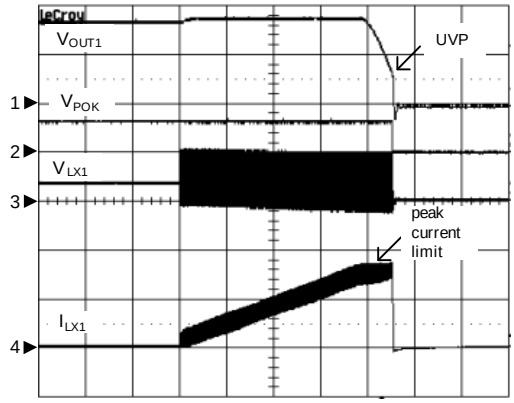
APW7255A, V_{OUT1}=1.8V, L=2.2µH,
C_{OUT}=10µF, C4=47pF, R1=300kΩ, R3=150kΩ
I_{OUT}=1mA,
CH1: V_{OUT1}, 50mV/Div, offset=1.8V
CH2: V_{LX1}, 5V/Div, DC
CH3: I_{LX1}, 100mA/Div, DC
TIME:10µs/Div

PWM Converter at Heavy Load



APW7255A, V_{OUT1}=1.8V, L=2.2µH,
C_{OUT}=10µF, C4=47pF, R1=300kΩ, R3=150kΩ
I_{OUT}=1A,
CH1: V_{OUT1}, 50mV/Div, offset=1.8V
CH2: V_{LX1}, 5V/Div, DC
CH3: I_{LX1}, 100mA/Div, DC
TIME:0.5µs/Div

Over Load Response-PWM Converter

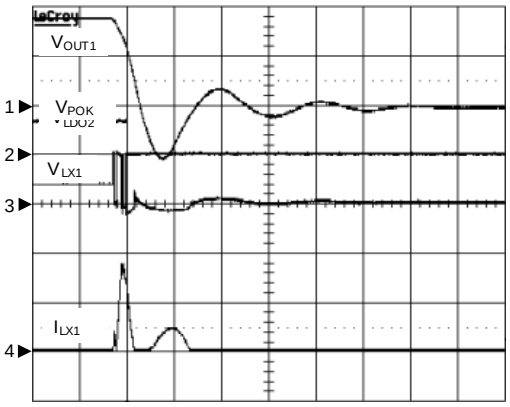


APW7255A, V_{OUT1}=1.8V, L=2.2µH,
C_{OUT}=10µF, C4=47pF, R1=300kΩ, R3=150kΩ
ramp up I_{OUT} till UVP shutdown,
CH1: V_{OUT1}, 1V/Div, DC
CH2: V_{POK}, 5V/Div, DC
CH3: V_{LX1}, 5V/Div, DC
CH4: I_{LX1}, 1A/Div, DC
TIME:200µs/Div

Operating Waveforms (Cont.)

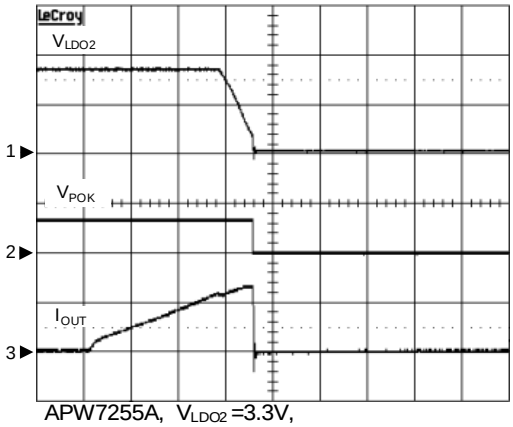
Please Refer to Typical Application Circuit, Test Condition is at T_A= 25°C unless otherwise specified.

Short Circuit Response-PWM Converter



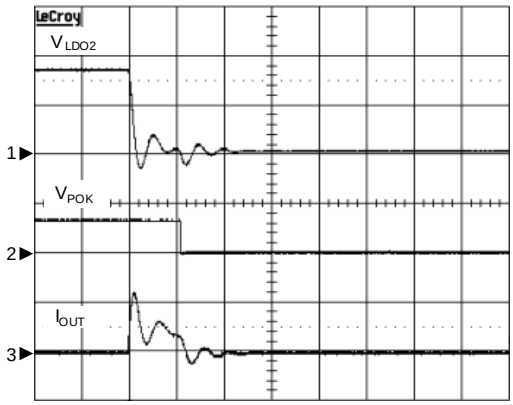
APW7255A, V_{OUT1} =1.8V, L=2.2µH,
C_{OUT}=10µF, C4=47pF, R1=300kΩ, R3=150kΩ
VOUT1 short to ground
CH1: V_{OUT1}, 1V/Div, DC
CH2: V_{POK}, 5V/Div, DC
CH3: V_{LX1}, 5V/Div, DC
CH4: I_{LX1}, 1A/Div, DC
TIME:10µs/Div

Over Load Response-LDO



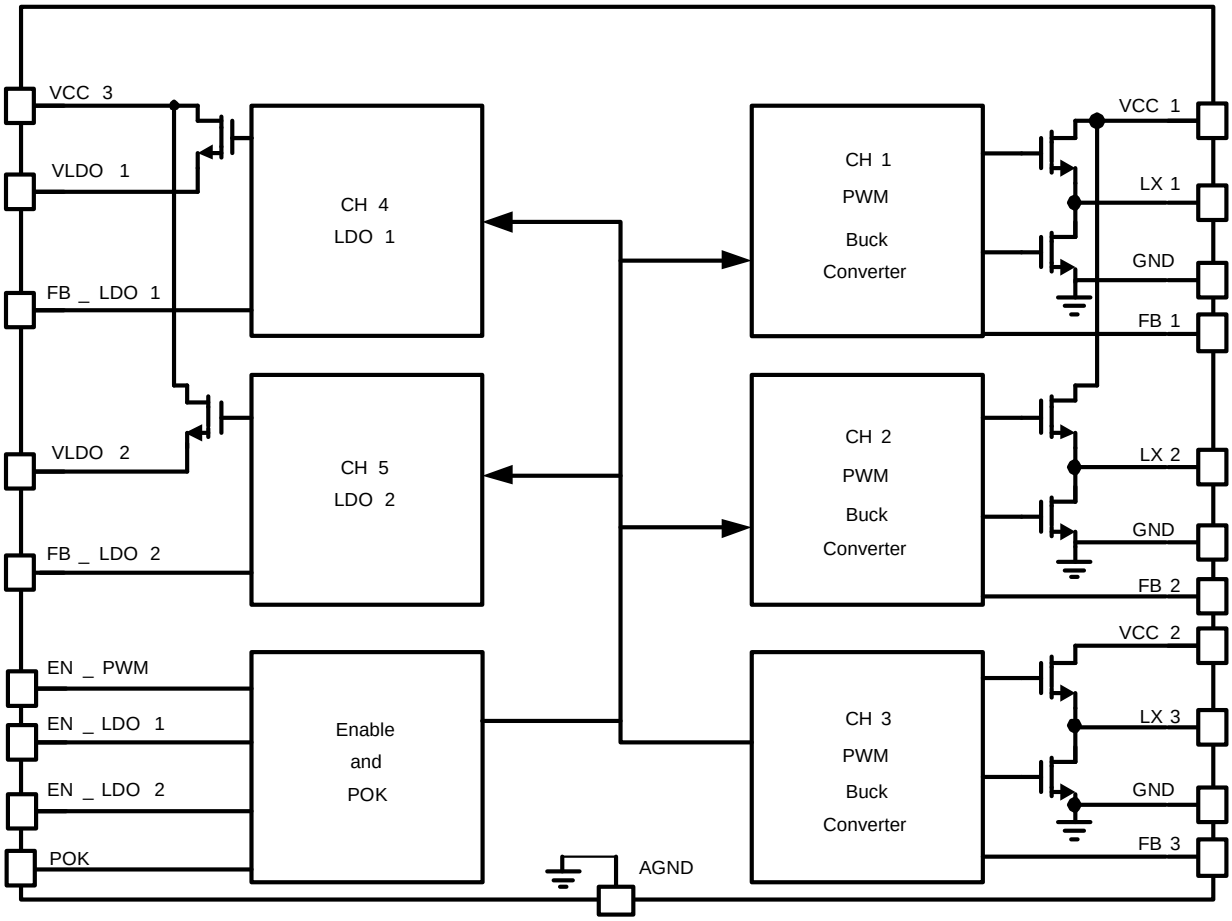
APW7255A, V_{LDO2} =3.3V,
C_{OUT}=2.2µF, R9=68kΩ, R8=15kΩ
ramp up I_{OUT} till UVP shutdown
CH1: V_{LDO2}, 2V/Div, DC
CH2: V_{POK}, 5V/Div, DC
CH3: I_{OUT}, 0.5A/Div, DC
TIME:200µs/Div

Short Circuit Response-LDO

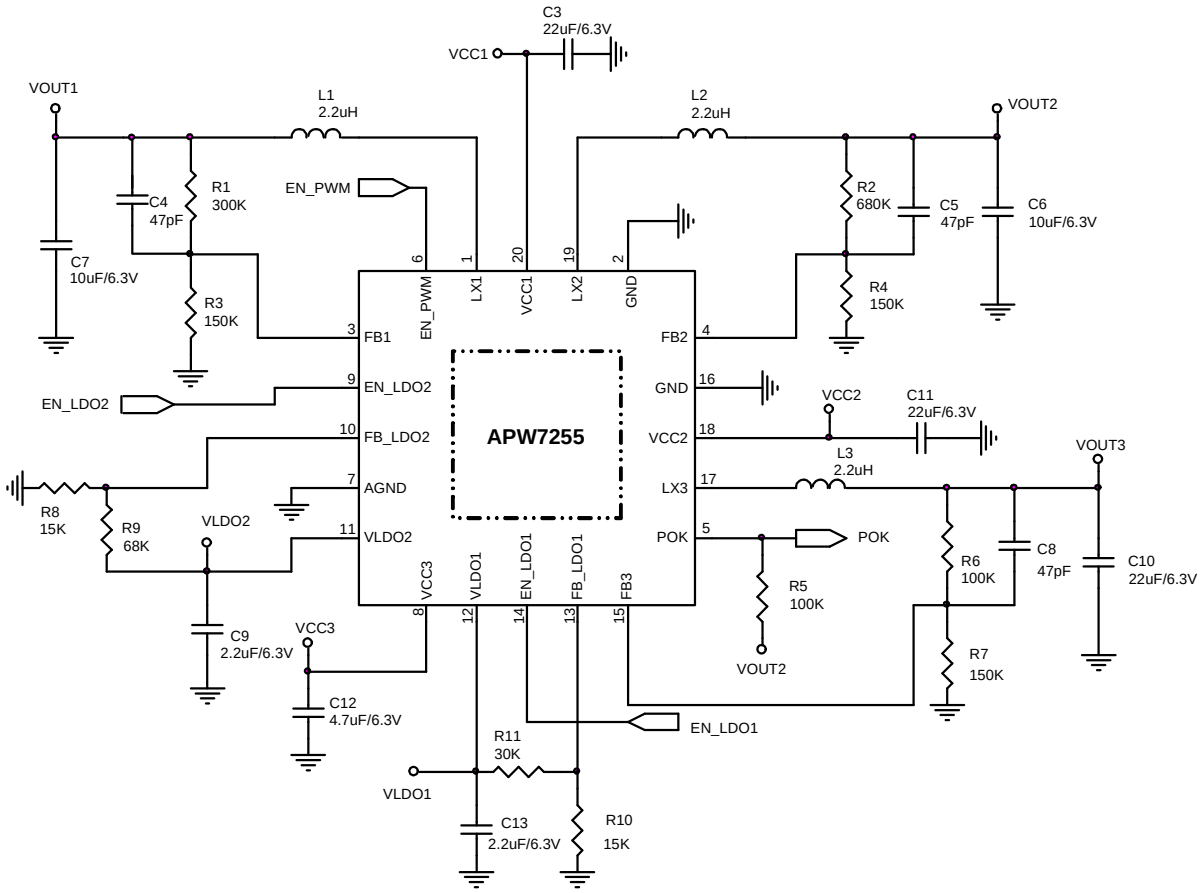


APW7255A, V_{LDO2} =3.3V,
C_{OUT}=2.2µF, R9=68kΩ, R8=15kΩ
VLDO2 short to ground
CH1: V_{LDO2}, 2V/Div, DC
CH2: V_{POK}, 5V/Div, DC
CH3: I_{OUT}, 5A/Div, DC
TIME:5µs/Div

Block Diagram



Typical Application Circuit



Function Description

Power-On-Reset (POR)

The APW7255 monitors the input voltage to prevent wrong logic control. The POR function initiates a soft-start process after input voltage exceeds its rising POR threshold during power on. The POR function also shuts off the output when the input voltage falls below its falling threshold.

Shutdown Control

The APW7255 has an active-low shutdown function. Forcing EN(EN_PWM, EN_LDO1, EN_LDO2) high (>1V) enables the VOUT; forcing EN low (<0.4V) disables the VOUT. The EN can not be left floating. If it is not used, connect it to VCC(VCC1, VCC2, VCC3) for normal operation.

Internal Soft-Start

An internal soft-start function controls rising rate of the output voltage to limit the surge current at start-up.

Current-Limit protection

The buck converter monitors the output current, flows through the high-side and low-side power MOSFETs, and limits the current peak at current-limit level to prevent the IC from damaging during overload, short-circuit conditions, If the feedback voltage < 0.3*V_{REF}, PWM enters UVP shutdown until recycling VCC3 power or toggling EN.

The LDO regulator monitors the current via the output PMOS and limits the maximum current. When the output current reaches the current-limit threshold, current-limit with current foldback circuit starts to work to prevent load and APW7255 from damages during overload or short-circuit conditions.

Thermal Shutdown

A thermal shutdown circuit limits the junction temperature of APW7255. When the junction temperature exceeds +150°C, a thermal sensor turns off the output PMOS, allowing the device to cool down. The regulator regulates the output against through initiation of a new soft-start cycle after the junction temperature cools by 120°C. The thermal shutdown is designed with a 30°C hysteresis to lower the average junction temperature during continuous thermal overload conditions, extending lifetime of the device.

PWM Soft-Stop

At the moment of shutdown controlled by EN signal, the APW7255 initiates a soft-stop process in converter to discharge the output voltage in the output capacitors. Certainly, the load current also discharges the output voltage. During soft-stop, the internal voltage ramp (V_{RAMP}) falls down to replace the reference voltage. The low side MOSFET turns on each cycle to discharge the output voltage. Therefore, the output voltage falls down slowly at the light load. After the soft-stop interval elapses, the soft-stop process ends and the converter turns off.

Power OK Indicator

POK is actively held low in shutdown and soft-start status. In the soft-start process, the POK is an open-drain, after CH2 of Converter is ready, the POK is released.

Power Sequence

The APW7255 provides difference power Sequences to choose for different applications. Figure 1 show the timing diagram of different version of the APW7255.

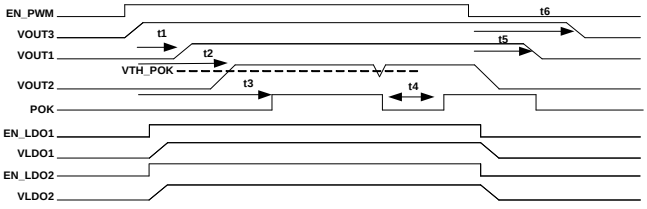


Figure 1. Power sequence

Application Information

Input Capacitor Selection

The buck converters in APW7255 have a pulsating input current, a low ESR input capacitor is required. This results in the best input voltage filtering, minimizing the interference with other circuits caused by high input voltage spikes. Also, the input capacitor must be sufficiently large to stabilize the input voltage during heavy load transients. For good input voltage filtering, usually a 22µF input capacitor is sufficient. It can be increased without any limit for better input-voltage filtering. Ceramic capacitors show better performance because of the low ESR value, and they are less sensitive against voltage transients and spikes compared to tantalum capacitors. Place the input capacitor as close as possible to the VCC1, VCC2 to GND pin of the device for better performance.
The LDO regulator in APW7255 requires proper input capacitors to supply surge current during stepping load transients to prevent the input rail from dropping. Because the parasitic inductor from the voltage sources or other bulk capacitors to the VCC3 limit the slew rate of the surge current, place the Input capacitors near VCC3 as close as possible. Input capacitors should be larger than 1µF and a minimum ceramic capacitor of 1µF is necessary.

Inductor Selection

For high efficiencies, the inductor should have a low DC resistance to minimize conduction losses. Especially at high-switching frequencies, the core material has a higher impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. A reasonable starting point for setting ripple current, ΔI_L, is 40% of maximum output current. The recommended inductor value can be calculated as below:

$$L \geq \frac{V_{OUT}(1-\frac{V_{OUT}}{V_{IN}})}{F_{SW} \cdot \Delta I_L}$$

$$I_{L(MAX)}=I_{OUT(MAX)}+ 1/2 \times \Delta I_L$$

To avoid the saturation of the inductor, the inductor should be rated at least for the maximum output current of the converter plus the inductor ripple current.

Output Voltage Setting

In the adjustable version, the output voltage is set by a resistive divider. The external resistive divider is connected to the output, allowing remote voltage sensing as shown in “Typical Application Circuits”. The output voltage can be calculated as below:

$$V_{OUT1} = V_{REF} \cdot (1+\frac{R1}{R3}) = 0.6 \cdot (1+\frac{R1}{R3})$$

Output Capacitor

The buck converter in APW7255 allows the use of tiny ceramic capacitors. The higher capacitor value provides the good load transients response. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. If required, tantalum capacitors may be used as well. The output ripple is the sum of the voltages across the ESR and the ideal output capacitor.

$$\Delta V_{OUT} \cong \frac{V_{OUT} \cdot (1-\frac{V_{OUT}}{V_{IN}})}{F_{SW} \cdot L}(ESR + \frac{1}{8 \cdot F_{SW} \cdot C_{OUT}})$$

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size. The LDO regulator in APW7255 needs a proper output capacitor to maintain circuit stability and improve transient response over temperature and current. In order to insure the circuit stability, the proper output capacitor value should be larger than 1µF. With X5R and X7R dielectrics, 1µF is sufficient at all operating temperatures. Large output capacitor value can reduce noise and improve load-transient response and PSRR.

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Application Information (Cont.)

Layout Consideration

The layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

1. The input capacitor should be placed close to the VCC1, VCC2, VCC3 and GND. Connecting the capacitor and VCC1, VCC2, VCC3 to GND with short and wide trace without any via holes for good input voltage filtering. The distance between VCC1, VCC2, VCC3 to GND to capacitor less than 2mm respectively is recommended.
2. To minimize copper trace connections that can inject noise into the system, the inductor should be placed as close as possible to the LX1, LX2, LX3 pin to minimize the noise coupling into other circuits.
3. The output capacitor should be place closed to LX1, LX2, LX3 and GND.
4. Since the feedback pin and network is a high impedance circuit the feedback network should be routed away from the inductor. The feedback pin and feedback network should be shielded with a ground plane or trace to minimize noise coupling into this circuit.
5. A star ground connection or ground plane minimizes ground shifts and noise is recommended.
6. To place regulator of output capacitors near the load is good for performance.

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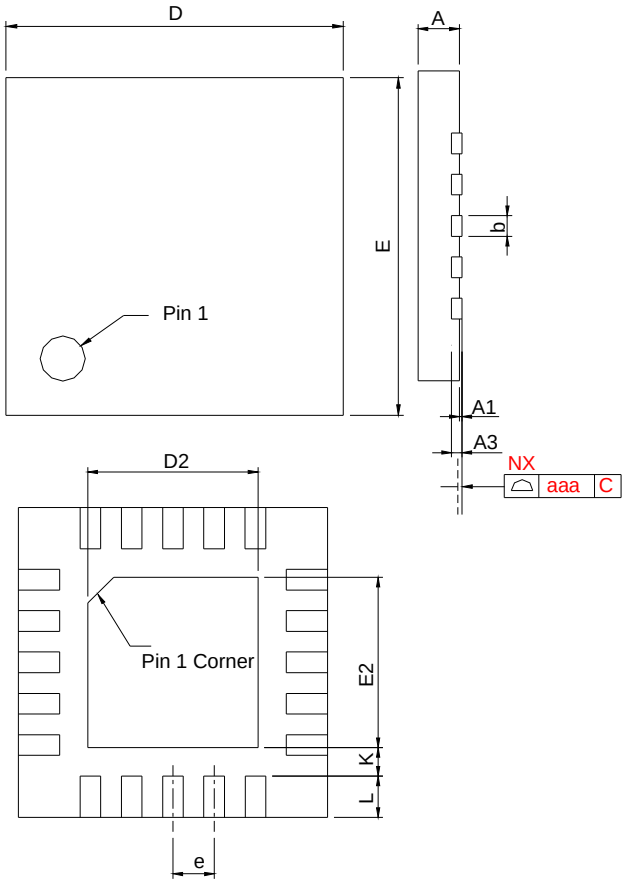
Package Information

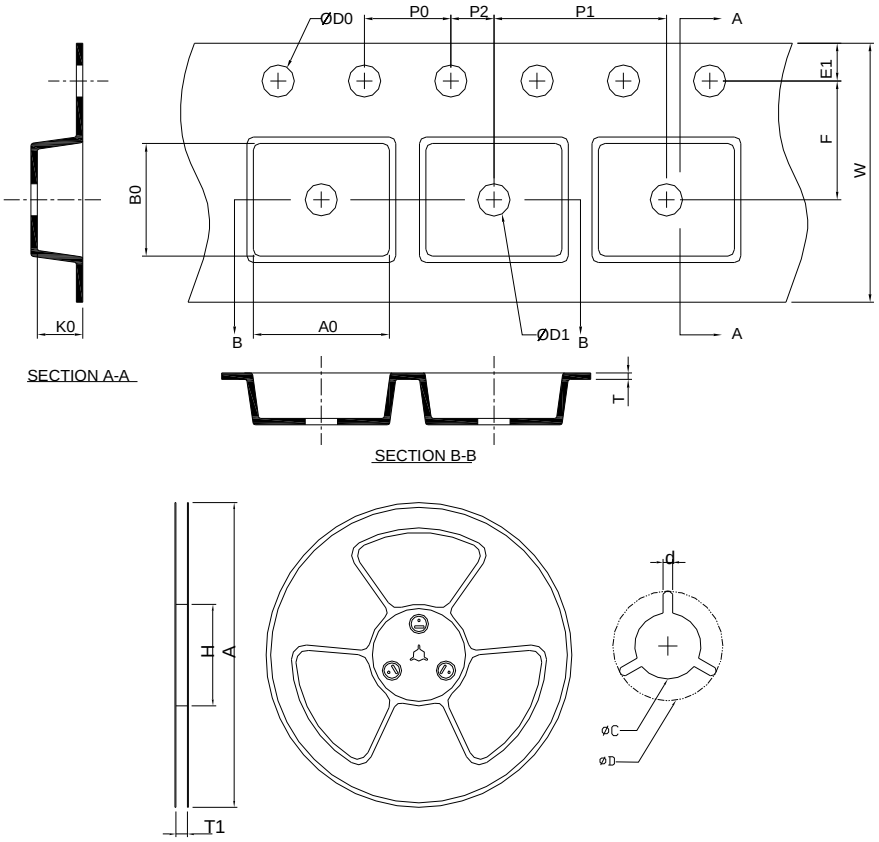
TQFN3x3-20



SYMBOL	TQFN3x3-20			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.15	0.25	0.006	0.010
D	2.90	3.10	0.114	0.122
D2	1.50	1.80	0.059	0.071
E	2.90	3.10	0.114	0.122
E2	1.50	1.80	0.059	0.071
e	0.40 BSC		0.016 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	
aaa	0.08		0.003	

Note : 1. Followed from JEDEC MO-220 WEEE

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN3x3-20	330±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.00±0.20

(mm)

Devices Per Unit

Package Type	Unit	Quantity
TQFN3x3-20	Tape & Reel	3000

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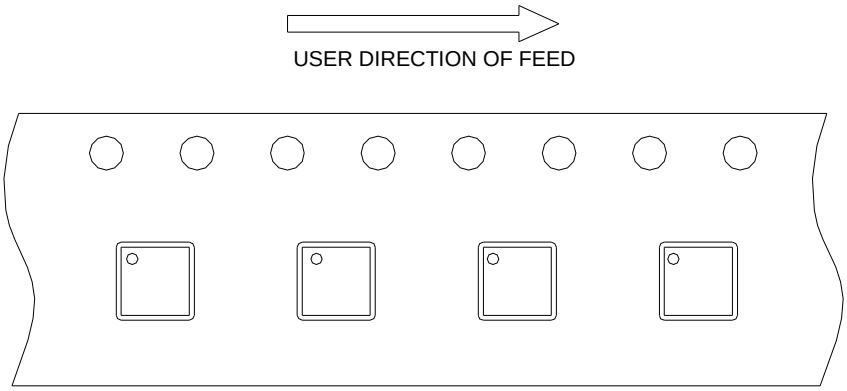
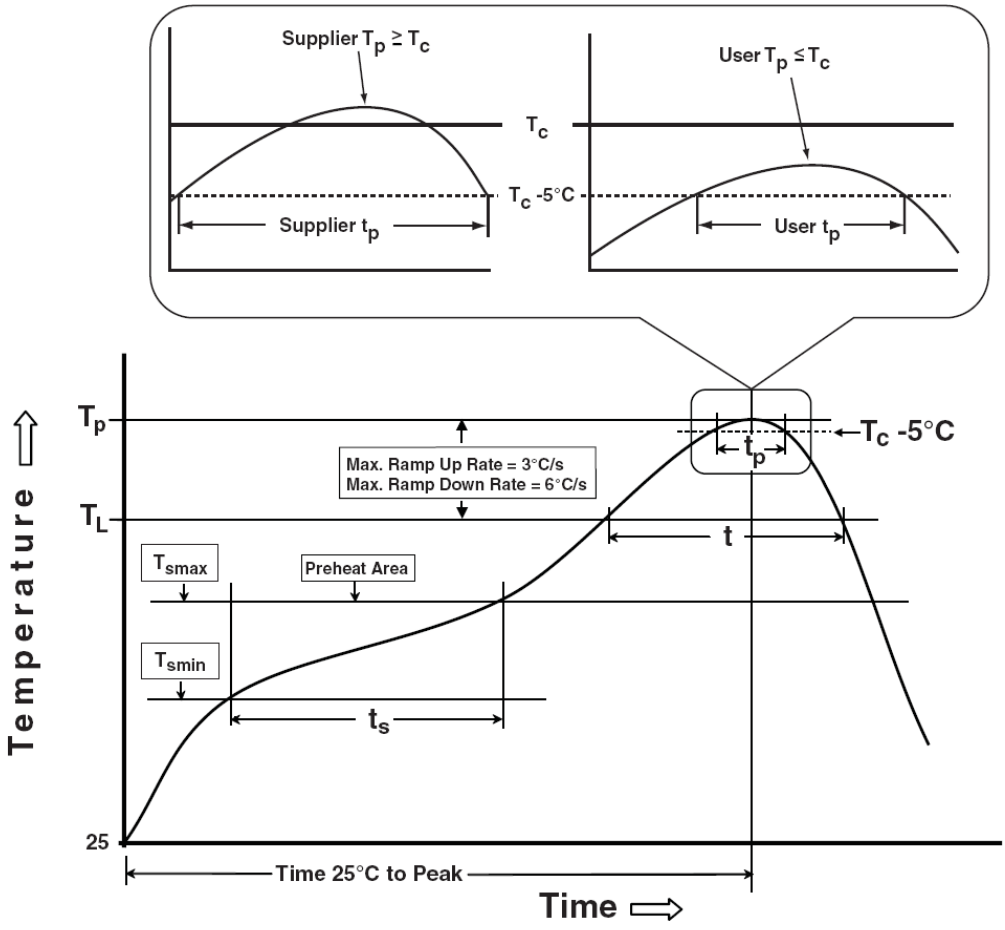
Taping Direction Information

TQFN3x3-20



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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