High Efficiency 16V, 500kHz Synchronous Step-Down Converter

Features

- Wide 4.5V to 16V Operating Input Range
- Low $R_{DS(ON)}$ Internal Power MOSFETs
- Low Quiescent Current
- Fast Load Transient Response
- Fixed 500kHz Switching Frequency
- Build-in soft start function
- Output Adjustable from 0.8 V to 5V
- Protection
  - -Output Over-Voltage Protection
  - -Output Under-Voltage Protection
  - -Over-Current Protection
  - -Input Over-Voltage Protection
  - -Over-Temperature Protection
- Available in FC-TSOT-23-6 Package
- Lead Free and Green Devices Available (RoHS Compliant)

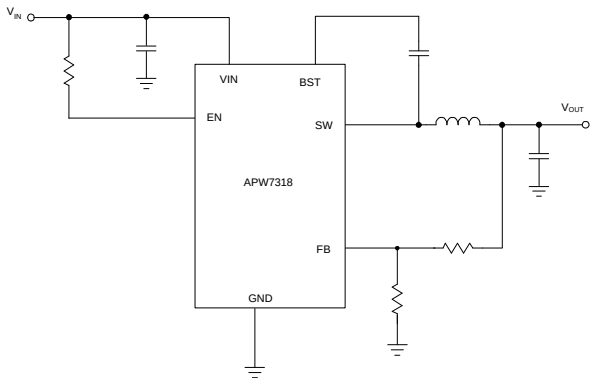
General Description

APW7318 is a high efficiency synchronous buck converter with integrated 60m/37mΩ of upper/lower power MOSFET. The APW7318 design with a COT-mode control scheme, can convert wide input voltage of 4.5V to 16V to the output voltage adjustable from 0.8V to 5V to provide excellent output voltage regulation.

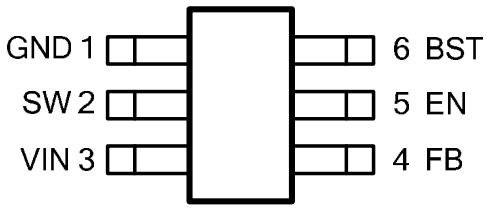
The APW7318 is equipped with an automatic PFM/PWM mode operation. At light load, the IC operates in the PFM mode to reduce the switching losses. The APW7318 provides very high efficiency over light to heavy loads with loading-modulated switching frequencies.

The APW7318 is also equipped with Power-on-reset, softstart, and whole protections (over-temperature, over-voltage, under-voltage, over-current and input over-voltage) into a single package.
This device, available in FC-TSOT-23-6 package, provides a very compact system solution external components and PCB area.

Simplified Application Circuit



Pin Configuration



FC-TSOT-23-6
Top View

Applications

- LCD TVs
- LCD Monitors
- Networking Systems
- Distributed Power Systems

Ordering and Marking Information

APW7318 □□□-□□□

- Assembly Material
- Handling Code
- Temperature Range
- Package Code

Package Code
CT : FC-TSOT23-6
Operating Ambient Temperature Range
I : -40 to 85°C
Handling Code
TR : Tape & Reel
Assembly Material
G : Halogen and Lead Free Device

APW7318 CT : 

XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldiering operations. ANPEC lead-free products meet or exceed the leadfree requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

Absolute Maximum Ratings (Note 1)

Symbol	Parameter		Rating	Unit
V_{IN}	VIN to GND Voltage		-0.3 ~ 18	V
V_{EN}	EN to GND Voltage		-0.3 ~ 18	V
V_{SW}	SW to GND Voltage	>20ns	-1 ~ V_{IN}+0.3	V
		<20ns	-3 ~ V_{IN}+3	V
V_{BST}	BST to GND Voltage		V_{SW}-0.3 ~V_{SW} +6	V
V_{BST_SW}	BST Supply Voltage (BST to SW)		-0.3 ~ 6	V
$V_{I/O}$	All other pins		-0.3 ~ 6	V
P_D	Power Dissipation		Internally Limited	W
T_J	Maximum Junction Temperature		-40 ~ 150	°C
T_{STG}	Storage Temperature		-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)		260	°C

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	60	°C/W
θ_{JC}	Junction-to-Case Resistance in free air (Note 2)	10	

Note 2: θ_{JA} and θ_{JC} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 4)

Symbol	Parameter	Range	Unit
V_{IN}	VIN Supply Voltage	4.5 ~ 16	V
V_{OUT}	Converter Output Voltage	0.8 ~ 5	V
I_{OUT}	Converter Output Current	0 ~ 3	A
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3 : Refer to the typical application circuit

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=12V, V_{EN}=5V and T_A= -40 to 85 °C. Typical values are at T_A=25°C.

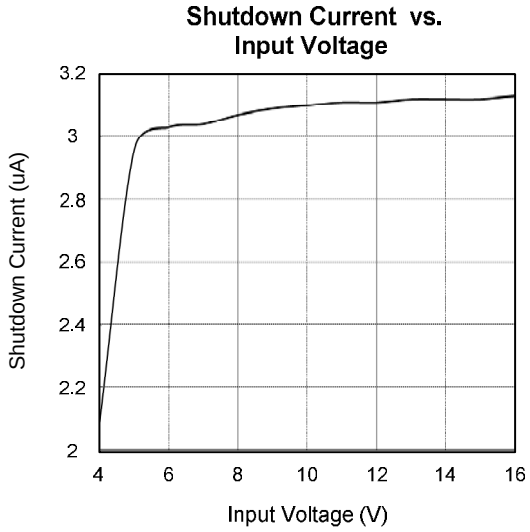
Symbol	Parameter	Test Conditions	APW7318			Unit
			Min	Typ	Max	
SUPPLY CURRENT						
I_{VIN}	VIN Supply Current	V_{IN}=12V, V_{FB}=0.66V, V_{EN}=3V, SW=NC	-	25	50	μA
I_{VIN_SD}	VIN Shutdown Supply Current	V_{IN}=4.5~18V, V_{EN}=0V	-	-	5	μA
POWER-ON-RESET (POR)						
	VIN POR Voltage Threshold	V_{IN} Rising	3.8	4	4.3	V
	VIN POR Voltage Hysteresis	V_{IN} Falling	-	0.2	-	V
REFERENCE VOLTAGE						
V_{REF}	Reference Voltage	Regulated on FB pin, T_J=25°C	792	800	808	mV
	Output Voltage Accuracy	T_J=-40~85°C, I_{OUT}=10mA	-1.5	-	+1.5	%
		I_{OUT}=10mA~3A T_J=25°C	-2	-	+2	%
	Load Regulation	I_{OUT}=0.5A~3A	-0.05	-	+0.05	%/A
	Line Regulation	4.5V≦V_{IN}≦18V, I_{OUT}=1A, V_{OUT}=3.3V	-0.02	-	+0.02	%/V
	FB Input Current	V_{FB}=5.5V, T_J= -40 ~ 125°C	-100	-	100	nA
OSCILLATOR AND DUTY CYCLE						
F_{OSC}	Oscillator Frequency		-	500	-	kHz
	Frequency Accuracy	T_J= 25°C	-10	-	10	%
	Frequency Accuracy	T_J= -40 ~ 85°C	-15	-	+15	%
	Maximum Converter's Duty		85	90	-	%
	Minimum on Time		-	-	100	ns
	Minimum off Time		-	200	-	ns

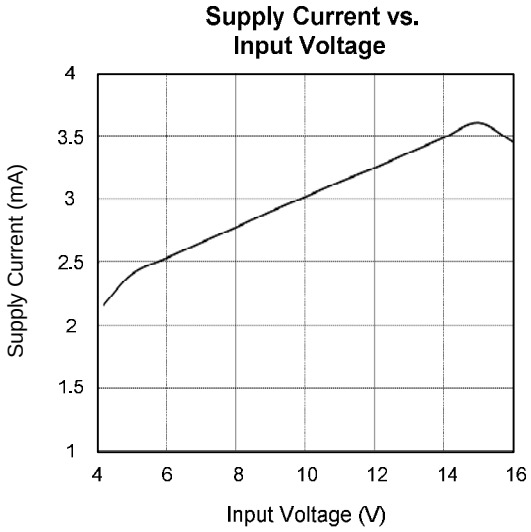
Electrical Characteristics(Cont.)

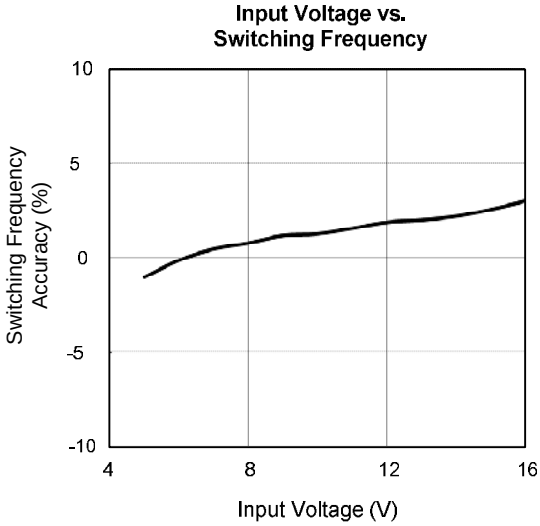
Unless otherwise specified, these specifications apply over V_{IN}=12V, V_{EN}=5V and T_A= -40 to 85 °C. Typical values are at T_A=25°C.

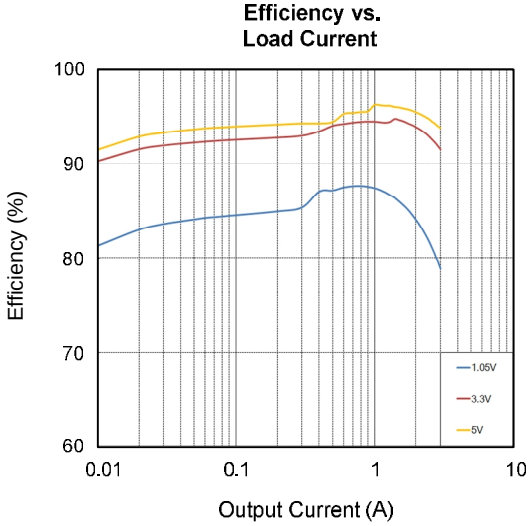
Symbol	Parameter	Test Conditions	APW7318			Unit
			Min	Typ	Max	
POWER MOSFET						
	High Side MOSFET Resistance	I_{OUT}=3A	-	60	-	mΩ
	Low Side MOSFET Resistance	I_{OUT}=3A	-	37	-	mΩ
	High Side MOSFET Leakage Current	V_{EN}=0V, V_{SW}=0V, V_{IN}=18V	-	-	1	μA
	Low Side MOSFET Leakage Current	V_{EN}=0V, V_{SW}=18V, V_{IN}=18V	-	-	1	μA
BOOTSTRAP POWER						
	Bootstrap Switch Drop Voltage	I_F = 10mA	-	0.1	0.2	V
	BOOT Leakage Current	V_{EN}=0V, V_{IN}=V_{SW}=18V, V_{BST}=23V	-	-	1	μA
T_D	Dead Time		-	20	-	ns
PROTECTIONS						
	Inductor Valley Current-Limit		4	5	6	A
	Input Over-Voltage Trip Point		18.5	19	19.5	V
	Out of Input Over-Voltage threshold		17	18	19	V
T_{OTP}	Over-temperature Trip Point		-	150	-	°C
	Over-temperature Hysteresis		-	35	-	°C
	Over- Voltage Protection		120	125	130	%V_{REF}
	Under- Voltage Protection		40	50	60	%V_{REF}
	Under-Voltage Hysteresis		-	3	-	%
	VOUT UVP Hiccup Delay Time		-	8	-	t_{SS}
	VOUT UVP Enable Delay Time	When EN=H to UVP Function Enabled	-	0.5	-	t_{SS}
	Low Side Switch Current-Limit	From Drain to Source	-	1	-	A
SOFT-START, ENABLE AND INPUT CURRENTS						
t_{SS}	Internal Soft-Start Time		-	1	-	ms
$R_{\_DISCHG}$	Output Dischage Device Capability	From EN=L to V_{OUT}=0.1V, C_{OUT}=66uF	-	-	250	Ω
	EN Logic High Threshold	V_{EN} rising	1.2	1.3	1.4	V
	EN Logic Low Threshold Hysteresis	V_{EN} falling	-	0.2	-	V
$T_{D(ON)}$	EN Turn On Delay		-	10	-	μs
	EN Input Current	V_{EN}=5.5V	-	-	1	μA

Typical Operating Characteristics





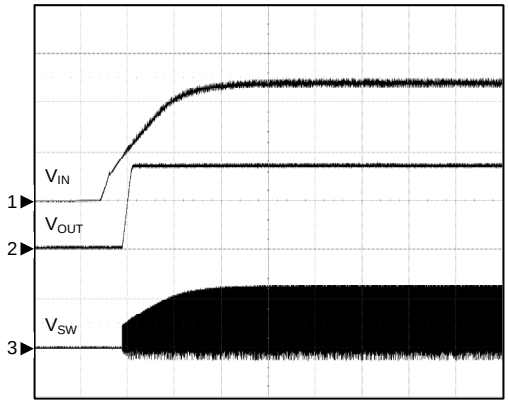




Operating Waveforms

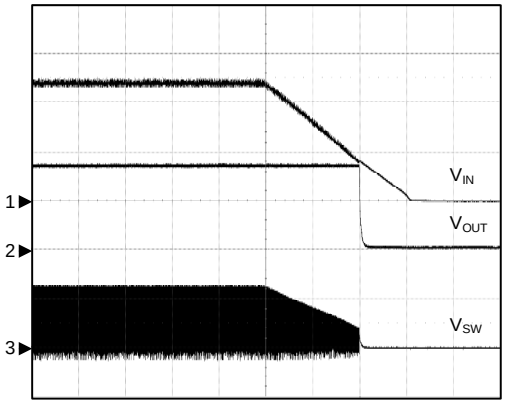
Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

Power On



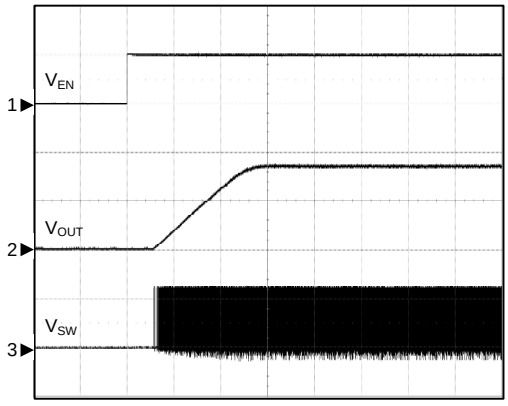
CH1: V_{IN}, 5V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: V_{SW}, 10V/Div, DC
TIME: 5ms/Div

Power Off



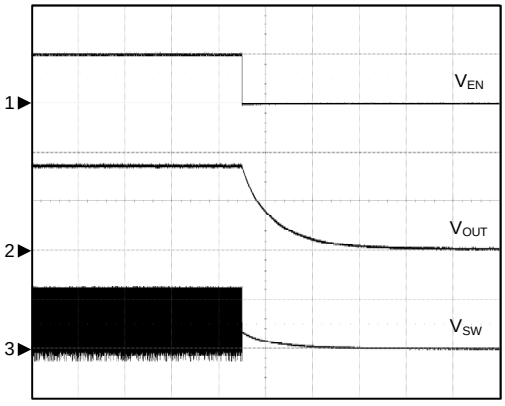
CH1: V_{IN}, 5V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: V_{SW}, 10V/Div, DC
TIME: 5ms/Div

Enable



CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: V_{SW}, 10V/Div, DC
TIME: 500us/Div

Shutsown

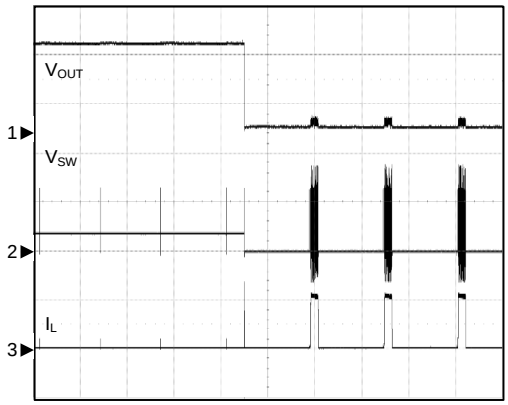


CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: V_{SW}, 10V/Div, DC
TIME: 500us/Div

Operating Waveforms (Cont.)

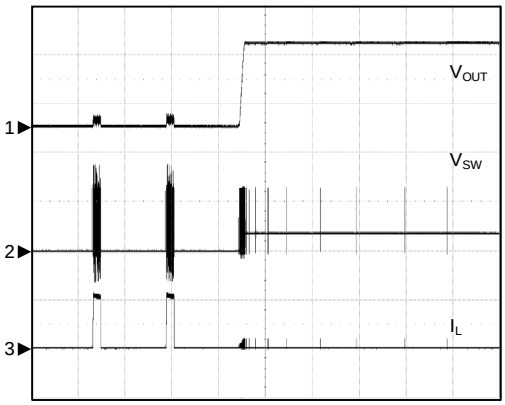
Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

Short-Current Entry



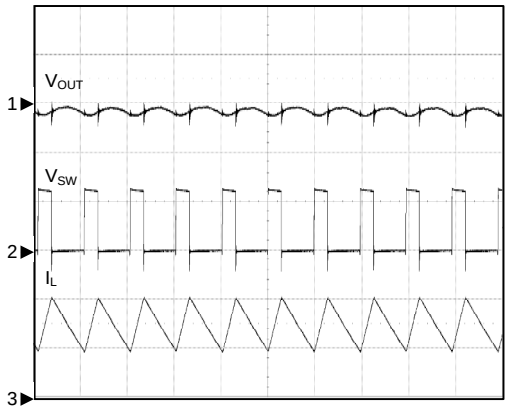
CH1: V_{OUT}, 2V/Div, DC
CH2: V_{SW}, 10V/Div, DC
CH3: I_L, 5A/Div, DC
TIME: 10ms/Div

Short-Current Recovery



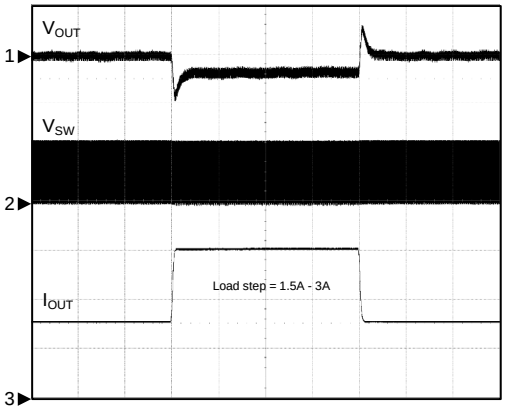
CH1: V_{OUT}, 2V/Div, DC
CH2: V_{SW}, 10V/Div, DC
CH3: I_L, 5A/Div, DC
TIME: 10ms/Div

Vout Ripple



CH1: V_{OUT}, 50mV/Div, DC
CH2: V_{SW}, 10V/Div, DC
CH3: I_L, 1A/Div, DC
TIME: 2us/Div

Load Transient

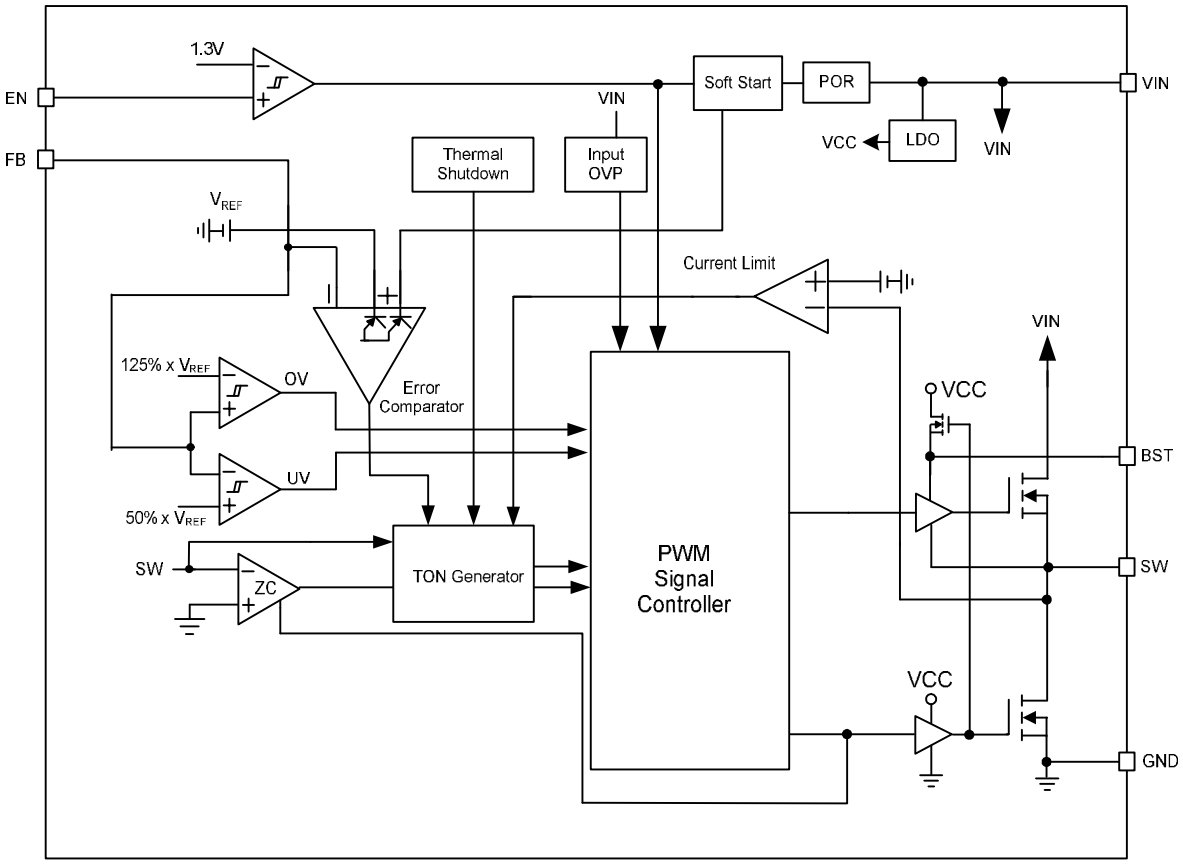


CH1: V_{OUT}, 100mV/Div, DC
CH2: V_{SW}, 10V/Div, DC
CH3: I_{OUT}, 1A/Div, DC
TIME: 200us/Div

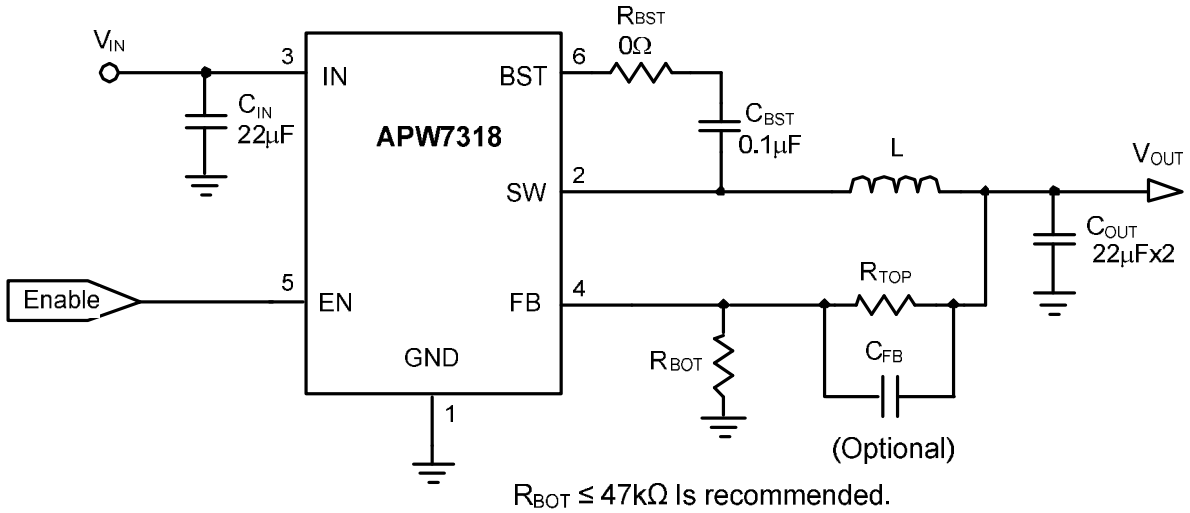
Pin Descriptions

PIN		FUNCTION
NO.	NAME	
1	GND	The GND terminal provides return path for the IC's bias current and the low-side MOSFET driver's pull-low current. Connect the pin to the system ground via very low impedance layout on PCBs.
2	SW	Power Switching Output. The SW is the junction of the high-side and low-side power MOSFET to supply power to the output LC filter.
3	VIN	Power Input. The VIN supplies the step-down converter switches. Connect a ceramic bypass capacitor from IN to GND.
4	FB	Output Feedback Input. The APW7318 senses the feedback voltage via FB and regulates the voltage at 0.6V. Connecting FB with a resistor-divider from the converter's output sets the output voltage.
5	EN	Enable pin of the PWM converter. When the EN is above high logic level, the device is in operation mode. When the EN is below low logic level, the device is in shutdown mode.
6	BST	High-side Gate driver supply Voltage input. The BST supplies the voltage to drive the high-side N-channel MOSFET.

Block Diagram



Typical Application Circuit



R_{BOT} ≤ 47kΩ Is recommended.

C_{IN} closed to IC. Less than 2mm is recommended.

Recommended Component Values

V_{IN} (V)	V_{OUT} (V)	R_{TOP} (Ω)	R_{BOT} (Ω)	L (H)	C_{OUT} (F)
12	1.05	13k	42.1k	2.2µ	22µ x 2
12	1.2	20.5k	42.1k	2.2µ	22µ x 2
12	3.3	40.5k	13k	4.7µ	22µ x 2
12	5	40.5k	7.74k	4.7µ	22µ x 2

Functional Description

The APW7318 integrates a synchronous buck PWM controller and high/low side power MOSFETs to generate V_{OUT}. It offers the lowest total solution cost that can provide up to 3A continuous output current over wide input supply range. Input voltage range of the PWM converter is 4.5V to 16V. User defined output voltage is possible and can be adjustable from 0.8V to 5V. The converter runs an adaptive on-time PWM operation at high-load condition and automatically reduces frequency to keep excellent efficiency down to several mA.

Constant-On-Time PWM Controller with Input Feed-Forward

The constant on-time control architecture is a pseudo-fixed frequency with input voltage feed-forward. This architecture relies on the output filter capacitor effective series resistance (ESR) to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal. The COT control mode can support output MLCC capacitor application currently through internal circuit designed. In PFM operation, the high-side switch on-time controlled by the on-time generator is determined solely by a one-shot whose pulse width is inversely proportional to input voltage and directly proportional to output voltage. In PWM operation, the high-side switch on-time is determined by a switching frequency control circuit in the on-time generator block. The switching frequency control circuit senses the switching frequency of the high-side switch and keeps regulating it at a constant frequency in PWM mode. The design improves the frequency variation and be more outstanding than a conventional constant on-time controller which has large switching frequency variation over input voltage, output current and temperature. Both in PFM and PWM, the on-time generator, which senses input voltage on VIN pin, provides very fast on-time response to input line transients.

Another one-shot sets a minimum off-time (typical: 200ns). The on-time one-shot is triggered if the error comparator is high, the low-side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

Power-On-Reset

A Power-On-Reset (POR) function is designed to prevent wrong logic controls when the VIN voltage is low. The POR function continually monitors the input supply voltage on the VIN pin if at least one of the enable pins is set high. When the rising VIN voltage reaches the rising POR voltage threshold (4V typical), the POR signal goes high and the chip initiates soft-start operations. There is a hysteresis to POR voltage threshold (about 200mV typical). When VIN voltage drop lower than 3.8V (typical), the POR disables the chip.

Soft- Start

The APW7318 has soft-start circuits to ramp up the output voltage of the converter to the programmed regulation setpoint at a predictable slew rate.

The figure 1 shows V_{OUT} soft-start sequence. When the EN pin is pulled above the rising EN threshold voltage, the device initiates a soft-start process to ramp up the output voltage.

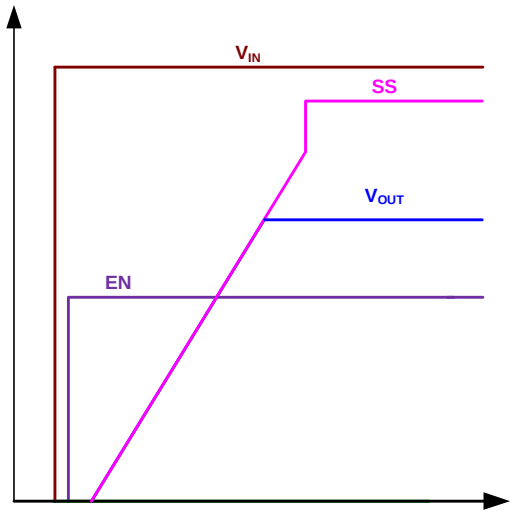


Figure 1. Soft-Start Sequence

When EN signal goes High, for UVP Function is Enabled after 0.5 t_{SS}. The over voltage and current limit protection functions are enabled. If the output capacitor has residue voltage before startup, both internal low-side and high-side MOSFETs are in off-state until the internal soft start voltage equal the V_{FB} voltage. This will ensure the output voltage starts from its existing voltage level.

Under Voltage Protection

In the process of operation, if a short-circuit occurs, the output voltage will drop quickly. When load current is bigger than current limit threshold value, the output voltage will fall out of the required regulation range. The under-voltage continually monitors the setting output voltage after internal soft start signal is okay. If a load step is strong enough to pull the output voltage lower than the under voltage threshold (50% of normal output voltage), the APW7318 enters hiccup mode to periodically restart the part (wait for eight times T_{SS} Time). This protection mode is especially useful when the output is dead-shorted to ground. The average short circuit current is greatly reduced to alleviate thermal issues and to protect the regulator. The APW7318 exits the hiccup mode once the output voltage V_{OUT} bigger than UVP Hysteresis (typical: 10%).

Over Voltage Protection (OVP)

The over-voltage function monitors the output voltage by FB pin. Once the voltage V_{FB} exceeds 125% of the reference voltage, the over-voltage protection comparator forces the high-side and low-side MOSFETs off and into discharge state. It's a common problem for OVP schemes with a latch. Once an over-voltage fault condition is set, toggling VIN power-on-reset signal or EN re-tiggered can reset it.

PWM Converter Current Limit

The current-limit circuit employs a "valley" current-sens-ing algorithm (See Figure 2). The APW7318 uses the internal low-side MOSFET's $R_{DS(ON)}$ of the synchronous rectifier as a current-sensing element. If the magnitude of the current-sense signal at SW pin is above the current limit threshold, the PWM is not allowed to initiate a new cycle. The actual peak current is greater than the current limit threshold by an amount equals to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are the functions of the sense resistance, inductor value, and input voltage.

The PWM controller uses the internal low-side MOSFETs on-resistance $R_{DS(ON)}$ to monitor the current for protection against shortened outputs. The cycle by cycle current limit threshold is 5A for APW7318.

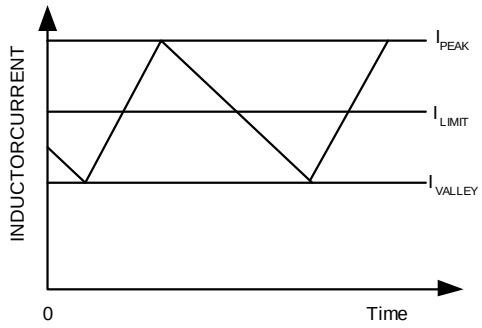


Figure 2. Current Limit Algorithm

Thermal Shutdown

A thermal shutdown circuit limits the junction temperature of APW7318. When the junction temperature exceeds +150℃, PWM converter is shut off, allowing the device to cool down. The regulator regulates the output again through initiation of a new soft-start cycle after the junction temperature cools by 35℃, resulting in a pulsed output during continuous thermal overload conditions. The thermal shutdown designed with a 35℃ hysteresis lowers the average junction temperature during continuous thermal overload conditions, extending life time of the device.

For normal operation, device power dissipation should be externally limited so that junction temperatures will not exceed +125℃

Application Information

Input Capacitor Selection

Because buck converters have a pulsating input current, a low ESR input capacitor is required. This results in the best input voltage filtering, minimizing the interference with other circuits caused by high input voltage spikes.

Also, the input capacitor must be sufficiently large to stabilize the input voltage during heavy load transients. For good input voltage filtering, usually a 22µF input capacitor is sufficient. It can be increased without any limit for better input-voltage filtering. Ceramic capacitors show better performance because of the low ESR value, and they are less sensitive against voltage transients and spikes compared to tantalum capacitors. Place the input capacitor as close as possible to the input and GND pin of the device for better performance.

Inductor Selection

For high efficiencies, the inductor should have a low DC resistance to minimize conduction losses. Especially at high-switching frequencies, the core material has a higher impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. A reasonable starting point for setting ripple current, ΔI_L, is 40% of maximum output current. The recommended inductor value can be calculated as below:

$$L \geq \frac{V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right)}{F_{SW}\cdot \Delta I_L}$$

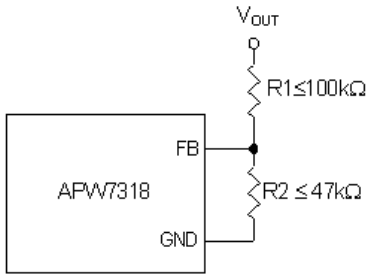
$$I_{L(MAX)} = I_{OUT(MAX)} + \frac{1}{2}\Delta I_L$$

To avoid saturation of the inductor, the inductor should be rated at least for the maximum output current of the converter plus the inductor ripple current.

Output Voltage Setting

The output voltage is set by a resistive divider. The external resistive divider is connected to the output, allowing remote voltage sensing as shown in “Typical Application Circuits”. A suggestion of maximum value of R2 is 47k to keep the minimum current that provides enough noise rejection ability through the resistor divider. The output voltage can be calculated as below:

$$V_{OUT} = V_{REF}\cdot\left(1+\frac{R1}{R2}\right) = 0.8\cdot\left(1+\frac{R1}{R2}\right)$$

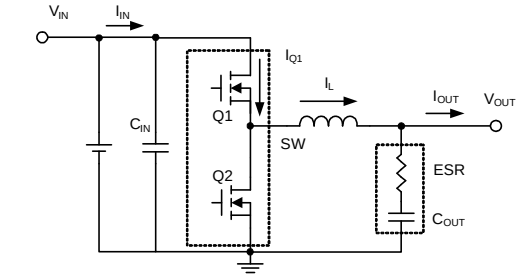


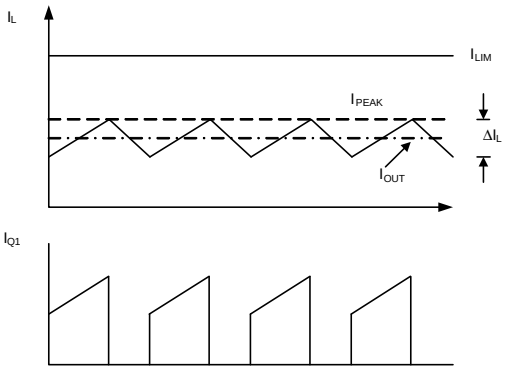
Output Capacitor Selection

The current-mode control scheme of the APW7318 allows the use of tiny ceramic capacitors. The higher capacitor value provides the good load transients response. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. If required, tantalum capacitors may be used as well. The output ripple is the sum of the voltages across the ESR and the ideal output capacitor.

$$\Delta V_{OUT} \cong \frac{V_{OUT}\cdot\left(1-\frac{V_{OUT}}{V_{IN}}\right)}{F_{SW}\cdot L}\cdot\left(ESR+\frac{1}{8\cdot F_{SW}\cdot C_{OUT}}\right)$$

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.





Application Information

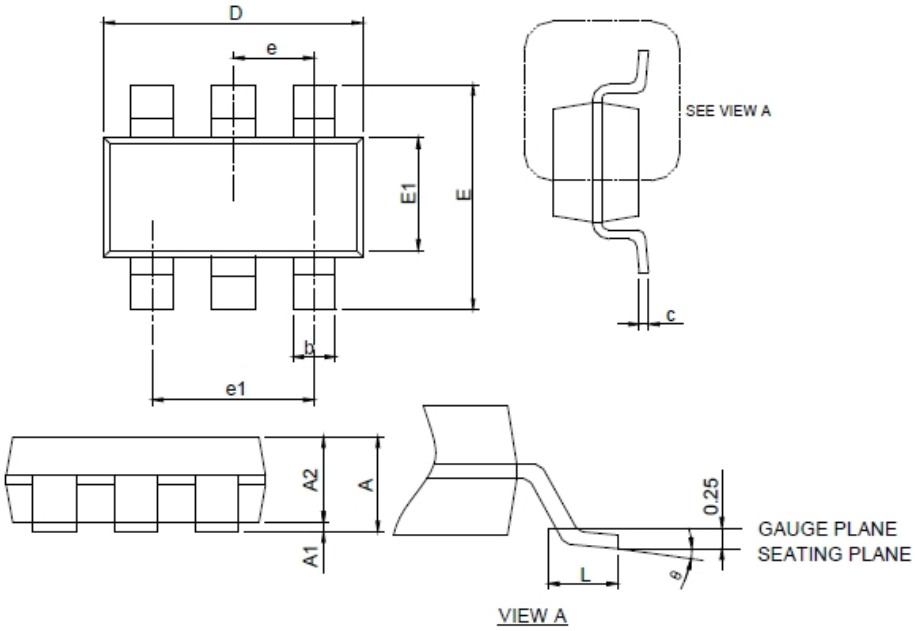
Layout Consideration

For all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

1. The input capacitor should be placed close to the VIN and GND. Connecting the capacitor and VIN/GND with short and wide trace without any via holes for good input voltage filtering. The distance between VIN/GND to capacitor less than 2mm respectively is recommended.
2. To minimize copper trace connections that can inject noise into the system, the inductor should be placed as close as possible to the SW pin to minimize the noise coupling into other circuits.
3. The output capacitor should be place closed to converter VOUT and GND.
4. Since the feedback pin and network is a high impedance circuit the feedback network should be routed away from the inductor. The feedback pin and feedback network should be shielded with a ground plane or trace to minimize noise coupling into this circuit.
5. A star ground connection or ground plane minimizes ground shifts and noise is recommended.

Package Information

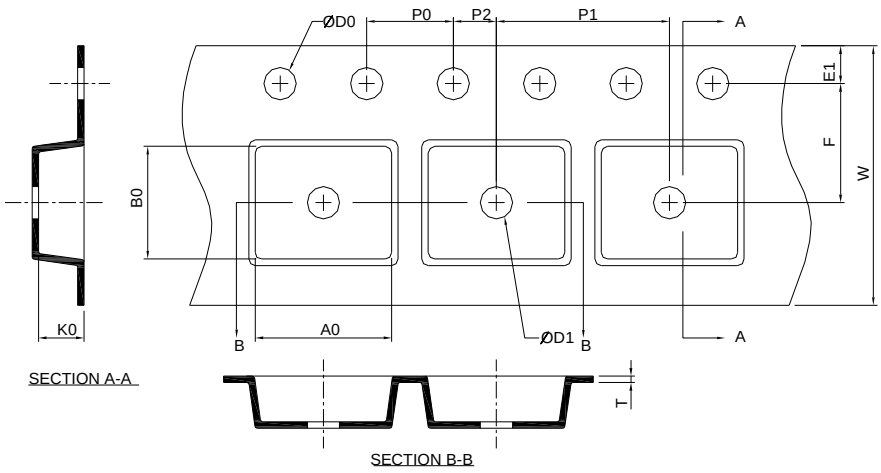
TSOT-23-6A

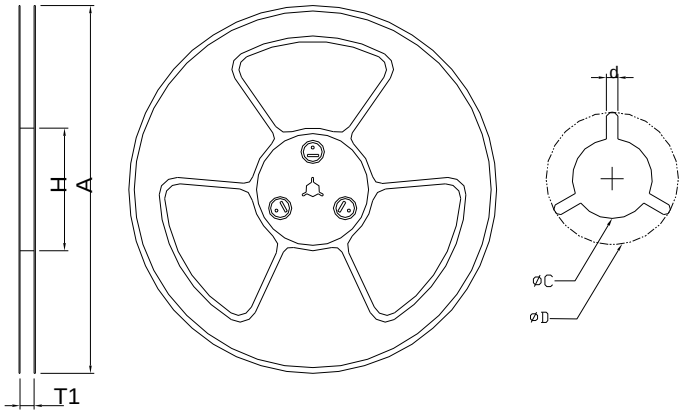


SYMBOL	TSOT-23-6A			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	1.00	0.028	0.039
A1	0.01	0.10	0.000	0.004
A2	0.70	0.90	0.028	0.035
b	0.30	0.50	0.012	0.020
c	0.08	0.20	0.003	0.008
D	2.70	3.10	0.106	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

Note : 1. Followed from JEDEC TO-178 AB.
2. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions





Application	A	H	T1	C	d	D	W	E1	F
	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
TSOT-23-6A	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.0 MIN.	0.6+0.00 -0.40	3.20±0.20	3.10±0.20	1.20±0.20

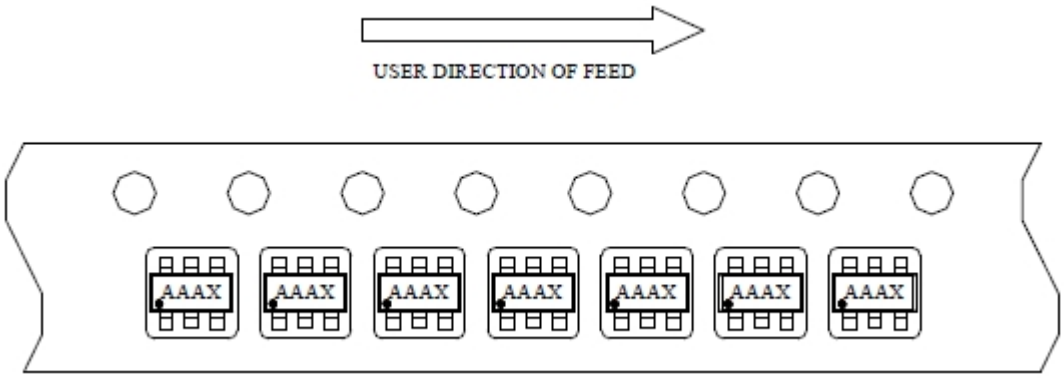
(mm)

Devices Per Unit

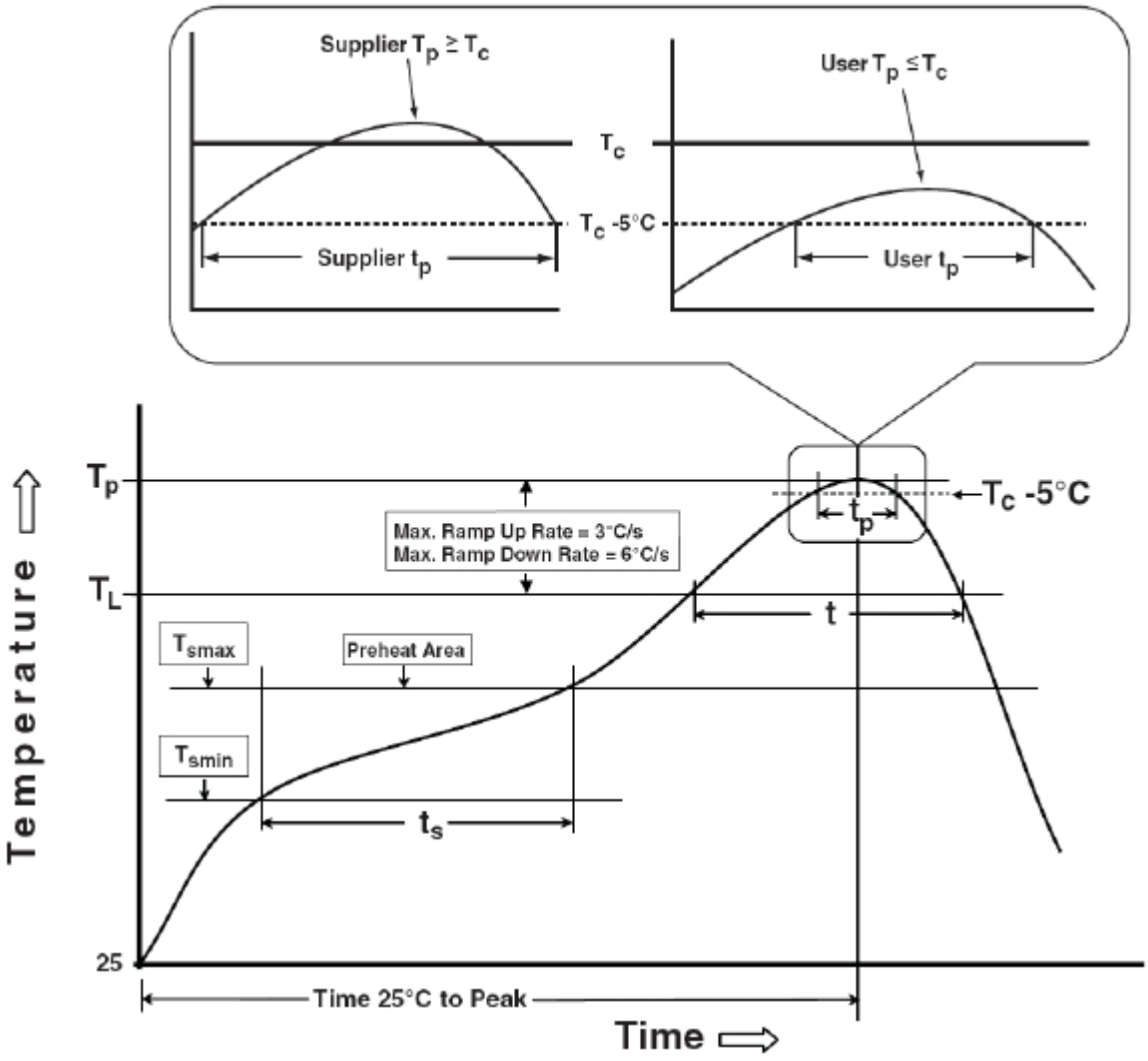
Package Type	Unit	Quantity
TSOT-23-6A	Tape & Reel	3000

Taping Direction Informationackage

TSOT-23-6A



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ Tj=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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