

3.5A, 5V, 1.2MHz Synchronous Step-Down Converter

Features

- **3.5A Continuous Output Current**
- **Operating Voltage Range : 2.7V~5.5V**
- **Fixed Switching Frequency : 1.2MHz (PWM)**
- **0.6V Reference Voltage**
- **PSM/PWM Operation**
- **Low RDS(ON) Internal Power MOSFETs**
- **OCP Protection and Thermal Shutdown**
- **Internal Compensation**
- **Short Circuit Protection with Hiccup mode**
- **Fold-back Switching Frequency**
- **Over Temperature Protection**
- **Input Over Voltage Protection**
- **TQFN2x2-12A package**
- **Lead Free and Green Devices Available (RoHS Compliant)**

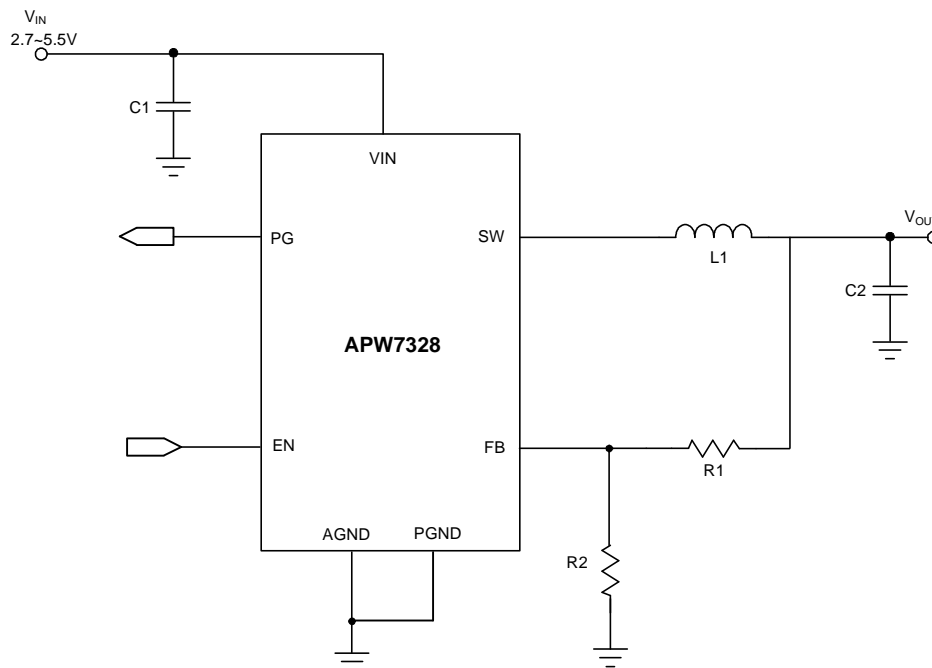
General Description

The APW7328 is a high efficiency monolithic synchronous buck converter. APW7328 operates with a constant 1.2MHz switching frequency and using the inductor current as a controlled quantity in the current mode architecture. The 2.7V to 5.5V input voltage range makes the APW7328 ideally suited for single Li-Ion battery powered applications. 100% duty cycle provides low dropout operation, extending battery life in portable electrical devices. The internally fixed 1.2MHz operating frequency allows the use of small surface mount inductors and capacitors.

Applications

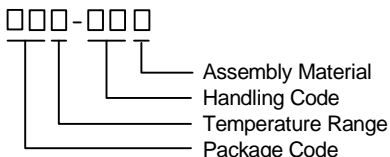

- **LCD TV**
- **Storage Drives**
- **Portable/Handheld Devices**
- **Wireless/Networking Cards**

Simplified Application Circuit



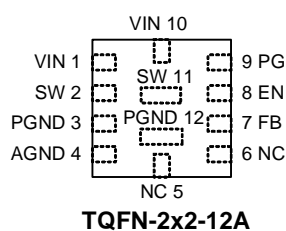
ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information

<p>APW7328</p>  <p> Assembly Material Handling Code Temperature Range Package Code </p>	<p> Package Code QB : TQFN-2x2-12A Operating Ambient Temperature Range I : -40 to 85°C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device </p>
<p>APW7328 QB :</p>  <p>X - Date Code</p>	

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Pin Configuration



Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN}	VIN to GND Voltage	-0.3 ~ 6	V
V_{SW}	SW to GND Voltage	>20ns	-0.3 ~ $V_{IN}+0.3$
		<20ns	-3 ~ 8
	EN, FB, PG to GND Voltage	-0.3 ~7	V
T_J	Maximum Junction Temperature	-40 ~ 150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air ^(Note 2)	80	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN}	VIN Supply Voltage	2.7 ~ 5.5	V
I_{OUT}	Converter Output Current	0 ~ 3.5	A
V_{OUT}	Output Voltage	1 ~ 3.3	V
L	Inductor	0.47~2.2	μH
C_{OUT}	Output Capacitor	4.7~22	μF
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over $V_{IN} = 5V$, $V_{EN} = 5V$ and $T_A = 25^\circ C$.

Symbol	Parameter	Test Conditions	APW7328			Unit
			Min	Typ	Max	
SUPPLY CURRENT						
I_{VIN1}	VIN Supply Current 1	$V_{IN} = 5V, V_{FB} = 0.7V, V_{EN} = 3V, SW = NC$	-	40	60	μA
I_{VIN2}	VIN Supply Current 2	$V_{IN} = 5V, V_{OUT} = 3.3V, \text{No Load}$	-	-	100	μA
I_{VIN_SD}	VIN Shutdown Supply Current	$V_{IN} = 5V, V_{EN} = 0V$	-	-	1	μA
UNDER-VOLTAGE-LOCKOUT (UVLO)						
	VIN UVLO Voltage Threshold	V_{IN} rising	2.35	2.5	2.65	V
	VIN UVLO Voltage Hysteresis	V_{IN} falling	0.3	0.4	0.5	V
REFERENCE VOLTAGE						
V_{REF}	Reference Voltage	Regulated on FB pin, $T_J = 25^\circ C$	0.591	0.600	0.609	V
OSCILLATOR AND DUTY CYCLE						
F_{OSC}	Oscillator Frequency	For APW7328	1.08	1.2	1.32	MHz
	Frequency Accuracy	$T_J = -40 \sim 85^\circ C$	-15	-	+15	%
	Minimum on Time		-	-	100	ns

Electrical Characteristics

Unless otherwise specified, these specifications apply over $V_{IN} = 5V$, $V_{EN} = 5V$ and $T_A = 25^\circ C$.

Symbol	Parameter	Test Conditions	APW7328			Unit
			Min	Typ	Max	
POWER MOSFET						
	High Side MOSFET Resistance	$I_{OUT}=2A$	-	70	-	m Ω
	Low Side MOSFET Resistance	$I_{OUT}=2A$	-	60	-	m Ω
	High Side MOSFET Leakage Current	$V_{EN}=0V, V_{SW}=0V, V_{IN}=5V$	-	-	10	μA
	Low Side MOSFET Leakage Current	$V_{EN}=0V, V_{SW}=5V, V_{IN}=5V$	-	-	10	μA
T_D	Dead Time		-	10	-	ns
PROTECTIONS						
	High Side MOSFET current-limit		3.7	4.7	5.7	A
	FB Frequency Foldback Threshold	Monitor V_{FB} falling below 0.4V to start foldback frequency	-	0.4	-	V
T_{OTP}	Over Temperature Trip Point		-	150	-	$^\circ C$
	Over Temperature Hysteresis		-	30	-	$^\circ C$
	Input Over Voltage Protection	Stop Switching	6.5	6.75	7	V
	Input Over Voltage Protection Hysteresis		0.1	0.3	0.5	V
	Over Voltage Protection	Stop switching, no latch	130	135	140	$\%V_{REF}$
	Over Voltage Protection Hysteresis		-	5	-	$\%V_{REF}$
	Hiccup Mode Protection	Monitor V_{REF} , enter Hiccup mode	25	30	35	$\%V_{REF}$
	Hiccup Mode Protection Hysteresis		-	5	-	$\%V_{REF}$
SOFT-START, ENABLE AND INPUT CURRENTS						
T_{SS}	Soft-Start Time		-	1	-	ms
	EN High-Level Voltage		1.2	-	-	V
	EN Low-Level Voltage		-	-	0.4	V
I_{FB}	FB Pin Input Current		-	-	0.1	μA

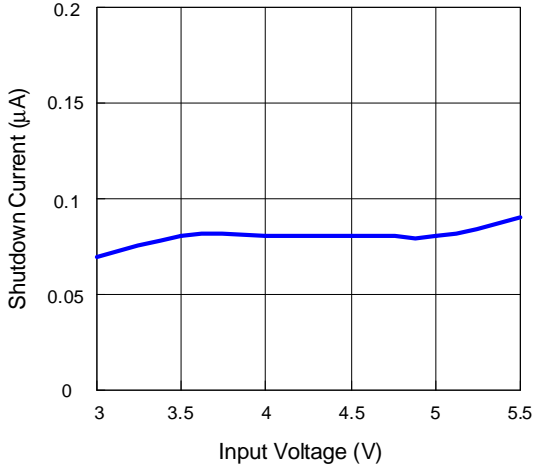
Electrical Characteristics

Unless otherwise specified, these specifications apply over $V_{IN}=5V$, $V_{EN}=5V$ and $T_A=25^\circ C$.

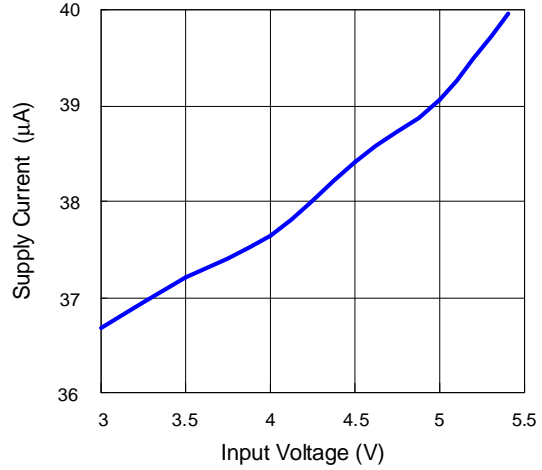
Symbol	Parameter	Test Conditions	APW7328			Unit
			Min	Typ	Max	
POWER GOOD						
	PG Low Threshold (PG goes high)	V_{FB} rising	85	90	95	$\%V_{REF}$
	PG Low Threshold Hysteresis	V_{FB} falling	-	3	-	$\%V_{REF}$
	PG Delay Time	The time from $V_{FB}=90\%*V_{FB}$ to PG goes high	-	90	-	μs
	PG High Threshold(PG goes low)	V_{FB} rising	105	110	115	$\%V_{REF}$
	PG High Threshold Hysteresis	V_{FB} falling	-	3	-	$\%V_{REF}$
	PG High Threshold Debounce Time		-	50	-	μs
	PG Internal Pull Up Resistor		-	500	-	$k\Omega$
	PG Pull Low Resistance	$V_{PG}=0.1V$	-	100	-	Ω
	PG Leakage Current	$EN=0V, V_{PG}=5V$	-	-	0.1	μA

Typical Operating Characteristics

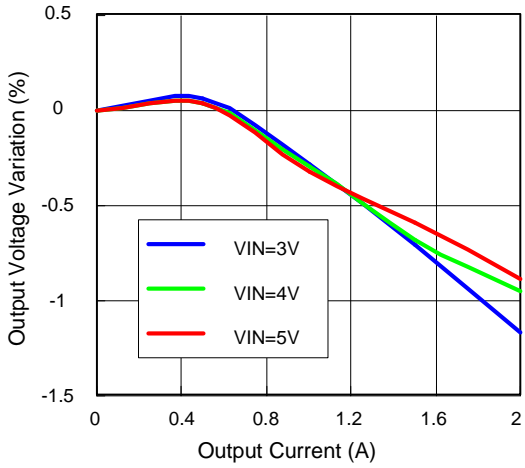
Shutdown Current vs. Input Voltage



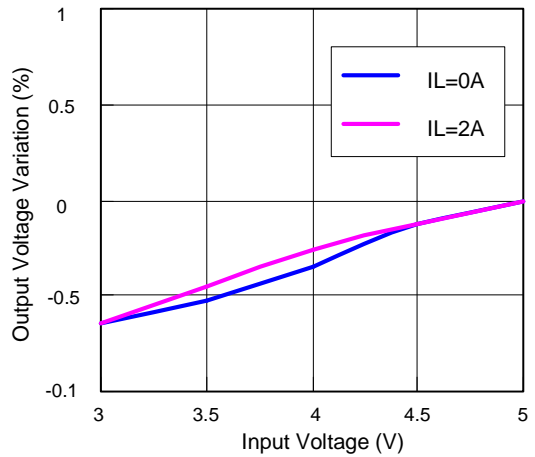
Supply Current vs. Input Voltage



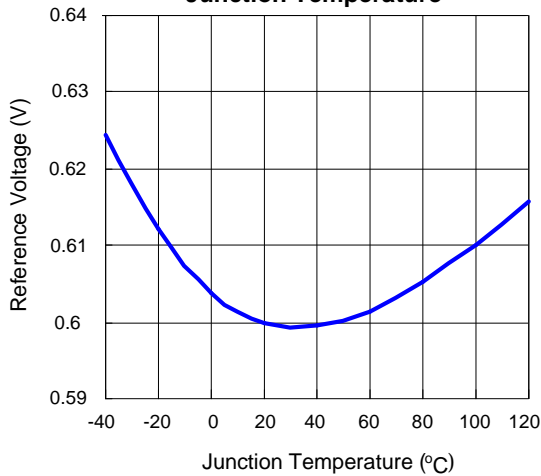
Load Regulation



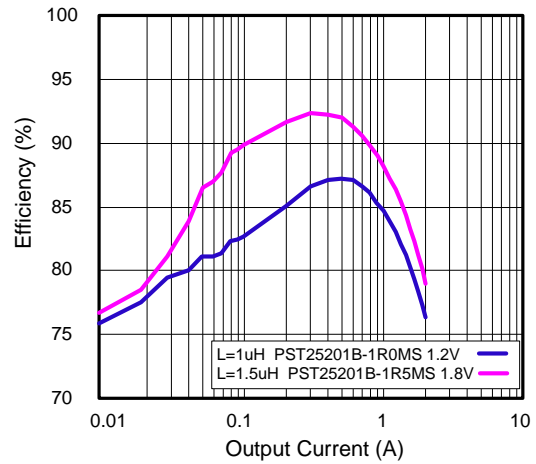
Line Regulation



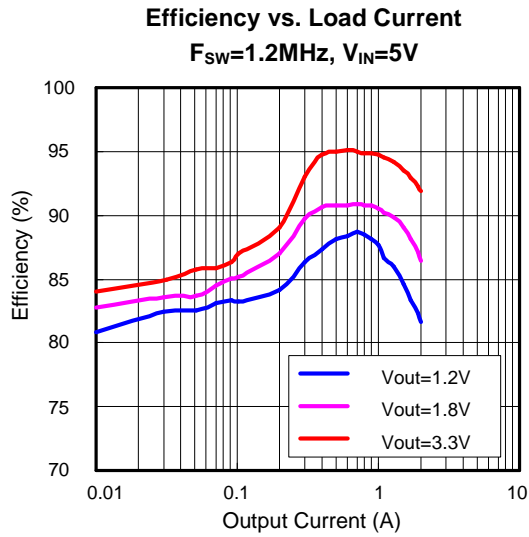
Reference Voltage vs. Junction Temperature



Efficiency vs. Load Current
F_{SW}=1.2MHz, V_{IN}=3.3V



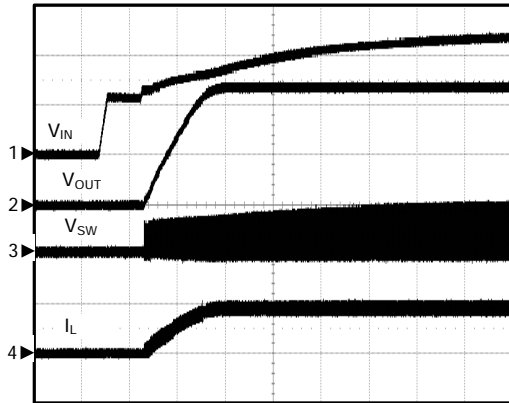
Typical Operating Characteristics



Operating Waveforms

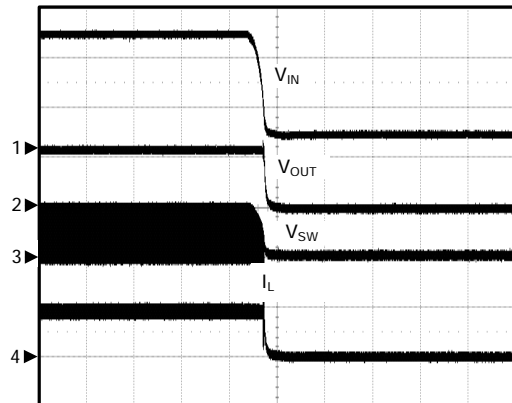
Refer to the typical application circuit. The test condition is $V_{IN}=5V$, $T_A=25^{\circ}C$ unless otherwise specified.

V_{IN} Power On with 2A Load



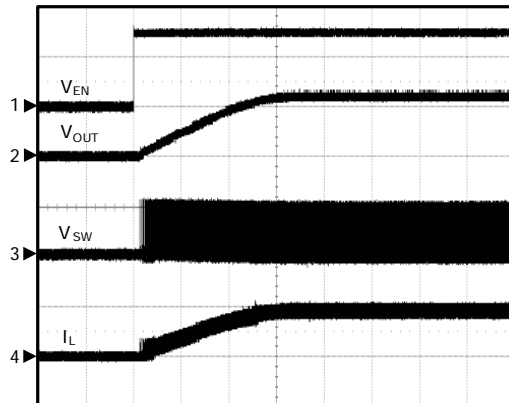
CH1: V_{IN} , 2V/Div
 CH2: V_{OUT} , 500mV/Div
 CH3: V_{SW} , 5V/Div
 CH4: I_L , 2A/Div
 TIME: 1ms/Div

V_{IN} Power Off with 2A Load



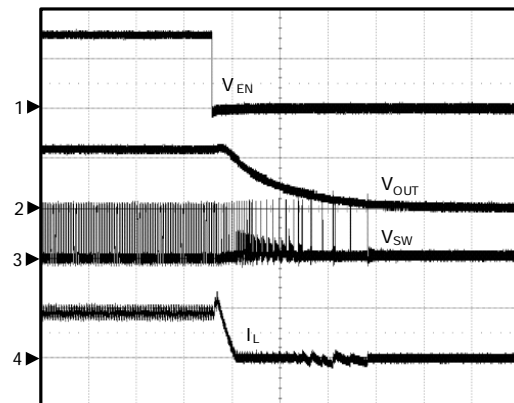
CH1: V_{IN} , 2V/Div
 CH2: V_{OUT} , 1V/Div
 CH3: V_{SW} , 5V/Div
 CH4: I_L , 2A/Div
 TIME: 10ms/Div

EN Start Up with 2A Load



CH1: V_{EN} , 2V/Div
 CH2: V_{OUT} , 1V/Div
 CH3: V_{SW} , 5V/Div
 CH4: I_L , 2A/Div
 TIME: 500 μ s/Div

EN Shutdown with 2A Load

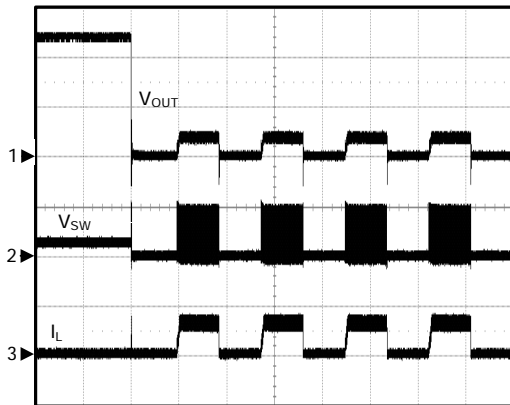


CH1: V_{EN} , 2V/Div
 CH2: V_{OUT} , 1V/Div
 CH3: V_{SW} , 5V/Div
 CH4: I_L , 2A/Div
 TIME: 10 μ s/Div

Operating Waveforms

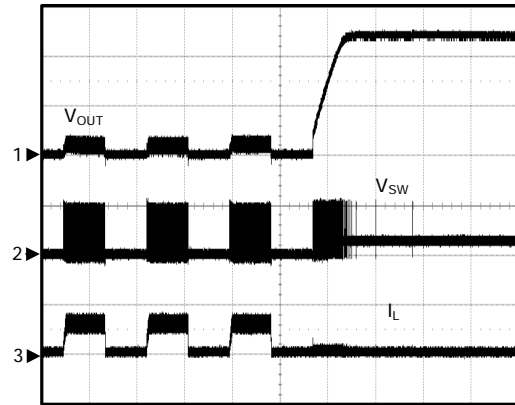
Refer to the typical application circuit. The test condition is $V_{IN}=5V$, $T_A=25^{\circ}C$ unless otherwise specified.

Short Circuit Entry



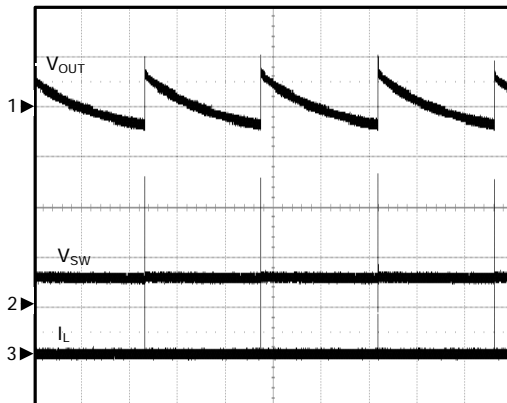
CH1: V_{OUT} , 500mV/Div
 CH2: V_{SW} , 5V/Div
 CH3: I_L , 5A/Div
 TIME: 2ms/Div

Short Circuit Recovery



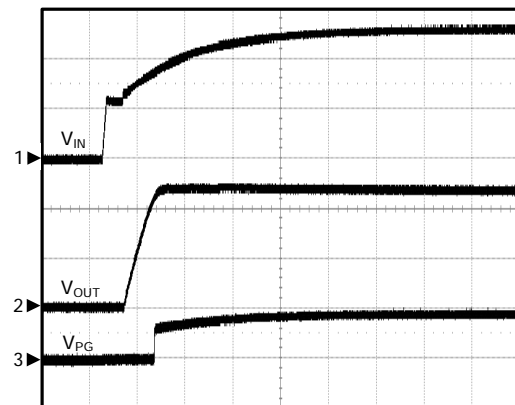
CH1: V_{OUT} , 500mV/Div
 CH2: V_{SW} , 5V/Div
 CH3: I_L , 5A/Div
 TIME: 2ms/Div

Output Ripple at 0A



CH1: V_{OUT} , 50mV/Div, AC
 CH2: V_{SW} , 2V/Div
 CH3: I_L , 1A/Div
 TIME: 20ms/Div

Power OK

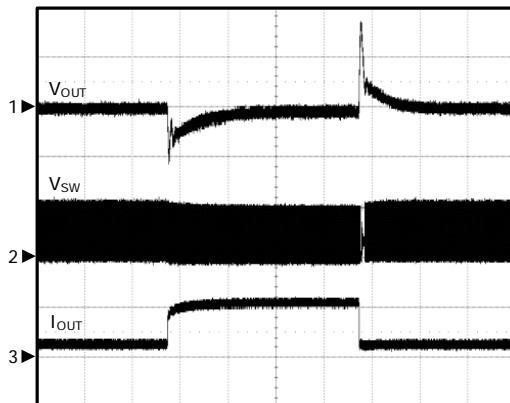


CH1: V_{IN} , 2V/Div
 CH2: V_{OUT} , 500mV/Div
 CH3: V_{PG} , 5V/Div
 TIME: 2ms/Div

Operating Waveforms

Refer to the typical application circuit. The test condition is $V_{IN}=5V$, $T_A=25^{\circ}C$ unless otherwise specified.

Load Transient

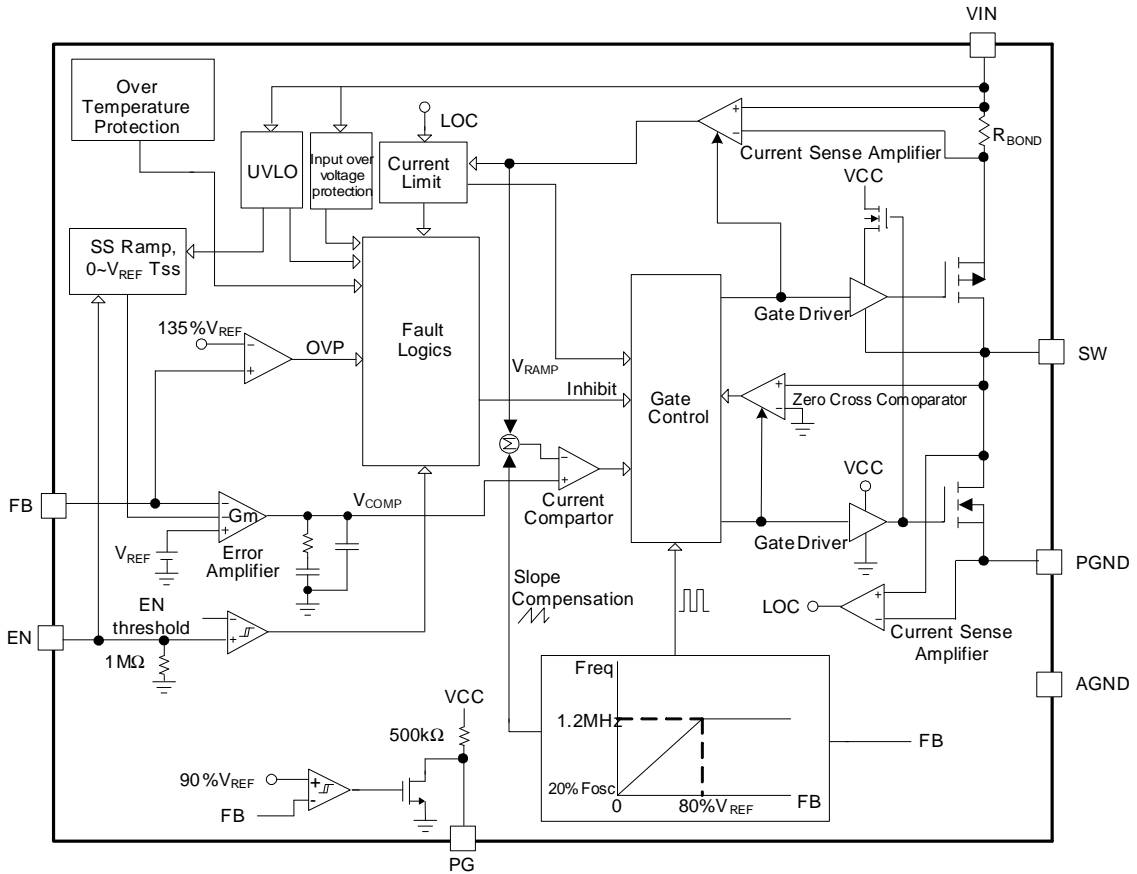


CH1: V_{OUT} , 100mV/Div, AC
 CH2: V_{SW} , 5V/Div
 CH3: I_{OUT} , 2A/Div
 TIME: 50µs/Div

Pin Description

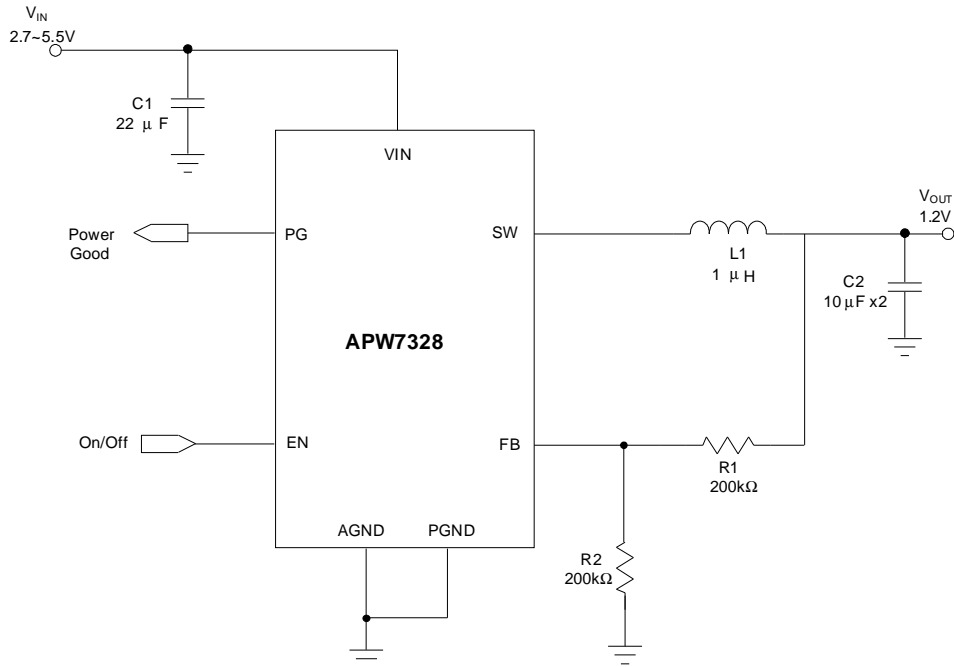
PIN		FUNCTION
NO.	NAME	
1,10	VIN	Power Input. Connect a ceramic bypass capacitor from VIN to GND.
2,11	SW	Power Switching Output. The SW is the junction of the high-side and low-side power MOSFET to supply power to the output LC filter.
3,12	PGND	Power ground. Connect this pin with large copper area to negative terminals of the input and output capacitors.
4	AGND	Ground for controller circuit
5,6	NC	NC
7	FB	Output Feedback Input. The APW7328 senses the feedback voltage via FB and regulates the voltage at 0.6V. Connecting FB with a resistor-divider from the converter's output sets the output voltage.
8	EN	Enable pin of the PWM converter. When the EN is above high logic level, the device is in operation mode. When the EN is below low logic level, the device is in shutdown mode. This pin can not be left open.
9	PG	Power Good Output. When V_{FB} has risen above 90% of V_{REF} during soft-start period, the PG will go high. This pin is an open-drain logic output that is pulled to the ground.

Block Diagram



Typical Application Circuit

For APW7328



Function Description

Main Control Loop

The APW7328 is a constant frequency, synchronous rectifier and current-mode switching regulator. In normal operation, the internal upper power MOSFET is turned on each cycle. The peak inductor current at which ICMP turn off the upper MOSFET is controlled by the voltage on the COMP node, which is the output of the error amplifier (EAMP). An external resistive divider connected between VOUT and ground allows the EAMP to receive an output feedback voltage V_{FB} at FB pin. When the load current increases, it causes a slightly decrease in V_{FB} relative to the 0.6V reference, which in turn causes the COMP voltage to increase until the average inductor current matches the new load current.

Enable/Shutdown

Driving EN to the ground places the APW7328 in shutdown mode. When in shutdown, the internal power MOSFETs turn off, all internal circuitry shuts down and the quiescent supply current reduces to 1 μ A typical.

Under Voltage Lockout (UVLO)

An under-voltage lockout function prevents the device from operating if the input voltage on VIN is lower than approximately 2.5V. The device automatically enters the shutdown mode if the voltage on VIN drops below approximately 2.5V. This under-voltage lockout function is implemented in order to prevent the malfunctioning of the converter.

Soft-Start

The APW7328 has a built-in soft-start to control the output voltage rise during start-up. During soft-start, an internal ramp voltage, connected to the one of the positive inputs of the error amplifier, raises up to replace the reference voltage (0.6V typical) until the ramp voltage reaches the reference voltage. Then, the voltage on FB regulated at reference voltage.

Over-Current-Protection and Hiccup

The APW7328 has a cycle-by-cycle over-current limit when the inductor current peak value exceeds the set current limit threshold. Meanwhile, the output voltage drops until FB is below 30% of the reference voltage the APW7328 enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-shortened to ground. The average short circuit current is greatly reduced to alleviate thermal issues and to protect the regulator. The APW7328 exits the hiccup mode once the over-current condition is removed.

Over-Temperature Protection (OTP)

The over-temperature circuit limits the junction temperature of the APW7328. When the junction temperature exceeds 150°C, a thermal sensor turns off the both power MOSFETs, allowing the devices to cool. The thermal sensor allows the converters to start a soft-start process and regulate the output voltage again after the junction temperature cools by 30°C. The OTP is designed with a 30°C hysteresis to lower the average Junction Temperature (T_J) during continuous thermal overload conditions, increasing the lifetime of the device.

Over-Voltage Protection (OVP)

The over-voltage function monitors the output voltage by FB pin. Once the FB voltage exceeds 135% of the reference voltage, the over-voltage protection comparator forces the low-side MOSFET and high-side MOSFET are off. AS soon as the output voltage is below 130% of the reference voltage, the low-side MOSFET off and the OVP comparator is disengaged, The chip restores its normal operation.

Function Description

Frequency Foldback

The foldback frequency is controlled by the FB voltage. When the output is short to the ground, the frequency of the oscillator will be reduced to $0.1 \times F_{SW}$. This lower frequency allows the inductor current to safely discharge, there by preventing current runaway. The oscillator's frequency will gradually increase to its designed rate when the feedback voltage on FB again approaches 0.6V.

Power Good

APW7328 has an open drain with 500k Ω pull-up resistor pin for power good indicator. In normal operation, when the output voltage rises 90% of its target value after 90 μ s, the PG goes high, when the output voltage outruns 110% of the target voltage, POK signal will be pulled low immediately.

Application Information

Input Capacitor Selection

Because buck converters have a pulsating input current, a low ESR input capacitor is required. This results in the best input voltage filtering, minimizing the interference with other circuits caused by high input voltage spikes. Also, the input capacitor must be sufficiently large to stabilize the input voltage during heavy load transients. For good input voltage filtering, usually a 22 μ F input capacitor is sufficient. It can be increased without any limit for better input-voltage filtering. Ceramic capacitors show better performance because of the low ESR value, and they are less sensitive against voltage transients and spikes compared to tantalum capacitors. Place the input capacitor as close as possible to the input and GND pin of the device for better performance.

Inductor Selection

For high efficiencies, the inductor should have a low DC resistance to minimize conduction losses. Especially at high-switching frequencies, the core material has a higher impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. A reasonable starting point for setting ripple current, ΔI_L , is 40% of maximum output current. The recommended inductor value can be calculated as below:

$$L \geq \frac{V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}} \right)}{F_{SW} \cdot \Delta I_L}$$

$$I_{L(MAX)} = I_{OUT(MAX)} + \frac{1}{2} \Delta I_L$$

To avoid saturation of the inductor, the inductor should be rated at least for the maximum output current of the converter plus the inductor ripple current.

Output Voltage Setting

In the adjustable version, the output voltage is set by a resistive divider. The external resistive divider is connected to the output, allowing remote voltage sensing as shown in "Typical Application Circuits". The output voltage can be calculated as below:

$$V_{OUT} = V_{REF} \cdot \left(1 + \frac{R1}{R2} \right) = 0.6 \cdot \left(1 + \frac{R1}{R2} \right)$$

Output Capacitor Selection

The current-mode control scheme of the APW7328 allows the use of tiny ceramic capacitors. The higher capacitor value provides the good load transients response. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. If required, tantalum capacitors may be used as well. The output ripple is the sum of the voltages across the ESR and the ideal output capacitor.

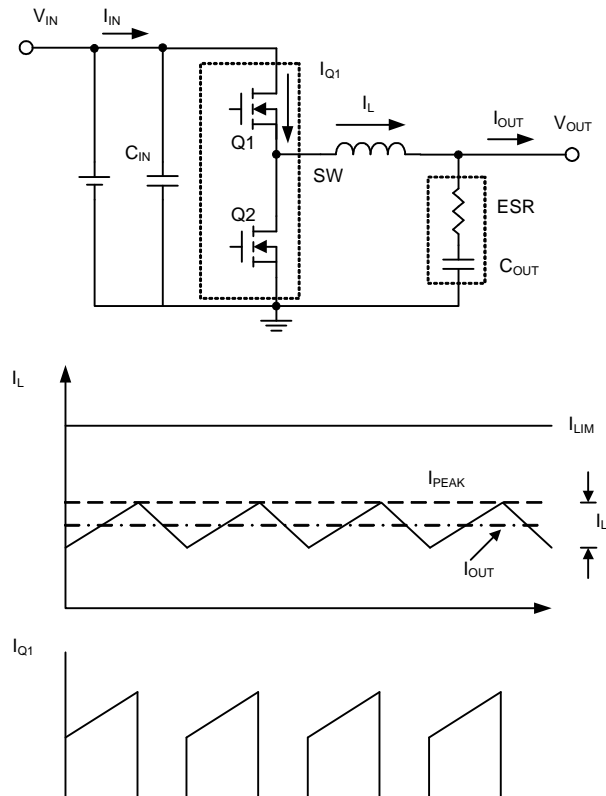
$$\Delta V_{OUT} \cong \frac{V_{OUT} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}} \right)}{F_{SW} \cdot L} \cdot \left(ESR + \frac{1}{8 \cdot F_{SW} \cdot C_{OUT}} \right)$$

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Application Information

OutPut Capacitor Selection

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.



3. The output capacitor should be place closed to converter VOUT and GND.
4. Since the feedback pin and network is a high impedance circuit the feedback network should be routed away from the inductor. The feedback pin and feedback network should be shielded with a ground plane or trace to minimize noise coupling into this circuit.
5. A star ground connection or ground plane minimizes ground shifts and noise is recommended.

Recommended Minimum Footprint

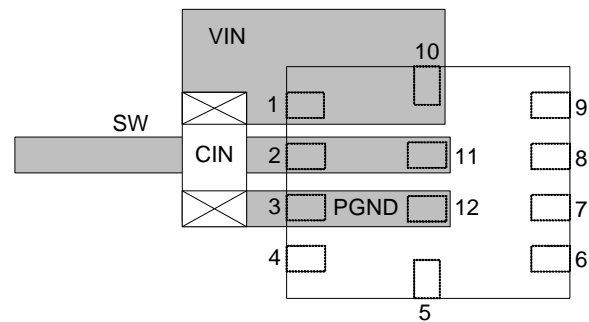


Figure 1. The 1210 Size Ceramic Capacitor Close to VIN and PGND

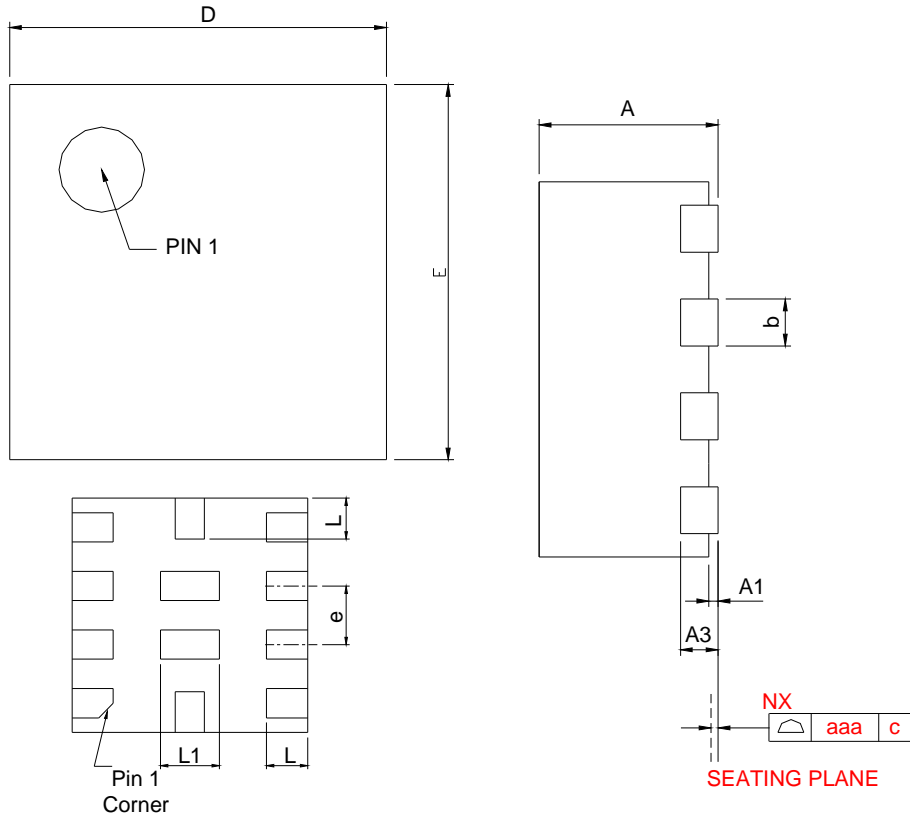
Layout Consideration

For all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

1. As shown in Figure 1, the 1210 size ceramic capacitor is used, please make sure the two ends of the ceramic capacitor be directly connected to VIN (the power input pin) and PGND (the power GND pin)
2. To minimize copper trace connections that can inject noise into the system, the inductor should be placed as close as possible to the SW pin to minimize the noise coupling into other circuits.

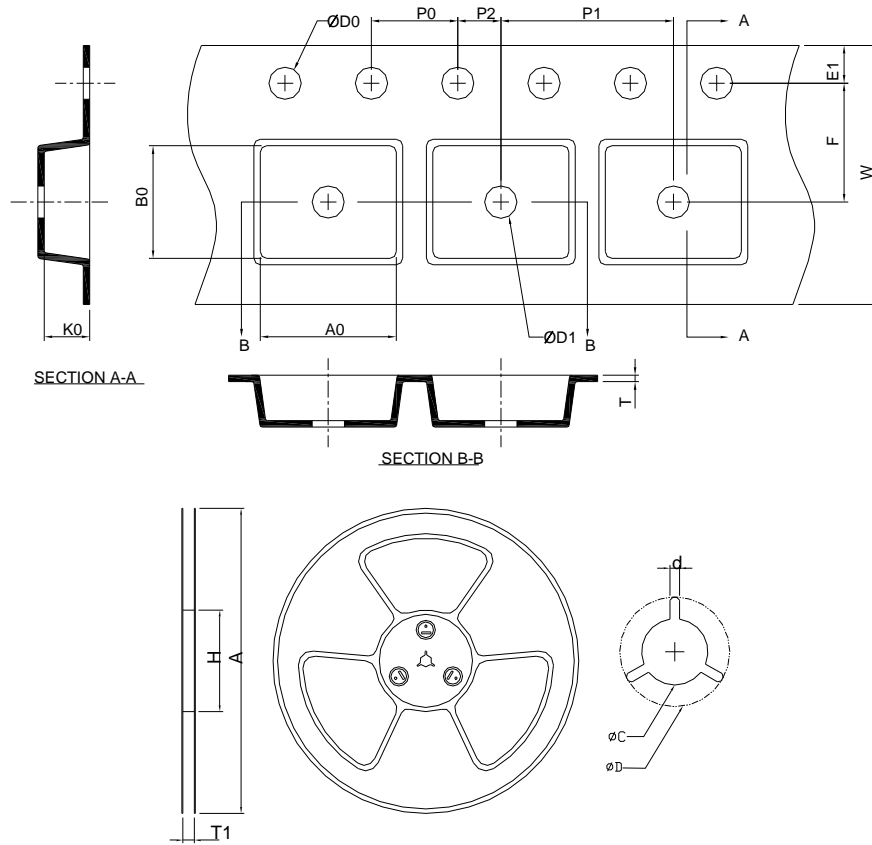
Package Information

TQFN2x2-12A



SYMBOL	TQFN2*2-12A			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	1.90	2.10	0.075	0.083
E	1.90	2.10	0.075	0.083
e	0.50 BSC		0.020 BSC	
L	0.30	0.40	0.012	0.016
L1	0.50 BSC		0.020 BSC	
aaa	0.08		0.003	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN2x2	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.20	1.75±0.10	3.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	2.35±0.20	2.35±0.20	1.00±0.20

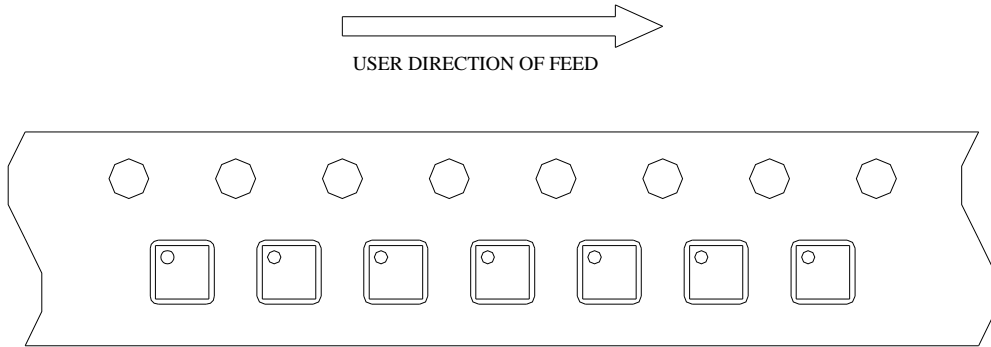
(mm)

Devices Per Unit

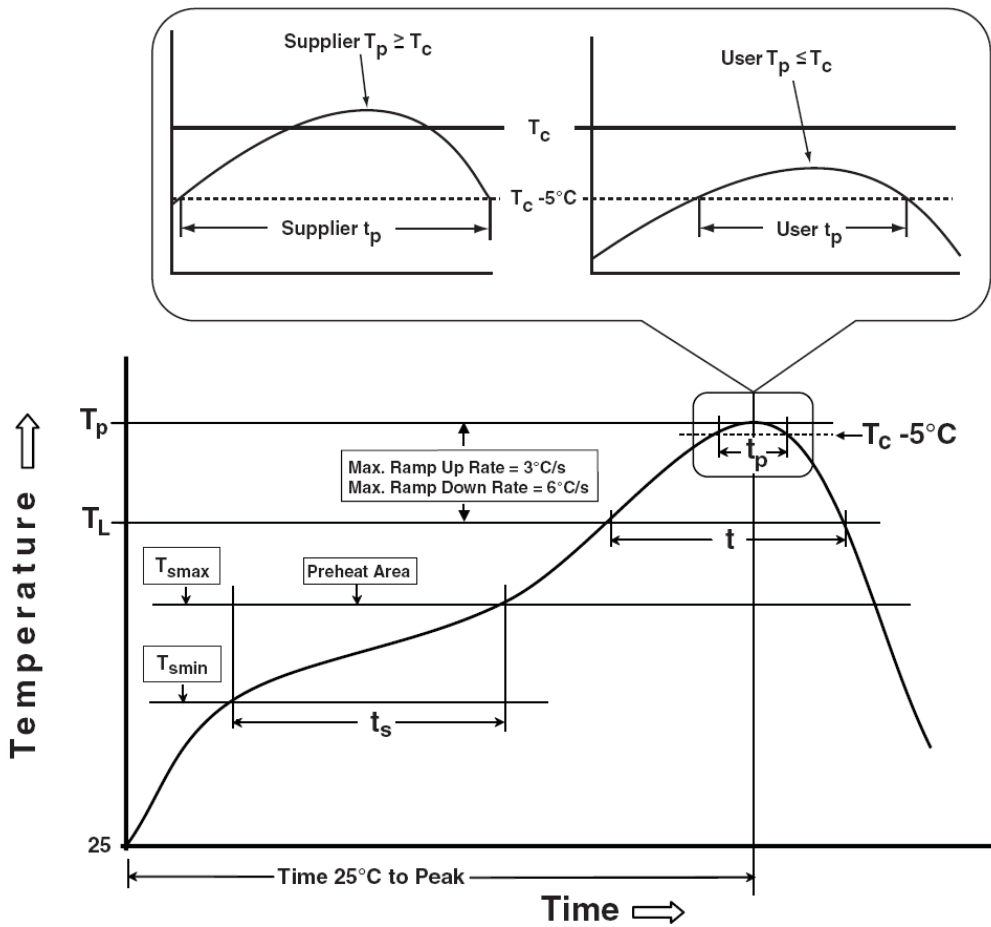
Package Type	Unit	Quantity
TQFN2x2	Tape & Reel	3000

Taping Direction Information

TQFN2x2



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak		
Temperature min (T_{smin})	100 °C	150 °C
Temperature max (T_{smax})	150 °C	200 °C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds	60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L)	183 °C	217 °C
Time at liquidous (t_L)	60-150 seconds	60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_p)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum.		
** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ 350-2000	Volume mm ³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ $T_j=125^\circ\text{C}$
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≥ 2KV
MM	JESD-22, A115	VMM ≥ 200V
Latch-Up	JESD 78	10ms, $1_{tr} \geq 100\text{mA}$

Customer Service

Anpec Electronics Corp.

Head Office :

No.6, Dusing 1st Road, SBIP,
Hsin-Chu, Taiwan, R.O.C.

Tel : 886-3-5642000

Fax : 886-3-5642050

Taipei Branch :

2F, No. 11, Lane 218, Sec 2 Jhongsing Rd.,
Sindian City, Taipei County 23146, Taiwan

Tel : 886-2-2910-3838

Fax : 886-2-2917-3838