High Efficiency Output 1A, 2.2MHz Buck Converter

Features

- **Wide Input Voltage from 2.5V to 6.0V**
- **0.6V to VIN Adjustable Output Voltage**
- **Optional fixed output voltage 1.8V or 2.5V**
- **Up to 95% Efficiency**
- **1A Output Current**
- **50uA Operating Quiescent Current**
- **100% Duty Cycle for Lowest Dropout**
- **Output Discharge Function**
- **2.2MHz Switching Frequency**
- **Power Good Output**
- **PWM/PFM Auto Switch**
- **Thermal Shutdown Protection**
- **Hiccup Short-Circuit Protection**
- **Lead Free Green Devices Available (RoHS)**

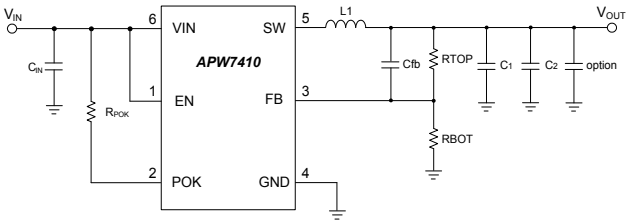
General Description

APW7410 is a high-frequency 1A synchronous buck converter with integrated 75mΩ high side and 50mΩ low side power MOSFET. The APW7410, design with a COT control scheme, can convert wide input voltage of 2.5V to 6V to the output voltage adjustable from 0.6V to 4V to provide excellent output voltage regulation.

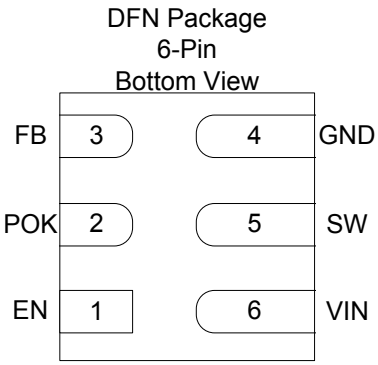
The APW7410 is equipped with an automatic PFM/PWM mode operation. At light load, the IC operates in the PFM mode to reduce the switching losses. At heavy load, the IC works in PWM mode.

The APW7410 is also equipped with Power-on-reset, Soft start, Enable/disable and whole protections (over-voltage, under-voltage, over-temperature and current-limit) into a single package. This device, available DFN1.5X1.5-6 and, provides a very compact system solution external components and PCB area.

Simplified Application Circuit



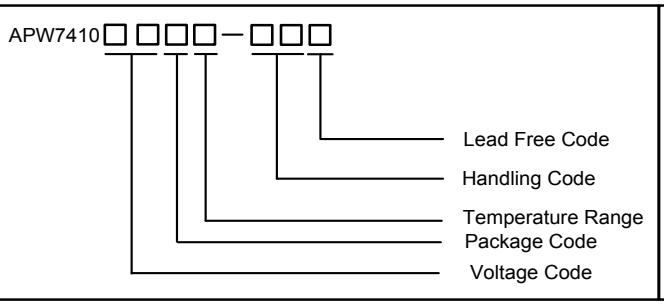
Pin Configuration



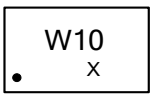
Applications

- **Battery-Powered Applications**
- **Point-of-Load**
- **Processor Supplies**
- **Hard Disk Drives (HDD) / Solid State Drives(SSD)**

Ordering and Marking Information



Voltage Code
Blank : V_{FB}=0.6V 18 : V_{FB}=1.8V 25 : V_{FB}=2.5V
Package Code
QA : DFN1.5x1.5-6
Operating Ambient Temperature Range
I : -40 to 85°C
Handling Code
TR : Tape & Reel
Assembly Material
G:Halogen and Leed Free Device



X -Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter		Rating	Unit
V_{IN}	VIN to GND Voltage		-0.3 ~ 7	V
V_{SW}	SW to GND Voltage	>20ns	-0.3 ~ V_{IN}+0.3	V
		<20ns	-3 ~ 8	V
Other Pins	EN,POK and FB to GND Voltage		-0.3 ~ 7	V
T_J	Junction Temperature		-40 ~ 150	°C
T_{STG}	Storage Temperature		-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature(10 Seconds)		260	°C
$V_{ESD-HBM}$	Minimum ESD Rating (Human Body Mode)		≧ ±2000	V
V_{ESD-MM}	Minimum ESD Rating (Machine Mode)		≧ ±200	V
$V_{ESD-CDM}$	Minimum ESD Rating (Charged Device Mode)		± 500	V

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under"recommended operating conditions"is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	129	°C/W
θ_{JC}	Junction-to-Case Resistance in free air (Note 2)	102	°C/W

Note 2: θ_{JA} and θ_{JC} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operation Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN}	VIN to GND Voltage	2.5 ~ 6	V
V_{OUT}	Adjustable Output Voltage Range	0.6 ~ V_{IN}	V
I_{OUT}	Converter Output Current	0 ~ 1	A
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the typical application circuit

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=2.5V ~ 6V, and T_A=-40°C ~ 85°C.

Symbol	Parameter	Test Conditions	Specification			Unit
			Min	Typ	Max	
Supply Current						
I_{IN}	V_{IN} Supply current	V_{FB}=0.63V, No Switching		50	65	uA
I_{SD}	V_{IN} Shutdown current	V_{EN}=0V		0.7	3.5	uA
Power-On-Reset (POR)						
V_{IN_POR}	V_{IN} POR High Threshold voltage	V_{IN} Rising	2.1	2.3	2.45	V
	V_{IN} POR Hysteresis voltage	V_{IN} Falling	50	100	150	mV
Power Switch						
F_{SW}	Switching Frequency	PWM Mode	2	2.2	2.4	MHz
	Dead Time (Note 4)	LG falling to UG rising		5		ns
		UG falling to LG rising		5		ns
$R_{DS(on)}$	High-side FET On-Resistance	I_{SW}=0.5A		75	160	mΩ
	Low-side FET On-Resistance	I_{SW}=0.5A		50	105	mΩ
D_{MAX}	Maximum Converter's Duty				100	%
R_{DIS}	Output discharge resistor			50	165	Ω
EN Input						
V_{EN}	EN enable threshold voltage	V_{EN} Rising			1	V
		V_{EN} Falling	0.4			
	Input leakage current into EN pin	V_{EN} =5V		0.01	0.1	uA
Soft - Start						
T_{SS1}	Soft-Start Time	From EN high to 95% of V_{OUT}	0.6	0.8	1.1	ms
T_{SS2}		From 0% to 95% of V_{OUT}	0.3	0.5	0.8	ms
	Hicup Time			3		T_{SS2}
Reference Voltage						
V_{REF}	Reference Voltage	I_{OUT}=1A, (APW7410) (Note 4)	594	600	606	mV
		I_{OUT}=0A, PFM Mode (Note 4)		600		
		I_{OUT}=1A, (APW7410-18) (Note 4)	1782	1800	1818	
		I_{OUT}=0A, PFM Mode (APW7410-18) (Note 4)		1800		
		I_{OUT}=1A, (APW7410-25) (Note 4)	2475	2500	2525	
		I_{OUT}=0A, PFM Mode (APW7410-25) (Note 4)		2500		
	FB Input Current	V_{FB}=0.6V, (APW7410)		0.01	0.05	uA
	Line Regulation (Note 5)	V_{IN}=2.6 to 6V, I_{OUT}=1A		0.02		%/V
	Load Regulation (Note 5)	I_{OUT}=0.5A to 1A		0.16		%/A

Note 4:These specifications apply over T_A=0°C~85°C

Note 5:Guarantee by engineering lot

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{IN}=2.5V ~ 6V, and T_A=-40°C ~ 85°C.

Symbol	Parameter	Test Conditions	Specification			Unit
			Min	Typ	Max	
Power OK						
POK	POK Threshold	POK in from Lower (POK Goes High)	91	95	98	$\%V_{REF}$
		POK Low Hysteresis (POK Goes Low)	3	5	8	$\%V_{REF}$
		POK out from Normal (POK Goes Low)	105	110	115	$\%V_{REF}$
		POK High Hysteresis (POK Goes High)	3	5	8	$\%V_{REF}$
	Power OK pull low resistance	When POK pin pull low, POK sink 1mA	220	300	480	Ω
	POK Leakage Current	V_{POK} =5V		0.01	0.1	uA
	Power Good Low to High Debounce	POK Low to High		20		us
Protection						
I_{LIM}	Low-side FET switch current limit		1.1	1.5	1.9	A
	High-side FET switch current limit		2	2.5	3	A
V_{UVP}	Under Voltage Protection		55	65	75	$\%V_{REF}$
V_{OVP}	Over Voltage Protection		105	110	115	$\%V_{REF}$
T_{OTP}	Thermal Shutdown Threshold (Note 5)	T_J Rising		150		°C
	Thermal Shutdown Hysteresis (Note 5)	T_J Falling		20		°C

Note 5: Guarantee by engineering lot

Typical Operating Characteristics

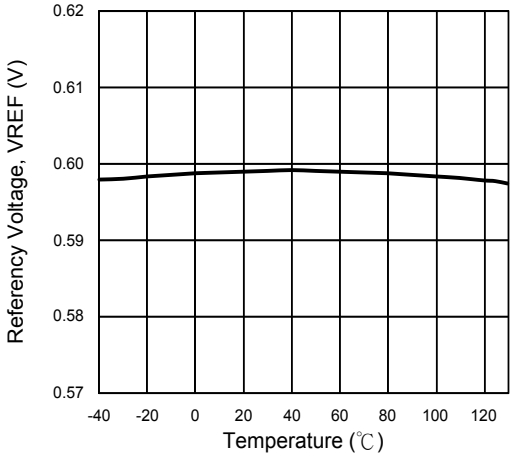


Figure 1. Reference Voltage vs. Temperature

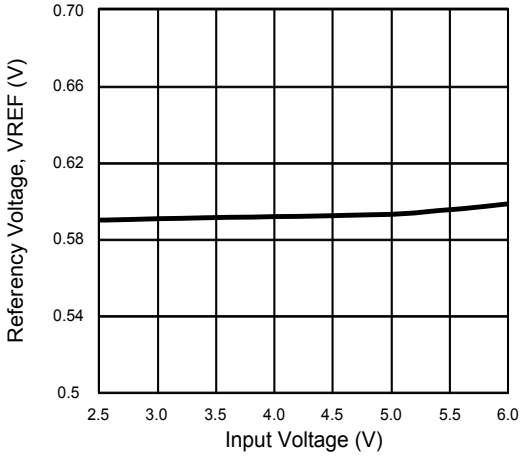


Figure 2. Reference Voltage vs. Input Voltage

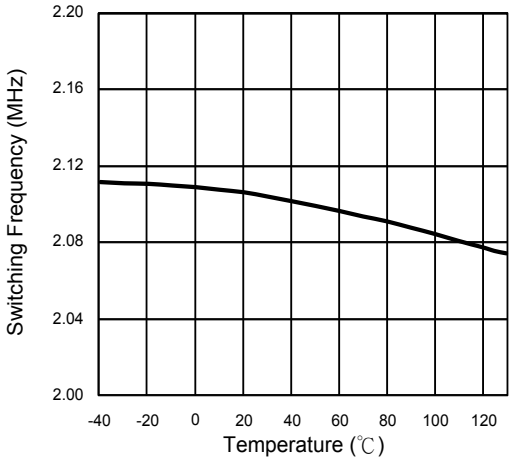


Figure 3. Switching Frequency vs. Temperature

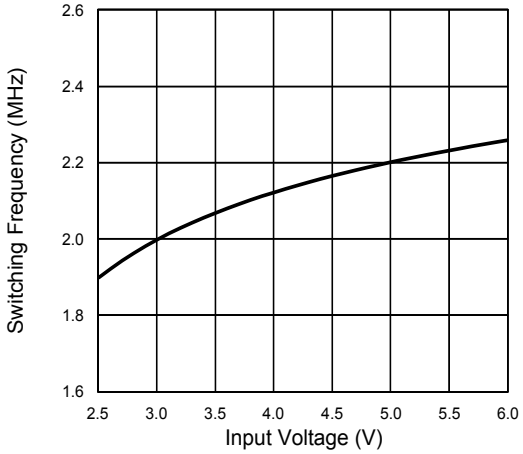


Figure 4. Switching Frequency vs. Input Voltage

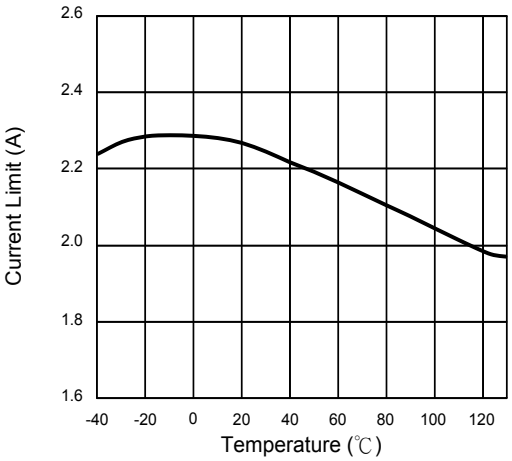


Figure 5. Current Limit vs. Temperature

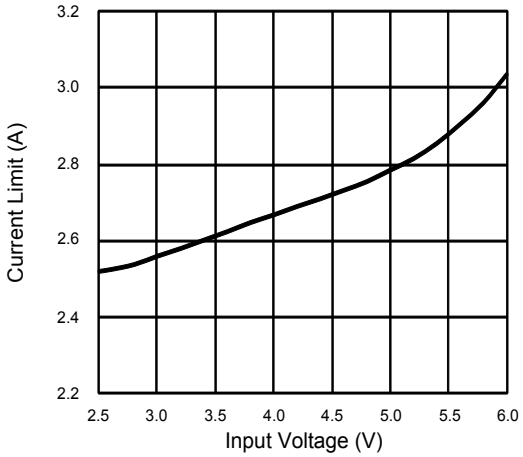


Figure 6. Current Limit vs. Input Voltage

Typical Operating Characteristics (Cont.)

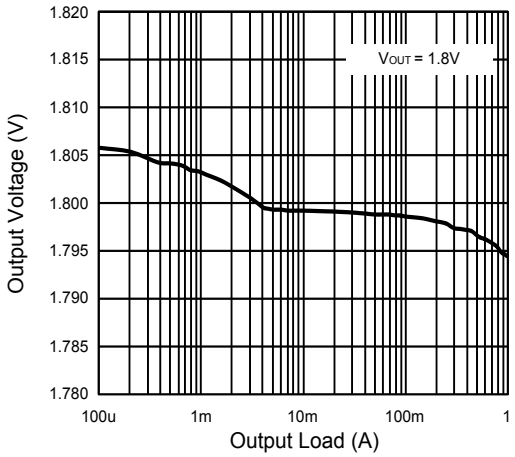


Figure 7. Load Regulation of V_{OUT}=1.8V

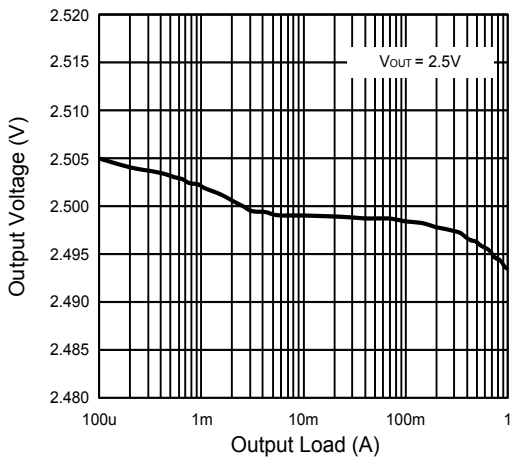


Figure 8. Load Regulation of V_{OUT}=2.5V

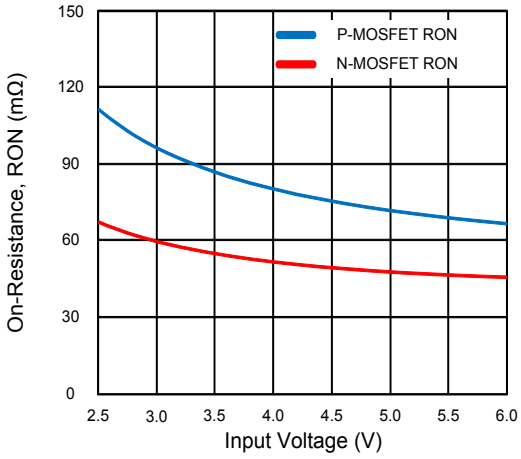


Figure 9. On-Resistance vs. Input Voltage

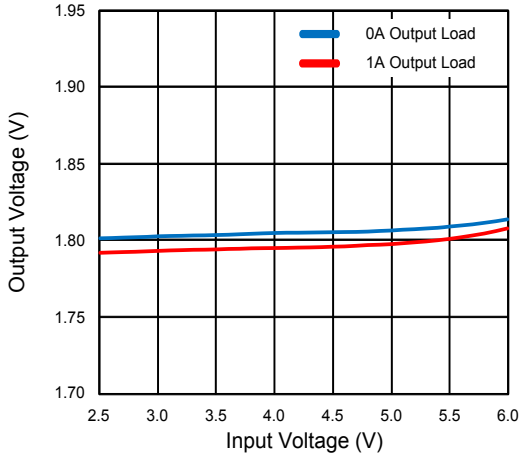


Figure 10. Line Regulation

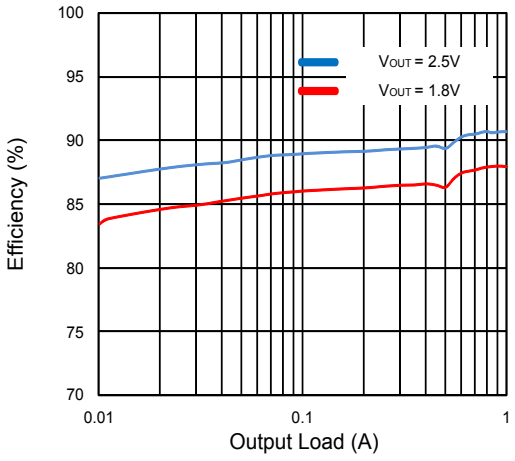
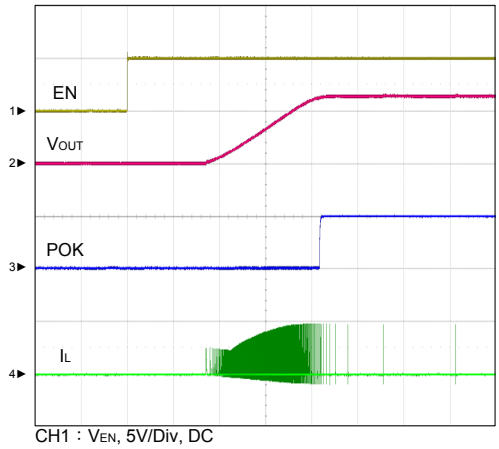


Figure 11. Efficiency

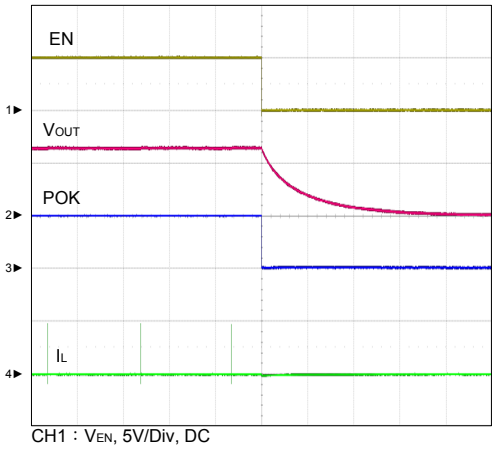
Operating Waveforms

Refer to the typical application circuit. The test condition is V_{IN}=5V, V_{OUT} =2.5V, T_A = 25°C unless otherwise specified



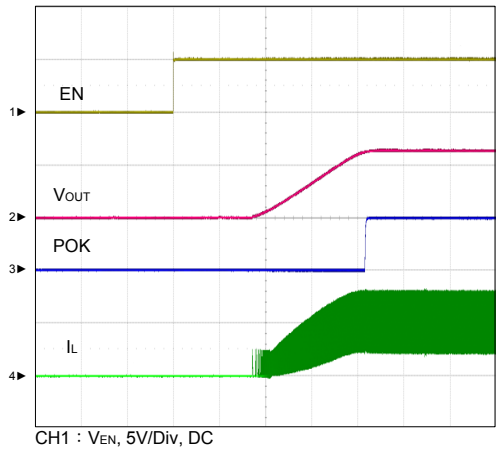
CH1 : VEN, 5V/Div, DC
CH2 : VOUT, 2V/Div, DC
CH3 : VPOK, 5V/Div, DC
CH4 : IL, 1A/Div, DC
TIME : 200us/Div

Figure 12. Enable without Loading



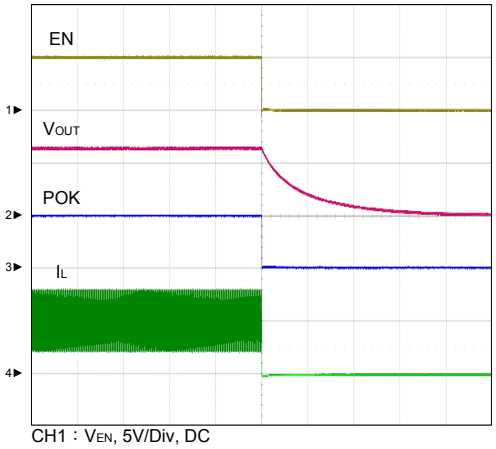
CH1 : VEN, 5V/Div, DC
CH2 : VOUT, 2V/Div, DC
CH3 : VPOK, 5V/Div, DC
CH4 : IL, 1A/Div, DC
TIME : 2ms/Div

Figure 13. Shutdown without Loading



CH1 : VEN, 5V/Div, DC
CH2 : VOUT, 2V/Div, DC
CH3 : VPOK, 5V/Div, DC
CH4 : IL, 1A/Div, DC
TIME : 200us/Div

Figure 14. Enable with 1A Loading

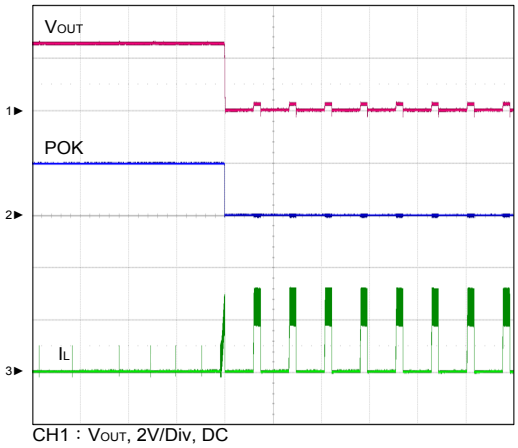


CH1 : VEN, 5V/Div, DC
CH2 : VOUT, 2V/Div, DC
CH3 : VPOK, 5V/Div, DC
CH4 : IL, 1A/Div, DC
TIME : 50us/Div

Figure 15. Shutdown with 1A Loading

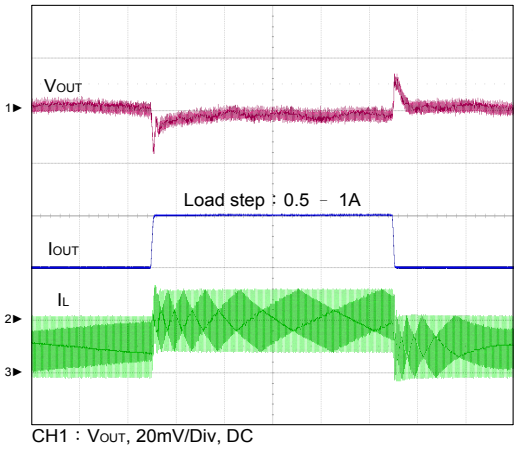
Operating Waveforms (Cont.)

Refer to the typical application circuit. The test condition is V_{IN}=5V, V_{OUT} =2.5V, T_A = 25°C unless otherwise specified



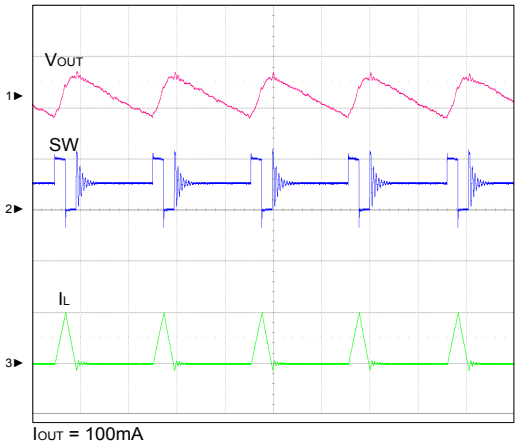
CH1 : VOUT, 2V/Div, DC
CH2 : POK, 5V/Div, DC
CH3 : IL, 2A/Div, DC
TIME : 5ms/Div

Figure 16. Hiccup Short Circuit Protection



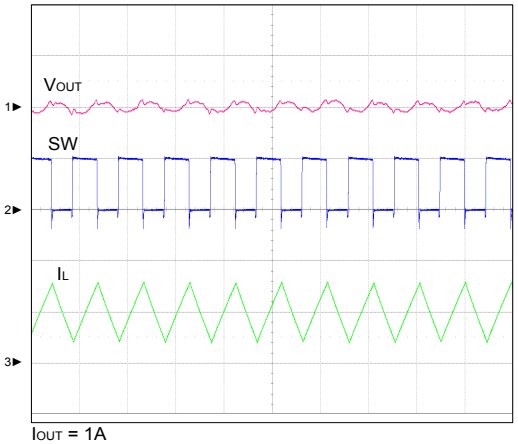
CH1 : VOUT, 20mV/Div, DC
CH2 : IOUT, 500mA/Div, DC
CH3 : IL, 1A/Div, DC
TIME : 20us/Div

Figure 17. Load Transient



IOUT = 100mA
CH1 : VOUT, 20mV/Div, DC, Offset=2.5V
CH2 : SW, 5V/Div, DC
CH3 : IL, 1A/Div, DC
TIME : 1us/Div

Figure 18. Normal Operation in Light Load



IOUT = 1A
CH1 : VOUT, 20mV/Div, DC, Offset=2.5V
CH2 : SW, 5V/Div, DC
CH3 : IL, 1A/Div, DC
TIME : 500ns/Div

Figure 19. Normal Operation in Heavy Load

Pin Descriptions

PIN		FUNCTION
NO.	NAME	
1	EN	Enable Input. When this pin is pulled high, it turns the IC on. When pulled low, it turns the IC off and turn on the discharge resistor.
2	POK	Power OK Output. When output voltage is higher than 95% of target V_{OUT}, POK is pulled high. If the POK pin is use, needs an external pull up resistor such as a 100kΩ from this pin to voltage source.
3	FB	Output Feedback pin. This pin is the negative input of the error amplifier used to compare the output voltage with eliminate either an internal fixed 0.6V reference. Connecting FB with a resistor-divider from the converter's output sets the output voltage. In fixed output voltage versions, this pin is simply connected to the output capacitors.
4	GND	Power and signal ground. Connect this pin directly to the GND plane.
5	SW	Power switching output. It is the junction of the high-side and low-side power MOSFET to supply power to the output LC filter.
6	VIN	Input Power. In order to get better thermal dissipation, all layers, top to bottom, below to VIN PAD define as VIN plane and connected by via holes. It is also to recommend to have larger area than VIN PAD as shown in the layout example. A high frequency 10uF ceramic, X5R type or better must be placed as close to these pins as possible connected to GND pin.

Typical Application Circuit

For APW7410

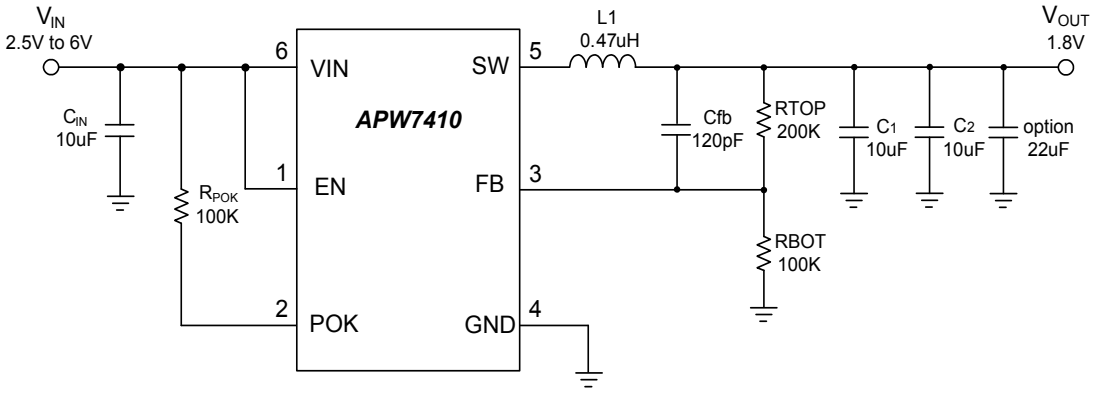


Figure 20. Typical Application Circuit of APW7410

For APW7410-18/APW7410-25

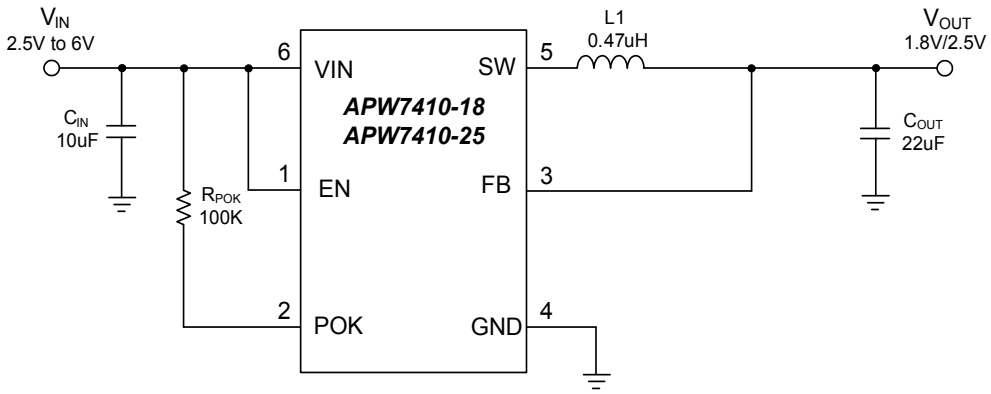


Figure 21. Typical Application Circuit of APW7410-18 and APW7410-25

Block Diagram

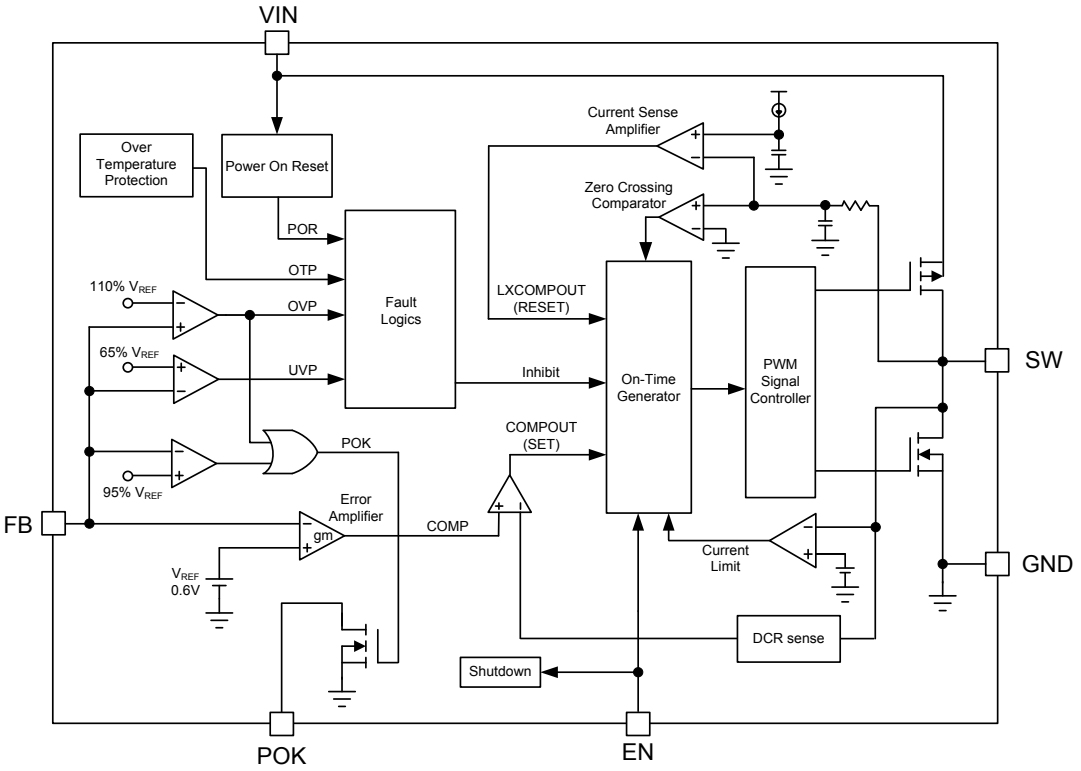


Figure 22. Function Block Diagram

Function Description

The APW7410 integrates a synchronous buck PWM controller and high/low side power MOSFETs to generate V_{OUT}. It offers the lowest total solution cost that can provide up to 1A continuous output current over wide input supply range. Input voltage range of the PWM converter is 2.5V to 6V. User defined output voltage is possible and can be adjustable from 0.6V to 4V. The converter runs an adaptive on-time PWM operation at high-load condition and automatically reduces frequency to keep excellent efficiency down to several milliamps.

Constant-On-Time PWM Controller with Input

Feed-Forward

The constant on-time control architecture is a pseudo-fixed frequency with input voltage feed-forward. This architecture relies on the output filter capacitor effective series resistance (ESR) to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal. The COT control mode can support output MLCC capacitor application currently through internal circuit designed. In PFM operation, the high-side switch on-time controlled by the on-time generator is determined solely by a one-shot whose pulse width is inversely proportional to input voltage and directly proportional to output voltage. In PWM operation, the high-side switch on-time is determined by a switching frequency control circuit in the on-time generator block. The switching frequency control circuit senses the switching frequency of the high-side switch and keeps regulating it at a constant frequency in PWM mode. The design improves the frequency variation and be more outstanding than a conventional constant on-time controller which has large switching frequency variation over input voltage, output current and temperature. Both in PFM and PWM, the on-time generator, which senses input voltage on VIN pin, provides very fast on-time response to input line transients.

Power-On-Reset

A Power-On-Reset (POR) function is designed to prevent wrong logic controls when the VIN voltage is low. The POR function continually monitors the input supply voltage on the VIN pin if at least one of the enable pins is set high. When the rising VIN voltage reaches the rising POR voltage threshold (2.3V typical), the POR signal goes high and the chip initiates soft-start operations. There is a hysteresis to POR voltage threshold (about 100mV typical). When VIN voltage drop lower than 2.2V, the POR disables the chip.

Soft- Start

The APW7410 has soft-start circuits to ramp up the output voltage of the converter to the programmed regulation set point at a predictable slew rate.
The figure 23. shows V_{OUT} soft-start sequence. When the EN pin is pulled above the rising EN threshold voltage, the device initiates a soft-start process to ramp up the output voltage.

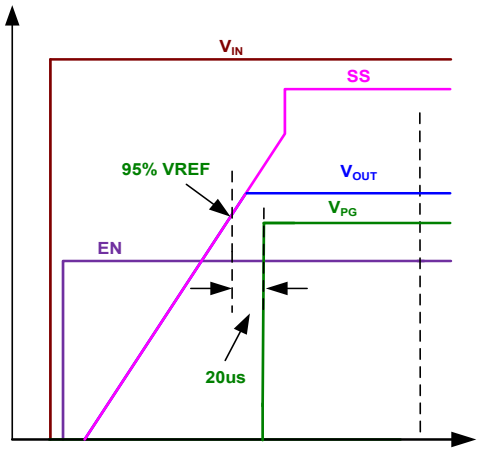


Figure 23. Soft-Start Sequence

Before the POK signal goes high, the under voltage protection is prohibited. The over voltage and current limit protection functions are enabled. If the output capacitor has residue voltage before startup, both internal low-side and high-side MOSFETs are in off-state until the internal soft start voltage equal the V_{FB} voltage. This will ensure the output voltage starts from its existing voltage level. The POK signal indicates the status of output voltage V_{OUT}.

Power-Good Output (POK)

POK is an open-drain output and the POK comparator continuously monitors the output voltage. POK is actively held low in shutdown, and standby. When PWM converter's output voltage is greater than 95% of its target value, the internal open-drain device will be pulled low. After 20us de-bounce time, the POK goes high. The When the output voltage V_{OUT} falls down 90% of the target voltage, the POK signal will be pulled low immediately.

Under Voltage Protection

In the process of operation, if a short-circuit occurs, the output voltage will drop quickly. When load current is bigger than current limit threshold value, the output voltage will fall out of the required regulation range. The under-voltage continually monitors the setting output voltage after internal soft start signal is okay. If a load step is strong enough to pull the output voltage lower than the under voltage threshold (65% of normal output voltage), the APW7410 enters hiccup mode to periodically restart the part (wait for 3ms typical). This protection mode is especially useful when the output is dead-shorted to ground. The average short circuit current is greatly reduced to alleviate thermal issues and to protect the regulator. The APW7410 exits the hiccup mode once the output voltage V_{OUT} bigger than UVP Hysteresis (typical: 10%).

Function Description (Cont.)

Over Voltage Protection (OVP)

The over-voltage function monitors the output voltage by FB pin. Once the voltage V_{FB} exceeds 110% of the reference voltage, the over-voltage protection comparator forces the high-side and low-side MOSFETs off and pull the POK pin to 0V. Once the V_{FB} drop below the OVP falling threshold, the POK pull low switch will turn off.

PWM Converter Current Limit

The current-limit circuit employs a “peak” current-sensing algorithm (See Figure 24). The APW7410 uses the internal High-side MOSFET’s $R_{DS(ON)}$ of the synchronous rectifier as a current-sensing element. If the magnitude of the current-sense signal at SW pin is above the current limit threshold, the PWM is not allowed to initiate a new cycle. The actual peak current is greater than the current limit threshold by an amount equals to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are the functions of the sense resistance, inductor value, and input voltage.

The PWM controller uses the internal High-side MOSFETs on-resistance $R_{DS(ON)}$ to monitor the current for protection against shortened outputs. The cycle by cycle current limit threshold is 2.5A for APW7410.

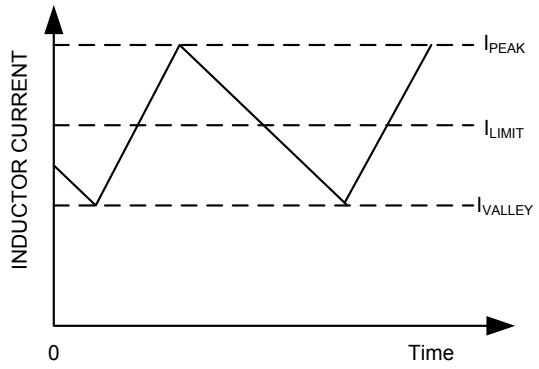


Figure 24. Current Limit Algorithm

Thermal Shutdown

A thermal shutdown circuit limits the junction temperature of APW7410. When the junction temperature exceeds +150°C, PWM converter is shut off, allowing the device to cool down. The regulator regulates the output again through initiation of a new soft-start cycle after the junction temperature cools by 20°C, resulting in a pulsed output during continuous thermal overload conditions. The thermal shutdown designed with a 20°C hysteresis lowers the average junction temperature during continuous thermal overload conditions, extending life time of the device.
For normal operation, device power dissipation should be externally limited so that junction temperatures will not exceed +125°C.

Application Information

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, selecting the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage. The maximum RMS current rating requirement is approximately $I_{OUT}/2$, where I_{OUT} is the load current. During power-up, the input capacitors have to handle great amount of surge current. For low-duty notebook applications, ceramic capacitor is recommended. The capacitors must be connected between the drain of high-side MOSFET and the source of low-side MOSFET with very low-impedance PCB layout.

Inductor Selection

The duty cycle (D) of a buck converter is the function of the input voltage and output voltage. Once an output voltage is fixed, it can be written as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

The inductor value (L) determines the inductor ripple current, I_{RIPPLE}, and affects the load transient response. Higher inductor value reduces the inductor's ripple current and induces lower output ripple voltage. The ripple current and ripple voltage can be approximated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{F_{SW} \times L} \times \frac{V_{out}}{V_{IN}}$$

Where F_{SW} is the switching frequency of the regulator. Although the inductor value and frequency are increased and the ripple current and voltage are reduced, a tradeoff exists between the inductor's ripple current and the regulator load transient response time. A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current. Increasing the switching frequency (F_{SW}) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFETs and the power dissipation of the converter. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current. Once the inductance value has been chosen, selecting an inductor that is capable of carrying the required peak current without going into saturation.In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This results in a larger output ripple voltage. Besides, the inductor needs to have low DCR to reduce the loss of efficiency.

Output Voltage Setting

In the adjustable version, the output voltage is set by a resistive divider. The external resistive divider is connected to the output, allowing remote voltage sensing as shown in "Typical Application Circuits". A suggestion of maximum value of RBOT is 100k to keep the minimum current that provides enough noise rejection ability through the resistor divider. The output voltage can be calculated as below:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{RTOP}{RBOT}\right) = 0.6 \times \left(1 + \frac{RTOP}{RBOT}\right)$$

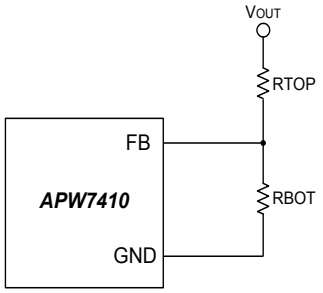


Figure 25. Output Voltage Setting

Output Capacitor Selection

Output voltage ripple and the transient voltage deviation are factors that have to be taken into consideration when selecting an output capacitor. Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, selecting high performance low ESR capacitors is intended for switching regulator applications. In addition to high frequency noise related MOSFET turn-on and turn-off, the output voltage ripple includes the capacitance voltage drop and ESR voltage drop caused by the AC peak-to-peak current. These two voltages can be represented by:

$$\Delta V_{COUT} = \frac{I_{RIPPLE}}{8 \times C_{OUT} \times F_{SW}}$$

$$\Delta V_{ESR} = I_{RIPPLE} \times R_{ESR}$$

These two components constitute a large portion of the total output voltage ripple. In some applications, multiple capacitors have to be paralleled to achieve the desired ESR value. If the output of the converter has to support another load with high pulsating current, more capacitors are needed in order to reduce the equivalent ESR and suppress the voltage ripple to a tolerable level. A small decoupling capacitor in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors must also be considered. To support a load transient that is faster than the switching frequency, more capacitors have to be used to reduce the voltage excursion during load step change. Another aspect of the capacitor selection is that the total AC current going through the capacitors has to be less than the rated RMS current specified on the capacitors to prevent the capacitor from over-heating.

Application Information (Cont.)

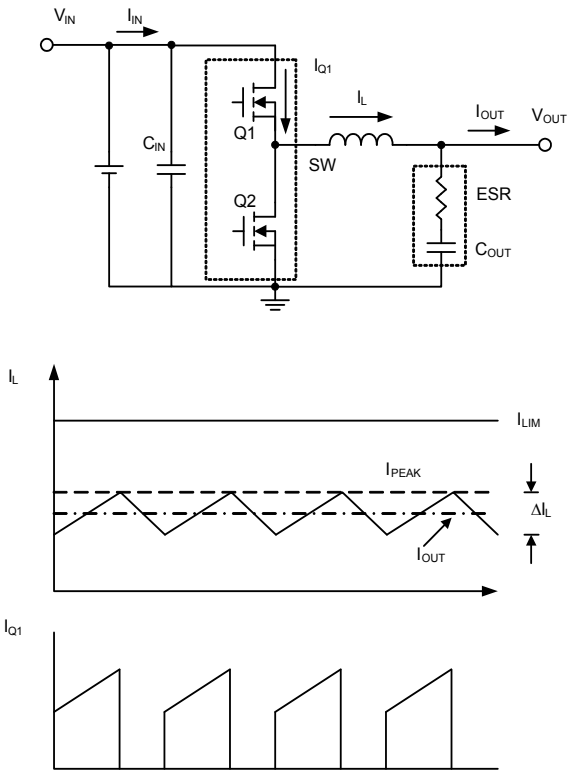


Figure 26. Buck Converter Application Information

Layout Consideration

For all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter

1. The input capacitor should be placed close to the VIN and GND. Connecting the capacitor and VIN/GND with short and wide trace without any via holes for good input voltage filtering. The distance between VIN/GND to capacitor less than 2mm respectively is recommended.
2. To minimize copper trace connections that can inject noise into the system, the inductor should be placed as close as possible to the SW pin to minimize the noise coupling into other circuits.
3. The output capacitor should be place closed to converter V_{OUT} and GND.
4. Since the feedback pin and network is a high impedance circuit the feedback network should be routed away from the inductor. The feedback pin and feedback network should be shielded with a ground plane or trace to minimize noise coupling into this circuit.
5. A star ground connection or ground plane minimizes ground shifts and noise is recommended.

Layout Example

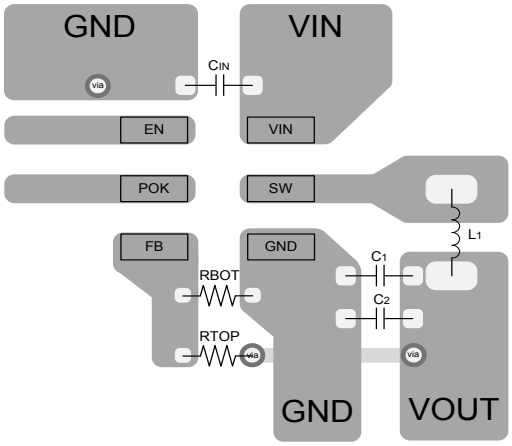
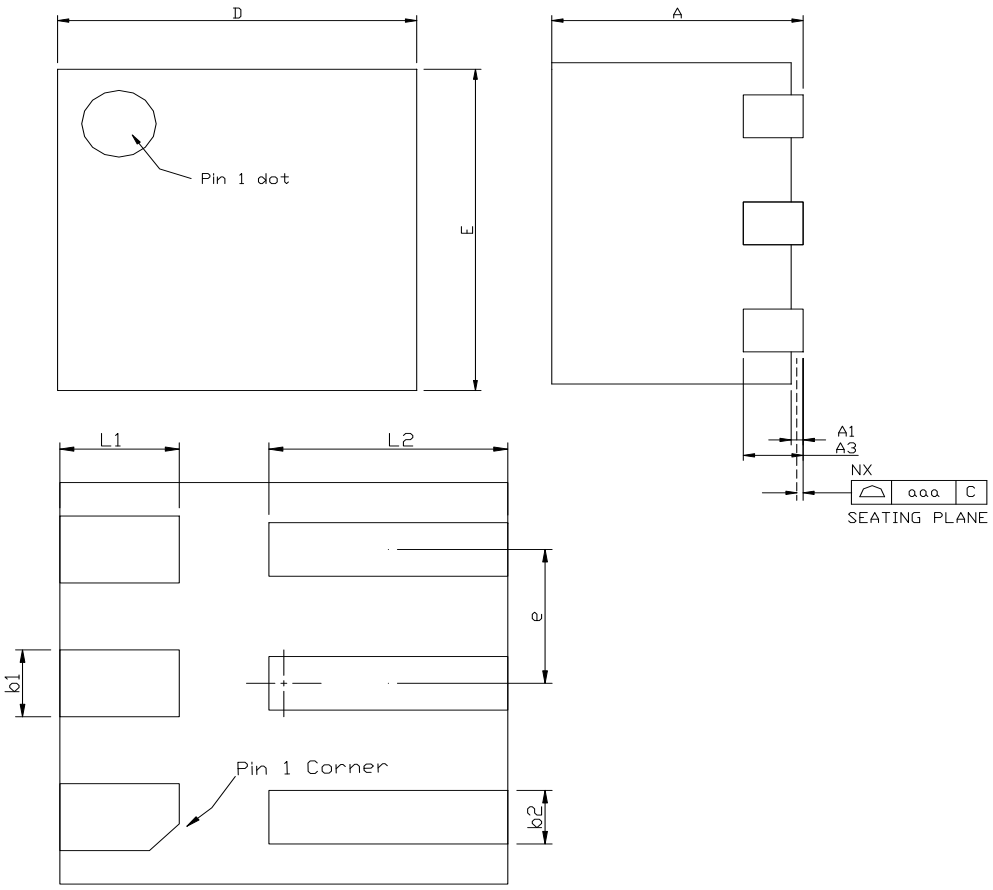


Figure 27. PCB Layout Recommendation

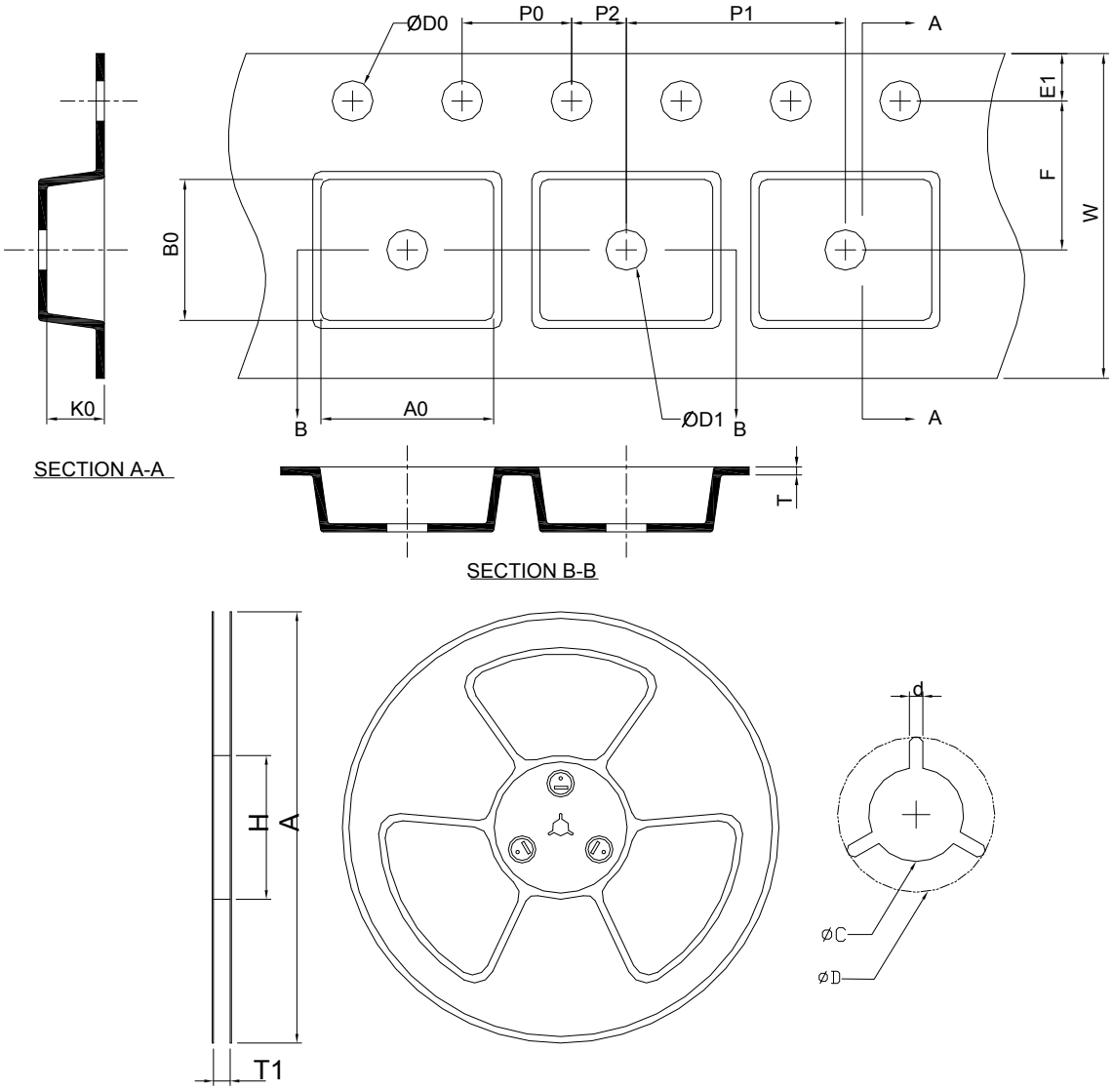
Package Information

DFN 1.5x1.5-6



SYMBOL	DFN 1.5*1.5-6			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b1	0.20	0.30	0.008	0.012
b2	0.15	0.25	0.006	0.010
D	1.45	1.55	0.057	0.061
E	1.45	1.55	0.057	0.061
e	0.50 BSC		0.020 BSC	
L1	0.30	0.50	0.012	0.020
L2	0.70	0.80	0.028	0.031
aaa	0.08		0.003	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
DFN1.5x1.5	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	0.5 MIN.	0.6+0.00 -0.40	1.70±0.10	1.70±0.10	1.10±0.10

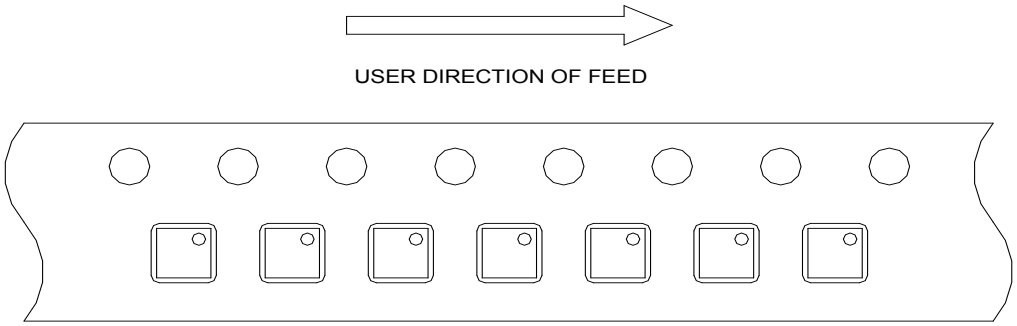
(mm)

Devices Per Unit

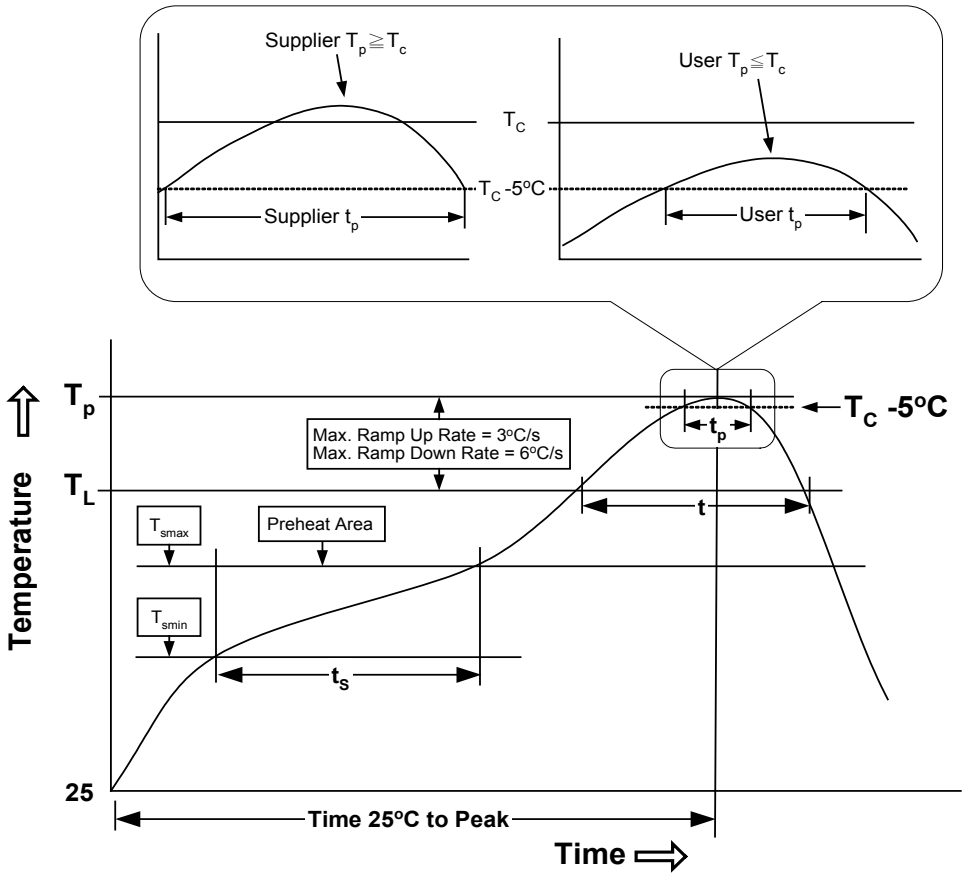
Package type	Packing	Quantity
DFN(1.5x1.5)	Tape & Reel	3000

Taping Direction Information

DFN 1.5x1.5-6



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Customer Service

Anpec Electronics Corp.
Head Office :
No.6, Dusing 1st Road, SBIP,
Hsin-Chu, Taiwan, R.O.C.
Tel : 886-3-5642000
Fax : 886-3-5642050

Taipei Branch :
2F, No. 11, Lane 218, Sec 2 Jhongsing Rd.,
Sindian City, Taipei County 23146, Taiwan
Tel : 886-2-2910-3838
Fax : 886-2-2917-3838