24V 3A 500kHz Synchronous Buck Converter

Features

- **Wide Input Voltage from 7V to 24V**
- **3A Continuous Output Current**
- **Adjustable Output Voltage from 0.791V to 13V**
- **Integrated Low $R_{DS(ON)}$ MOSFETs**
- **Fixed 500kHz Switching Frequency**
- **Stable with Low ESR Ceramic Output Capacitors**
- **Power-On-Reset Detection**
- **Over-Temperature Protection**
- **Current-Limit Protection with HICCUP Mode**
- **Small TSOT-23-8A Package**
- **Lead Free and Green Devices Available (RoHS Compliant)**

General Description

APW7415S is a 3A synchronous buck converter with integrated low $R_{DS(ON)}$ power MOSFETs. The APW7415S design with a current-mode control scheme, can convert wide input voltage of 7V to 24V to the output voltage adjustable from 0.791V to 13V to provide excellent output voltage regulation.

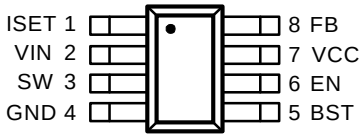
The APW7415S is equipped advance asynchronous modulation mode operation. Increase efficiency at light load.

The APW7415S is also equipped with Power-on-reset, soft start, and whole protections (under-voltage, over-temperature, and current-limit) into a single package. This device, available TSOT-23-8A, provides a very compact system solution external components and PCB area.

Applications

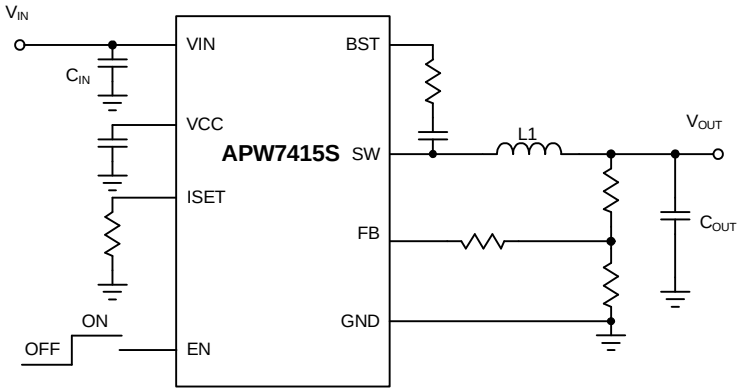
- **Notebook Systems and I/O Power**
- **Digital Set-Top Boxes**
- **Flat-Panel Television and Monitors**
- **Distributed Power Systems**

Pin Configuration

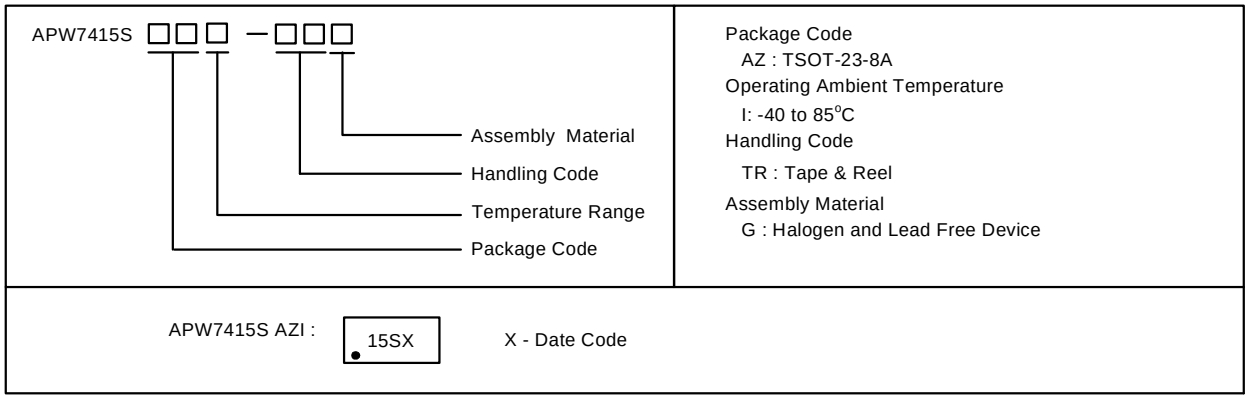


APW7415S
TSOT-23-8A

Simplified Application Circuit



Ordering and Marking Information



Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN}, V_{EN}	VIN Supply to GND Voltage and EN to GND Voltage	-0.3 ~ 27	V
V_{SW}	SW to GND Voltage	-0.3 ~ 27	V
V_{BST-SW}	BST to SW Voltage	-0.3 ~ 6	V
	ISET, VCC and FB to GND Voltage	-0.3 ~ 6	V
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature(10 Seconds)	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air (Note 2)	100	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN}	VIN Supply Voltage	7 ~ 24	V
V_{EN}	EN Input Voltage	0 ~ 24	V
V_{OUT}	Converter Output Voltage	0.791~13	V
I_{OUT}	Converter Output Current	0 ~ 3	A

Recommended Operating Conditions (Cont.) (Note 3)

Symbol	Parameter	Range	Unit
C_{OUT}	Converter Output Capacitance	22 ~ 47	µF
L1	Inductance	1.5 ~ 10	µH
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3 : Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=12V, V_{EN}=3V and T_A= -40 to 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7415S			Unit
			Min	Typ	Max	
SUPPLY CURRENT						
I_{VIN}	VIN Supply Current	V_{FB}=0.9V, SW=NC	-	1	1.2	mA
I_{VIN_SD}	VIN Shutdown Supply Current	V_{EN}=0V	-	-	10	µA
POWER-ON-RESET (POR)						
	VIN POR Voltage Threshold	V_{IN} Rising	6.3	6.5	6.8	V
	VIN POR Hysteresis		-	0.4	-	V
REFERENCE VOLTAGE						
V_{REF}	Reference Voltage		-	0.791	-	V
	Output Voltage Accuracy	T_J=25°C, I_{OUT}=10mA	-1	-	+1	%
I_{FB}	FB input current		-	10	50	nA
V_{VCC}	VCC Regulator		-	4.9	-	V
	VCC Load Regulation	I_{VCC}=3mA	-	3	-	%
OSCILLATOR AND DUTY CYCLE						
F_{SW}	Switching Frequency		430	500	570	kHz
D_{AMX}	Maximum Duty Cycle		-	93	-	%
	Minimum on-time		-	-	100	ns
POWER MOSFET						
	High Side MOSFET Resistance		-	100	-	mΩ
	Low Side MOSFET Resistance		-	40	-	mΩ
	High Side Switch Leakage Current	V_{EN}=0V, V_{IN}=24V, V_{SW}=0V	-	-	1	µA
	Low Side Switch Leakage Current	V_{EN}=0V, V_{IN}=24V, V_{SW}=24V	-	-	1	µA
PROTECTIONS						
I_{LIM}	High Side MOSFET Current-Limit		4	5	6	A
	Under-Voltage Protection (UVP)		40	50	60	%V_{REF}
	FB Over Voltage Protection		120	125	130	%V_{REF}
	FB OVP Hysteresis		-	20	-	%V_{REF}
	Hiccup Delay time		-	1	-	T_{SS}
T_{OTR}	OTP Rising Threshold (Note 4)		-	150	-	°C
	OTP Hysteresis (Note 4)		-	30	-	°C

Electrical Characteristics (cont.)

Unless otherwise specified, these specifications apply over V_{IN}=12V, V_{EN}=3V and T_A= -40 to 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7415S			Unit
			Min	Typ	Max	
SOFT-START, ENABLE						
T_{SS}	Soft Start Time		-	1.5	-	ms
	EN Rising Threshold Voltage		1.2	1.4	1.6	V
	EN Falling Threshold Hysteresis		-	0.2	-	V
	EN turn off delay		-	8	-	us
	EN Input Current	V_{EN}=2V	-	2	-	uA
	Force CCM Threshold	V_{ISET}	4.5	-	-	V
	ISET Source Current		5.6	6.2	6.8	uA

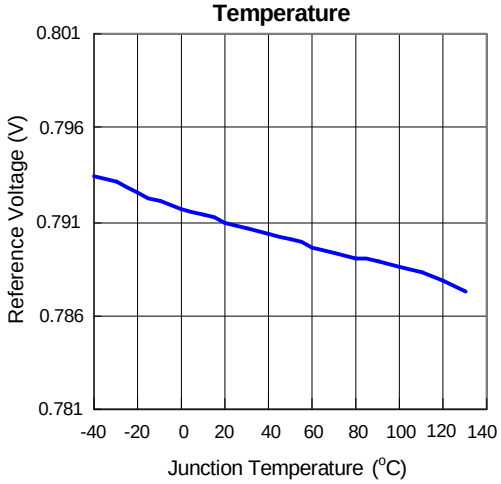
Note4: Guaranteed by design.

Pin Description

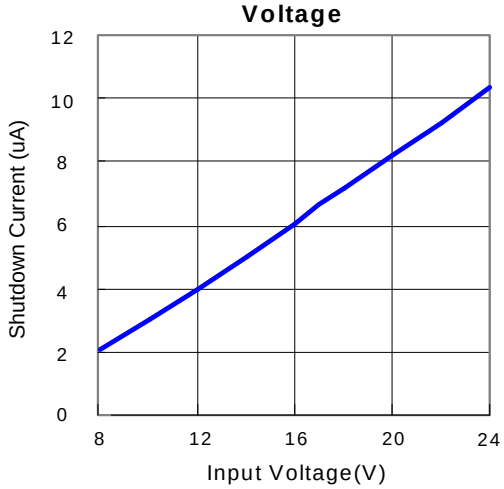
PIN		FUNCTION
NO.	NAME	
1	ISET	A resistor is connected from ISET pin to ground to set a ISET voltage force APW7415S into non-synchronous mode when load is small. Drive ISET pin floating or pull high to VCC will force APW7415S into CCM.
2	VIN	Power Input. VIN supplies the power to the control circuitry, gate driver. Connecting a ceramic bypass capacitor and a suitably large capacitor between VIN and GND eliminates switching noise and voltage ripple on the input to the IC.
3	SW	Power Switching Output. SW is the Source of the N-Channel power MOSFET to supply power to the output LC filter.
4	GND	Signal and power ground.
5	BST	High-Side Gate Drive Boost Input. BS supplies the voltage to drive the high-side N-channel MOSFET. At least 10nF capacitor should be connected from SW to BST to supply the high side switch.
6	EN	Enable Input. EN is a digital input that turns the regulator on or off. EN threshold is 1.4V with 0.2V hysteresis.
7	VCC	Bias Supply. Decouple with a 0.1uF capacitor or higher is recommended.
8	FB	Output feedback Input. The IC senses the feedback voltage via FB and regulates FB voltage at 0.791V. Connecting FB with a resistor-divider from the converter's output to set the output voltage.

Typical Operating Characteristics

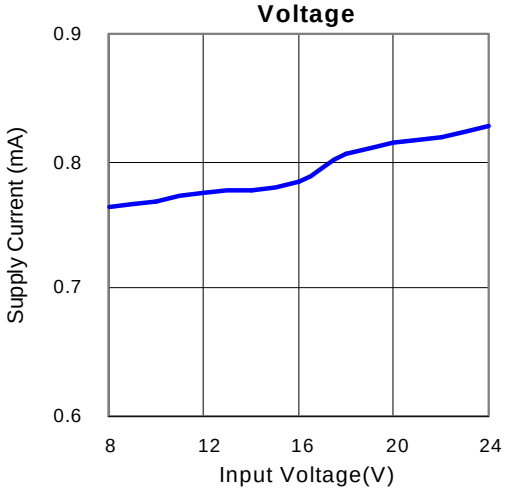
Reference Voltage vs. Junction Temperature



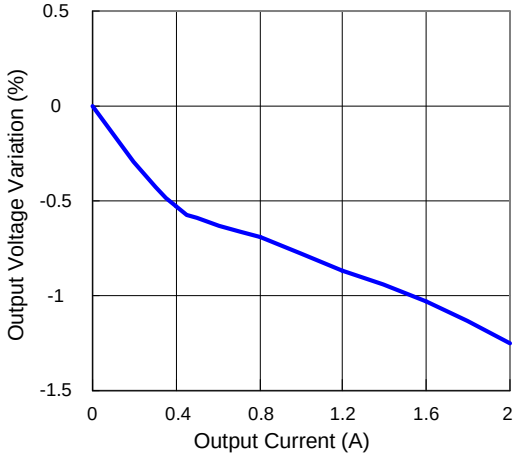
Shutdown Current vs. Input Voltage



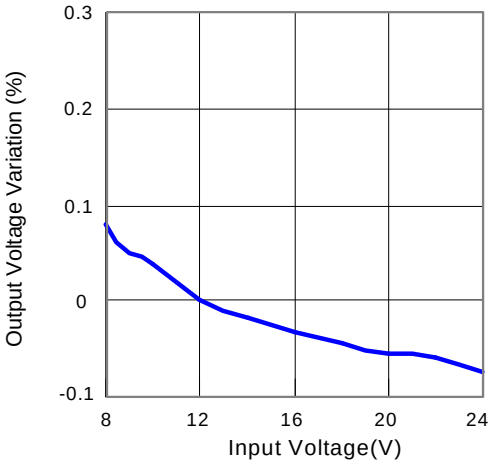
Supply Current vs. Input Voltage



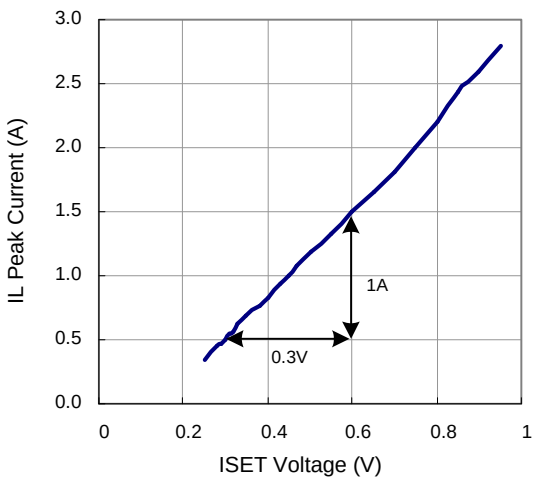
Load Regulation



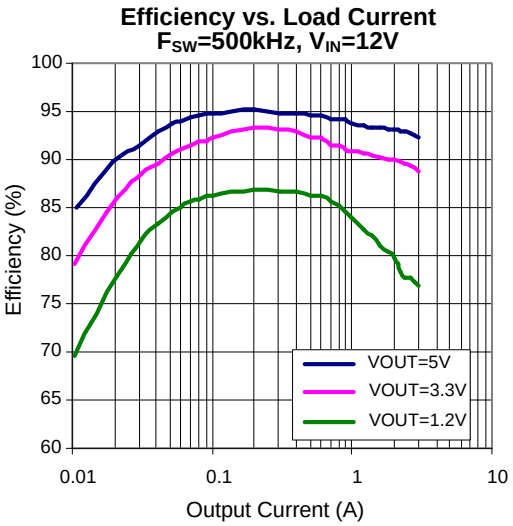
Line Regulation

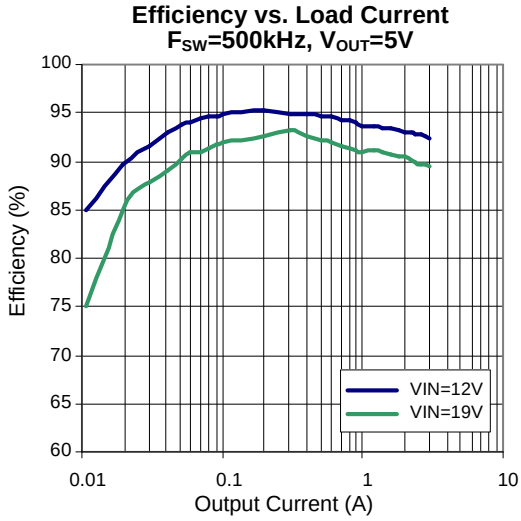


IL Peak Current vs. ISET Voltage



Typical Operating Characteristics

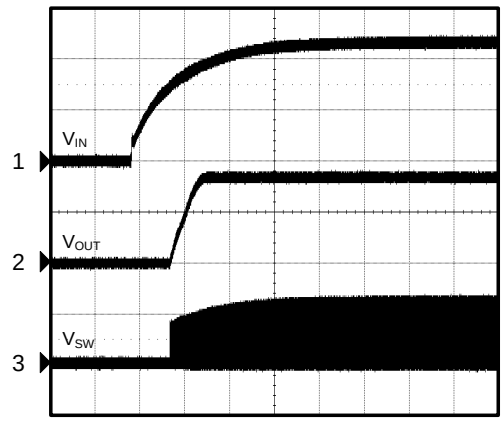




Operating Waveforms

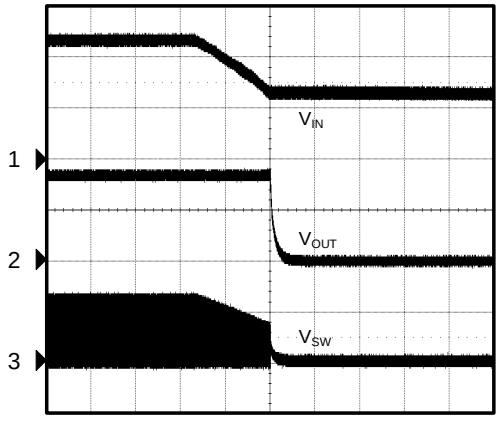
Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

Power On



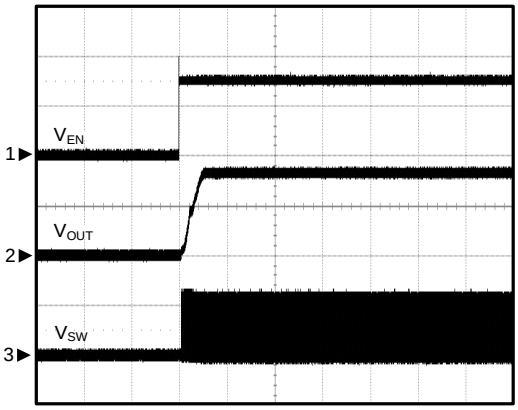
CH1: V_{IN}, 5V/Div
CH2: V_{OUT}, 2V/Div
CH3: V_{SW}, 10V/Div
Time: 2ms/Div

Power Off



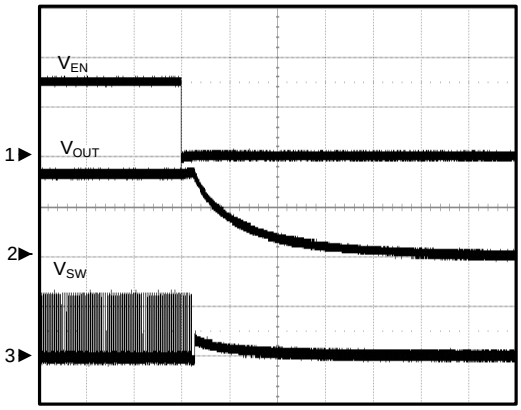
CH1: V_{IN}, 5V/Div
CH2: V_{OUT}, 2V/Div
CH3: V_{SW}, 10V/Div
Time: 2ms/Div

Enable



CH1: V_{EN}, 2V/Div
CH2: V_{OUT}, 2V/Div
CH3: V_{SW}, 10V/Div
TIME: 2ms/Div

Shutdown

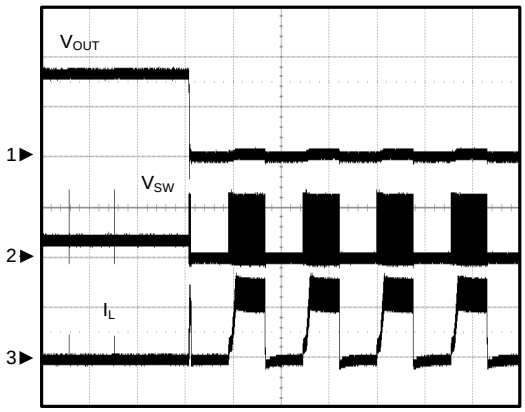


CH1: V_{EN}, 2V/Div
CH2: V_{OUT}, 2V/Div
CH3: V_{SW}, 10V/Div
TIME: 50us/Div

Operating Waveforms

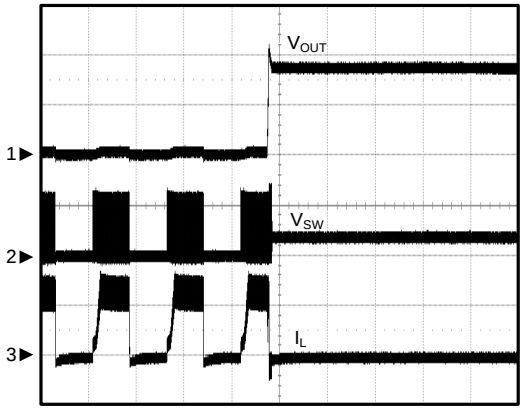
Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

Short-Current Entry



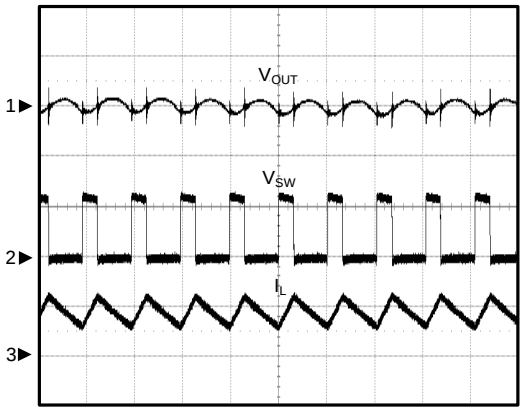
CH1: V_{OUT}, 2V/Div
CH2: V_{SW},10V/Div
CH3: I_L,2A/Div
TIME: 2ms/Div

Short-Current Recovery



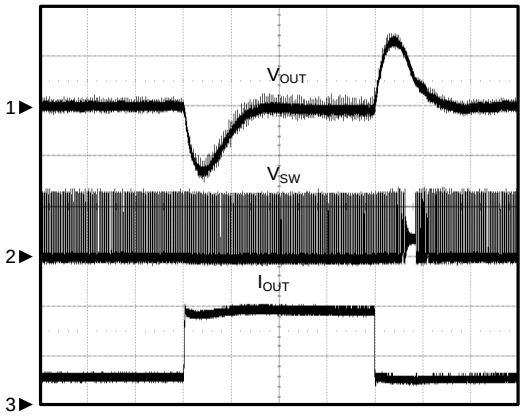
CH1: V_{OUT}, 2V/Div
CH2: V_{SW},10V/Div
CH3: I_L,2A/Div
TIME: 2ms/Div

Vout Ripple



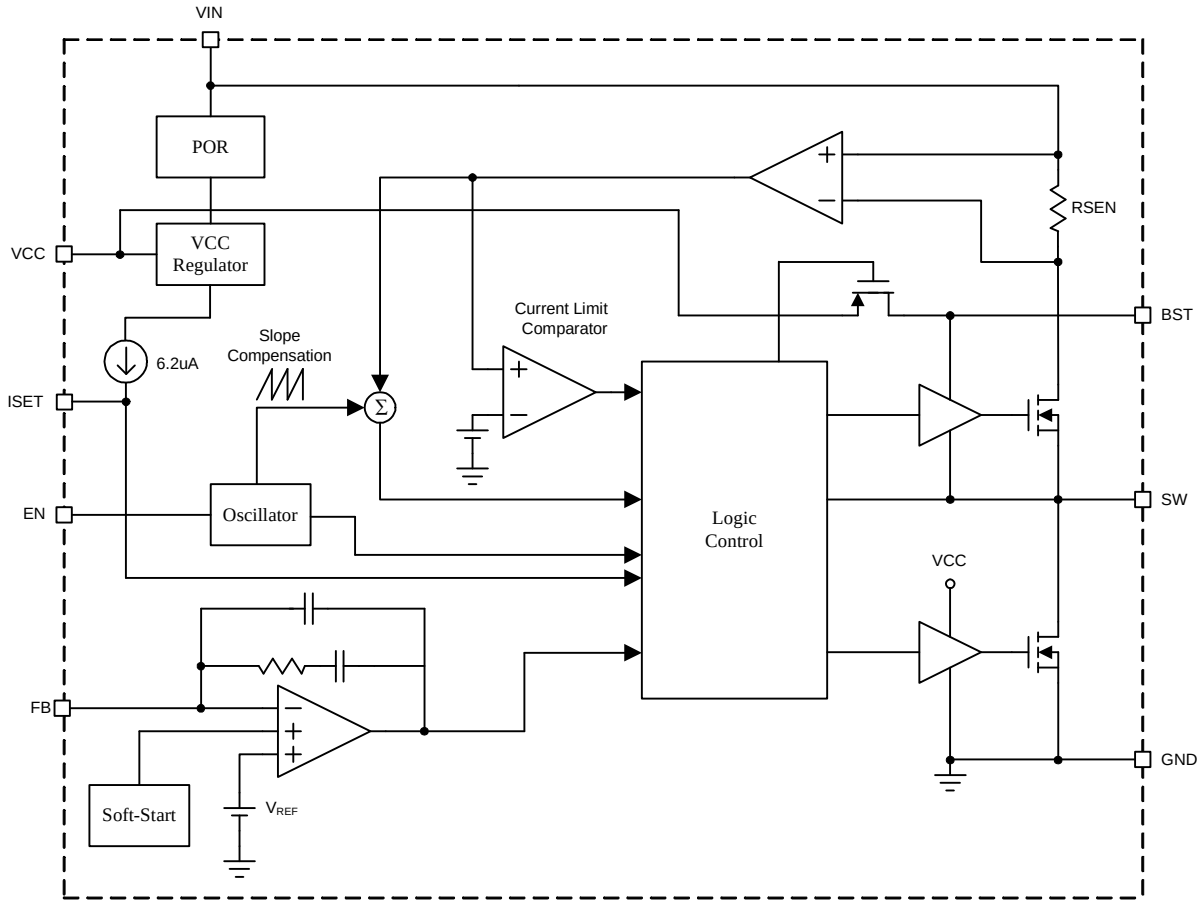
CH1: V_{OUT}, 50mV/Div,AC
CH2: V_{SWX},10V/Div
CH3: I_L,2A/Div
TIME: 2us/Div

Load Transient



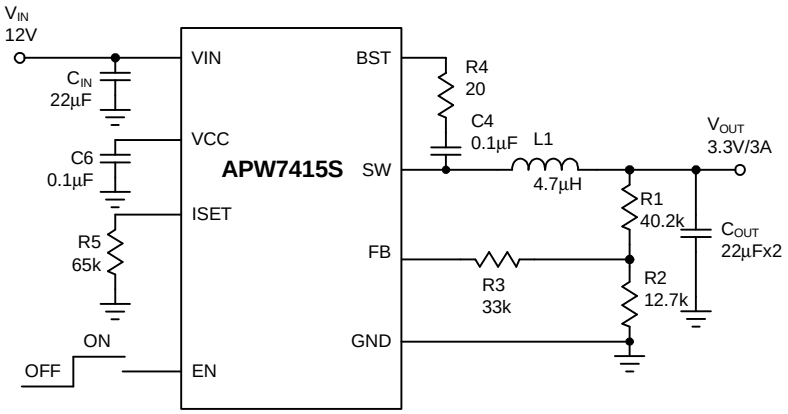
CH1: V_{OUT}, 100mV/DIV,AC
CH2: V_{SW} ,10V/Div
CH3: I_{OUT},1A/Div
TIME: 50us/Div

Block Diagram



Typical Application Circuit

Dual Power Input : VIN Pre-existing & VOUT setting less than VIN POR



Single Power Input : VIN divided to EN & VOUT setting more than VIN POR

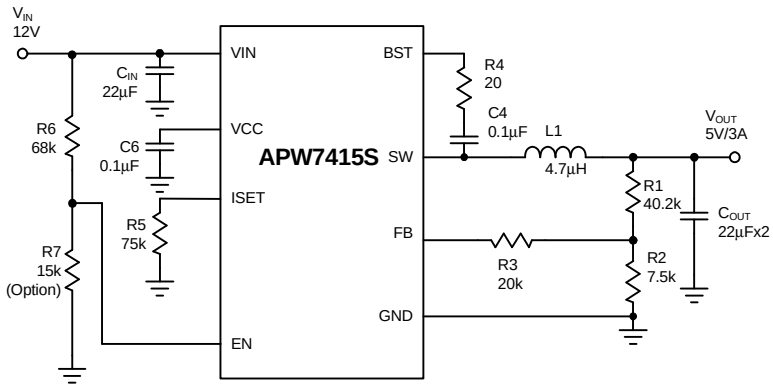


Table 1. Components Selection for Different Output Voltage

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	R3 (kΩ)	R4 (Ω)	R5 (kΩ)	L (uH)	C_{OUT} (uF)
1.05	20.5	62.6	100	20~60	47	1.5	44
1.2	20.5	39.6	75	20~60	47	1.8	44
3.3	40.2	12.7	33	20~60	65	4.7	44
5	40.2	7.5	20	20~60	75	4.7	44

Function Description

Main Control Loop

The APW7415S is a constant frequency, synchronous rectifier and current-mode switching regulator. In normal operation, the internal upper power MOSFET is turned on each cycle. The peak inductor current at which ICMP turn off the upper MOSFET is controlled by the voltage on the COMP node, which is the output of the error amplifier (EAMP). An external resistive divider connected between VOUT and ground allows the EAMP to receive an output feedback voltage V_{FB} at FB pin. When the load current increases, it causes a slightly decrease in V_{FB} relative to the 0.791V reference, which in turn causes the COMP voltage to increase until the average inductor current matches the new load current.

Enable/Shutdown

Driving EN to the ground places the APW7415S in shutdown mode. When in shutdown, the internal power MOSFETs turn off, all internal circuitry shuts down and the quiescent supply current reduces to 1μA typical.

Under Voltage Lockout (UVLO)

An under-voltage lockout function prevents the device from operating if the input voltage on VIN is lower than approximately 6.5V. The device automatically enters the shutdown mode if the voltage on VIN drops below approximately 6.3V. This under-voltage lockout function is implemented in order to prevent the malfunctioning of the converter.

Soft-Start

The APW7415S has a built-in soft-start to control the output voltage rise during start-up. During soft-start, an internal ramp voltage, connected to the one of the positive inputs of the error amplifier, raises up to replace the reference voltage (0.791V typical) until the ramp voltage reaches the reference voltage. Then, the voltage on FB regulated at reference voltage.

Over-Current-Protection and Hiccup

The APW7415S has a cycle-by-cycle over-current limit when the inductor current peak value exceeds the set current limit threshold. Meanwhile, the output voltage drops until FB is below the Under-Voltage (UV) threshold below the reference. Once UV is triggered, the APW7415S enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-shorted to ground. The average short circuit current is greatly reduced to alleviate thermal issues and to protect the regulator. The APW7415S exits the hiccup mode once the over-current condition is removed.

Over-Temperature Protection (OTP)

The over-temperature circuit limits the junction temperature of the APW7415S. When the junction temperature exceeds 150°C, a thermal sensor turns off the both power MOSFETs, allowing the devices to cool. The thermal sensor allows the converters to start a soft-start process and regulate the output voltage again after the junction temperature cools by 30°C. The OTP is designed with a 30°C hysteresis to lower the average Junction Temperature (T_J) during continuous thermal overload conditions, increasing the lifetime of the device.

Over-Voltage Protection (OVP)

The over-voltage function monitors the output voltage by FB pin. Once the FB voltage exceeds 125% of the reference voltage, the over-voltage protection comparator forces the low-side MOSFET on. This action actively pulls down the output voltage to prevent the end device be damage. As soon as the output voltage is below 105% of the reference voltage, the low-side MOSFET off and the OVP comparator is disengaged. The chip restores its normal operation.

Function Description

Frequency Foldback

The foldback frequency is controlled by the FB voltage. When the output is short to the ground, the frequency of the oscillator will be reduced to 0.25 x F_{SW}. This lower frequency allows the inductor current to safely discharge, there by preventing current runaway. The oscillator's frequency will gradually increase to its designed rate when the feedback voltgae on FB again approaches 0.791V.

Application Information

Input Capacitor Selection

Because buck converters have a pulsating input current, a low ESR input capacitor is required. This results in the best input voltage filtering, minimizing the interference with other circuits caused by high input voltage spikes. Also, the input capacitor must be sufficiently large to stabilize the input voltage during heavy load transients. For good input voltage filtering, usually a 22µF input capacitor is sufficient. It can be increased without any limit for better input-voltage filtering. Ceramic capacitors show better performance because of the low ESR value, and they are less sensitive against voltage transients and spikes compared to tantalum capacitors. Place the input capacitor as close as possible to the input and GND pin of the device for better performance.

Inductor Selection

For high efficiencies, the inductor should have a low DC resistance to minimize conduction losses. Especially at high-switching frequencies, the core material has a higher impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. A reasonable starting point for setting ripple current, ΔI_L, is 40% of maximum output current. The recommended inductor value can be calculated as below:

$$L \geq \frac{V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right)}{F_{SW}\cdot \Delta I_L}$$

$$I_{L(MAX)} = I_{OUT(MAX)} + \frac{1}{2}\Delta I_L$$

To avoid saturation of the inductor, the inductor should be rated at least for the maximum output current of the converter plus the inductor ripple current.

Output Voltage Setting

In the adjustable version, the output voltage is set by a resistive divider. The external resistive divider is connected to the output, allowing remote voltage sensing as shown in “Typical Application Circuits”. The output voltage can be calculated as below:

$$V_{OUT} = V_{REF}\cdot\left(1+\frac{R1}{R2}\right) = 0.791\cdot\left(1+\frac{R1}{R2}\right)$$

If V_{OUT} setting less than V_{IN} POR,suggest using Dual Power Input of Typical Application Circuit.
If V_{OUT} setting more than V_{IN} POR, suggest using Single Power Input of Typical Application Circuit.

Output Capacitor Selection

The current-mode control scheme of the APW7415S allows the use of tiny ceramic capacitors. The higher capacitor value provides the good load transients response. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. If required, tantalum capacitors may be used as well. The output ripple is the sum of the voltages across the ESR and the ideal output capacitor.

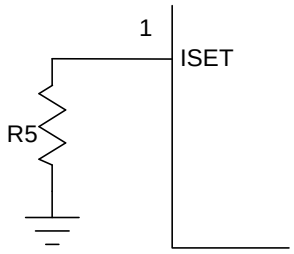
$$\Delta V_{OUT} \cong \frac{V_{OUT}\cdot\left(1-\frac{V_{OUT}}{V_{IN}}\right)}{F_{SW}\cdot L}\cdot\left(ESR+\frac{1}{8\cdot F_{SW}\cdot C_{OUT}}\right)$$

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Application Information

ISET Resistor Selection

The ISET resistor is used to set the transition point from PFM to PWM. It should be chosen to provide the best combination of efficiency, stability, ripple, and transient. If the ISET resistor is set lower, then stability and ripple improves, but efficiency during PWM mode and transient degrades. Likewise, if the ISET resistor is set higher, then the efficiency during PFM mode and transient improves, but stability and ripple degrades. So the optimal balance point of ISET resistor for good efficiency, stability, ripple and transient should be found out. Adjust the ISET threshold by connecting a resistor(R5) from ISET pin to ground. An internal 6.2uA current source charges the external resistor.



Generally, R5 is then given by:

V_{ISET}=R5x6.2uA

The Optimized ISET resistor can be got from the following steps:

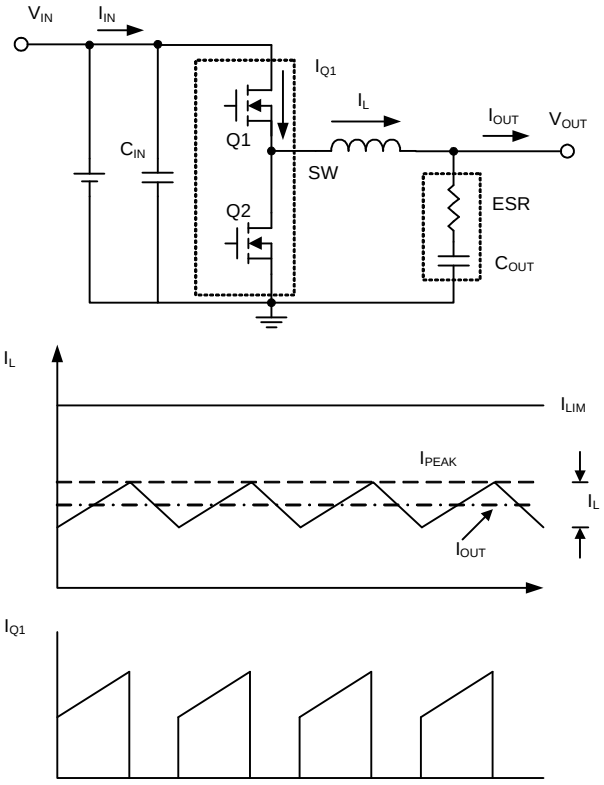
(1) Find IL Peak Current, $\Delta IL = \frac{(V_{IN} - V_{OUT})}{L} \times \frac{V_{OUT}}{V_{IN} \times F_{SW}}$

(2) ΔIL increase 1mA, VISET each additional 0.3mV. So used ΔIL*0.3, can find corresponding VISET (page 5, IL Peak Current vs. ISET Voltage)

(3) VISET divided by 6.2uA, can find corresponding R5

OutPut Capacitor Selection

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.



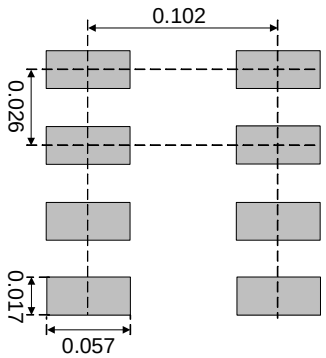
Application Information

Layout Consideration

For all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

1. The input capacitor should be placed close to the VIN and GND. Connecting the capacitor and VIN/GND with short and wide trace without any via holes for good input voltage filtering. The distance between VIN/GND to capacitor less than 2mm respectively is recommended.
2. To minimize copper trace connections that can inject noise into the system, the inductor should be placed as close as possible to the SW pin to minimize the noise coupling into other circuits.
3. The output capacitor should be place closed to converter VOUT and GND.
4. Since the feedback pin and network is a high impedance circuit the feedback network should be routed away from the inductor. The feedback pin and feedback network should be shielded with a ground plane or trace to minimize noise coupling into this circuit.
5. A star ground connection or ground plane minimizes ground shifts and noise is recommended.

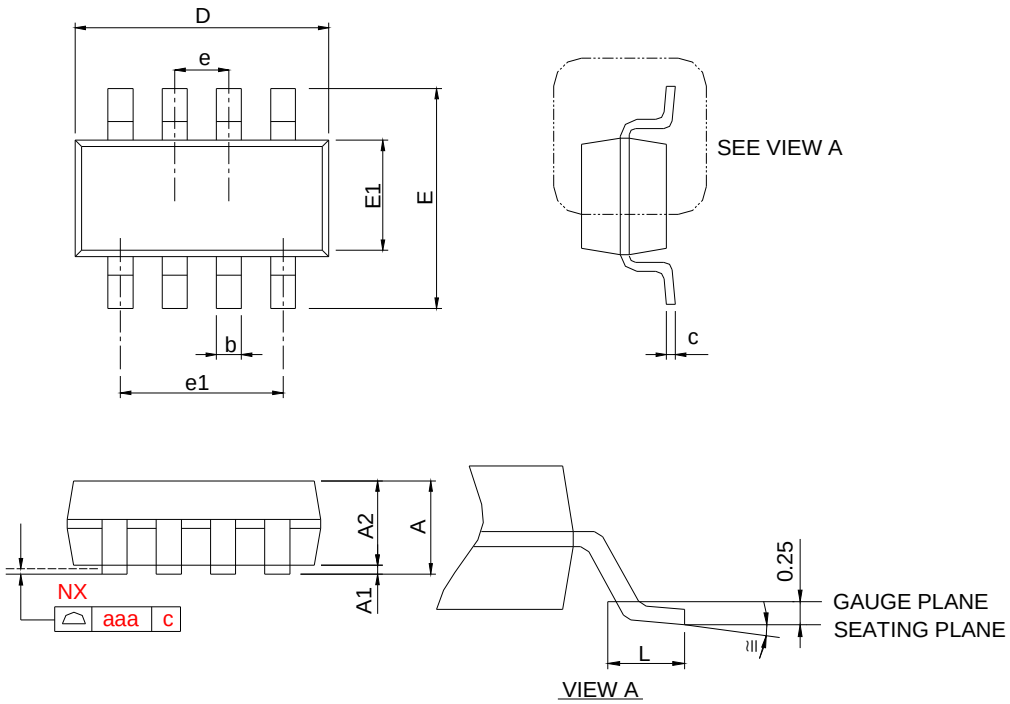
Recommended Minimum Footprint



TSOT-23-8A

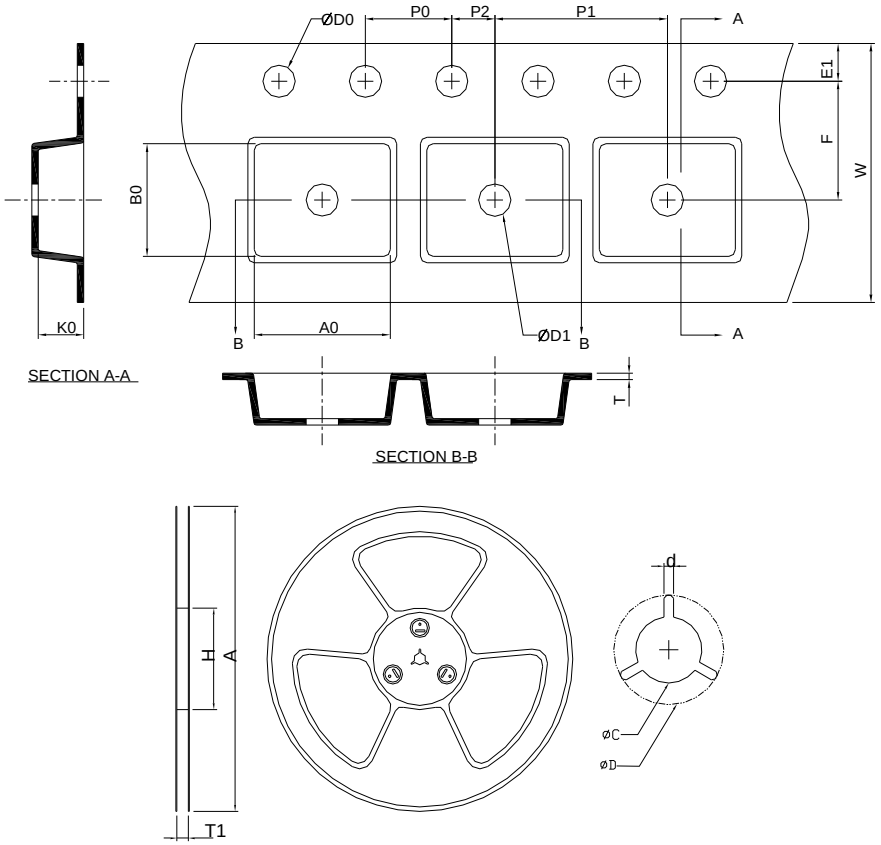
Package Information

TSOT-23-8A



SYMBOL	TSOT-23-8A			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	1.00	0.028	0.039
A1	0.01	0.10	0.000	0.004
A2	0.70	0.90	0.028	0.035
b	0.22	0.40	0.009	0.016
c	0.08	0.20	0.003	0.008
D	2.70	3.10	0.106	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.65 BSC		0.026 BSC	
e1	1.95 BSC		0.077 BSC	
L	0.30	0.60	0.012	0.024
θ	0^o	8^o	0^o	8^o
aaa	0.10		0.004	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TSOT-23-8A	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.0 MIN.	0.6+0.00 -0.40	3.20±0.20	3.10±0.20	1.20±0.20

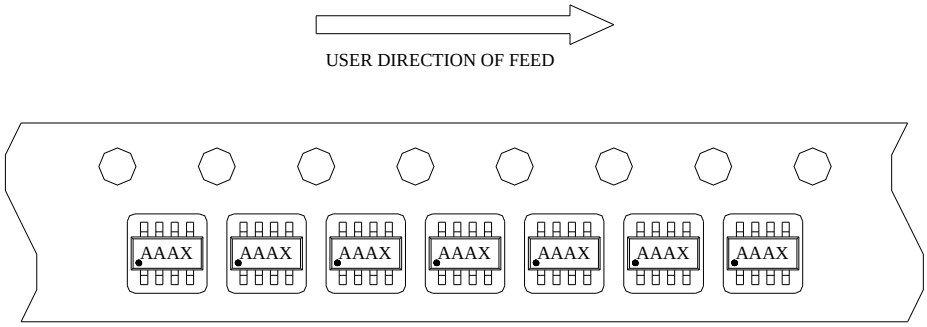
(mm)

Devices Per Unit

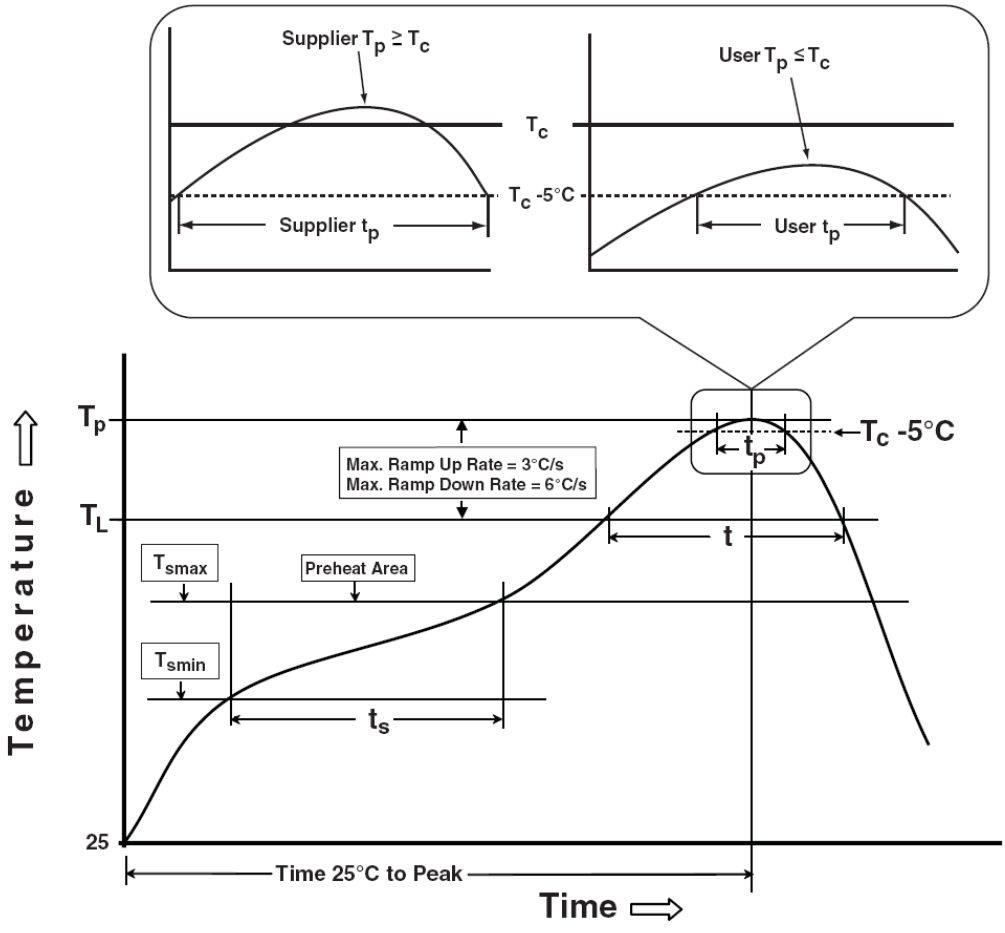
Package Type	Unit	Quantity
TSOT-23-8A	Tape & Reel	3000

Taping Direction Information

TSOT-23-8A



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ Tj=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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