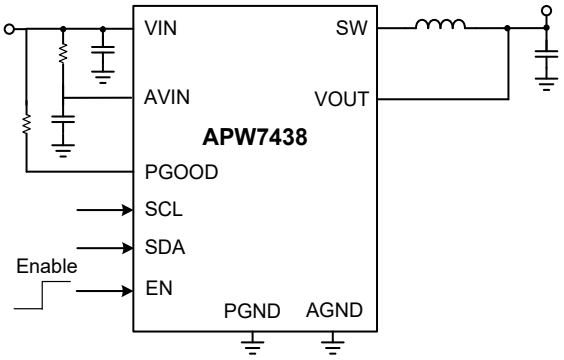
APW7438A/B

7A Constant On Time Synchronous Buck Regulator with I2C Production

Features

- **Pseudo frequency COT control**
- **Extremely fast line/load transient response**
- **I²C for output adjustment (3.4 Mbps)**
- **1.2 MHz switching frequency I²C Interface**
- **Extremely low-R_{DSON} MOSFETS**
- **Input voltage rail 2.7V to 6V**
- **Up to 7A output current**
- **Power save mode for light-load efficiency**
- **UVLO, OVP, and OCP**
- **-40°C to 85°C ambient temperature**
- **Available in QFN 2mm x 3mm 14 package**
- **RoHS compliant**

Simplified Application Circuit



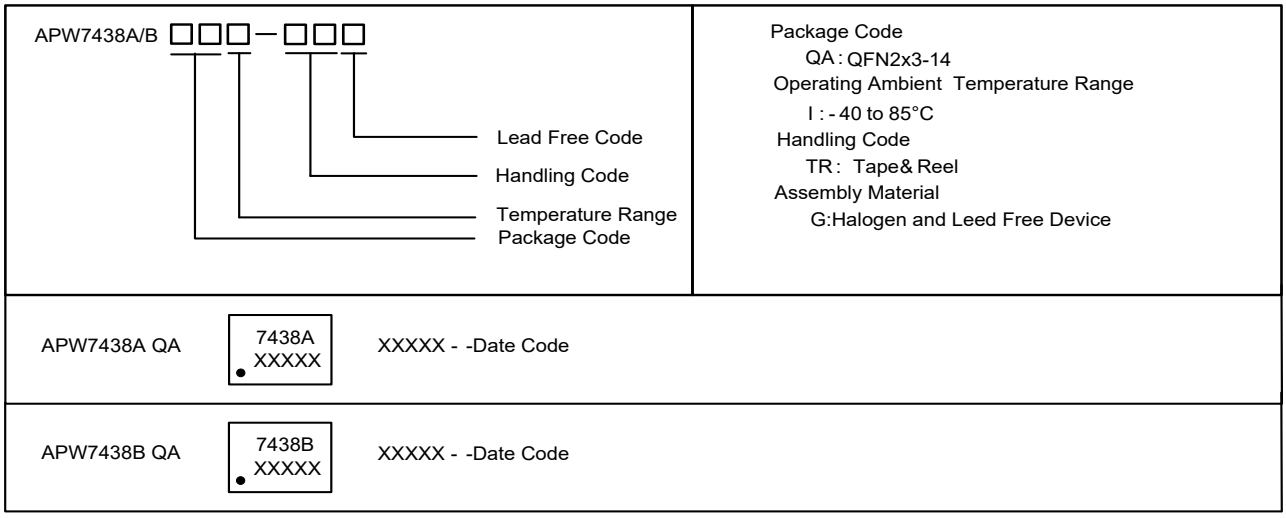
General Description

The APW7438A/B is a digitally controlled step-down regulator IC with an integrated 20mΩ high-side P-channel MOSFET and an 8mΩ low-side N-channel MOSFET.
It features ANPEC's proprietary COT-mode control scheme for near-instantaneous correction to line/load transients for a voltage range of 2.7V to 6V, and 7A with constant frequency.
The APW7438A/B is equipped with an automatic PFM/PWM mode operation. At light load, the IC operates in the PFM mode to reduce the switching losses and provides high efficiency over light to heavy loads with loading-modulated frequency.
The APW7438A/B has an I²C serial interface port for output voltage margining and monitoring, if required (it can also operate in default mode).
In addition it includes robust fault monitoring functions.
The APW7438A is available in 0.8V default output voltage (no voltage divider is necessary) which can be changed from 0x01 Register.

Applications

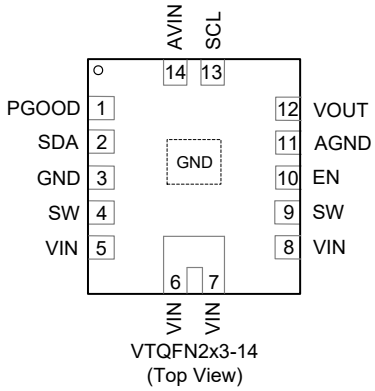
- **High performance hard disk drive (HDD)**
- **Solid-state drive**
- **Data center applications**
- **Raid/host bus adaptors**
- **Optical transceivers**

Ordering and Marking Information



Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Pin Configuration



VTQFN2x3-14
(Top View)

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{VIN}	VIN, SW to GND	-0.3 ~ 7	V
V_{sw}	SW to GND (shorter than 50 ns)	-2 ~ 7	V
Other Pins	AVIN, VOUT, SDA, SCL, EN, PGOOD to GND	-0.3 ~ 7	V
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature(10 Seconds)	260	°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2) QFN2x3-14	49	°C/W
θ_{JC}	Junction-to-Case Resistance in free air (Note 2)	20	°C/W

Note 2: θ_{JA} and θ_{JC} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 4)

Symbol	Parameter	Range	Unit
V_{VIN}	VIN to GND Voltage	2.7 ~ 6	V
I_{OUT}	Converter Output Current	0 ~ 7	A
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 4 : Refer to the typical application circuit

Electrical Characteristics

Test Condition: V_{VIN}=2.7~6V, T_J= -40 to 85°C. Typical values are at T_J=25°C.

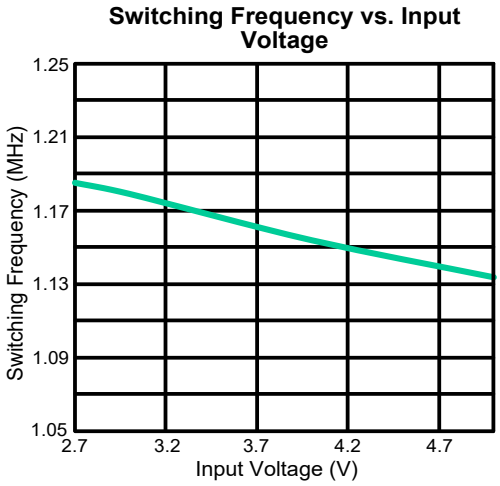
Symbol	Parameter	Test Conditions	APW7438A/B			Unit
			Min	Typ	Max	
Input Voltage						
I_Q	Input current	ILOAD = 0, PSM enabled	60	100	160	µA
I_{VIN}	V_{VIN} Shutdown Supply Current	EN= GND, T_A=25°C	-	0.1	1.2	µA
		EN= GND, T_A= -40 ~ 85°C	-	0.1	6.5	µA
UVLO	Under voltage rising threshold	VIN rising	2.3	2.55	2.65	V
UVLO HYST	UVLO hysteresis		0.1	0.15	0.22	V
OVPR	Over voltage rising threshold		6	6.2	6.4	V
OVPF	Over voltage falling hysteresis		0.1	0.2	0.3	V
VREF						
TSS	Softstart time	From VOUT 0%~90% of VREF	0.65	1	1.35	ms
TSS2	VREF slew rate	SLEW : Ctrl2(3:2) = 01	4.5	8	10	mV /µs
THICCUP	Hiccup time	VOUT = 0.2V	-	9.8	-	ms
Output Voltage						
VOUT	APW7438A Default VOUT	VOUT = 0.8V, (VIN = 2.7V – 5V), VSEL =[6:0]0101000	0.792	0.8	0.808	V
	APW7438B Default VOUT	VOUT = 0.6V, (VIN = 2.7V – 5V), VSEL =[6:0]0000000	0.594	0.6	0.606	V
	Line regulation	VIN from 3V to 5.5V, ILOAD = 1A[1]	-	0.1	-	%
	Load regulation	ILOAD = 0A to 5A[1]	-	0.23	-	%/A
	VOUT input current		-	0	0.2	µA
UVP	VOUT under voltage threshold	VOUT below this threshold will initiate a hiccup sequence	79	82	85	%V REF

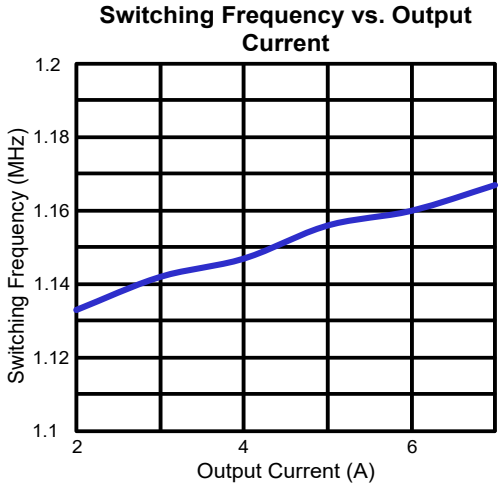
Electrical Characteristics (Cont.)

Test Condition: V_{VIN}=2.7~6V, T_J= -40 to 85°C. Typical values are at T_J=25°C.

Symbol	Parameter	Test Conditions	APW7438A/B			Unit
			Min	Typ	Max	
Switch (SW)						
RDSON_H	High side on resistance	VIN = 5V	10	20	32.5	mΩ
RDSON_L	Low side on resistance	VIN = 5V	4	8	12.9	mΩ
OCP	Current limit		7.5	10	12.5	A
T_{OTR}	Thermal shut down threshold		-	150	-	°C
	Hysteresis		-	40	-	°C
F_{SW}	Switching Frequency		1	1.2	1.4	MHz
RSWDISC	SW discharge resistance	EN = low; Discharge: Ctrl3(0) = 1	170	200	270	Ω
EN						
V_{IH}	Input high		1.1	-	-	V
V_{IL}	Input low		-	-	0.4	V
	Input current		-	0	1	µA
PGOOD						
V_{POK}	PGOOD VOUT lower threshold	VOUT rising, percentage of VREF	85	90	95	%V REF
	PGOOD VOUT upper threshold	VOUT falling, percentage of VREF	105	110	115	%V REF
	Hysteresis	Percentage of VREF 5%	2	5	9	%V REF
	PGOOD pull down resistance		6	13	25	Ω
	PGOOD leakage current		-	0	0.2	µA
	PGOOD delay	PGOOD rising edge delay	-	45	-	ms
7 Bit DAC						
	Differential linearity	Monotonicity assured by design	-	-	0.8	LSB
SDA and SCL						
V_{IH}	Input high		1.2	-	-	V
V_{IL}	Input low		-	-	0.4	V
	Input current		-	0	0.2	µA
VOL	Low level output voltage	Logic0 output voltage, Isink = 2mA[1]	0	-	0.2 *VDD	V
IOL	Low level output current	VOL = 0.4V[1]	3	-	-	mA

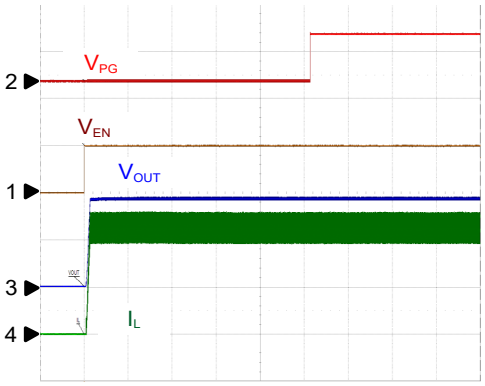
Typical Operating Characteristics





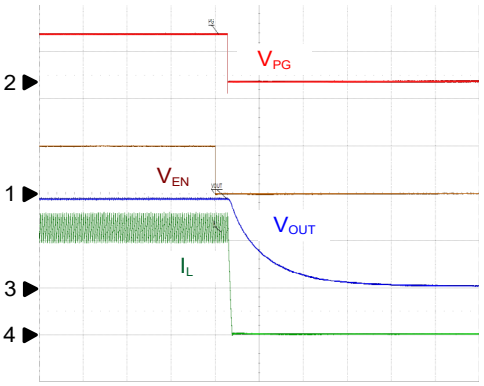
Operating Waveforms

Turn On Response



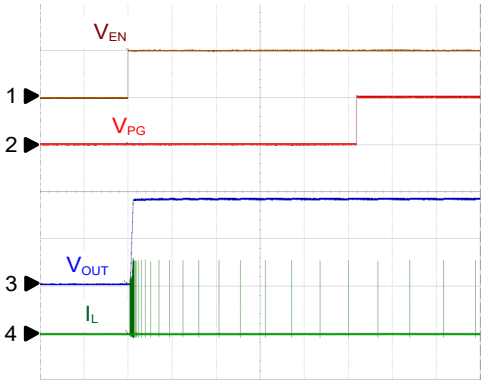
CH1:V_{EN},5V/Div, DC
CH2:V_{PG},5V/Div, DC
CH3:V_{OUT},500mV/Div, DC
CH4:I_L,2A/Div, DC
TIME:10ms/Div

Turn Off Response



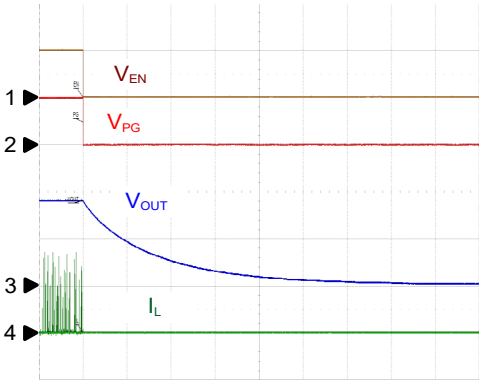
CH1:V_{EN},5V/Div, DC
CH2:V_{PG},5V/Div, DC
CH3:V_{OUT},500mV/Div, DC
CH4:I_L,2A/Div, DC
TIME:20µs/Div

Turn On Response



CH1:V_{EN},5V/Div, DC
CH2:V_{PG},5V/Div, DC
CH3:V_{OUT},500mV/Div, DC
CH4:I_L,500mA/Div, DC
TIME:10ms/Div

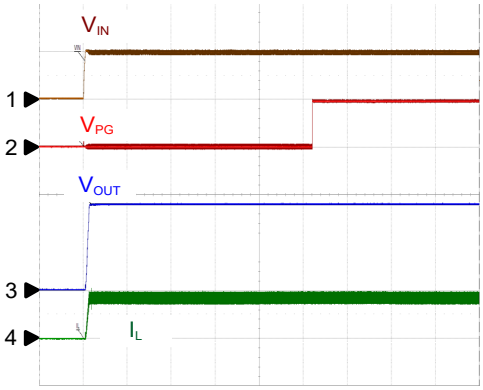
Turn Off Response



CH1:V_{EN},5V/Div, DC
CH2:V_{PG},5V/Div, DC
CH3:V_{OUT},500mV/Div, DC
CH4:I_L,500mA/Div, DC
TIME:5s/Div

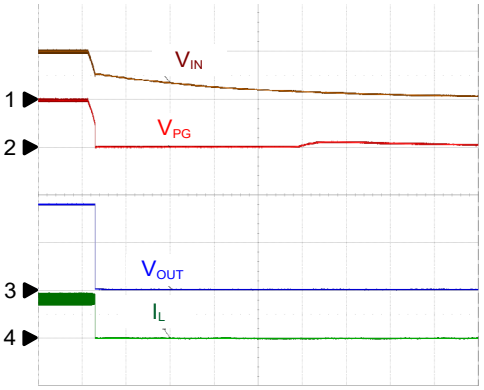
Operating Waveforms (Cont.)

UVLO at Rising



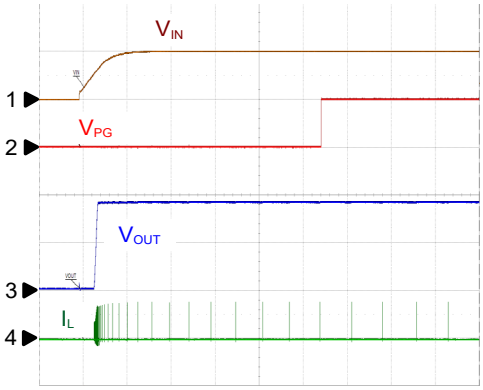
CH1:V_{IN},5V/Div, DC
CH2:V_{PG},5V/Div, DC
CH3:V_{OUT},500mV/Div, DC
CH4:I_L,5A/Div, DC
TIME:10ms/Div

UVLO at Falling



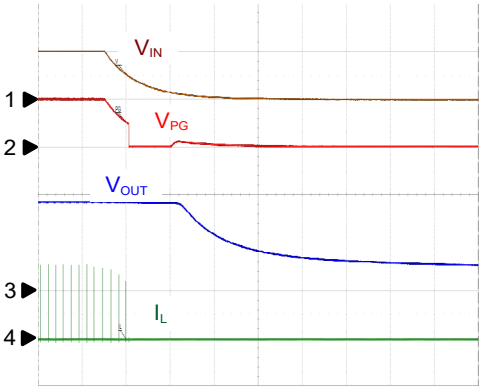
CH1:V_{IN},5V/Div, DC
CH2:V_{PG},5V/Div, DC
CH3:V_{OUT},500mV/Div, DC
CH4:I_L,5A/Div, DC
TIME:50ms/Div

UVLO at Rising



CH1:V_{IN},5V/Div, DC
CH2:V_{PG},5V/Div, DC
CH3:V_{OUT},500mV/Div, DC
CH4:I_L,1A/Div, DC
TIME:10ms/Div

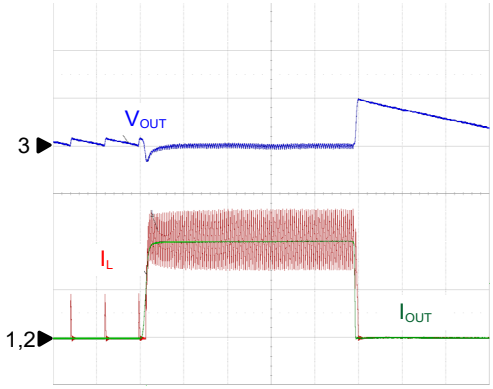
UVLO at Falling



CH1:V_{IN},5V/Div, DC
CH2:V_{PG},5V/Div, DC
CH3:V_{OUT},500mV/Div, DC
CH4:I_L,500mA/Div, DC
TIME:50ms/Div

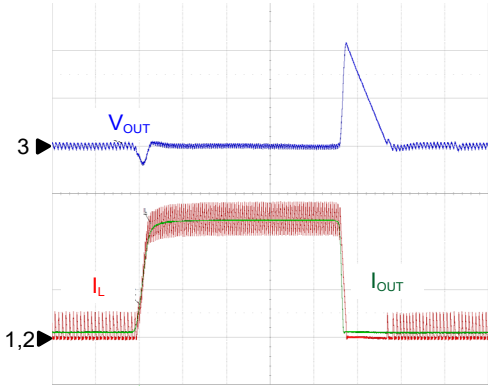
Operating Waveforms (Cont.)

Load Transient 1



CH1:I_{OUT},1A/Div, DC
CH2:I_L,1A/Div, DC
CH3:V_{OUT},50mV/Div, AC
TIME:20μs/Div

Load Transient 2

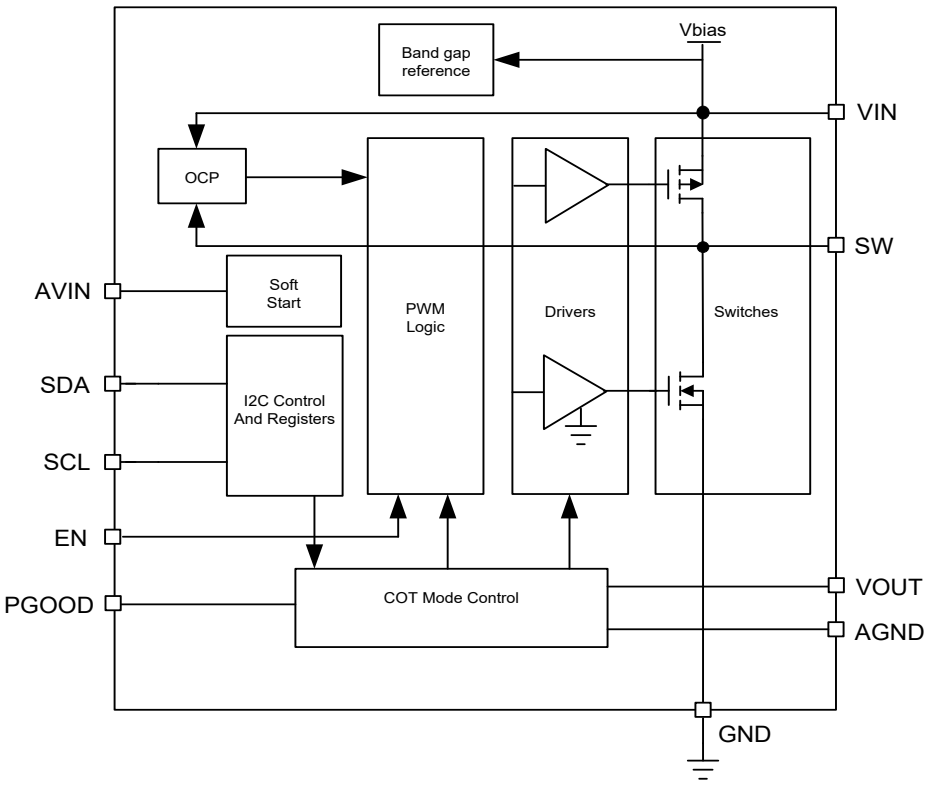


CH1:I_{OUT},2A/Div, DC
CH2:I_L,2A/Div, DC
CH3:V_{OUT},50mV/Div, AC
TIME:20μs/Div

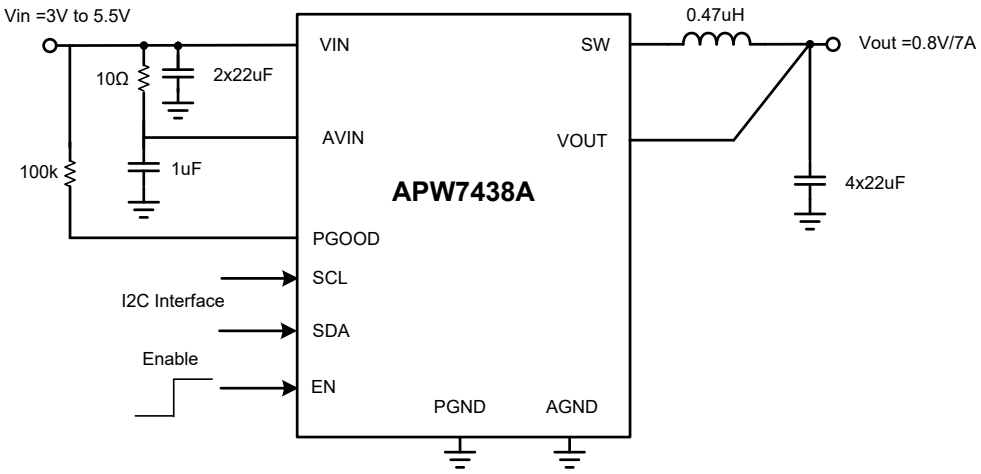
Pin Descriptions

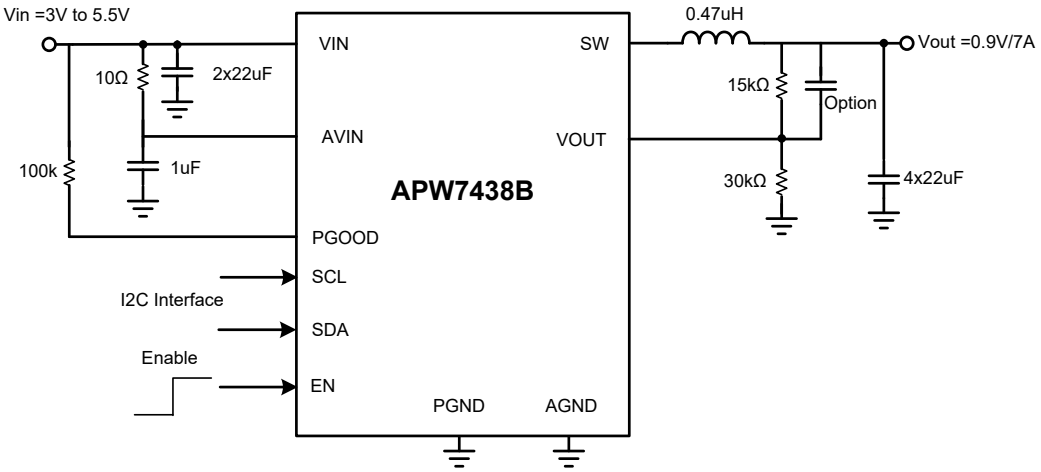
PIN QFN NO.	NAME	Function
1	PGOOD	Open drain status output, requires external pull-up resistor. This pin goes low, when VOUT exceeds the defined power good range.
2	SDA	Serial data bus (bidirectional) for I^2C. Connect directly to GND, if unused.
3	GND	Ground. Connect to ground plane.
4,9	SW	Switching node. Drives the external L-C low pass filter.
5,6,7,8	VIN	Input of IC and buck stage. Connect to input rail VIN (between 2.7V and 6V). A minimum input capacitance of one 1μF and one 22μF of X5R or a multilayer ceramic, should be placed very close to IC between this node and GND.
10	EN	Enable for switching regulator. Force high to enable, force low to disable the IC.
11	AGND	Analog ground. Connect to ground plane.
12	VOUT	Output voltage sense. Connect directly to output rail or resistive voltage divider output.
13	SCL	Serial clock input for I^2C. Connect directly to GND, if unused.
14	AVIN	Analog VIN voltage input pin.
Exposed Pad	GND	Ground. Connect to ground plane.

Block Diagram



Typical Application Circuit





I²C Programming

I²C SERIAL CONTROL INTERFACE

The APW7438A/B has a bidirectional I²C interface that compatible with the I²C (Inter IC) bus protocol and supports standard mode (100-kHz), fast mode (400-kHz) and the high-speed mode (up to 3.4Mbps in wire mode) data transfer rates for single byte write and read operations. This is a slave only device that does not support a multi-master bus environment or wait state insertion. The control interface is used to program the registers of the device and to read device status.

The APW7438A/B supports the standard-mode I²C bus operation (100 kHz maximum), the fast I²C bus operation (400 kHz maximum) and the high-speed mode (up to 3.4Mbps in wire mode). The APW7438A/B performs all I²C operations without I²C wait cycles.

General I²C Operation

The I²C bus uses two signals; SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data is transferred on the bus serially one bit at a time. The address and data can be transferred in byte (8-bit) format, with the most significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus.

The bus uses transitions on the data pin (SDA) while the clock is high to indicate a start and stop conditions. A high-to-low transition on SDA indicates a start and a low-to-high transition indicates a stop. Normal data bit transitions must occur within the low time of the clock period. These conditions are shown in Figure 1. The master generates the 7-bit slave address and the R/$\overline{W}$ bit — a 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ) to open communication with another device and then waits for an acknowledge condition. The APW7438A/B holds SDA low during the acknowledge clock period to indicate an acknowledgment. When this occurs, the master transmits the next byte of the sequence.

Each device is addressed by a unique 7-bit slave address plus R/$\overline{W}$ bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. An external pull-up resistor must be used for the SDA and SCL signals to set the high level for the bus.

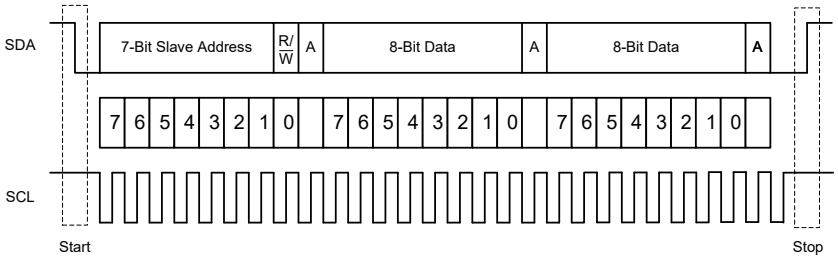


Figure 1. Typical I²C sequence

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in Figure 1. **The APW7438A/B I²C Slave Address is a hard-coded 7-bit address "0010010" (12H).**

Single-Byte Transfer

The serial control interface supports single-byte R/$\overline{W}$ operations for sub-addresses 0x00 to 0xFF.

Supplying a sub-address for each sub-address transaction is referred to as random I²C addressing. The APW7438A/B also supports sequential I²C addressing. For write transactions, if a sub-address is issued followed by data for that sub-address and the 15 sub-addresses that follow, a sequential I²C write transaction has taken place, and the data for all 16 sub-addresses is successfully received by the APW7438A/B. For I²C sequential write transactions, the sub-address then serves as the start address, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines how many sub-addresses are written. As was true for random addressing, sequential addressing requires that a complete set of data be transmitted. If only a partial set of data is written to the last sub-address, the data for the last sub-address is discarded. However, all other data written is accepted; only the incomplete data is discarded.

I²C Programming (Cont.)

Single-Byte Write

As shown in Figure 2, a single-byte data write transfer begins with the master device transmitting a start condition followed by the I²C device address and the R/$\overline{W}$ bit. The R/$\overline{W}$ bit determines the direction of the data transfer. For a write data transfer, the R/$\overline{W}$ bit will be a 0. After receiving the correct I²C device address and the R/$\overline{W}$ bit, the APW7438A/B responds with an acknowledge bit. Next, the master transmits the address byte or bytes corresponding to the APW7438A/B internal memory address being accessed. After receiving the address byte, the APW7438A/B again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the APW7438A/B again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data write transfer.

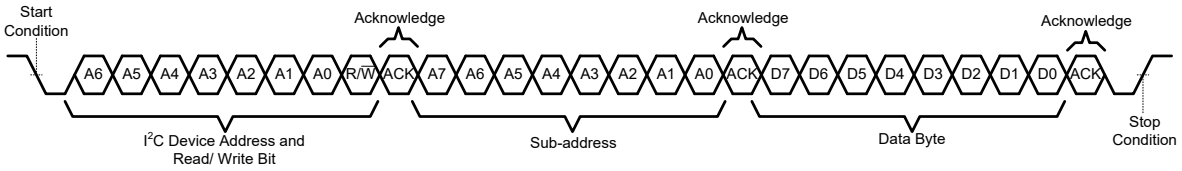


Figure 2. Single-Byte Write Transfer

Single-Byte Read

As shown in Figure 3, a single-byte data read transfer begins with the master device transmitting a start condition followed by the I²C device address and the R/$\overline{W}$ bit. For the data read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte or bytes of the internal memory address to be read. As a result, the R/$\overline{W}$ bit becomes a 0. After receiving the APW7438A/B address and the R/W bit, APW7438A/B responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the APW7438A/B address and the R/$\overline{W}$ bit again. This time the R/$\overline{W}$ bit becomes a 1, indicating a read transfer. After receiving the address and the R/$\overline{W}$ bit, the APW7438A/B again responds with an acknowledge bit. Next, the APW7438A/B transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not acknowledge followed by a stop condition to complete the single byte data read transfer.

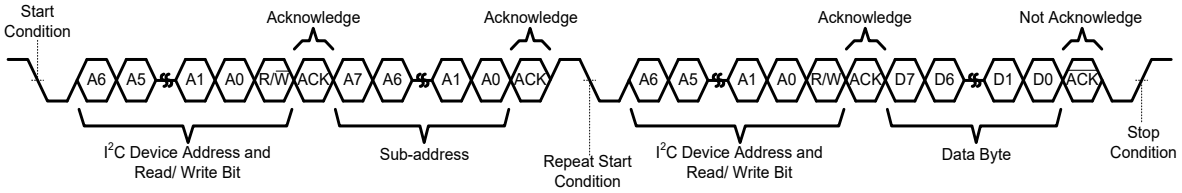


Figure 3. Single-Byte Read Transfer

I²C Programming (Cont.)

SMBus Control Timing						
	SMBDAT and SMBCLK Leakage Current		-	0.01	1	μA
F_{SMB}	SMBus Operating Frequency		-	-	100 400	KHz
T_{BUF}	Bus free time between stop and start condition	SCL=100KHz SCL=400KHz	4.7 1.3	- -	- -	μs
T_{HD_STA}	Hold time after start condition	After this period, the first clock is generated SCL=100KHz SCL=400KHz	4 0.6	- -	- -	μs
T_{SU_STA}	Repeated start condition setup time	SCL=100KHz SCL=400KHz	4.7 0.6	- -	- -	μs
T_{SU_STO}	Stop condition setup time	SCL=100KHz SCL=400KHz	4 0.6	- -	- -	μs
T_{HD_DAT}	Data hold time	SCL=100KHz SCL=400KHz	300 300	- -	- -	ns
T_{SU_DAT}	Data setup time	SCL=100KHz SCL=400KHz	250 100	- -	- -	ns
T_{LOW}	Clock low period	SCL=100KHz SCL=400KHz	4.7 1.3	- -	- -	μs
T_{HIGH}	Clock high period	SCL=100KHz SCL=400KHz	4 0.6	-	- -	μs
T_{F_SMB}	Fall time of SMB DAT/CLK	SCL=100KHz SCL=400KHz	-	-	300 300	ns
T_{R_SMB}	Rise time of SMB DAT/CLK	SCL=100KHz SCL=400KHz	-	-	1000 300	ns
C_b	Capacitive Load for Each B μ s Line	SCL=100KHz SCL=400KHz	-	-	400 400	pF

Timing Diagram

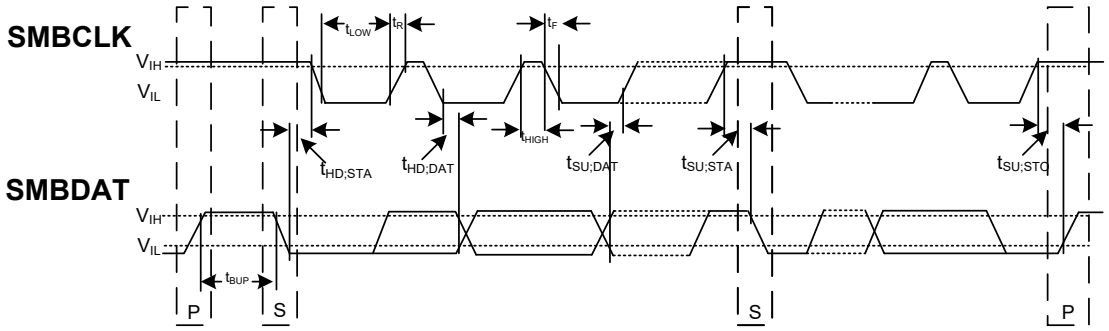


Figure 4: SMBus Common AC Specification

Register Map

Address	Name	Default Value
00h	Status	44
01h	V_{SEL} APW7438A Default	A8
	V_{SEL} APW7438B Default	80
02h	Ctrl1	80
03h	Ctrl2	05
04h	Vender	10
05h	Die	02
06h	Ctrl3	02

REG00 Status Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	ILIM	UVLO	VIN_OVP	VOUT_OVP	VOUT_UVP	PG	OTW	OTP
Read/Write	R	R	R	R	R	R	R	R
Power On Default	0	1	0	0	0	1	0	0

Bit Name	Bit Definition
ILIM	A real time status of low-side current limit condition. It indicates "1" when the current flowing through low-side MOSFET is greater than OCP threshold.
UVLO	UVLO=1, VIN > 2.55V UVLO=0, VIN < 2.40V
VIN_OVP	Latched to 1 if a VIN OVP event occurs.
VOUT_OVP	Latched to 1 if a VOUT OV event occurs.
VOUT_UVP	Latch to 1 if the VOUT under voltage is reached
PG	Indicate if PMIC output is ready (PG=1), otherwise PG = 0
OTW	OTW = 1, TEMP > 130° OTW = 0, TEMP < 130°
OTP	Latch to 1 if the over temperature is reached

REG01 V_{SEL} Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	EN	V_{SEL}[6:0]						
Read/Write	R/W	R/W						
Power On Default	1	0	0	0	0	0	0	0

Bit Name	Bit Definition
EN	EN=0 Device disabled EN=1 Device enabled
V_{SEL}[6:0]	7-bit DAC value to set VREF. The default value is determined by the part ordering code. 0000000: FB=0.6V, (APW7438B Default), 0000001: 0.605V...0101000: 0.8V, (APW7438A Default)... 1111111: 1.235V

REG02 Ctrl1 Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	FREQ[2:0]			Reserve				MODE
Read/Write	R/W	R/W	R/W	R	R	R	R	R/W
Power On Default	1	0	0	0	0	0	0	0

Bit Name	Bit Definition
FREQ[2:0]	000: 2.2Mhz 001: 1.8Mhz 010: 1.5Mhz 100: 1.2Mhz (Default) 101: 1Mhz 110: 0.8Mhz
MODE	0: Auto PFM mode 1: PWM mode only

Register Map (Cont.)

REG03 Ctrl2 Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reserve				SLEW_RATE[1:0]		PG_CTRL	PG_SET
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	0	1	0	1
Bit Name	Bit Definition							
SLEW_RATE[1:0]	00: 32mV/us 01: 8mV/us 10: 4mV/us 11: 2mV/us							
PG_CTRL	0: enable PG function 1: disable PG function;							
PG_SET	When PG CTRL is 1, PG pin is pulled high if PG Set is 0; otherwise pull down PG pin							

REG04 Vendor ID Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	VID[3:0]				DIE_ID			
Read/Write	R							
Power On Default	0	0	0	1	0	0	0	0
Bit Name	Bit Definition							

REG05 DIE Register

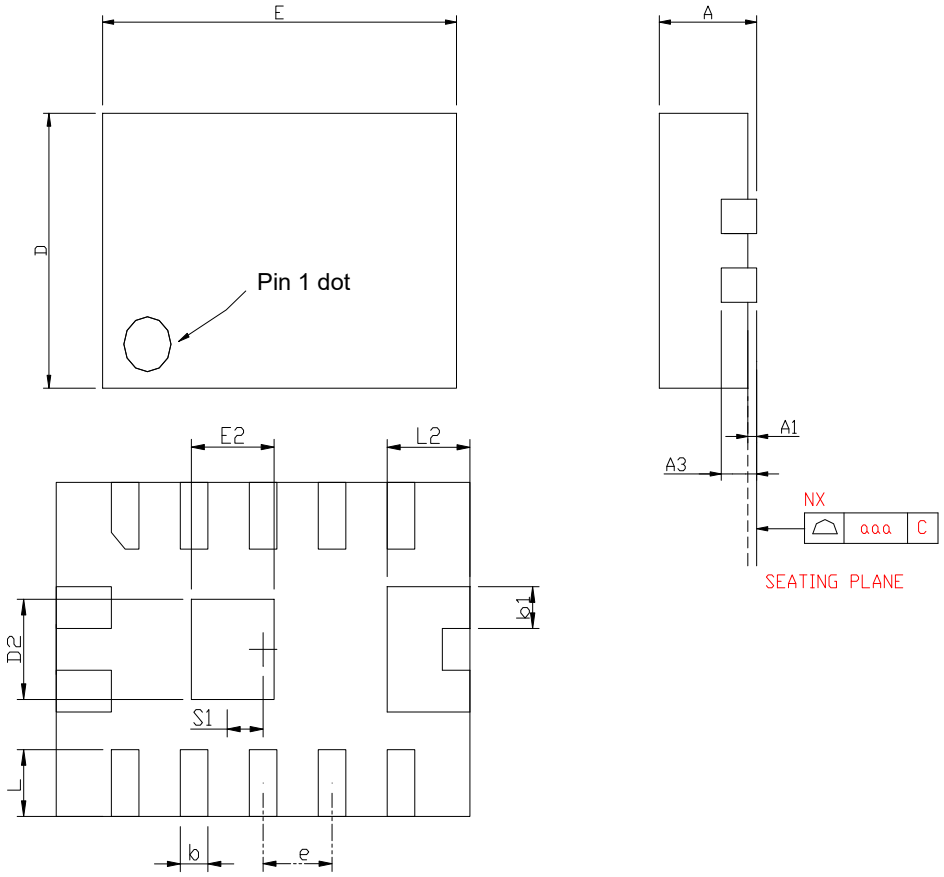
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reserve				Die_Rev			
Read/Write	R	R	R	R	R			
Power On Default	0	0	0	0	0	0	1	0
Bit Name	Bit Definition							

REG06 Ctrl3 Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reserve	SS[1:0]		VOUTOV_L	VINOV_L	SW_RATE	DLY_DIS	DISCHARGE
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	0	0	1	0
Bit Name	Bit Definition							
SS	Set Buckx Softstart Time 00: 1.0ms 01: 0.5ms 10: 0.25ms 11: 0.125ms							
VOUTOV_L	1: VOUTOVP Latch 0:VOUTOVP non_latch							
VINOVP_L	1: VINOVP Latch 0:VINOVP non_latch							
SW_RATE	Switch node rise rate. 0: High switch node rise rate 1: Low switch node rise rate (20% Off)							
DLY_DIS	0: No PGOOD delay 1: 45mSec PGOOD delay enable							
Discharge	0:No discharge 1:When the regulator is disabled, the output voltage is discharged through the SW pin							

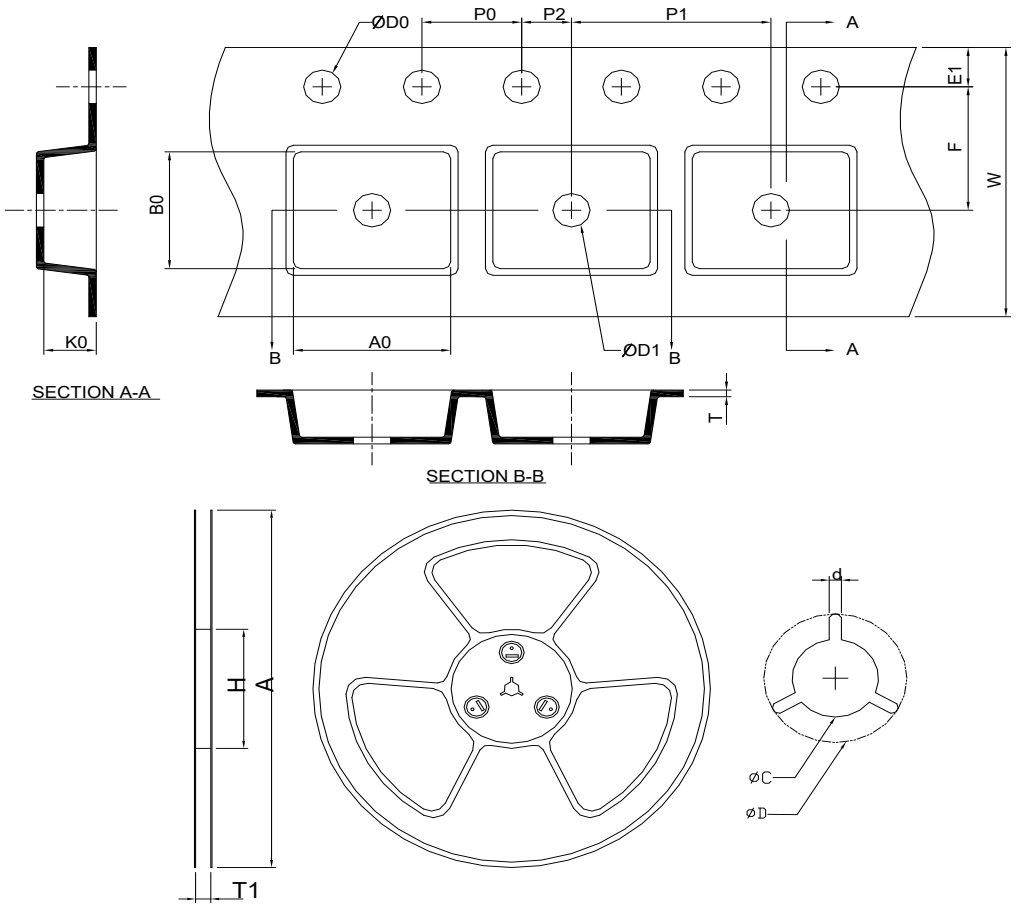
Package Information

QFN2x3-14



SYMBOL	Q FN2x3-14			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.80	0.90	0.031	0.035
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.15	0.25	0.006	0.010
b1	0.20	0.30	0.008	0.012
D	1.90	2.10	0.075	0.083
E	2.90	3.10	0.114	0.122
D2	0.50	0.70	0.020	0.028
E2	0.50	0.70	0.020	0.028
e	0.50 BSC		0.020 BSC	
L	0.35	0.45	0.014	0.018
L1	0.55	0.65	0.022	0.026
S1	0.21	0.31	0.008	0.012
aaa	0.08		0.003	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
QFN(2x3)	178.0±2.00	50 MIN.	16.5+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.20	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	2.20±0.20	3.20±0.20	1.30±0.20

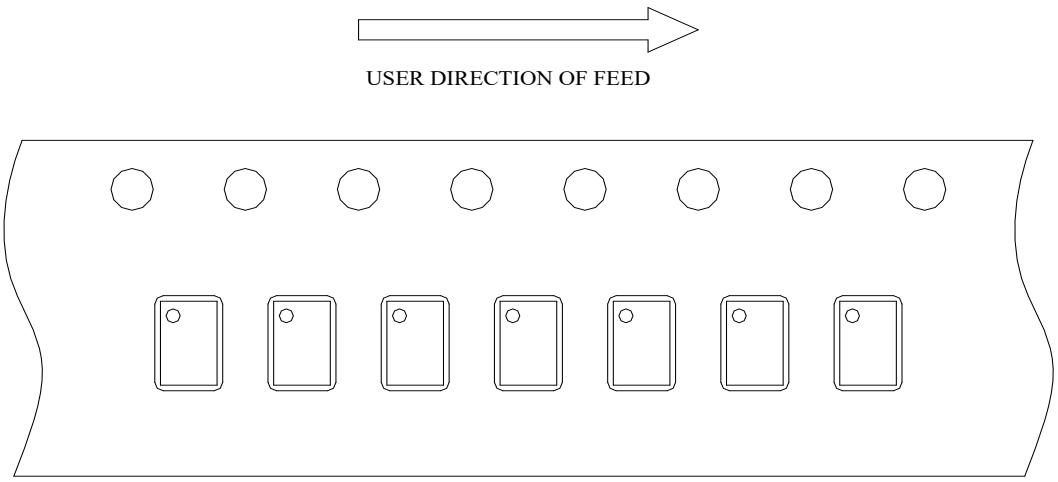
(mm)

Devices Per Unit

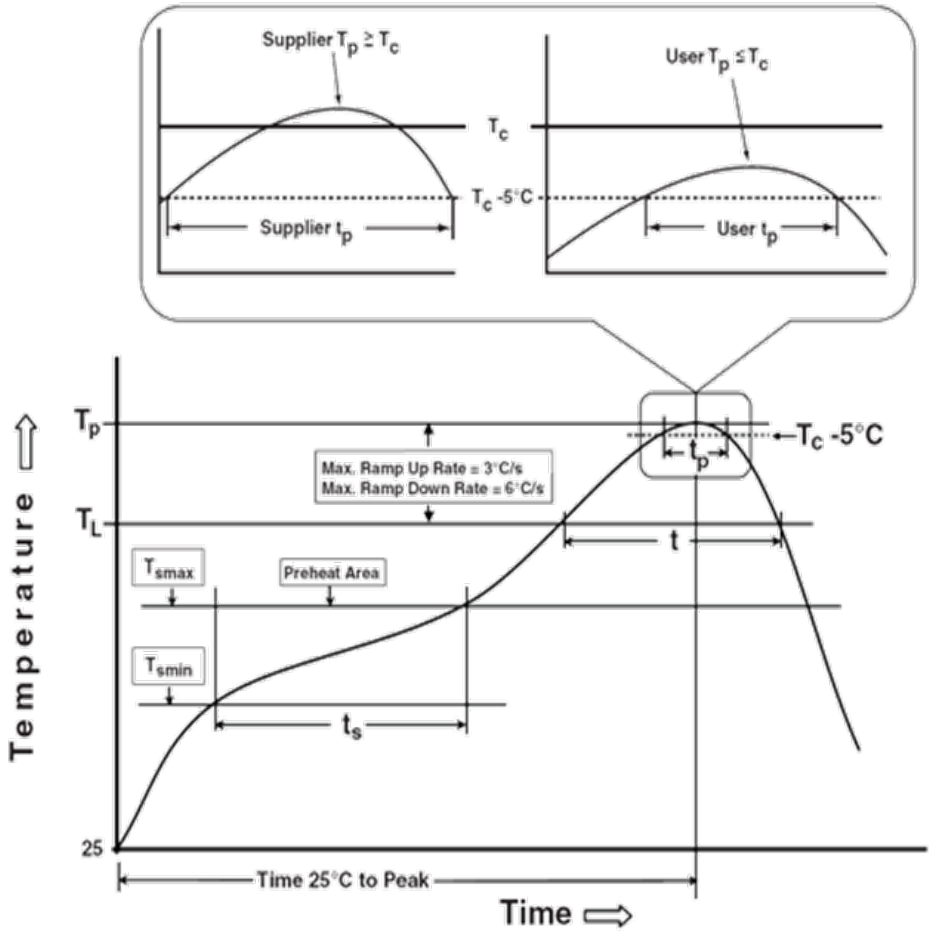
Package type	Packing	Quantity
QFN(2x3)	Tape & Reel	3000

Taping Direction Information

QFN2x3-14



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≧ 2KV
MM	JESD-22, A115	VMM ≧ 200V
Latch-Up	JESD 78	10ms, 1_{tr} ≧ 100mA

Customer Service

Anpec Electronics Corp.
Head Office :
No.6, Dusing 1st Road, SBIP,
Hsin-Chu, Taiwan, R.O.C.
Tel : 886-3-5642000
Fax : 886-3-5642050

Taipei Branch :
2F, No. 11, Lane 218, Sec 2 Jhongsing Rd.,
Sindian Dist, Sinbei City 23146, Taiwan
Tel : 886-2-2910-3838
Fax : 886-2-2917-3838