

## 1.5MHz, 1A Synchronous Buck Regulator

### Features

- **1A Output Continuous Current**
- **1.2A Output Peak Current**
- **Wide 3V~5.5V Input Voltage**
- **Fixed 1.5MHz Switching Frequency**
- **Low Dropout Operating at 100% Duty Cycle**
- **30mA Quiescent Current**
- **Integrate Synchronous Rectifier**
- **0.6V Reference Voltage**
- **Current-Mode Operation with Internal Compensation**
  - Stable with Ceramic Output Capacitors
  - Fast Line Transient Response
- **Short-Circuit Protection**
- **Over-Temperature Protection with Hysteresis**
- **Available in SOT-23-5/TSOT-23-5A Packages**
- **Lead Free and Green Devices Available (RoHS Compliant)**

### General Description

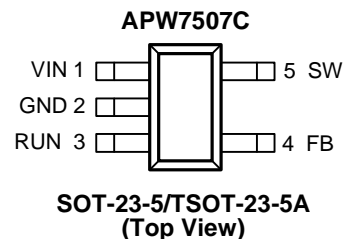
APW7507C is a 1.5MHz high efficiency monolithic synchronous buck regulator. Design with current mode scheme, the APW7507C is stable with ceramic output capacitor. Input voltage from 3V to 5.5V makes the APW7507C ideally suited for single Li-Ion battery powered applications. 100% duty cycle provides low dropout operation, extending battery life in portable electrical devices. The internally fixed 1.5MHz operating frequency allows the using of small surface mount inductors and capacitors. The synchronous switches included inside increase the efficiency and eliminate the need of an external Schottky diode.

The APW7507C is available in SOT-23-5/TSOT-23-5A packages.

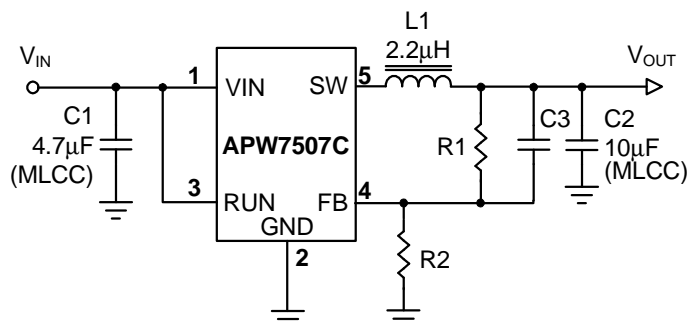
### Applications

- **HD STB**
- **BT Mouse**
- **PND Instrument**
- **Portable Instrument**

### Pin Configuration



### Simplified Application Circuit



ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

## Ordering and Marking Information

APW7507C    □□□-□□□ <div style="display: flex; align-items: center;"> <div style="border-left: 1px solid black; height: 40px; margin-right: 5px;"></div> <div style="border-left: 1px solid black; height: 30px; margin-right: 5px;"></div> <div style="border-left: 1px solid black; height: 20px; margin-right: 5px;"></div> <div style="border-left: 1px solid black; height: 10px;"></div> </div> <div style="margin-left: 10px;"> Assembly Material  Handling Code  Temperature Range  Package Code </div>	Package Code BT : TSOT-23-5A    B : SOT-23-5 Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW7507C BT : <span style="border: 1px solid black; padding: 0 5px;">W56X</span>	X - Date Code
APW7507C B : <span style="border: 1px solid black; padding: 0 5px;">W56X</span>	X - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

## Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
$V_{IN}$	Input Bias Supply Voltage ( $V_{IN}$ to GND)	-0.3 ~ 6	V
	RUN, FB, SW to GND Voltage	-0.3 ~ $V_{IN}+0.3$	V
$P_D$	Power Dissipation	Internally Limited	W
	Maximum Junction Temperature	150	°C
$T_{STG}$	Storage Temperature	-65 ~ 150	°C
$T_{SDR}$	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
$\theta_{JA}$	Junction-to-Ambient Resistance in Free Air <small>(Note 2)</small>	TSOT-23-5A	°C/W
		SOT-23-5	
		220	
		250	

Note 2:  $\theta_{JA}$  is measured with the component mounted on a high effective thermal conductivity test board in free air.

## Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
$V_{IN}$	Input Bias Supply Voltage (VIN to GND)	3 ~ 5.5	V
$V_{OUT}$	Converter Output Voltage	0.6 ~ $V_{IN}$	V
$I_{OUT}$	Converter Output Current	0 ~ 1	A
	Converter Output Peak Current, 10ms pulse, 1% duty cycle	1.2	
L1	Converter Output Inductor	1.0 ~ 10	$\mu$ H
$C_{IN}$	Converter Input Capacitor	4.7 ~ 100	$\mu$ F
$C_{OUT}$	Converter Output Capacitor	4.7 ~ 100	$\mu$ F
$T_A$	Ambient Temperature	-40 ~ 85	$^{\circ}$ C
$T_J$	Junction Temperature	-40 ~ 125	$^{\circ}$ C

Note 3: Refer to the typical application circuit

## Electrical Characteristics

Unless otherwise specified, these specifications apply over  $V_{IN}=3.3\sim 5.5V$  and  $T_A = 25^{\circ}C$ .

Symbol	Parameter	Test Conditions	APW7507C			Unit
			Min.	Typ.	Max.	
SUPPLY VOLTAGE AND CURRENT						
V <sub>IN</sub>	Input Voltage Range		3	-	5.5	V
I <sub>Q</sub>	Quiescent Current	V <sub>FB</sub> = 0.66V, V <sub>IN</sub> =3.3V	-	30	60	μA
I <sub>SD</sub>	Shutdown Input Current	RUN = GND	-	-	0.5	μA
POWER-ON-RESET (POR)						
	Rising POR Threshold		2.45	2.7	2.95	V
	POR Hysteresis		-	0.1	-	V
REFERENCE VOLTAGE						
V <sub>REF</sub>	Reference Voltage		0.588	0.6	0.612	V
	Output Voltage Accuracy	0A < I <sub>OUT</sub> < 1 A	-2.5	-	+2.5	%
I <sub>FB</sub>	FB Input Current		-50	-	50	nA
INTERNAL POWER MOSFETS						
F <sub>SW</sub>	Switching Frequency	V <sub>FB</sub> = 0.6V	1.2	1.5	1.9	MHz
	Foldback Frequency	V <sub>FB</sub> = 0.1V	-	210	-	kHz
	Foldback Threshold Voltage on FB	V <sub>FB</sub> Falling	-	0.2	-	V
	Foldback Hysteresis		-	50	-	mV
R <sub>P-FET</sub>	High Side P-FET Switch ON Resistance	I <sub>SW</sub> =200mA	-	0.26	-	Ω
R <sub>N-FET</sub>	Low Side N-FET Switch ON Resistance	I <sub>SW</sub> =200mA	-	0.23	-	Ω
	Minimum On-Time		-	-	100	ns
	Maximum Duty Cycle		-	-	100	%
PROTECTION						
I <sub>LM</sub>	Maximum Inductor Current-Limit	I <sub>P-FET</sub> , V <sub>IN</sub> = 3.3~5.5V	1.3	2.3	-	A
T <sub>OTP</sub>	Over-Temperature Protection	T <sub>J</sub> Rising (Note 4)	-	150	-	°C
	Over-Temperature Protection Hysteresis	(Note 4)	-	30	-	

## Electrical Characteristics

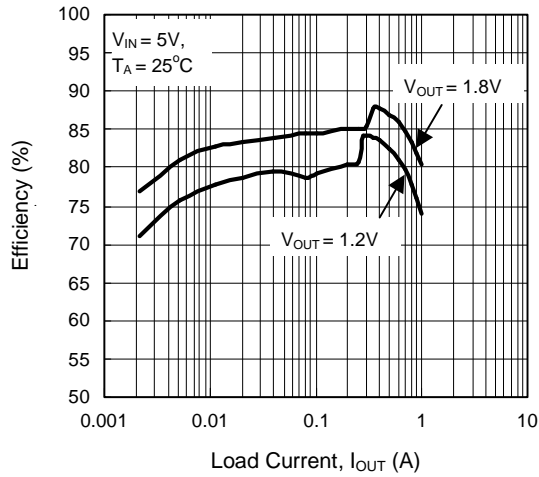
Unless otherwise specified, these specifications apply over  $V_{IN}=3.3\sim 5.5V$  and  $T_A=25\text{ }^{\circ}C$ .

Symbol	Parameter	Test Conditions	APW7507C			Unit
			Min.	Typ.	Max.	
START-UP AND SHUTDOWN						
tss	Soft-Start Duration	(Note 4)	-	0.7	-	ms
	RUN Input High Threshold		-	-	1	V
	RUN Input Low Threshold		0.4	-	-	V
	RUN Leakage Current	V <sub>RUN</sub> = 5V, V <sub>IN</sub> = 5V	-1	-	1	μA

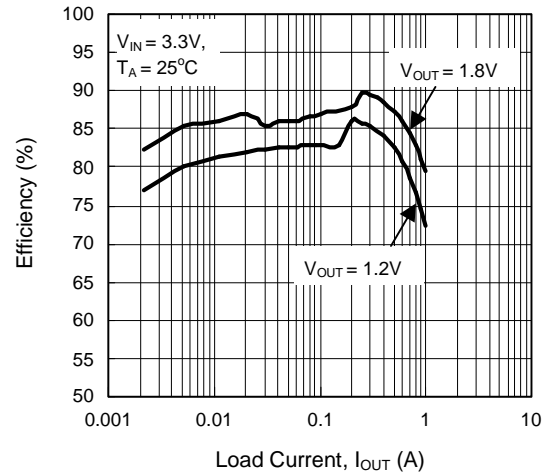
Note 4: Guarantee by design, not production test.

## Typical Operating Characteristics

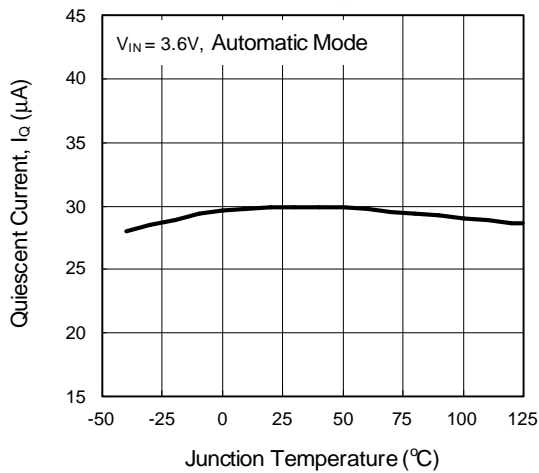
Efficiency vs. Load Current



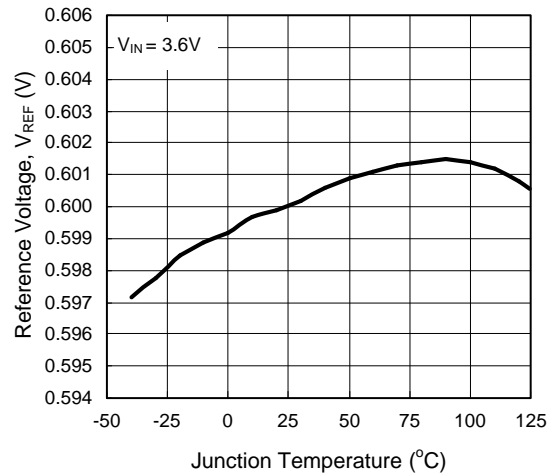
Efficiency vs. Load Current



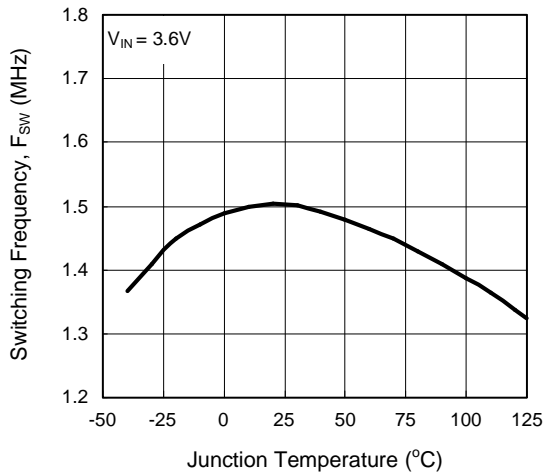
Quiescent Current vs. Junction Temperature



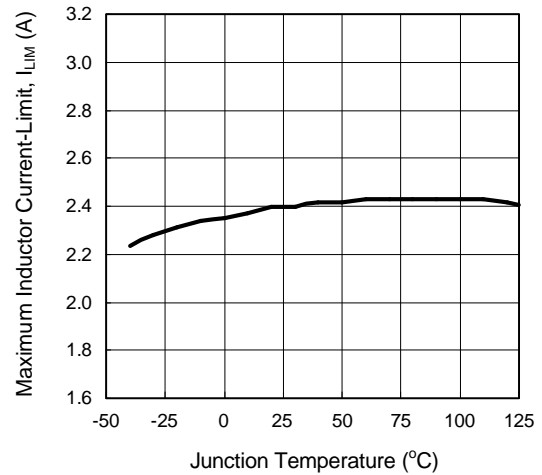
Reference Voltage vs. Junction Temperature



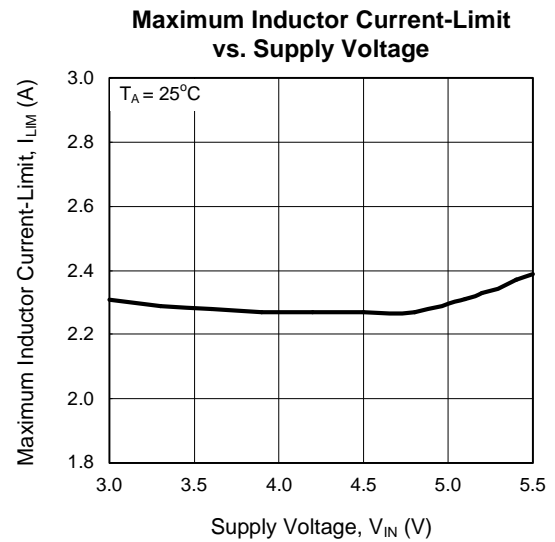
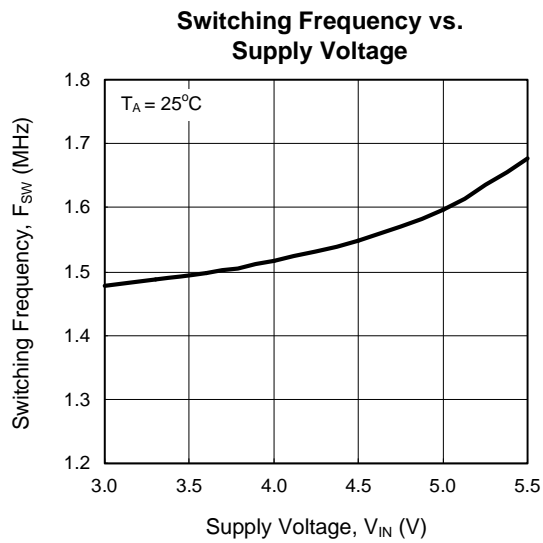
Switching Frequency vs. Junction Temperature



Maximum Inductor Current-Limit vs. Junction Temperature



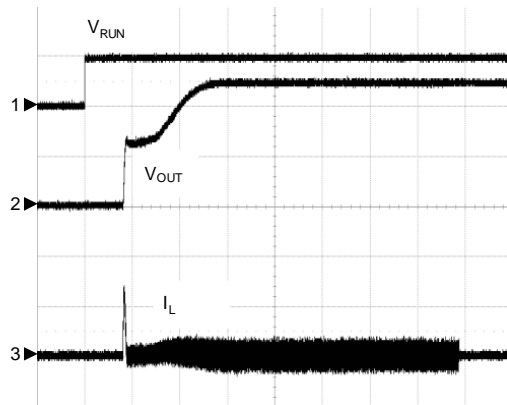
## Typical Operating Characteristics



## Operating Waveforms

Refer to the typical application circuit. The test condition is  $V_{IN}=5V$ ,  $V_{OUT}=1.2V$ ,  $T_A=25^{\circ}C$  unless otherwise specified.

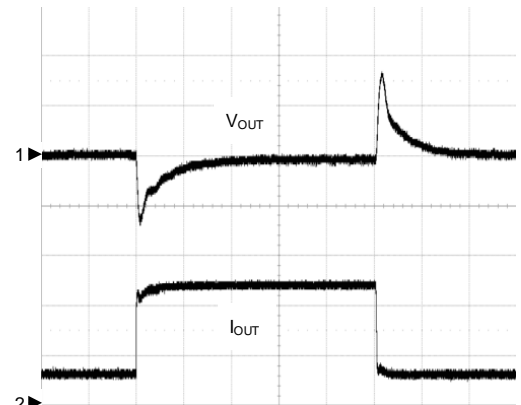
### Soft-Start



No load

CH1:  $V_{RUN}$ , 5V/Div, DC  
CH2:  $V_{OUT}$ , 500mV/Div, DC  
CH3:  $I_L$ , 0.5A/Div, DC  
TIME: 200 $\mu$ s/Div

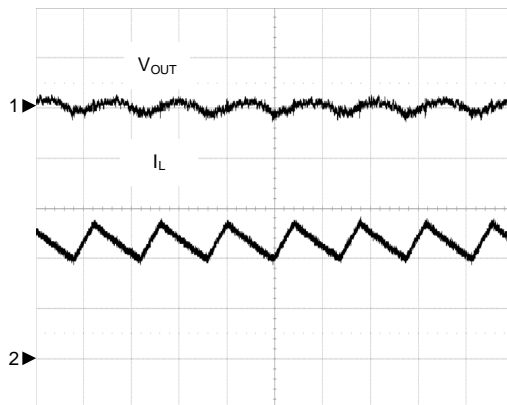
### Load Transient Response



$I_{OUT}=0.3A$  to  $1.2A$  to  $0.3A$  (rise / fall time = 0.5 $\mu$ s)

CH1:  $V_{OUT}$ , 100mV/Div, DC offset 1.2V  
CH2:  $I_{OUT}$ , 0.5A/Div, DC  
TIME: 20 $\mu$ s/Div

### Normal Operation



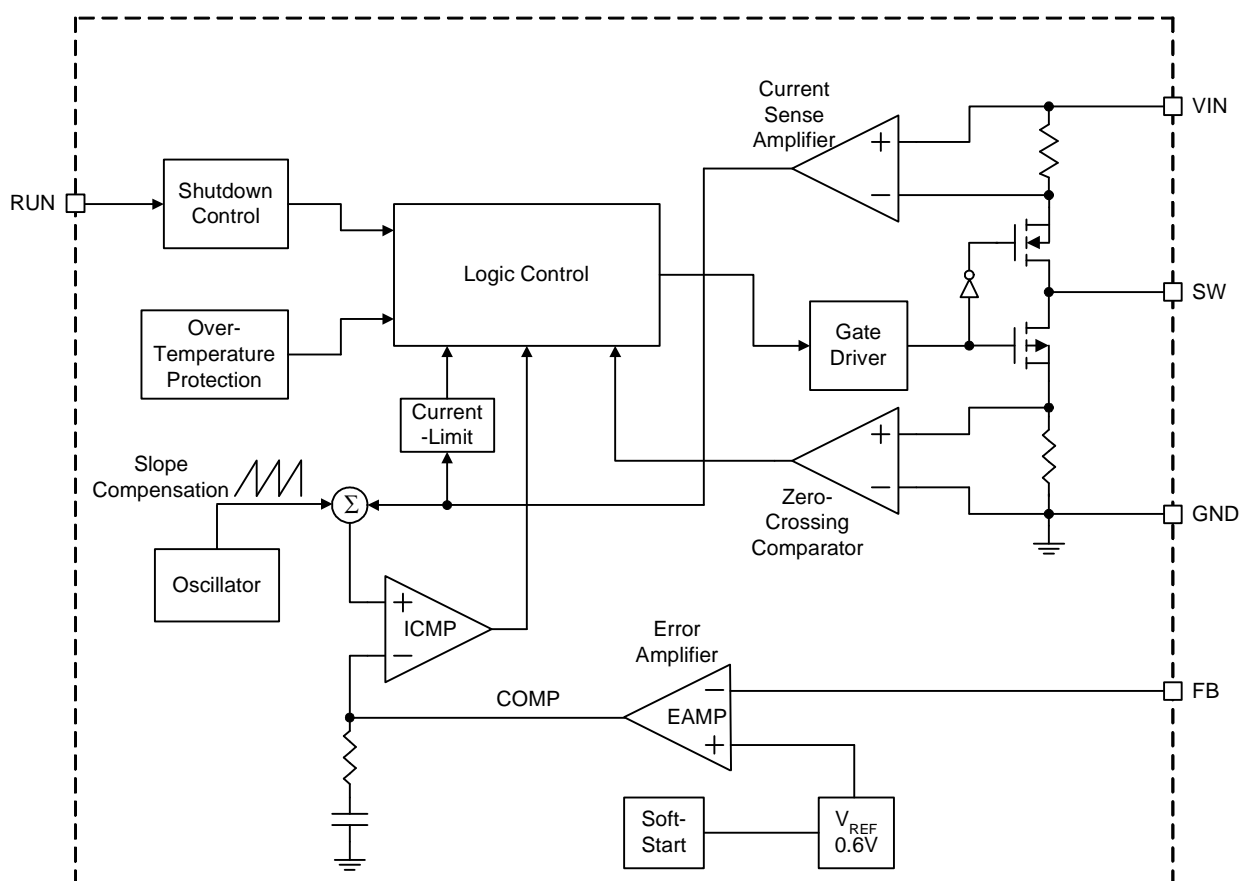
$I_{OUT}=1.2A$ (Peak)

CH1:  $V_{OUT}$ , 20mV/Div, DC offset 1.2V  
CH2:  $I_L$ , 0.5A/Div, DC  
TIME: 500ns/Div

## Pin Description

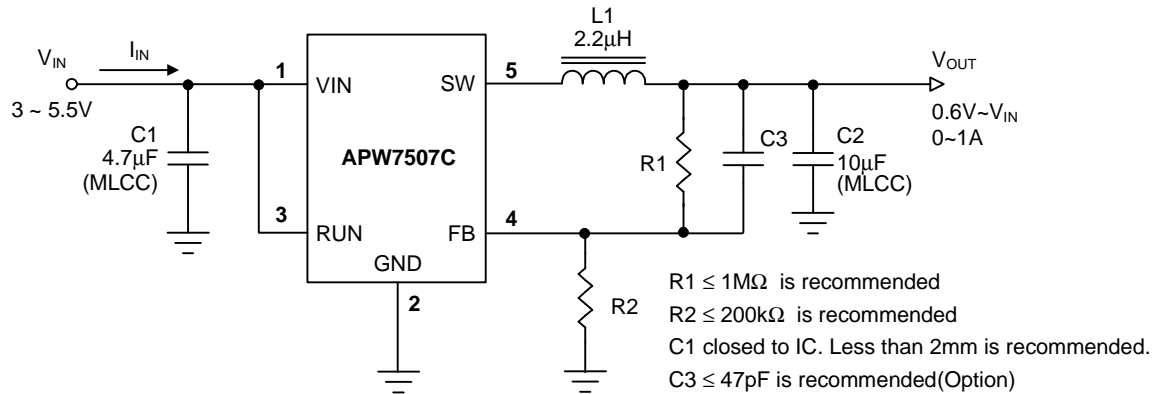
PIN		FUNCTION
NO.	NAME	
1	VIN	Device and Converter Supply Pin. Must be closely decoupled to GND with a 4.7 $\mu$ F or greater ceramic capacitor.
2	GND	Power and Signal Ground.
3	RUN	Enable Control Input. Forcing this pin above 1.0V enables the device. Forcing this pin below 0.4V shuts it down. In shutdown, all functions are disabled to decrease the supply current below 0.5 $\mu$ A. <b>Do not leave RUN pin floating.</b>
4	FB	Feedback Input Pin. The buck regulator senses feedback voltage via FB and regulates the FB voltage at 0.6V. Connecting FB with a resistor-divider from the output sets the output voltage of the buck converter.
5	SW	Switch Node Connected to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFETs switches.

## Block Diagram





## Typical Application Circuit



## Function Description

### Main Control Loop

The APW7507C is a constant frequency, synchronous rectifier and current-mode switching regulator. In normal operation, the internal P-channel power MOSFET is turned on each cycle. The peak inductor current at which ICMP turn off the P-FET is controlled by the voltage on the COMP node, which is the output of the error amplifier (EAMP). An external resistive divider connected between  $V_{OUT}$  and ground allows the EAMP to receive an output feedback voltage  $V_{FB}$  at FB pin. When the load current increases, it causes a slightly decrease in  $V_{FB}$  relative to the 0.6V reference, which in turn causes the COMP voltage to increase until the average inductor current matches the new load current.

### Power-On-Reset (POR)

The APW7507C keeps monitoring the voltage on VIN pin to prevent wrong logic operations which may occur when VIN voltage is not high enough for the internal control circuitry to operate. The VIN POR has a rising threshold of 2.7V (typical) with 0.1V of hysteresis.

### Soft-Start

The APW7507C has a built-in soft-start to control the output voltage rise during start-up. During soft-start, an internal ramp voltage, connected to the one of the positive inputs of the error amplifier, raises up to replace the reference voltage (0.6V typical) until the ramp voltage reaches the reference voltage. Then, the voltage on FB regulated at reference voltage.

### Enable/Shutdown

Driving RUN to the ground places the APW7507C in shutdown mode. When in shutdown, the internal power MOSFETs turn off, all internal circuitry shuts down and the quiescent supply current reduces to 0.5 $\mu$ A maximum.

### Pulse Frequency Modulation Mode (PFM)

The APW7507C is a fixed frequency, peak current mode PWM step-down converter. At light loads, the APW7507C will automatically enter in pulse frequency mode opera-

tion to reduce the dominant switching losses. In PFM operation, the inductor current may reach zero or reverse on each pulse. A zero current comparator turn off the N-FET, forcing DCM operation at light load. These controls get very low quiescent current, help to maintain high efficiency over the complete load range.

### Slope Compensation and Inductor Peak Current

The APW7507C is a peak current mode PWM step down converter. To prevent sub-harmonic oscillations, the APW7507C sense the peak current and add slope compensation to stable the converter. It is accomplished internally by adding a compensating ramp to the inductor current signal at duty cycles in excess of 40%. Normally, this results in a reduction of maximum inductor peak current for duty cycles > 40%. However, the APW7507C uses a special scheme that counteracts this compensating ramp, which allows the maximum inductor peak current to remain unaffected throughout all duty cycles.

### Adaptive Shoot-Through Protection

The gate driver incorporates adaptive shoot-through protection to high-side and low-side MOSFETs from conducting simultaneously and shorting the input supply. This is accomplished by ensuring the falling gate has turned off one MOSFET before the other is allowed to rise.

During turn-off the low-side MOSFET, the internal LGATE voltage is monitored until it is below 1.5V threshold, at which time the UGATE is released to rise after a constant delay. During turn-off the high-side MOSFET, the UGATE voltage is also monitored until it is above 1.5V threshold, at which time the LGATE is released to rise after a constant delay.

## Function Description (Cont.)

### Over-Temperature Protection (OTP)

The over-temperature circuit limits the junction temperature of the APW7507C. When the junction temperature exceeds 150°C, a thermal sensor turns off the both power MOSFETs, allowing the devices to cool. The thermal sensor allows the converters to start a soft-start process and regulate the output voltage again after the junction temperature cools by 30°C. The OTP is designed with a 30°C hysteresis to lower the average Junction Temperature ( $T_J$ ) during continuous thermal overload conditions, increasing the lifetime of the device.

### Short-Circuit Protection

When the output is shortened to the ground, the frequency of the oscillator is reduced to about 210kHz, 1/7 of the nominal frequency. This frequency foldback ensures that the inductor current has more time to decay, thereby preventing runaway. The oscillator's frequency will progressively increase to 1.5MHz when  $V_{FB}$  or  $V_{OUT}$  rises above 0V.

## Application Information

### Input Capacitor Selection

Because buck converters have a pulsating input current, a low ESR input capacitor is required. This results in the best input voltage filtering, minimizing the interference with other circuits caused by high input voltage spikes. Also, the input capacitor must be sufficiently large to stabilize the input voltage during heavy load transients. For good input voltage filtering, usually a 4.7μF input capacitor is sufficient. It can be increased without any limit for better input-voltage filtering. Ceramic capacitors show better performance because of the low ESR value, and they are less sensitive against voltage transients and spikes compared to tantalum capacitors. Place the input capacitor as close as possible to the input and GND pin of the device for better performance.

### Inductor Selection

For high efficiencies, the inductor should have a low DC resistance to minimize conduction losses. Especially at high-switching frequencies, the core material has a higher impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. A reasonable starting point for setting ripple current,  $\Delta I_L$  is 40% of maximum output current. The recommended inductor value can be calculated as below:

$$L \geq \frac{V_{OUT} \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)}{F_{SW} \cdot \Delta I_L}$$

$$I_{L(MAX)} = I_{OUT(MAX)} + 1/2 \times \Delta I_L$$

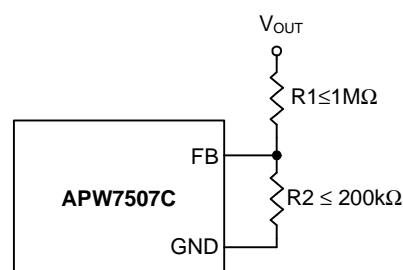
To avoid the saturation of the inductor, the inductor should be rated at least for the maximum output current of the converter plus the inductor ripple current.

### Output Voltage Setting

In the adjustable version, the output voltage is set by a resistive divider. The external resistive divider is connected to the output, allowing remote voltage sensing as

shown in “Typical Application Circuits”. A suggestion of maximum value of R2 is 200kΩ to keep the minimum current that provides enough noise rejection ability through the resistor divider. The output voltage can be calculated as below:

$$V_{OUT} = V_{REF} \cdot \left( 1 + \frac{R1}{R2} \right) = 0.6 \cdot \left( 1 + \frac{R1}{R2} \right)$$

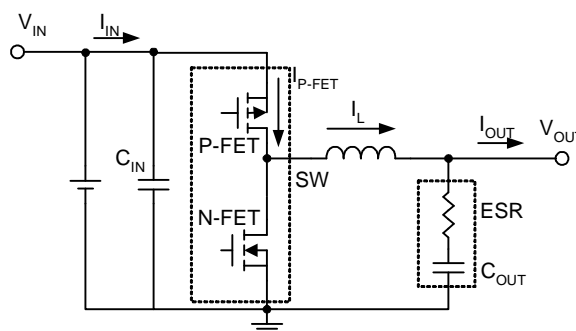


### Output Capacitor Selection

The current-mode control scheme of the APW7507C allows the use of tiny ceramic capacitors. The higher capacitor value provides the good load transients response. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. If required, tantalum capacitors may be used as well. The output ripple is the sum of the voltages across the ESR and the ideal output capacitor.

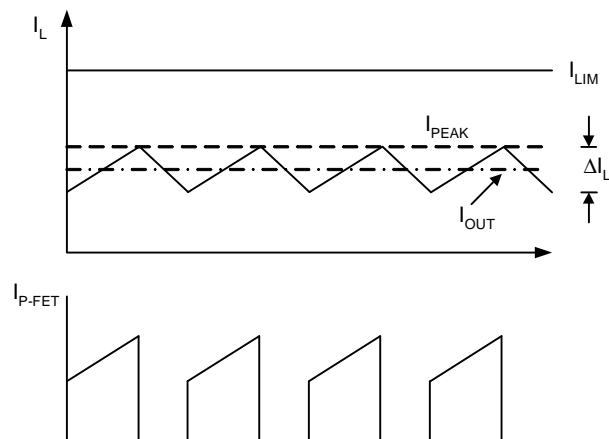
$$\Delta V_{OUT} \cong \frac{V_{OUT} \cdot \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)}{F_{SW} \cdot L} \cdot \left( ESR + \frac{1}{8 \cdot F_{SW} \cdot C_{OUT}} \right)$$

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

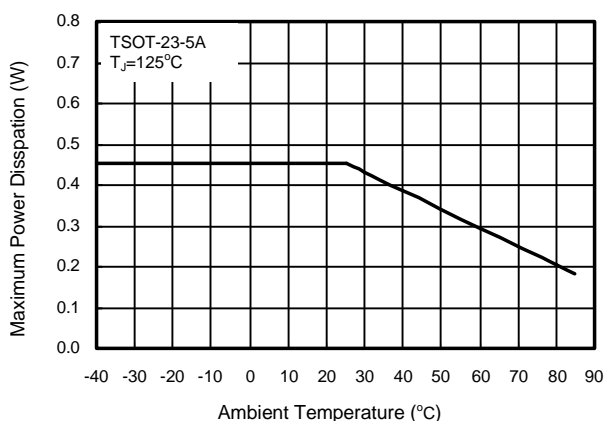


## Application Information (Cont.)

### Output Capacitor Selection (Cont.)



The maximum power dissipation on the device can be shown as follow figure:



### Thermal Consideration

In most applications, the APW7507C does not dissipate much heat due to its high efficiency. But, in applications where the APW7507C is running at high ambient temperature with low supply voltage and high duty cycles, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 150°C, both power switches will be turned off and the SW node will become high impedance.

To avoid the APW7507C from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The power dissipated by the part is approximated:

$$P_D \cong I_{OUT}^2 \times (R_{P-FET} \times D + R_{N-FET} \times (1-D))$$

The temperature rise is given by:

$$T_R = (P_D)(\theta_{JA})$$

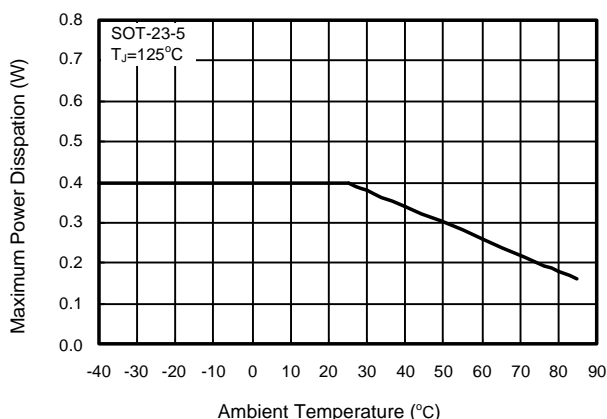
Where  $P_D$  is the power dissipated by the regulator, D is duty cycle of main switch

$$D = V_{OUT}/V_{IN}$$

The  $\theta_{JA}$  is the thermal resistance from the junction of the die to the ambient temperature. The junction temperature,  $T_J$ , is given by:

$$T_J = T_A + T_R$$

Where  $T_A$  is the ambient temperature.



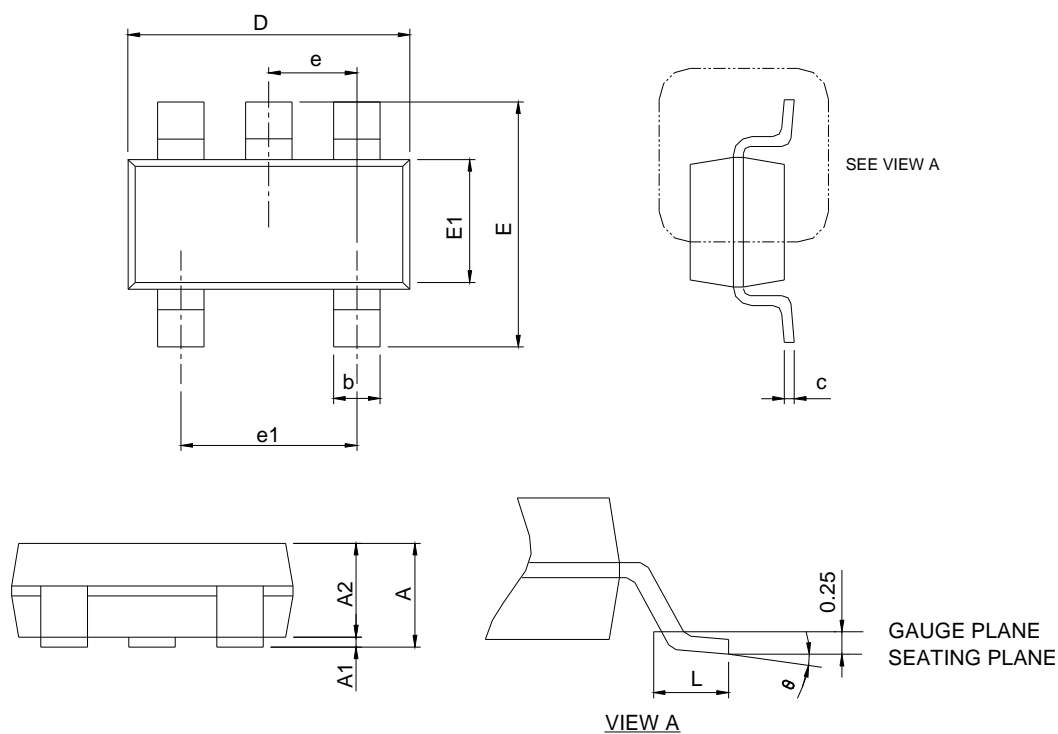
## Layout Consideration

For all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

1. The input capacitor should be placed close to the VIN and GND. Connecting the capacitor and VIN/GND with short and wide trace without any via holes for good input voltage filtering. The distance between VIN/GND to capacitor less than 2mm respectively is recommended.
2. To minimize copper trace connections that can inject noise into the system, the inductor should be placed as close as possible to the SW pin to minimize the noise coupling into other circuits.
3. The output capacitor should be placed close to converter VOUT and GND.
4. Since the feedback pin and network is a high impedance circuit the feedback network should be routed away from the inductor. The feedback pin and feedback network should be shielded with a ground plane or trace to minimize noise coupling into this circuit.
5. A star ground connection or ground plane minimizes ground shifts and noise is recommended.

## Package Information

### TSOT-23-5A



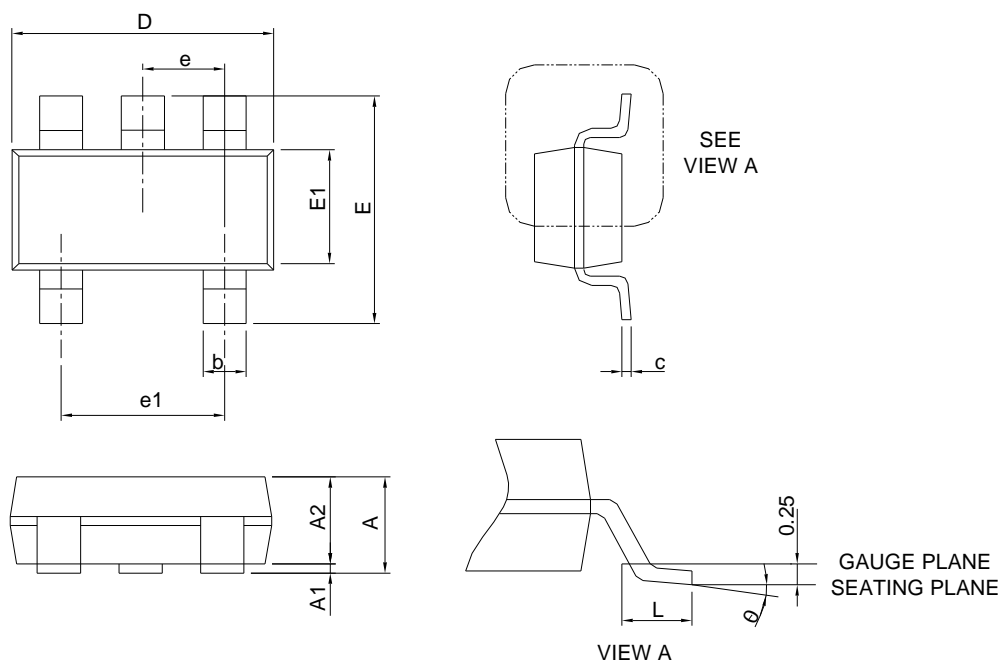
SYMBOL	TSOT-23-5A			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	1.00	0.028	0.039
A1	0.01	0.10	0.000	0.004
A2	0.70	0.90	0.028	0.035
b	0.30	0.50	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.70	3.10	0.106	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.95 BSC		0.037 BSC	
e1	1.90BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
$\theta$	0°	8°	0°	8°

Note : 1. Followed from JEDEC TO-178 AA.

2. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

## Package Information

SOT-23-5



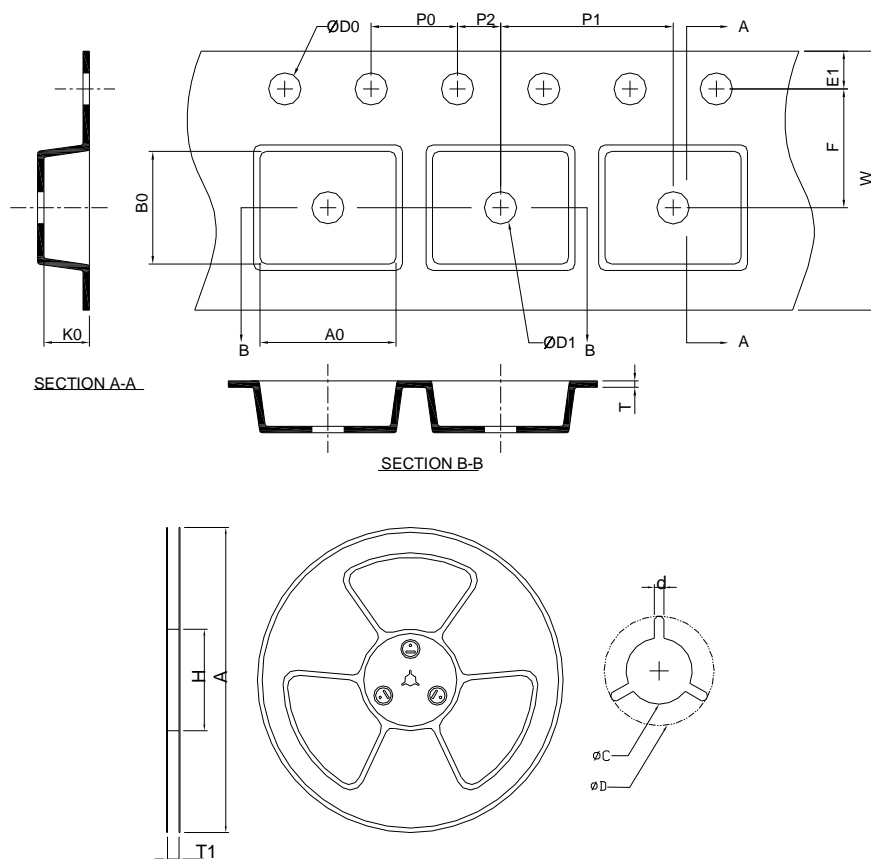
SYMBOL	SOT-23-5			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.45		0.057
A1	0.00	0.15	0.000	0.006
A2	0.90	1.30	0.035	0.051
b	0.30	0.50	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.70	3.10	0.106	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

Note : 1. Follow JEDEC TO-178 AA.

2. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.



## Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TSOT-23-5A	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.0 MIN.	0.6+0.00 -0.40	3.20±0.20	3.10±0.20	1.50±0.20
Application	A	H	T1	C	d	D	W	E1	F
SOT-23-5	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.0 MIN.	0.6+0.00 -0.40	3.20±0.20	3.10±0.20	1.50±0.20

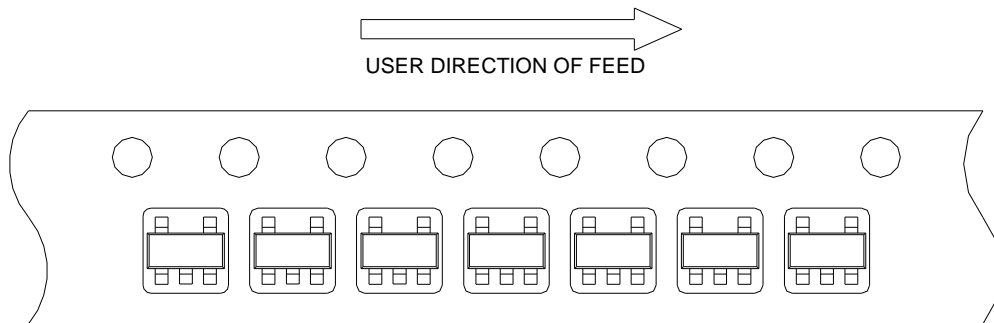
(mm)

## Devices Per Unit

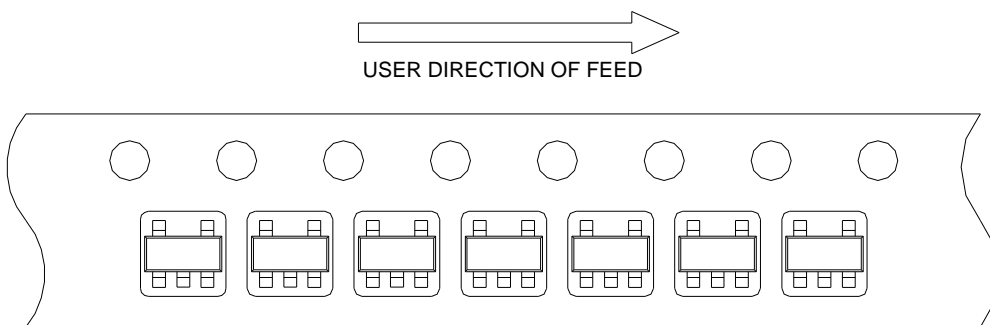
Package Type	Unit	Quantity
TSOT-23-5A	Tape & Reel	3000
SOT-23-5	Tape & Reel	3000

## Taping Direction Information

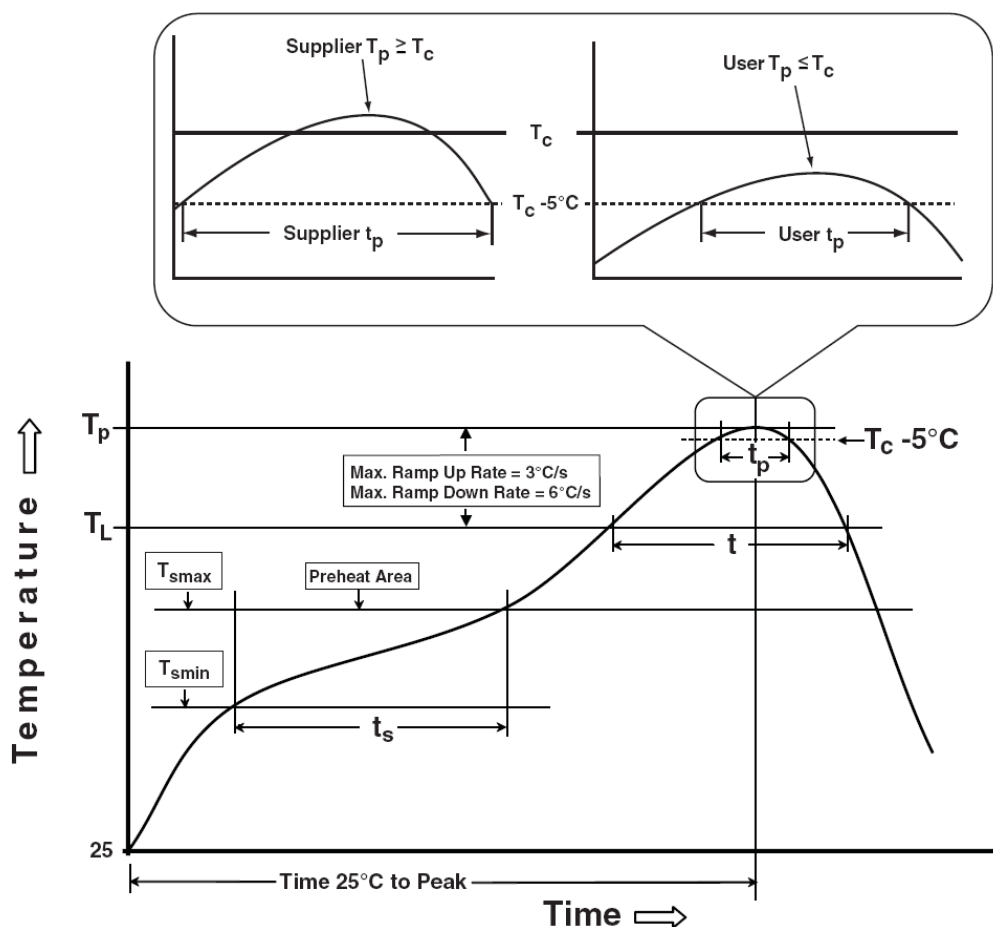
TSOT-23-5A



SOT-23-5



## Classification Profile



## Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
<b>Preheat &amp; Soak</b>		
Temperature min ( $T_{smin}$ )	100 °C	150 °C
Temperature max ( $T_{smax}$ )	150 °C	200 °C
Time ( $T_{smin}$ to $T_{smax}$ ) ( $t_s$ )	60-120 seconds	60-120 seconds
Average ramp-up rate ( $T_{smax}$ to $T_p$ )	3 °C/second max.	3 °C/second max.
Liquidous temperature ( $T_L$ )	183 °C	217 °C
Time at liquidous ( $t_L$ )	60-150 seconds	60-150 seconds
Peak package body Temperature ( $T_p$ )*	See Classification Temp in table 1	See Classification Temp in table 2
Time ( $t_p$ )** within 5°C of the specified classification temperature ( $T_c$ )	20** seconds	30** seconds
Average ramp-down rate ( $T_p$ to $T_{smax}$ )	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature ( $T_p$ ) is defined as a supplier minimum and a user maximum.		
** Tolerance for time at peak profile temperature ( $t_p$ ) is defined as a supplier minimum and a user maximum.		

## Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm <sup>3</sup> <350	Volume mm <sup>3</sup> ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm <sup>3</sup> <350	Volume mm <sup>3</sup> 350-2000	Volume mm <sup>3</sup> >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

## Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ Tj=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≥ 2KV
MM	JESD-22, A115	VMM ≥ 200V
Latch-Up	JESD 78	10ms, 1 <sub>tr</sub> ≥ 100mA

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