The Synchronous Buck Converter with 300mA LDO

Features

- **Wide Input Operating Range: 4.5V~5.5V**
- **Synchronous Buck Regulators for SoC:**
  -Fixed 1.2V
  - 1.2A peak Output Current for Core Power
  - 2MHz Switching Frequency
- **Low-Dropout Linear Regulators for System Power:**
  - Fixed 3.3V, 300mA Output Current with high PSRR
- **Thermal-Overload Protection**
- **Power-OK Indicator after LDO Ready**
- **TDFN2x2-8 Package**
- **Lead Free Green Devices Available (RoHS Compliant)**

Applications

- **IP-Cam**
- **Car Recorder**
- **Security**

General Description

The APW7566A is P-channel low dropout linear regulator and synchronous buck converter which needs input voltage from 4.5 to 5.5V.

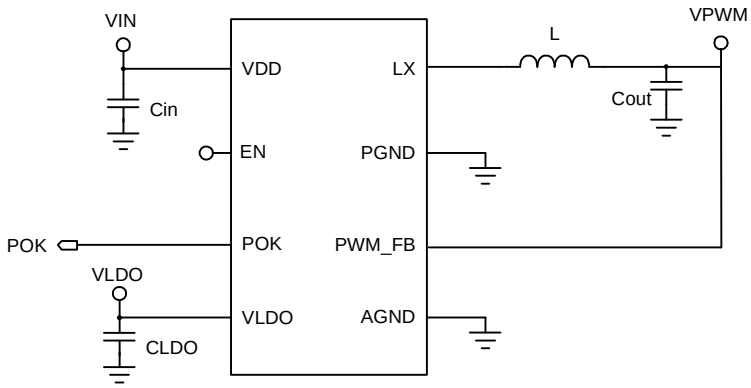
Synchronous buck converter is integrated high side and low side power MOSFET. It is equipped with an automatic PSM/PWM mode operation. At light load, the IC operates in the PSM mode to reduce the switching losses. At heavy load, the IC works in PWM mode.

Low dropout linear regulator delivers current up to 300mA to set output voltage, and it also can work with low ESR ceramic capacitors. Typical dropout voltage is only 240mV at 300mA loading.

The APW7566A is equipped with Power-on-reset, shutdown control, soft start, over-temperature and current-limit into a single package to protect the device against wrong logic control and over-temperature and current over-loads.

The APW7566A available TDFN2x2-8 provides a very compact system solution external components and PCB area.

Simplified Application Circuit



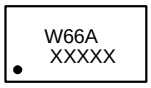
Ordering and Marking Information

APW7566A □□□□-□□□

Lead Free Code
Handling Code
Temperature Range
Package Code
Product Code

Package Code
QB:TQFN2x2- 8
Operating Ambient Temperature Range
I : - 40 to 85°C
Output Voltage Code:
Blank:1.05V
A:1.2V
Handling Code
TR : Tape&Reel
Assembly Material
G:Halogen and Leed Free Device

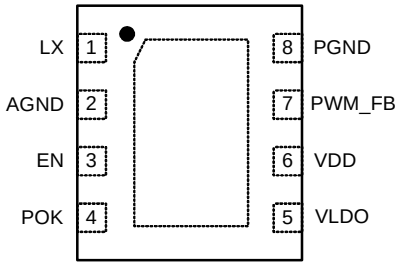
APW7566AQB:



XXXXX -Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Pin Configuration



TDFN2x2-8
(TOP View)

Absolute Maximum Ratings (Note 1)

Symbol	Parameter		Rating	Unit
	VDD,VLDO to GND Voltage		-0.3 ~ 7	V
	LX to GND Voltage	>20ns	-1 ~ (V_{VDD})+0.3	V
		<20ns	-3 ~ (V_{VDD})+3	V
	All other pins		-0.3 ~7	V
	Power Dissipation		Internally Limited	W
T_J	Maximum Junction Temperature		-40 ~ 150	°C
T_{STG}	Storage Temperature		-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)		260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2) TDFN 2x2-8	165	°C/W
θ_{JC}	Junction-to-Case Resistance in free air (Note 3) TDFN 2x2-8	20	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad is soldered directly on the PCB.

Note 3: The case temperature is measured at the center of the exposed pad on the underside.

Recommended Operating Conditions (Note 4)

Symbol	Parameter	Range	Unit
V_{VDD}	VDD Supply Voltage	4.5 ~ 5.5	V
I_{OUT}	Peak Converter Output Current	0 ~ 1.2	A
I_{LDO}	VLDO Output Current	0 ~ 0.3	A
L	Inductor	0.47~2.2	µH
C_{OUT}	VOUT Output Capacitor	4.7~22	µF
C_{LDO}	VLDO Output Capacitor	1~22	µF
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 4: Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over VDD=5V. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7566A			Unit
			Min	Typ	Max	
SUPPLY CURRENT						
I_{VDD}	Quiescent Current	V_{PWM_FB}=0.6V	-	250	300	µA
I_{SD}	Shutdown Quiescent		-	-	5	µA
POWER-ON-RESET (PWM/LDO)						
	POR Threshold		2.3	2.6	2.85	V
	POR Hysteresis		-	0.1	-	V
OUTPUT VOLTAGE (PWM)						
	Output Voltage Accuracy	APW7566A	1.176	1.2	1.224	V
	Line Regulation	I_{OUT}=1mA, V_{VDD}=4.5V to 5.5V	-	-	0.7	%/V
	Load Regulation	I_{PWM}=300mA to 800mA, V_{VDD}= 5V			0.5	%

Electrical Characteristics (Cont.)

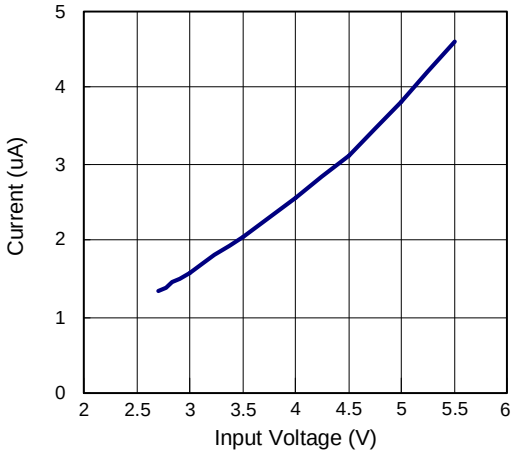
Unless otherwise specified, these specifications apply over VDD=5V. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7566A			Unit
			Min	Typ	Max	
OUTPUT VOLTAGE (LDO)						
	Output Voltage Accuracy	I_{LDO} =1mA~0.3A, T_A=-40~85°C	3.218	3.3	3.382	V
	Line Regulation	I_{LDO}=1mA, V_{VDD}=4.5V to 5.5V	-	-	0.2	%/V
	Load Regulation	I_{LDO}=1mA to 300mA, V_{VDD}=4.5V	-	-	0.9	%
V_{DROP}	Dropout Voltage	I_{LDO}=300mA	-	240	330	mV
PSRR	Power Supply Rejection Ratio	I_{LDO}=50mA, C_{LDO}=2.2µF f=1kHz	-	50	-	dB
	Discharge Resistance		-	1	-	KΩ
POWER MOSFETS(PWM)						
R_{P-FET}	High Side P-MOS $R_{DS(ON)}$	I_{LX}=200mA	-	0.35	0.4	Ω
R_{N-FET}	Low Side N-MOS $R_{DS(ON)}$	I_{LX}=200mA	-	0.35	0.4	Ω
T_D	Dead Time	(Note 5)		10		ns
POWER-OK AND DELAY						
	POK Threshold(POK goes high)	Rising	-	90% V_{LDO}	-	V
	POK Delay Time	The time from V_{LDO}=90%*V_{LDO} to POK goes high	-	16	-	ms
	POK Debounce Time		-	100	-	µs
	POK Pull Low Resistance	V_{POK}=0.1V	-	500	-	Ω
ENABLE AND SHUTDOWN						
	Enable Voltage Threshold	V_{EN} Rising	1	-	-	V
	Shutdown Voltage Threshold	V_{EN} Falling	-	-	0.4	V
PROTECTIONS(PWM)						
	Maximum Inductor Current-Limit		1.5	1.6	-	A
	Soft-Start Time		-	0.7	-	ms
F_{SW}	Switching Frequency	V_{PWM_FB} =0.6V	1.7	2	2.3	MHz
UVP	Under Voltage Protection		-	40	50	%
	Maximum Duty Cycle		-	95	-	%
PROTECTIONS(LDO)						
	Current Limit		330	450	750	mA
PROTECTIONS(PWM, LDO)						
T_{OTP}	Over-Temperature Protection	T_J Rising	-	150	-	°C
	Over-Temperature Protection Hysteresis	T_J Falling	-	30	-	°C

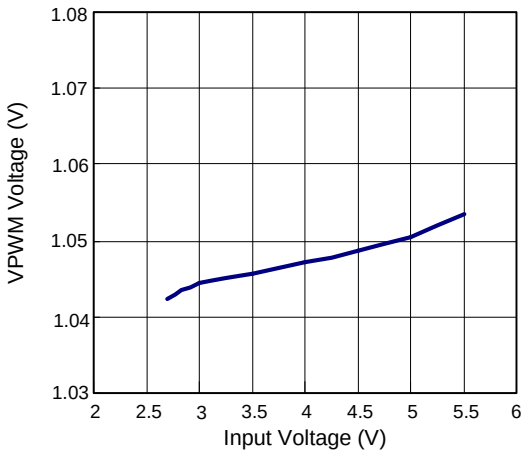
Note 5: Guaranteed by design.

Typical Operating Characteristics

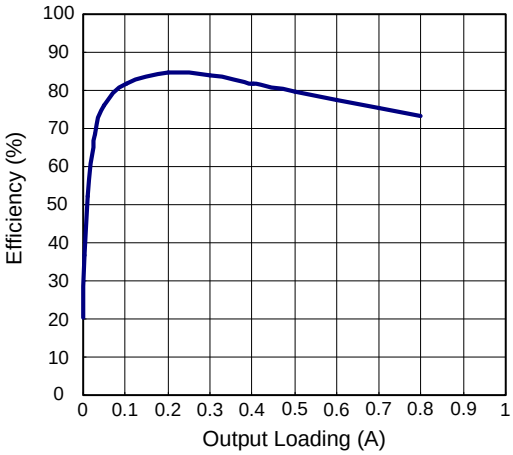
Shutdown Current VS Input Voltage



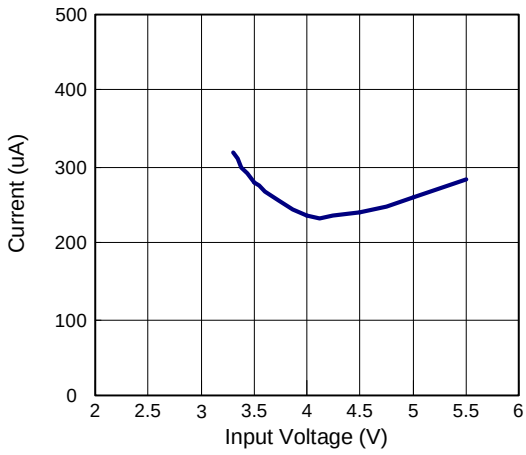
VPWM Voltage VS Input Volatge



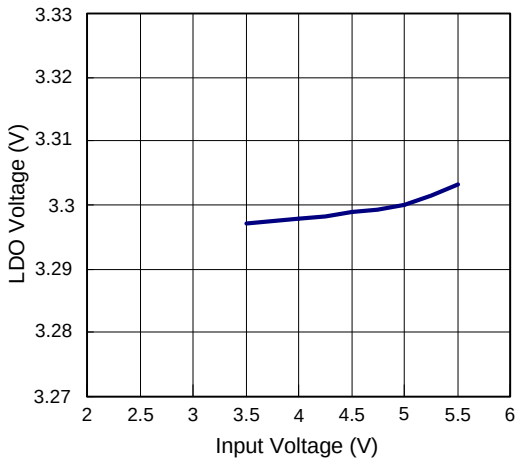
Efficiency VS Input Voltage



No Switch Current VS Input Voltage

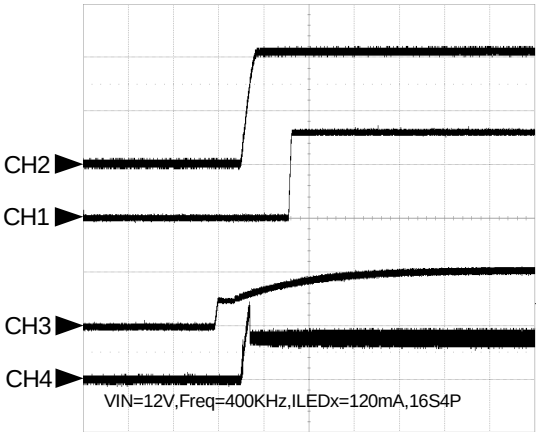


LDO Voltage VS Input Voltage



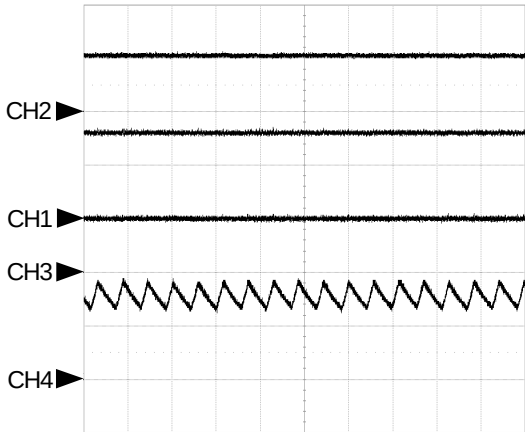
Operating Waveforms

Power on VIN – Loading=0.8A



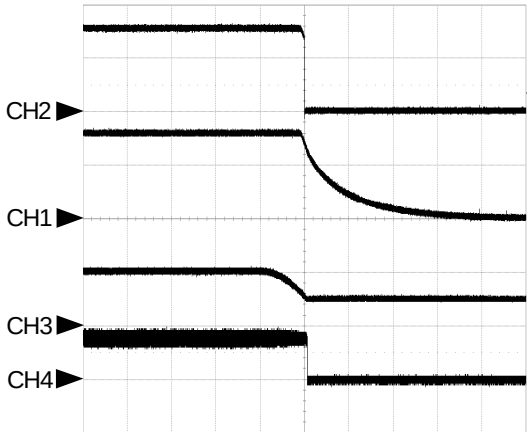
CH1:V_{LDO}-50V/div
CH2:V_{PWM}-500mV/div
CH3:V_{IN}-5V/div
CH4:I_L-1A/div
Time:2ms/div

Normal Operation – Loading=0.8A



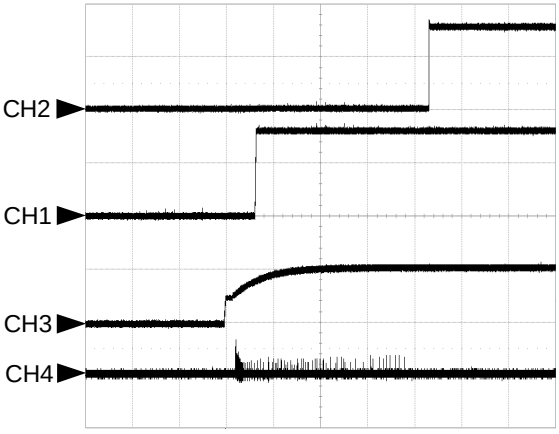
CH1:V_{LDO}-2V/div
CH2:V_{PWM}-1V/div
CH3:V_{IN}-5V/div
CH4:I_L-500mA/div
Time:1us/div

Power on VIN – Loading=0.8A



CH1:V_{POK}-2V/div
CH2:V_{LDO}-2V/div
CH3:V_{IN}-5V/div
CH4:I_L-1A/div
Time:5ms/div

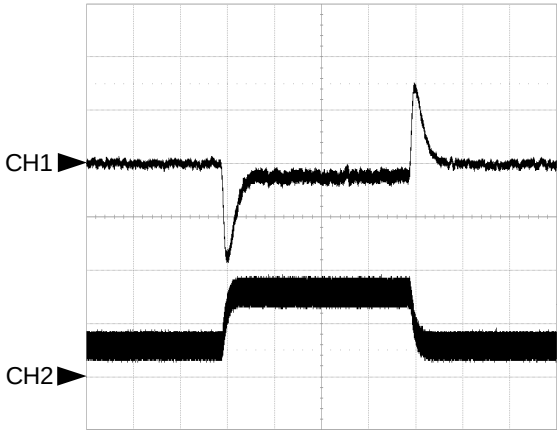
Power on VIN - POK



CH1:V_{LDO}-2V/div
CH2:V_{POK}-2V/div
CH3:V_{VIN}-5V/div
CH4:I_L-200mA/div
Time:5ms/div

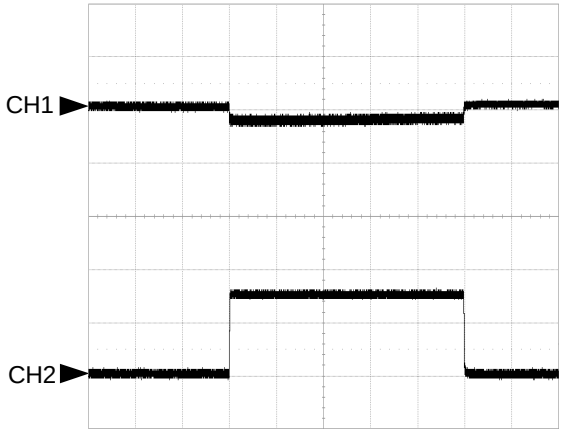
Operating Waveforms

Load Transient
0.3A to 0.8A to 0.3A



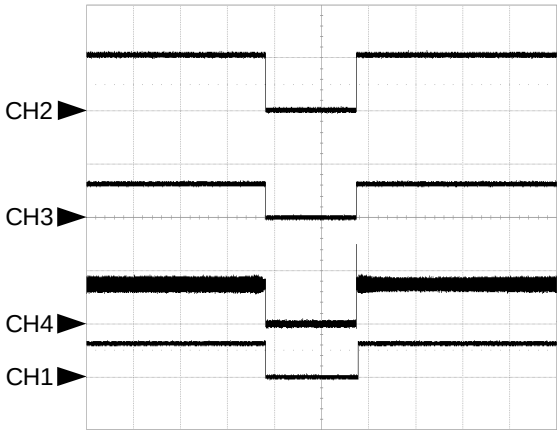
CH1:V_{PWM}-20mV/div
CH2:I_L-500mA/div
Time:50us/div

LDO Load Transient - 0A to 0.3A to 0A



CH1:V_{LDO}-100mV/div
CH2:I_{LDO}-200mA/div
Time:2ms/div

OTP – Loading=0.8A

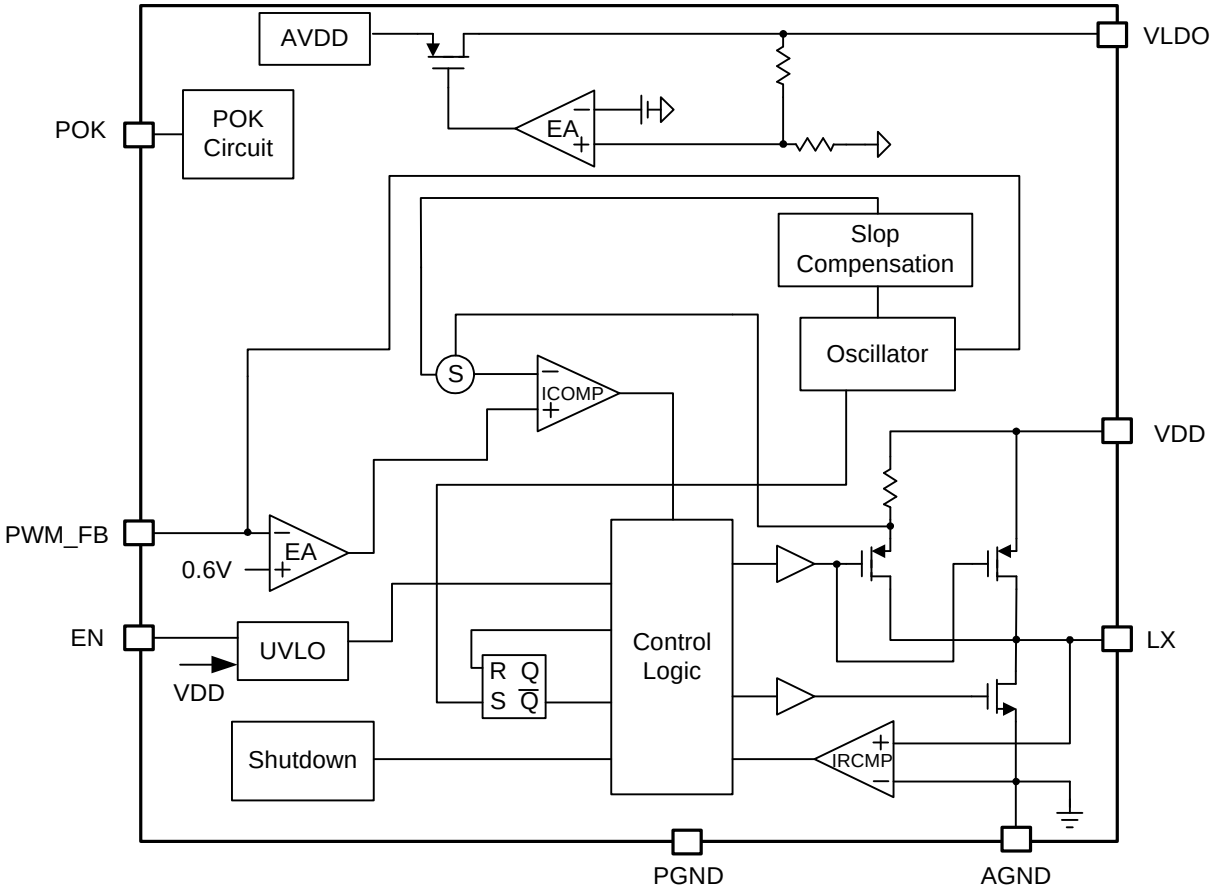


CH1:V_{POK}-5V/div
CH2:V_{PWM}-1V/div
CH3:V_{LDO}-5V/Div
CH4:I_L-1A/div
Time:500ms/div

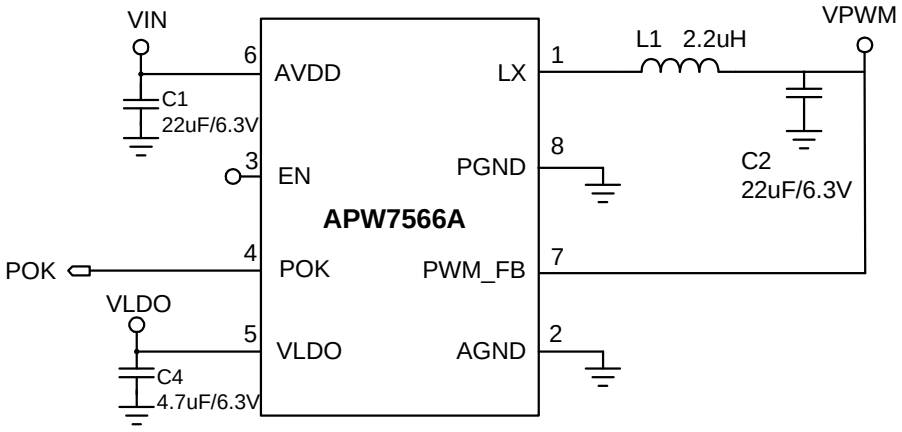
Pin Description

PIN		Function
NO.	Name	
1	LX	Power Switching Output. The LX is the junction of the high-side and low-side power MOSFET to supply power to the output LC filter.
2	AGND	Connect this pin with large copper area to negative terminals of the input and output capacitors.
3	EN	Enable Control Input. Forcing this pin above 1.0V enables the device, or forcing this pin below 0.4V to shut it down. In shutdown, all functions are disabled. This pin is floating as the device will be enabling.
4	POK	Power Good function. Its monitor VLDO output voltage.
5	VLDO	Regulator Output Pin.
6	VDD	Power Input. Connect a ceramic bypass capacitor from VDD to GND. VDD is supply VLDO output power.
7	PWM_FB	Output Feedback Input. The APW7566A senses the feedback voltage via PWM_FB and regulates the voltage at 1.05V/1.2V.
8	PGND	Connect this pin with large copper area to negative terminals of the input and output capacitors.

Block Diagram



Typical Application Circuit



***Recommend:**

The C1 capacitor must be close to the IC side less than 3mm.

Function Description

Power-On-Reset (POR)

The APW7566A monitors the input voltage to prevent wrong logic control. The POR function initiates a soft-start process after input voltage exceeds its rising POR threshold during power on. The POR function also shuts off the output when the input voltage falls below its falling threshold.

Internal Soft-Start

An internal soft-start function controls rising rate of the output voltage to limit the surge current at start-up.

Current-Limit protection

The buck converter monitors the output current, flows through the high-side and low-side power MOSFETs, and limits the current peak at current-limit level to prevent the IC from damaging during overload, short-circuit conditions.

Thermal Shutdown

A thermal shutdown circuit limits the junction temperature of APW7566A. When the junction temperature exceeds +150°C, a thermal sensor turns off the output PMOS, allowing the device to cool down. The regulator regulates the output against through initiation of a new soft-start cycle after the junction temperature cools by 150°C. The thermal shutdown is designed with a 30°C hysteresis to lower the average junction temperature during continuous thermal overload conditions, extending lifetime of the device.

Power OK Indicator

POK is actively held low in shutdown and soft-start status. In the soft-start process, the POK is an open-drain, after Converter is ready, the POK is released.

Power Sequence

The APW7566A provides difference power Sequences to choose for different applications. Figure 1 show the timing diagram of different version of the APW7566A.

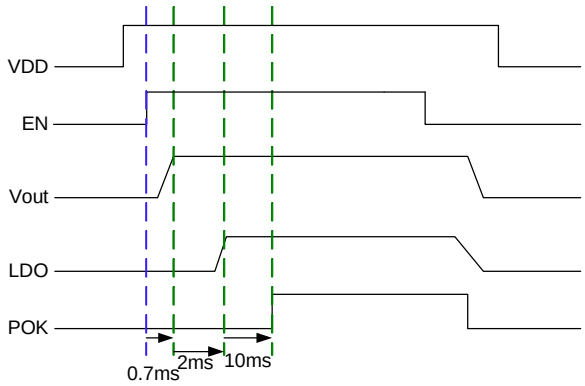


Figure 1. Power Sequence

Under Voltage Protection

The APW7566A had UVP function. In the process of operation, if a short-circuit occurs, the output voltage will drop quickly. When load current is bigger than current limit threshold value, the output voltage will fall out of the required regulation range. If a load step is strong enough to pull the output voltage lower than the under voltage threshold (40% of normal output voltage), APW7566A shuts down the output gradually and latches off both high and low side MOSFETs.

Application Information

Input Capacitor Selection

The buck converters in APW7566A have a pulsating input current; a low ESR input capacitor is required. This results in the best input voltage filtering, minimizing the interference with other circuits caused by high input voltage spikes. Also, the input capacitor must be sufficiently large to stabilize the input voltage during heavy load transients. For good input voltage filtering, usually a 22μF input capacitor is sufficient. It can be increased without any limit for better input-voltage filtering. Ceramic capacitors show better performance because of the low ESR value, and they are less sensitive against voltage transients and spikes compared to tantalum capacitors. Place the input capacitor as close as possible to the VDD to GND pin of the device for better performance.

Inductor Selection

For high efficiencies, the inductor should have a low DC resistance to minimize conduction losses. Especially at high-switching frequencies, the core material has a higher impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. A reasonable starting point for setting ripple current, ΔI_L, is 40% of maximum output current. The recommended inductor value can be calculated as below:

$$L \geq \frac{V_{OUT}(1-\frac{V_{OUT}}{V_{IN}})}{F_{SW} \cdot \Delta I_L}$$

$$I_{L(MAX)}=I_{OUT(MAX)}+1/2x\Delta IL$$

To avoid the saturation of the inductor, the inductor should be rated at least for the maximum output current of the converter plus the inductor ripple current.

Output Capacitor

The buck converter in APW7566A allows the use of tiny ceramic capacitors. The higher capacitor value provides the good load transients response. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. If required, tantalum capacitors may be used as well. The output ripple is the sum of the voltages across the ESR and the ideal output capacitor.

$$\Delta V_{OUT} \cong \frac{V_{OUT} \cdot (1-\frac{V_{OUT}}{V_{IN}})}{F_{SW} \cdot L}(ESR + \frac{1}{8 \cdot F_{SW} \cdot C_{OUT}})$$

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size. The LDO regulator in APW7566A needs a proper output capacitor to maintain circuit stability and improve transient response over temperature and current. In order to insure the circuit stability, the proper output capacitor value should be larger than 4.7μF. With X5R and X7R dielectrics, 4.7μF is sufficient at all operating temperatures. Large output capacitor value can reduce noise and improve load-transient response and PSRR.

Application Information

Layout Consideration

The layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

1. The input capacitor should be placed close to the VDD and GND. Connecting the capacitor and VDD to GND with short and wide trace without any via holes for good input voltage filtering. The distance between VDD to GND to capacitor less than 2mm respectively is recommended.
2. To minimize copper trace connections that can inject noise into the system, the inductor should be placed as close as possible to the LX pin to minimize the noise coupling into other circuits.
3. The output capacitor should be place closed to LX and GND.
4. Since the feedback pin and network is a high impedance circuit the feedback network should be routed away from the inductor. The feedback pin and feedback network should be shielded with a ground plane or trace to minimize noise coupling into this circuit.

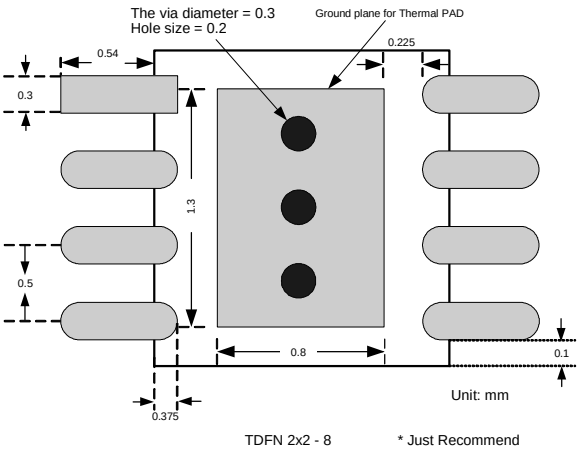
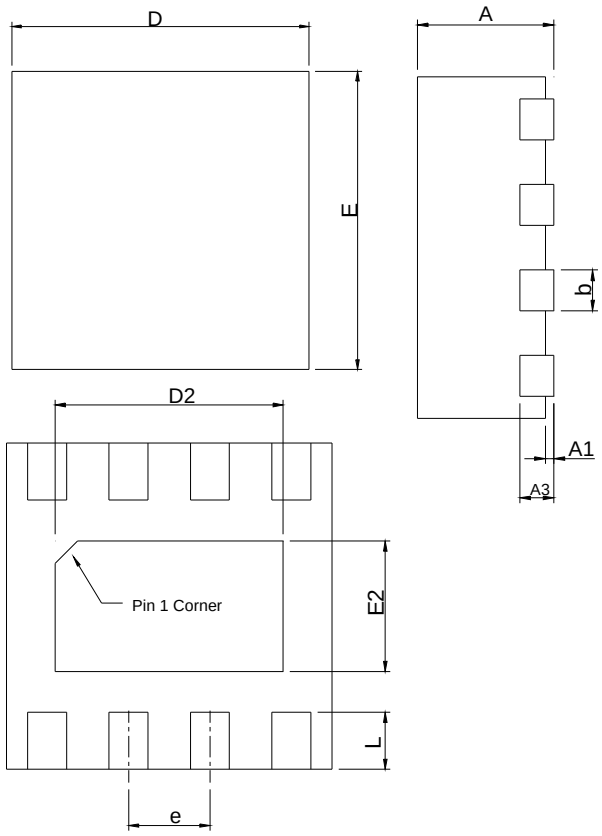


Figure2. Recommended Minimum Footprint

Package Information

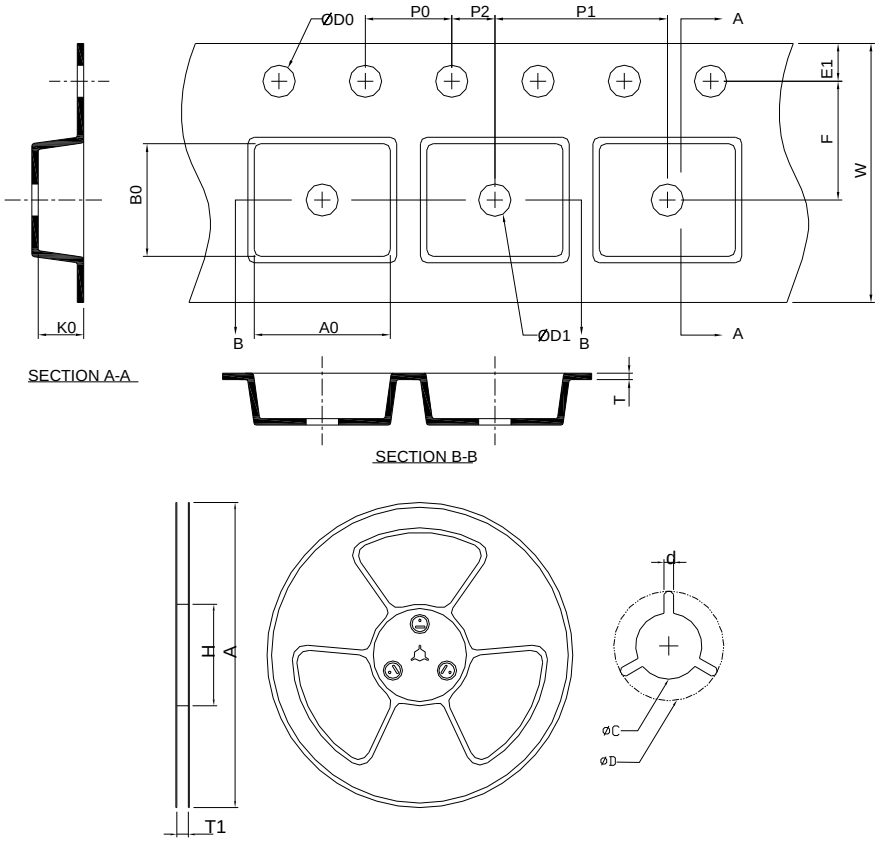
TDFN2x2-8



SYMBOL	TDFN2x2-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	1.90	2.10	0.075	0.083
D2	1.00	1.60	0.039	0.063
E	1.90	2.10	0.075	0.083
E2	0.60	1.00	0.024	0.039
e	0.50 BSC		0.020 BSC	
L	0.30	0.45	0.012	0.018

Note : 1. Follow from JEDEC MO-229 WCCD-3.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TDFN2x2-8	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.20	1.75±0.10	3.50±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.4	2.35 MIN	2.35 MIN	1.00±0.20

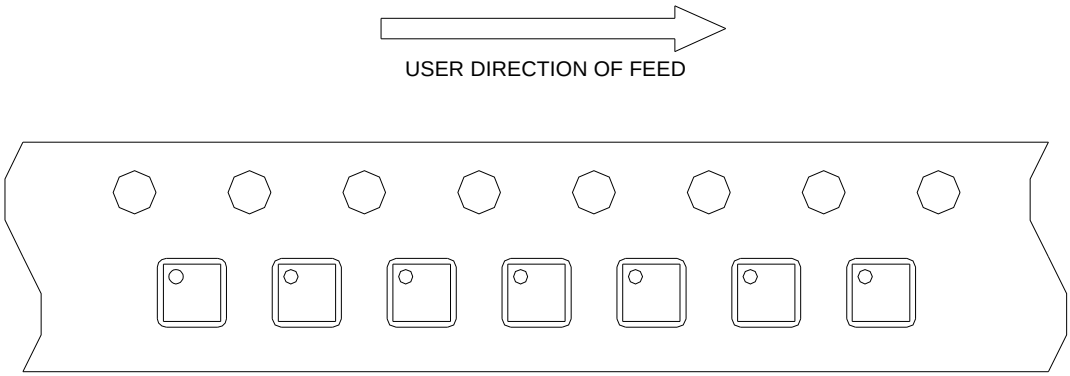
(mm)

Devices Per Unit

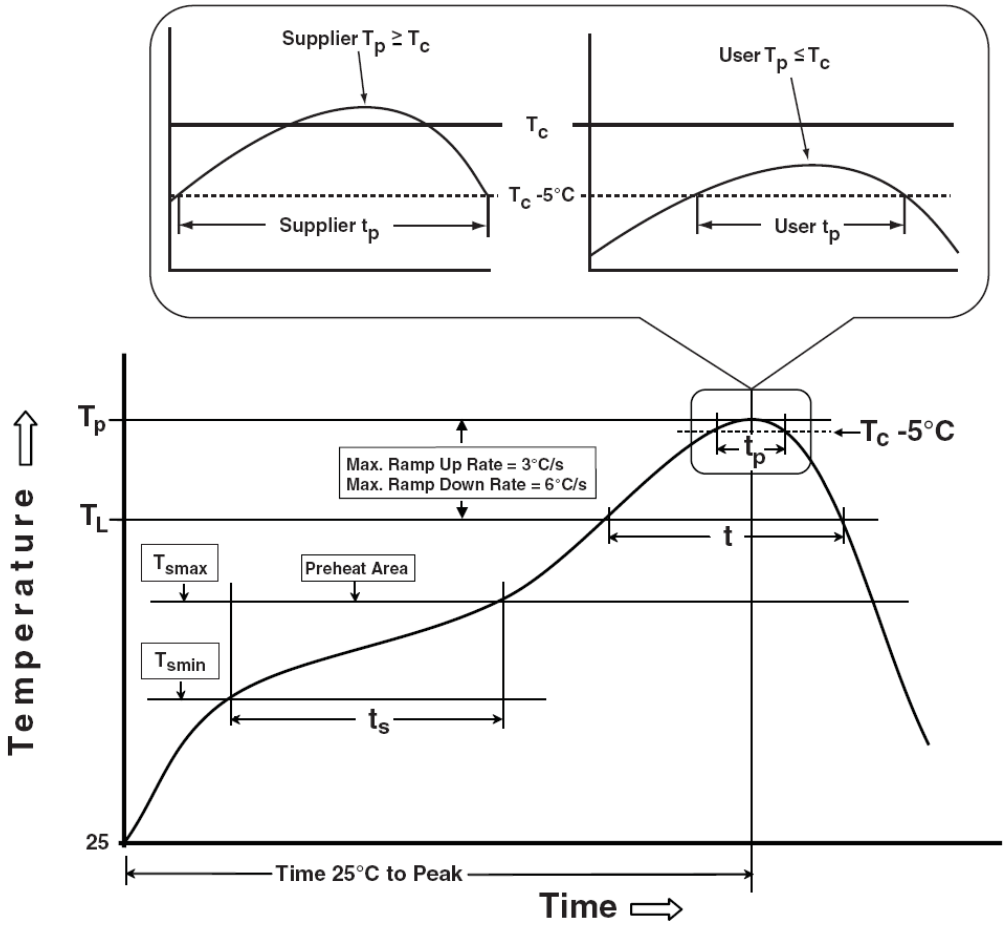
Package Type	Unit	Quantity
TDFN2x2-8	Tape & Reel	3000

Taping Direction Information

TDFN2x2-8



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ 125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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