

Features

■ SuperCap Charger

- **Linear SuperCap Charger**
- **High Charge Current up to 640mA**
- **3.9V-6V Input Operating Voltage Range**
- **Autonomous Charging with or without Host Management**
 - SuperCap Charge Enable
 - Charge Current Profile Limits Inrush Current
 - Internal Cell Auto Balance
- **High Accuracy**
 - $\pm 0.5\%$ Charge Voltage Regulation
 - $\pm 10\%$ Charge Current Regulation
 - $\pm 7.5\%$ Input Current Regulation
- **Safety**
 - Thermal Shutdown
 - Input Over-Voltage Protection
 - Input Over-Current Protection

■ Voltage Rail

- **Provide 4 Buck Single Phase PWM Converters**
 - DC1: 0.6V - 1.5V at 2.5A
 - DC2: 0.6V - 3.3V at 1.5A
 - DC3: 0.6V - 3.3V at 1A
 - DC4: 0.6V - 3.3V at 1.5A
- **Provide 3 LDO Output**
 - RTCLDO 1.5V-3.05V, 10mA
 - LDO1 0.6V-3.3V, 150mA, Reference = 0.6V
 - LDO2 1.5V-3.05V, 300mA, Controlled by I²C
- **TQFN 5x5-40 Package**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **DVR**

General Description

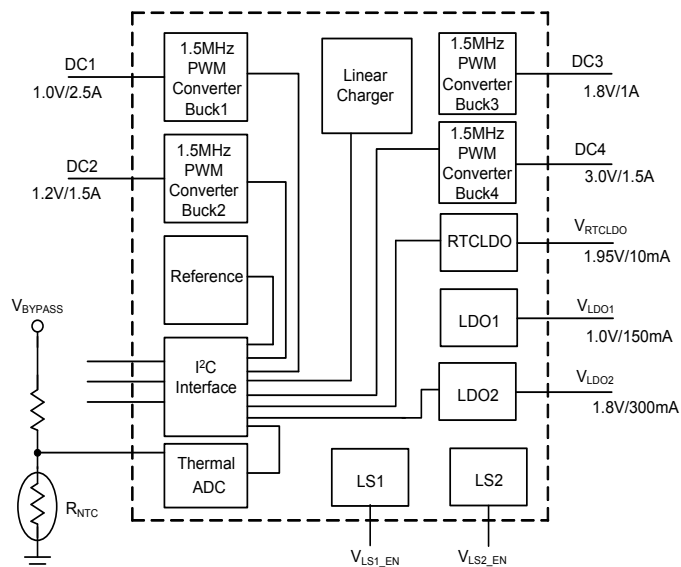
The APW7702 is a Power Management IC (PMIC) with a super capacitor charger system designed to provide complete Power Management solution for the driving video recorder (DVR) applications. The IC operates from a single supply voltage of 3.9V to 5.5V allowing it to be used in Adapter/USB. The APW7702 is designed to provide maximum number of regulators in the smallest available cost effective package. Included in the IC are: One linear supercap charger; Four sync. Buck converters for DC1 ~ DC4; Three LDOs with one for RTC application, and Two Load Switch Enable Signal Control for external load switches application.

For the Bucks, the IC is equipped with all the standard protection features such as current limit, over voltage and internal under voltage lock out protection as well as thermal shutdown.

The serial interface is an I²C communication interface which allows supply sequencing as well as controlled margining of ramp up and ramp down of all supplies to optimize battery power consumption. The I²C interface also allows for adjustability of VRs' voltage. Also, the power sequenc is defined by strobes and delay times under I²C Control.

The device is available in a 40-pin, 5x5 mm² thin QFN package for best thermal performance while optimizing the cost.

Simplified Application Circuit

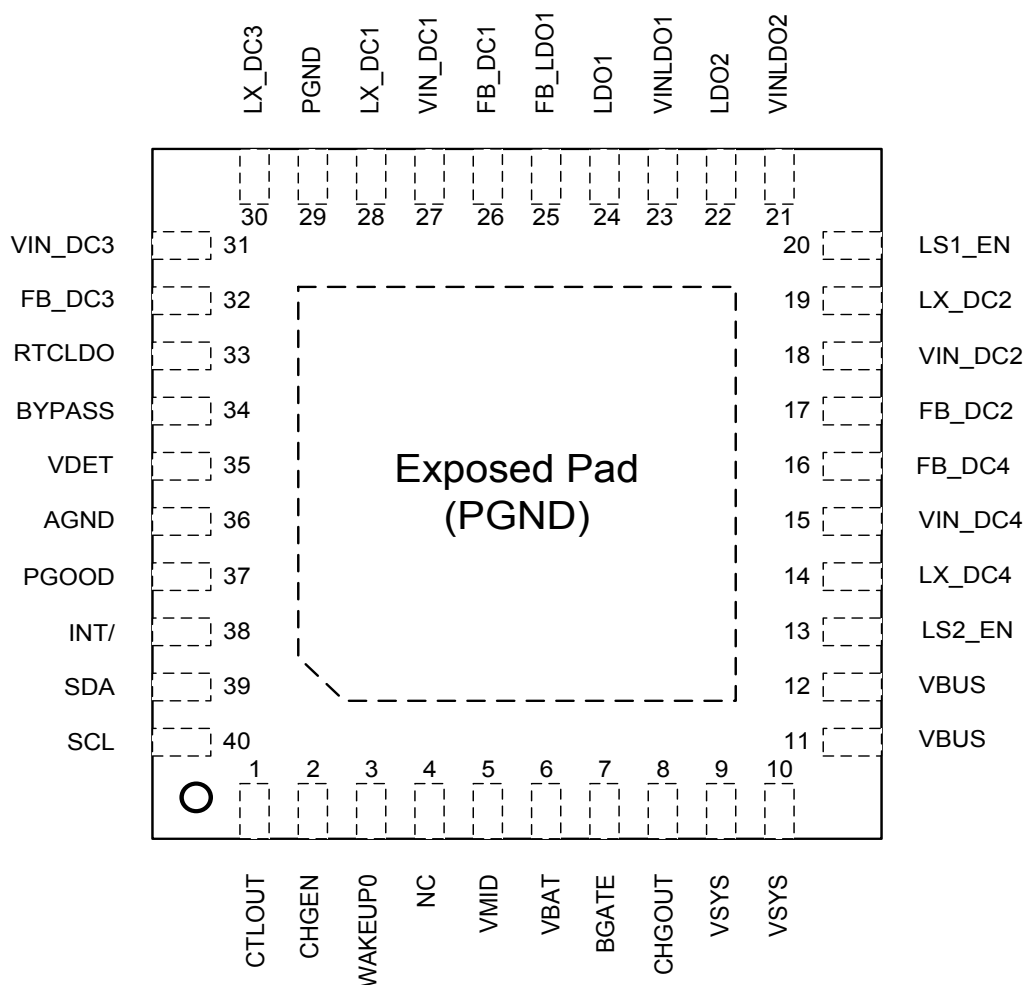


Ordering and Marking Information

APW7702 □□-□□□ Assembly Material Handling Code Temperature- Range Package Code	Package Code QB: TQFN5x5-40 Operating Ambient Temperature Range I : -40 to 85°C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW7702 QB : APW7702 XXXXX XXXXX - Date Code	

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldering operations. ANPEC lead-free products meet or exceed the leadfree requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

Pin Configuration



Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{VBUS}	VBUS to GND Voltage	-0.3 ~ 20	V
$V_{V_{SYS}}$	VSYS to GND Voltage	-0.3 ~ 6.5	V
	VIN_DC1, VIN_DC2, VIN_DC3, VIN_DC4, VINLDO1, VINLDO2, LS1_EN, LS2_EN to GND Voltage	-0.3 ~ 6.5	V
	LX_DC1, LX_DC2, LX_DC3, LX_DC4 to GND Voltage	-0.3 ~ 6.5	V
	FB_DC1, FB_DC2, FB_DC3, FB_DC4, RTCLDO, LDO1, LDO2, FB_LDO1 to GND Voltage	-0.3 ~ 6.5	V
	All other pins to GND Voltage	-0.3 ~ 6.5	V
	PGND to AGND	-0.3 ~ 0.3	V
T_J	Maximum Junction Temperature	-40 ~ 150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)	260	°C

Note1: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	30	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of TQFN5x5-40 is soldered directly on the PCB.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{VBUS}	USB/Adapter Input Voltage	3.9~5.5	V
V_{SUPCAP}	SuperCap Charge Voltage	4.08~5.424	V
V_{DC1}	Buck1 Output Voltage	0.6~1.5	V
I_{DC1}	Buck1 Output Current	~2.5	A
V_{DC2}	Buck2 Output Voltage	0.6~3.3	V
I_{DC2}	Buck2 Output Current	~1.5	A
V_{DC3}	Buck3 Output Voltage	0.6~3.3	V
I_{DC3}	Buck3 Output Current	~1	A
V_{DC4}	Buck4 Output Voltage	0.6~3.3	V
I_{DC4}	Buck4 Output Current	~1.5	A
V_{RTCLDO}	RTCLDO Output Voltage	1.5 ~ 3.05	V
I_{RTCLDO}	RTCLDO Output Current	~10	mA
V_{LDO1}	LDO1 Output Voltage	0.6~3.3	V
I_{LDO1}	LDO1 Output Current	~150	mA
V_{LDO2}	LDO2 Output Voltage	1.5~3.3	V
I_{LDO2}	LDO2 Output Current	~300	mA
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3 : Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over $V_{BUS} < V_{ACOV}$, and $T_A = -40$ to 85°C . Typical values are at $T_A = 25^\circ\text{C}$.

• SuperCap Charger

Symbol	Parameter	Test Conditions	APW7702			Unit
			Min	Typ	Max	
QUIESCENT CURRENTS						
I _{BUS}	Input Supply Current (VBUS)	V _{BUS} = 5.2V, RTCLDO enabled, All other rails disable. No Load, Charge Diabie, T _A = 25°C	-	600	-	μA
VBUS						
V _{BUS}	USB Input Voltage Range	Valid range for charging	3.9	-	6	V
V _{BUS_POR}	USB Valid	V _{BUS} Rising	3.4	3.6	3.8	V
V _{BUS_POR_HYS}	USB Valid Hysteresis	V _{BUS} Falling	-	200	-	mV
V _{ACOV}	USB Over Voltage Rising Threshold	V _{BUS} rising	6	6.2	6.4	V
V _{ACOV_HYS}	USB Over Voltage Falling Hysteresis	V _{BUS} falling	-	200	-	mV
POWER PATH MANAGEMENT						
R _{ON(RBFET)}	Internal Top Reverse Blocking MOSFET On-Resistance Between USB and SYSTEM	Measured between V _{BUS} and V _{SYS} , V _{BUS} = 5.2V, I _{SYS} =1A	-	100	-	mΩ
R _{ON(HSET)}	Internal High Side MOSFET On-Resistance Between SYSTEM and CHGOUT	Measured between HS D-S terminal voltage, V _{SYS} = 5.1V, I _{DS} =256mA	-	50	-	mΩ
V _{FWD}	Forward Voltage In Supplement Mode	V _{SYS} –V _{SUPCAP}	-	60	-	mV
BYPASS LDO						
V _{BYPASS}	BYPASS Output Voltage	V _{VBUS} =5V, I _{BYPASS} =0mA	-	4.0	-	V
		V _{VBUS} =5V, I _{BYPASS} =20mA	3.0	-	4.5	V
I _{BYPASS}	BYPASS Output Current	V _{VBUS} =5V, BYPASS Short to GND	-	40	-	mA
SUPERCAP CHARGER						
V _{SUPCAP_ACC}	Charge Voltage Regulation Accuracy	V _{SUPCAP} =5.04V	-0.5	-	0.5	%
	Charge Voltage Regulation Range	I ² C selectable; Default 5.04V	4.08	-	5.424	V
	Charge Voltage Regulation Accuracy		-1	-	1	%
	V _{SUPCAP} Input Voltage Range	VBUS No Connected	2.7	-	5.424	V
I _{CHG_ACC}	Charge Current Regulation Accuracy	V _{SUPCAP} = 5.04V, I _{CHG} = 255mA, T _A = 25°C	-10	-	10	%
	Supercap Charge Current Range, V _{CHGOUT} > V _{SUPCAP} , V _{BUS} = 5.2V	ICHG[2:0]=000	-	100	-	mA
		ICHG[2:0]=001 (Default)	-	255	-	
		ICHG[2:0]=010	-	440	-	
		ICHG[2:0]=011	-	640	-	
V _{MID}	Internal Auto-balance Output Voltage	V _{SUPCAP} = 5.04V	-	2.52	-	V
I _{MID_SOURCE}	V _{MID} Current Sourcing Capability		-	1	-	A
I _{MID_SINK}	V _{MID} Current Sinking Capability		-	1	-	A

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over $V_{BUS} < V_{ACOV}$, and $T_A = -40$ to 85°C . Typical values are at $T_A = 25^{\circ}\text{C}$.

• SuperCap Charger (Cont.)

Symbol	Parameter	Test Conditions	APW7702			Unit
			Min	Typ	Max	
INPUT CURRENT REGULATION						
	Input Current Limit	IVBUS [2:0]=000	50	-	150	mA
		IVBUS [2:0]=001	400	-	600	mA
		IVBUS [2:0]=010	750	-	900	mA
		IVBUS [2:0]=011	1080	-	1300	mA
		IVBUS [2:0]=100	1410	-	1700	mA
		IVBUS [2:0]=101	1740	-	2100	mA
		IVBUS [2:0]=110	2000	-	2500	mA
THERMAL SHUTDOWN						
T _{SHUT}	Thermal Shutdown Rising Temperature	Temperature increasing	-	160	-	°C
T _{SHUT_HYS}	Thermal Shutdown Hysteresis		-	30	-	°C
I/O PIN CHARACTERISTICS (SDA, SCL, /INT, CSN, CSP, WAKEUP0, CHGEN, CLTOUT, PGOOD)						
V _{IL}	Input Low Voltage	Include SDA, SCL, /INT, WAKEUP0, CHGEN, CLTOUT Input Pins	-	-	0.4	V
V _{IH}	Input High Voltage	Include SDA, SCL, /INT, WAKEUP0, CHGEN, CLTOUT Input Pins	1.5	-	-	V
V _{O_LOW}	Output Low Saturation Voltage	Sink current=5mA Include PGOOD, /INT Pins	-	-	0.4	V
I _{BIAS_IO}	High Level Leakage Current	Pull up to 5V, Include SDA, SCL, Input Pins	-	-	1	µA
		Pull up to 5V, Include WAKEUP0, CHGEN, CTLOUT Pins	-	50	-	µA
		Pull up to 5V, Include PGOOD and /INT Input Pins	-	-	0.2	µA
T _{INT_L}	/INT Pulled Low Time	/INT Pulled Low Time When Fault Event still Exists. The Period is 1ms	-	10	-	µs
f _{SCL}	SCL Clock Frequency		-	-	400	kHz
V _{DET_FALL}	VDET Falling Threshold	PGOOD Signal Pulled Low	0.98	1	1.02	V
V _{DET_HYS}			-	50	-	mV
PGOOD Definition (Relative with all DC/DC Converters, Load Switch and LDOs)						
	PGOOD Delay Time	Default, All VRs are regulated	-	64	-	ms
	WAKEUP0 Hard Reset Detect Time	RSTTMR_EN =0	-	16	-	sec
	VBUS POR OKAY to Wakup0 Enable Delay Time		-	150	-	µs
	VSYS POR OKAY to VR Starts to Rise Up Delay Time	From VSYS POR POK to DC1 Starts to Rise Up Period	-	30	-	ms
	WAKEUP0 Deglitch Time		500	-	-	µs

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over $V_{IN_DC1} = 5V$, and $T_j = -40$ to $85^\circ C$. Typical values are at $T_j = 25^\circ C$.

• BUCK1

Symbol	Parameter	Test Conditions	APW7702			Unit
			Min	Typ	Max	
$I_{Q_NSW_DC1}$	Consumption Current (No Switching Current)	$V_{IN_DC1} = 5V$, No Load, No Switching	-	40	-	μA
$I_{Q_SW_DC1}$	Switching Current	$V_{IN_DC1} = 5V$, In Switching	-	5	-	mA
I_{SHUN_DC1}	Shutdown IQ	$V_{IN_DC1} = 5V$, In Shutdown	-	-	1	μA
V_{REF_DC1}	FB_DC1 Voltage	Selectable in I ² C	0.555	-	0.66	V
		Feedback Voltage step	-	15	-	mV
		Voltage Accuracy, $V_{FB_DC1} = 0.6V$	-2	-	2	%
	DC Load Regulation	$V_{OUT_DC1} = 1V$, $I_{OUT_DC1} = 0.75A \sim 2.5A$	-	0.3	-	%/A
		$V_{OUT_DC1} = 1V$, $I_{OUT_DC1} = 0.1A \sim 2.5A$	-	0.6	-	%/A
	DC Line Regulation	$V_{IN_DC1} = 2.7V$ to $5.5V$, $V_{OUT_DC1} = 1V$, $I_{OUT_DC1} = 2.5A$	-	0.4	-	%/V
I_{CL_DC1}	Current Limit	$T_A = -40^\circ C \sim 85^\circ C$	3.8	4	-	A
	PSM Peak Current	PSM Inductor Current Peak Value	-	0.5	-	A
F_{SW_DC1}	Switching Frequency	$I_{OUT_DC1} = 0A$, Force PWM, $T_A = -40^\circ C \sim 85^\circ C$	1350	1500	1650	KHz
		$I_{OUT_DC1} = 2.5A$, $T_A = -40^\circ C \sim 85^\circ C$	1275	1500	1725	KHz
D_{MAX_DC1}	Maximum Duty Cycle		-	-	100	%
$T_{ON_MIN_DC1}$	Minimum On Time		-	60	80	ns
T_{SS_DC1}	Soft Start	$V_{OUT_DC1} = 1V$, 0 to 95% of V_{OUT_DC1} , No load	-	750	-	μs
$R_{DS(ON)_H_DC1}$	High Side Ron	$I_{OUT_DC1} = 100mA$	-	100	-	m Ω
$R_{DS(ON)_L_DC1}$	Low Side Ron	$I_{OUT_DC1} = 100mA$	-	35	-	m Ω
R_{DIS_DC1}	Output Discharge Resistor		-	250	-	Ω
	Output Voltage UVP	percentage of regulation voltage	60	70	80	%
	Output Voltage OVP	percentage of regulation voltage	120	125	130	%

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over VIN_DC2= 5V, and Tj= -40 to 85°C. Typical values are at Tj=25°C.

• BUCK2

Symbol	Parameter	Test Conditions	APW7702			Unit
			Min	Typ	Max	
I _{Q_NSW_DC2}	Consumption Current (No Switching Current)	VIN_DC2=5V, No Load, No Switching	-	40	-	μA
I _{Q_SW_DC2}	Switching Current	VIN_DC2 = 5V, In Switching	-	5	-	mA
I _{SHUN_DC2}	Shutdown IQ	VIN_DC2 = 5V , In Shutdown		-	1	μA
V _{REF_DC2}	FB_DC2 Voltage	Selectable in I ² C	0.555	-	0.66	V
		Feedback Voltage step	-	15	-	mV
		Voltage Accuracy, V _{FB_DC2} =0.6V	-2	-	2	%
	DC Load Regulation	V _{OUT_DC2} =1.2V, I _{OUT_DC2} = 0.5A~1.5A	-	0.3	-	%/A
		V _{OUT_DC2} = 1.2V, I _{OUT_DC2} =0.1A~1.5A	-	0.6	-	%/A
	DC Line Regulation	VIN_DC2=2.7V to 5.5V, V _{OUT_DC2} =1.2V, I _{OUT_DC2} =1.5A	-	0.4	-	%/V
I _{CL_DC2}	Current Limit	T _A =-40°C ~ 85°C	2.2	3	-	A
	PSM Peak Current	PSM Inductor Current Peak Value	-	0.5	-	A
F _{SW_DC2}	Switching Frequency	I _{OUT_DC2} =0A, Force PWM, T _A =-40°C ~ 85°C	1350	1500	1650	KHz
		I _{OUT_DC2} =1.5A, T _A =-40°C ~ 85°C	1275	1500	1725	KHz
D _{MAX_DC2}	Maximum Duty Cycle		-	-	100	%
T _{ON_MIN_DC2}	Minimum On Time		-	60	80	ns
T _{SS_DC2}	Soft Start	V _{OUT_DC2} =1.2V, 0 to 95% of V _{OUT_DC2} , No load	-	750	-	μs
R _{DS(ON)_H_DC2}	High Side Ron	I _{OUT_DC2} =100mA	-	130	-	mΩ
R _{DS(ON)_L_DC2}	Low Side Ron	I _{OUT_DC2} =100mA	-	65	-	mΩ
R _{DIS_DC2}	Output Discharge Resistor		-	250	-	Ω
	Output Voltage UVP	percentage of regulation voltage	60	70	80	%
	Output Voltage OVP	percentage of regulation voltage	120	125	130	%

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over $V_{IN_DC3}=5V$, and $T_J=-40$ to $85^{\circ}C$. Typical values are at $T_J=25^{\circ}C$.

• BUCK3

Symbol	Parameter	Test Conditions	APW7702			Unit
			Min	Typ	Max	
$I_{Q_NSW_DC3}$	Consumption Current (No Switching Current)	$V_{IN_DC3}=5V$, No Load, No Switching	-	40	-	μA
$I_{Q_SW_DC3}$	Switching Current	$V_{IN_DC3}=5V$, In Switching	-	5	-	mA
I_{SHUN_DC3}	Shutdown IQ	$V_{IN_DC3}=5V$, In Shutdown	-	-	1	μA
V_{REF_DC3}	FB_DC3 Voltage	Selectable in I ² C	0.555	-	0.66	V
		Feedback Voltage step	-	15	-	mV
		Voltage Accuracy, $V_{FB_DC3}=0.6V$	-2	-	2	%
	DC Load Regulation	$V_{OUT_DC3}=3V$, $I_{OUT_DC3}=0.25A\sim1A$	-	0.3	-	%/A
		$V_{OUT_DC3}=1.8V$, $I_{OUT_DC3}=10mA\sim1A$	-	0.6	-	%/A
	DC Line Regulation	$V_{IN_DC3}=2.7V$ to $5.5V$, $V_{OUT_DC3}=1.8V$, $I_{OUT_DC3}=1A$	-	0.4	-	%/V
I_{CL_DC3}	Current Limit	$T_A=-40^{\circ}C \sim 85^{\circ}C$	1.75	2	-	A
	PSM Peak Current	PSM Inductor Current Peak Value	-	0.5	-	A
F_{SW_DC3}	Switching Frequency	$I_{OUT_DC3}=0A$, Force PWM, $T_A=-40^{\circ}C \sim 85^{\circ}C$	1350	1500	1650	KHz
		$I_{OUT_DC3}=1A$, $T_A=-40^{\circ}C \sim 85^{\circ}C$	1275	1500	1725	KHz
D_{MAX_DC3}	Maximum Duty Cycle		-	-	100	%
$T_{ON_MIN_DC3}$	Minimum On Time		-	60	80	ns
T_{SS_DC3}	Soft Start	$V_{OUT_DC3}=1.8V$, 0 to 95% of V_{OUT_DC3} , No load	-	750	-	μs
$R_{DS(ON)_H_DC3}$	High Side Ron	$I_{OUT_DC3}=100mA$	-	210	-	m Ω
$R_{DS(ON)_L_DC3}$	Low Side Ron	$I_{OUT_DC3}=100mA$	-	105	-	m Ω
R_{DIS_DC3}	Output Discharge Resistor		-	250	-	Ω
	Output Voltage UVP	percentage of regulation voltage	60	70	80	%
	Output Voltage OVP	percentage of regulation voltage	120	125	130	%

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over VIN_DC3= 5V, and T_j= -40 to 85°C. Typical values are at T_j=25°C.

• BUCK4

Symbol	Parameter	Test Conditions	APW7702			Unit
			Min	Typ	Max	
I _{O_NSW_DC4}	Consumption Current (No Switching Current)	VIN_DC4=5V, No Load, No Switching	-	40	-	μA
I _{O_SW_DC4}	Switching Current	VIN_DC4 = 5V, In Switching	-	5	-	mA
I _{SHUN_DC4}	Shutdown IQ	VIN_DC4 = 5V , In Shutdown	-	-	1	μA
V _{REF_DC4}	FB_DC4 Voltage	Selectable in I ² C	0.555	-	0.66	V
		Feedback Voltage step	-	15	-	mV
		Voltage Accuracy, V _{FB_DC4} =0.6V	-2	-	2	%
	DC Load Regulation	V _{OUT_DC4} =3V, I _{OUT_DC4} = 0.5A~1.5A	-	0.3	-	%/A
		V _{OUT_DC4} = 3V, I _{OUT_DC4} = 0.1A~1.5A	-	0.6	-	%/A
	DC Line Regulation	VIN_DC4 = 3.5V to 5.5V, V _{OUT_DC4} =3V, I _{OUT_DC4} = 1.5A	-	0.4	-	%/V
I _{CL_DC4}	Current Limit	T _A =-40°C ~ 85°C	2.2	3	-	A
	PSM Peak Current	PSM Inductor Current Peak Value	-	0.5	-	A
F _{SW_DC4}	Switching Frequency	I _{OUT_DC4} =0A, Force PWM, T _A =-40°C ~ 85°C	1350	1500	1650	KHz
		I _{OUT_DC4} =1.5A, T _A =-40°C ~ 85°C	1275	1500	1725	KHz
D _{MAX_DC4}	Maximum Duty Cycle		-	-	100	%
T _{ON_MIN_DC4}	Minimum On Time		-	60	80	ns
T _{SS_DC4}	Soft Start	V _{OUT_DC4} =3V, 0 to 95% of V _{OUT_DC4} , No load	-	750	-	μs
R _{DS(ON)_H_DC4}	High Side Ron	I _{OUT_DC4} =100mA	-	130	-	mΩ
R _{DS(ON)_L_DC4}	Low Side Ron	I _{OUT_DC4} =100mA	-	65	-	mΩ
R _{DIS_DC4}	Output Discharge Resistor		-	250	-	Ω
	Output Voltage UVP	percentage of regulation voltage	60	70	80	%
	Output Voltage OVP	percentage of regulation voltage	120	125	130	%

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over $V_{SYS}=5V$, and $T_J=-40$ to $85^{\circ}C$. Typical values are at $T_J=25^{\circ}C$.

• RTCLDO

Symbol	Parameter	Test Conditions	APW7702			Unit
			Min	Typ	Max	
	RTCLDO Output Voltage	Adjustable by I^2C	1.5	-	3.05	V
I_{RTCLDO_Max}	RTCLDO Source Capability	$V_{VIN_RTCLDO}=3.7V$, $V_{OUT_RTCLDO}=1.95V$	-	-	10	mA
	DC Output Voltage Accuracy	$I_{OUT_RTCLDO}=10mA$, $V_{VIN_RTCLDO}>V_{OUT_RTCLDO}+150mV$, $V_{OUT_RTCLDO}=1.95V$	-3	-	3	%
	Load Regulation	$I_{OUT_RTCLDO}=0mA\sim 10mA$, $V_{VIN_RTCLDO}=3.7V$, $V_{OUT_RTCLDO}=1.95V$	-3	-	3	%
	Line Regulation	$V_{VIN_RTCLDO}=3.7V\sim 5V$, $I_{OUT_RTCLDO}=10mA$, $V_{OUT_RTCLDO}=1.95V$	-3	-	3	%
$V_{DROPOUT_RTC}$	VSYS-VOUT_RTCLDO Dropout Voltage	$I_{OUT_RTCLDO}=10mA$, $V_{OUT_RTCLDO}=1.95V$, $T_A=25^{\circ}C$	-	150	200	mV
		$T_J=-40\sim 125^{\circ}C$	-	200	265	mV
I_{CL_RTC}	Short Circuit Current Limit	$V_{OUT_RTCLDO1}$ Short to GND, $V_{VIN_RTCLDO}=5V$	-	150	-	mA
$R_{DS(ON)_RTC}$	R_{LDORTC}		-	10	-	Ω

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over VINLDO1= 1.8V, and T_j= -40 to 85°C. Typical values are at T_j=25°C.

• LDO1

Symbol	Parameter	Test Conditions	APW7702			Unit
			Min	Typ	Max	
	LDO1 Output Voltage Range	Output Adjustable, V _{FB_LDO1} =0.6V	0.6	-	3.3	V
	DC Output Voltage Accuracy	I _{LDO1} =10mA, V _{VINLDO1} > V _{LDO1} +30mV,	-2	-	2	%
	Load Regulation	I _{LDO1} =0mA to 150mA, V _{VINLDO1} =1.8V, V _{LDO1} =1.0V	-1.5	-	1.5	%
	Line Regulation	V _{VINLDO1} =1.8V to 5V, I _{LDO1} =150mA, V _{LDO1} =1.0V	-1.5	-	1.5	%
	VINLDO1 POR Voltage Threshold	VINLDO1 Rising	0.9	1	1.1	V
	VINLDO1 POR Voltage Hysteresis	VINLDO1 Falling	-	0.2	-	V
V _{DROPOUT_LDO1}	VINLDO1-VLDO1 Dropout Voltage	I _{LDO1} =150mA, V _{VINLDO1} =1.8V, T _A =25°C	-	-	650	mV
I _{CL_LDO1}	Short Circuit Current Limit	V _{LDO1} Short to GND, V _{VINLDO1} =5V	260	300	-	mA
	Output Voltage UVP	percentage of regulation voltage	40	50	60	%
	Output Voltage OVP	percentage of regulation voltage	120	125	130	%
T _{SS_LDO1}	Soft Start Time	Time to Ramp V _{LDO1} from 5% to 95%, No Load	-	50	-	μs
R _{DIS_LDO1}	Discharge Resistor	Internal Discharge resistor when shutdown occur	100	375	500	Ω
R _{DS(ON)_LDO1}	LDO1 R _{DS(ON)}		-	3	-	Ω
	PSRR	frequency=1kHz, V _{VINLDO1} =1.8V, V _{LDO1} =1.0V loading=10mA	-70	-	-	dB

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over $V_{INLDO2} = 5V$, and $T_J = -40$ to $85^{\circ}C$. Typical values are at $T_J = 25^{\circ}C$.

• LDO2

Symbol	Parameter	Test Conditions	APW7702			Unit
			Min	Typ	Max	
	LDO2 Output Voltage Range	Output Adjustable by I ² C	1.5	-	3.3	V
	DC Output Voltage Accuracy	$I_{LDO2} = 10mA$, $V_{VINLDO2} > V_{LDO2} + 20mV$,	-2	-	2	%
	Load Regulation	$I_{LDO2} = 0mA$ to $300mA$, $V_{VINLDO2} = 3.3V$, $V_{LDO2} = 1.8V$	-1.5	-	1.5	%
	Line Regulation	$V_{VINLDO2} = 3.3V$ to $5.5V$, $I_{LDO2} = 300mA$, $V_{LDO2} = 1.8V$	-1	-	1	%
$V_{DROPOUT_LDO2}$	VINLDO2 POR Voltage Threshold	$V_{VINLDO2}$ Rising	2.9	3	3.1	V
I_{CL_LDO2}	VINLDO2 POR Voltage Hysteresis	$V_{VINLDO2}$ Falling	-	0.2	-	V
	VINLDO2-VLDO2 Dropout Voltage	$I_{LDO2} = 300mA$, $V_{VINLDO2} = 3.3V$, $T_A = 25^{\circ}C$	-	-	900	mV
	Short Circuit Current Limit	V_{LDO2} Short to GND, $V_{VINLDO2} = 5V$	350	450	-	mA
T_{SS_LDO2}	Output Voltage UVP	percentage of regulation voltage	40	50	60	%
R_{DIS_LDO2}	Output Voltage OVP	percentage of regulation voltage	120	125	130	%
$R_{DS(ON)_LDO2}$	Soft Start Time	Time to Ramp V_{LDO2} from 5% to 95%, No Load	-	150	-	μs
	Discharge Resistor	Internal Discharge resistor when shutdown occur	100	375	500	Ω
	LDO2 $R_{DS(ON)}$		-	2	-	Ω
	PSRR	frequency=1kHz, $V_{VINLDO2} = 2.7V$, $V_{LDO2} = 1.8V$ loading=10mA	-70	-	-	dB

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over $T_J = -40$ to 85°C , Typical values are at $T_J = 25^\circ\text{C}$.
External Load Switch, Use LS1/2_EN to be an enable trigger signal

• LS1/2

Symbol	Parameter	Test Conditions	APW7702			Unit
			Min	Typ	Max	
V_{LDO_LS}	Internal LDO Voltage	Supply source from V_{SYS} , No Load	2.5	3	3.5	V
V_{OH}	Output High Voltage	LS_ENx Voltage High Range, ILS_ENx=0mA, supply source is the internal LDO output V_{LDO_LS}	2.5	3	3.5	V
V_{OL}	Output Low Voltage	LS_ENx Voltage Low Range	-	0	-	V
	$V_{LDO_LS} - V_{LS_ENx}$ Dropout Voltage	$I_{LS_ENx}=5\text{mA}$, $V_{SYS}=3.6\text{V}$, $T_A=25^\circ\text{C}$	-	150	300	mV
		$T_J = -40 \sim 125^\circ\text{C}$	-	225	400	mV
R_{LDO_LS}	V_{SYS} to V_{LDO_LS} $R_{DS(ON)}$		-	30	-	Ω
R_{LS_Source}	V_{LDO_LS} to V_{LS_ENx} $R_{DS(ON)}$		-	30	-	Ω
R_{LS_Sink}	Output Sink Capability		-	6	-	Ω
	Short Circuit Current Limit	V_{LS_ENx} Short to GND, $V_{SYS}=3.6\text{V}$	-	30	-	mA
	LS_ENx pin pulled low resistor		-	10	-	k Ω

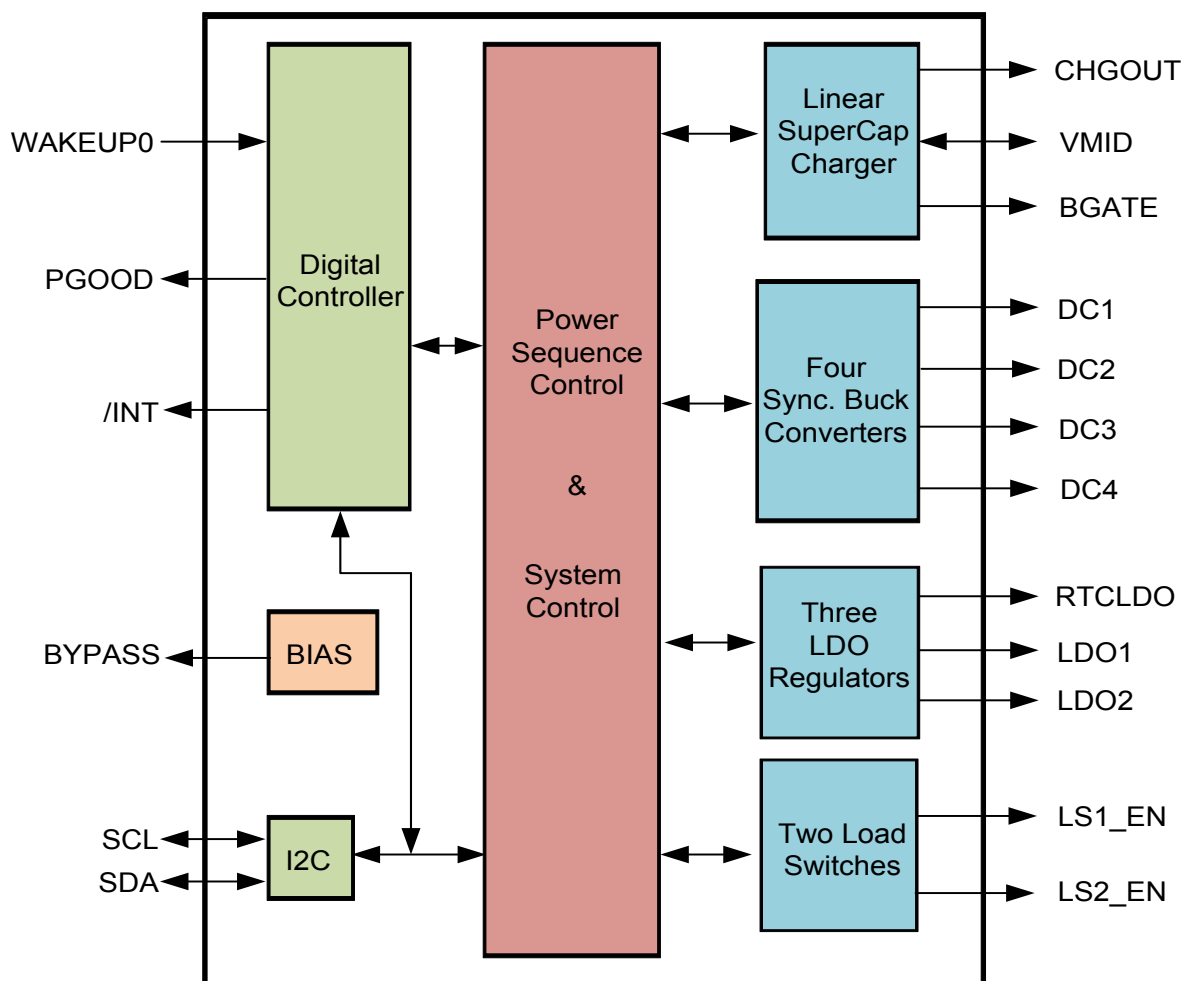
Pin Description

PIN		FUNCTION
NO.	NAME	
1	CLTOUT	Input Pin. If CLTOUT=L, the device disables fault latch behavior. If CLTOUT=H, the device enables fault latch behavior. When fault is occurred, the device could write register 0x2F any bit to clear fault and check CHGEN status to determine charge action or not.
2	CHGEN	Input CHGEN Pin to determine Pin or Register Control. If CHGEN=H, the device enables charge whether the register 03[0] bit is 0 or 1. If CHGEN=L, the device will check the register 03[0] bit to program charge state.
3	WAKEUP0	Push-Button input pin. When the pin signal is triggered from high to low, the device starts to power up.
4	NC	NO used.
5	VMID	Connects to the Midpoint of the 2-Cell supercap stack. An internal leakage balancing amplifier drives this pin to a voltage which is exactly half of VSUPCAP. If the balance function is not used, floating is recommended.
6	VBAT	Battery connection point to the positive terminal of the battery pack. Connect a 10 μ F closely to the VBAT pin.
7	BGATE	The pin drives the gate of an external P-channel MOSFET for the discharge path from battery to system.
8	CHGOUT	In switching mode, junction point of the Internal high-side MOSFET Source, output filter inductor and the cathode of the low-side Diode. In linear mode, connect the CHGOUT and VBAT (CSN) together.
9, 10	VSYS	System connection point. The external MOSFET is connected between BAT and SYS by BGATE Driver signal controlled.
11, 12	VBUS	Charger input voltage. The internal MOSFET (RBFET) is connected between VBUS and VSYS with VBUS on source. Place a 1 μ F ceramic capacitor from VBUS to PGND and place it as close as possible to IC.
13	LS2_EN	Load switch 2 output enable pin.
14	LX_DC4	DC4 PWM Regulator LX Pin. Connect to external inductor for output LC filter.
15	VIN_DC4	DC4 PWM converter Input Pin.
16	FB_DC4	DC4 output feedback voltage pin.
17	FB_DC2	DC2 output feedback voltage pin.
18	VIN_DC2	DC2 PWM converter Input Pin.
19	LX_DC2	DC2 PWM Regulator LX Pin. Connect to external inductor for output LC filter.
20	LS1_EN	Load switch 1 output enable pin.
21	VINLDO2	LDO2 input voltage pin.
22	LDO2	LDO2 output voltage pin.
23	VINLDO1	LDO1 input voltage pin.
24	LDO1	LDO1 output voltage pin.
25	FB_LDO1	LDO1 output feedback voltage pin. The LDO1 internal reference is 0.6V.
26	FB_DC1	DC1 output feedback voltage pin.
27	VIN_DC1	DC1 PWM converter Input Pin.

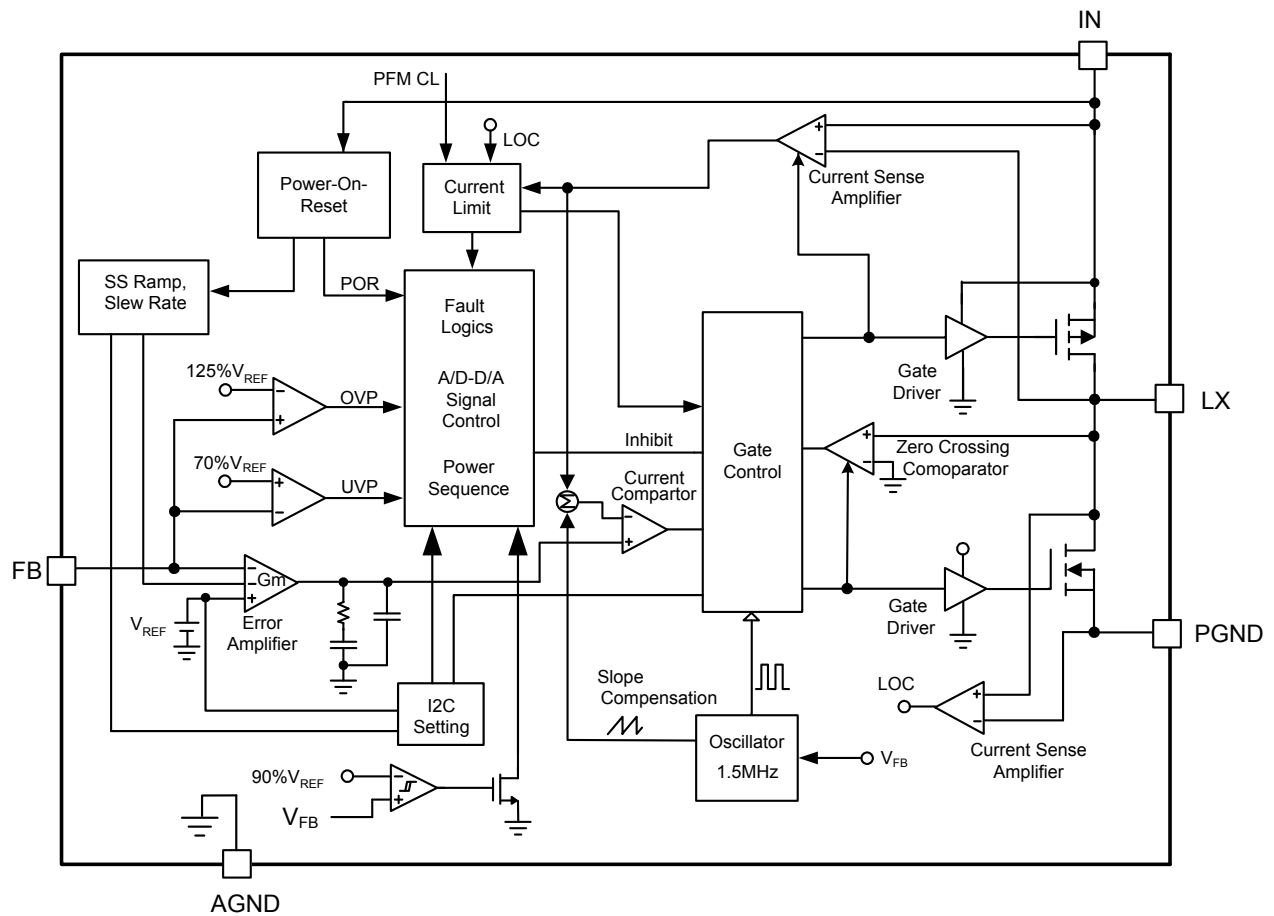
Pin Description

PIN		FUNCTION
NO.	NAME	
28	LX_DC1	DC1 PWM Regulator LX Pin. Connect to external inductor for output LC filter.
29	PGND	Power ground connection for high-current power converter node. Internally, PGND is connected to the anode of the low side diode. On PCB layout, connect directly to ground connection of input and output capacitors of the charger. A single point connection is recommended between power PGND and the analog AGND near the IC PGND pin.
30	LX_DC3	DC3 PWM Regulator LX Pin. Connect to external inductor for output LC filter.
31	VIN_DC3	DC3 PWM converter Input Pin.
32	FB_DC3	DC3 output feedback voltage pin.
33	RTCLDO	RTCLDO output voltage pin. The pin voltage is adjustable by I ² C.
34	BYPASS	Internal bias voltage. It is not recommended to connect any load to the pin.
35	VDET	Detect pin for VRs power good okay. When the VDET voltage is lower than falling threshold, the PMIC will pull low PGOOD signal. When VDET voltage is higher than rising threshold, the PMIC will automatically pull high PGOOD signal.
36	AGND	IC Analog ground.
37	PGOOD	Power Good Indicator. Pulled low when either buck converter output is out of regulation.
38	/INT	Open interrupt output. Connect the /INT to the pull up rail via 10k Ω resistor. The /INT pin sends active low, 10 μ s pulse to host to report charger device status and fault.
39	SDA	I ² C interface data.
40	SCL	I ² C interface clock.

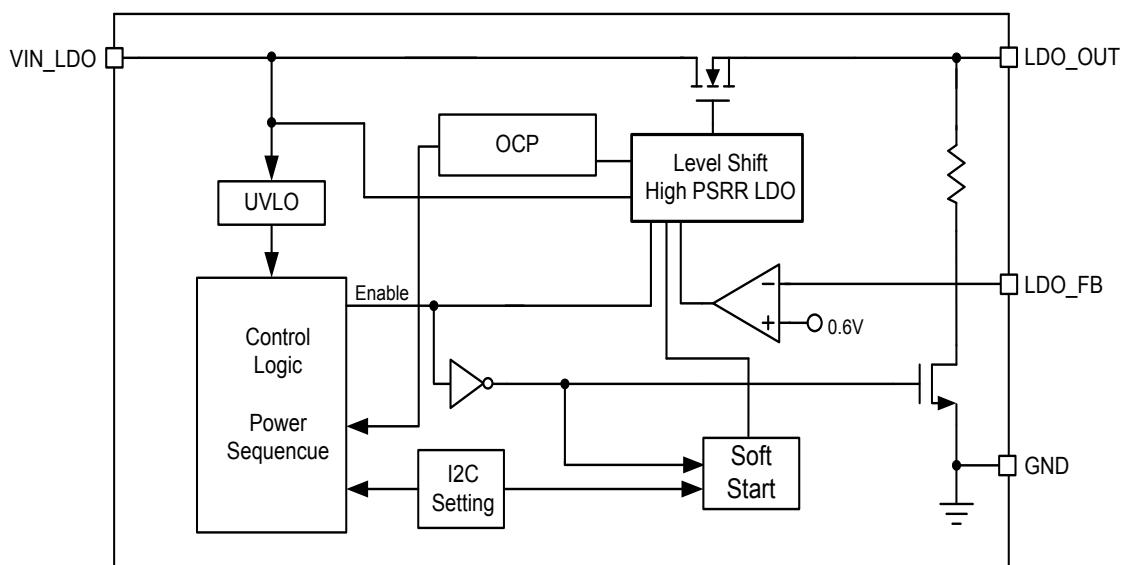
Block Diagram



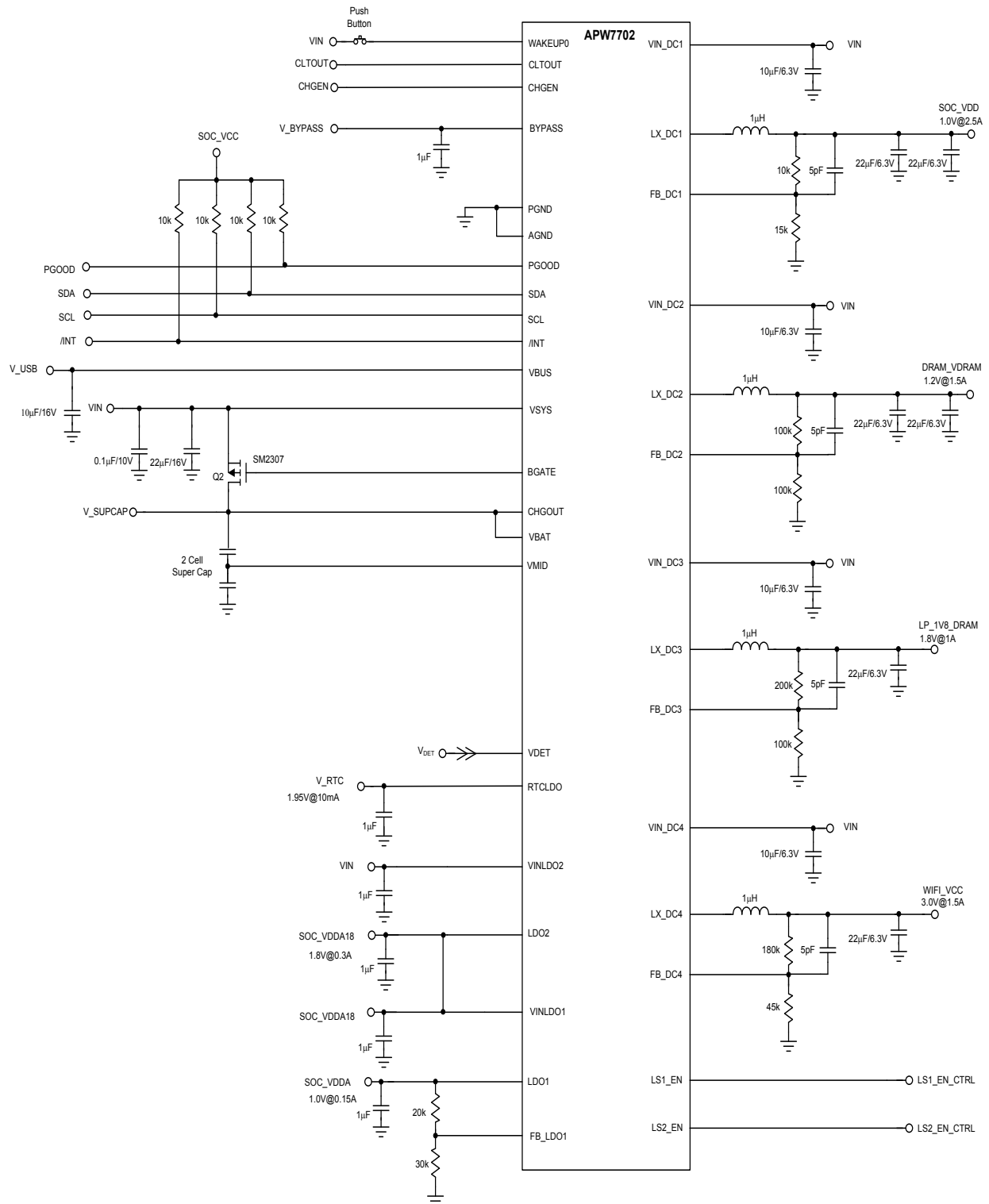
Block Diagram (Cont.) Buck Converter



LDO

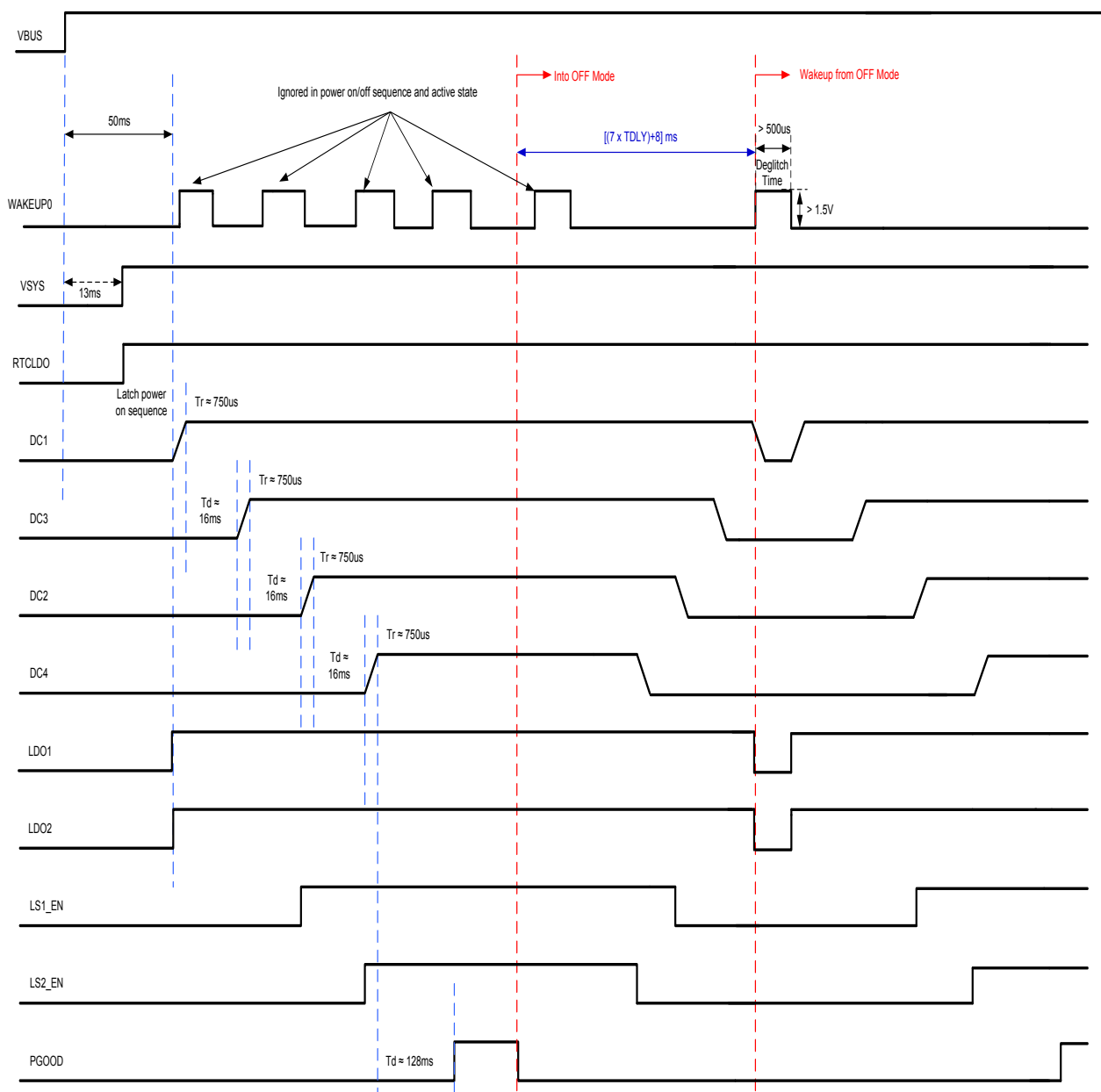


Typical Application Circuit



Power Sequence

Initial VBUS Power On



LOW Quiescent Current

To reduce the quiescent current consumption, you can refer to the following two ways.

1. VSUPCAP plug in --> VBUS plug in --> all power rail enable --> VBUS plug out --> 0x00 change from 1E to 3E (OFF=1) --> Read 0x19 & 0x1A --> Write 0xA5 bit 6=0 ➔ It can achieve low quiescent current target.
2. VSUPCAP plug in --> 0x16 change from 80 to 81 --> VBUS plug in --> all power rail enable --> VBUS plug out --> 0x00 change from 1E to 3E (OFF=1) --> Write 0xA5 bit 6=0 ➔ It can achieve low quiescent current target.

I²C Programming

I²C SERIAL CONTROL INTERFACE

The APW7702 DAP has a bidirectional I²C interface that compatible with the I²C (Inter IC) bus protocol and supports standard mode (100-kHz), fast mode (400-kHz) and the high-speed mode (up to 3.4Mbps in wire mode) data transfer rates for single byte write and read operations. This is a slave only device that does not support a multi-master bus environment or wait state insertion. The control interface is used to program the registers of the device and to read device status.

The DAP supports the standard-mode I²C bus operation (100 kHz maximum), the fast I²C bus operation (400 kHz maximum) and the high-speed mode (up to 3.4Mbps in wire mode). The DAP performs all I²C operations without I²C wait cycles.

General I²C Operation

The I²C bus uses two signals; SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data is transferred on the bus serially one bit at a time. The address and data can be transferred in byte (8-bit) format, with the most significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus.

The bus uses transitions on the data pin (SDA) while the clock is high to indicate a start and stop conditions. A high-to-low transition on SDA indicates a start and a low-to-high transition indicates a stop. Normal data bit transitions must occur within the low time of the clock period. These conditions are shown in Figure 1. The master generates the 7-bit slave address and the R/W bit a zero indicates a transmission (WRITE), a “one” indicates a request for data (READ) to open communication with another device and then waits for an acknowledge condition. The APW7702 holds SDA low during the acknowledge clock period to indicate an acknowledgment. When this occurs, the master transmits the next byte of the sequence.

Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. An external pull-up resistor must be used for the SDA and SCL signals to set the high level for the bus.

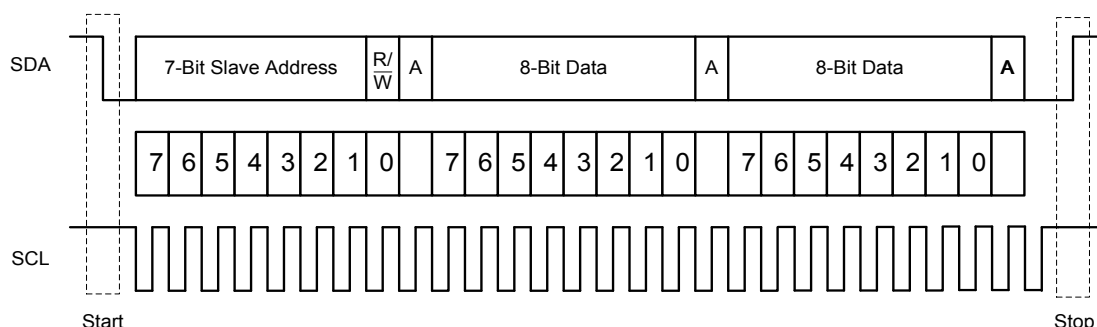


Figure 1. Typical I²C sequence

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in Figure 1. The device 7-bit address is defined as “0100100” (24H).

I²C Programming (Cont.)

Single-Byte Transfer

The serial control interface supports single-byte R/W operations for sub-addresses 0x00 to 0xFF.

Supplying a sub-address for each sub-address transaction is referred to as random I²C addressing. The APW772 also supports sequential I²C addressing. For write transactions, if a sub-address is issued followed by data for that sub-address and the 15 sub-addresses that follow, a sequential I²C write transaction has taken place, and the data for all 16 sub-addresses is successfully received by the APW7702. For I²C sequential write transactions, the subaddress then serves as the start address, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines how many sub-addresses are written. As was true for random addressing, sequential addressing requires that a complete set of data be transmitted. If only a partial set of data is written to the last subaddress, the data for the last sub-address is discarded. However, all other data written is accepted; only the incomplete data is discarded.

Single-Byte Write

As shown in Figure 2, a single-byte data write transfer begins with the master device transmitting a start condition followed by the I²C device address and the R/W bit. The R/W bit determines the direction of the data transfer. For a write data transfer, the R/W bit will be a 0. After receiving the correct I²C device address and the R/W bit, the DAP responds with an acknowledge bit. Next, the master transmits the address byte or bytes corresponding to the APW7702 internal memory address being accessed. After receiving the address byte, the APW7702 again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the APW7702 again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data write transfer.

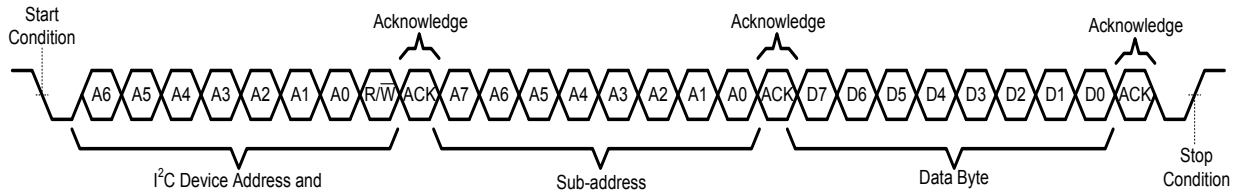


Figure 2. Single-Byte Write Transfer

I²C Programming (Cont.)

Single-Byte Read

As shown in Figure 3, a single-byte data read transfer begins with the master device transmitting a start condition followed by the I²C device address and the R/W bit. For the data read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte or bytes of the internal memory address to be read. As a result, the R/W bit becomes a 0. After receiving the APW7702 address and the R/W bit, APW7702 responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the APW7702 address and the R/W bit again. This time the R/W bit becomes a 1, indicating a read transfer. After receiving the address and the R/W bit, the APW7702 again responds with an acknowledge bit. Next, the APW7702 transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not acknowledge followed by a stop condition to complete the single byte data read transfer.

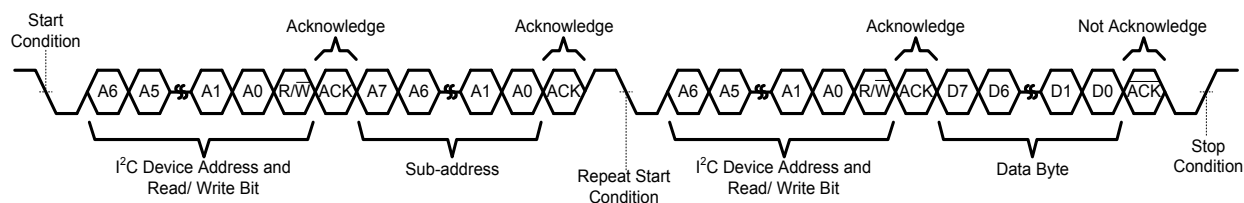


Figure 3. Single-Byte Read Transfer

I²C Programming (Cont.)

SMBus Control Timing						
	SMBDAT and SMBCLK Leakage Current		-	0.01	1	μA
F _{SMB}	SMBus Operating Frequency		-	-	100 400	KHz
T _{BUF}	Bus free time between stop and start condition	SCL=100KHz SCL=400KHz	4.7 1.3	- -	- -	μs
T _{HD_STA}	Hold time after start condition	After this period, the first clock is generated SCL=100KHz SCL=400KHz	4 0.6	- -	- -	μs
T _{SU_STA}	Repeated start condition setup time	SCL=100KHz SCL=400KHz	4.7 0.6	- -	- -	μs
T _{SU_STO}	Stop condition setup time	SCL=100KHz SCL=400KHz	4 0.6	- -	- -	μs
T _{HD_DAT}	Data hold time	SCL=100KHz SCL=400KHz	300 300	- -	- -	ns
T _{SU_DAT}	Data setup time	SCL=100KHz SCL=400KHz	250 100	- -	- -	ns
T _{LOW}	Clock low period	SCL=100KHz SCL=400KHz	4.7 1.3	- -	- -	μs
T _{HIGH}	Clock high period	SCL=100KHz SCL=400KHz	4 0.6	- -	- -	μs
T _{F_SMB}	Fall time of SMB DAT/CLK	SCL=100KHz SCL=400KHz	-	-	300 300	ns
T _{R_SMB}	Rise time of SMB DAT/CLK	SCL=100KHz SCL=400KHz	-	-	1000 300	ns
C _b	Capacitive Load for Each Bus Line	SCL=100KHz SCL=400KHz	-	-	400 400	pF

I²C Programming (Cont.)

Timing Diagram

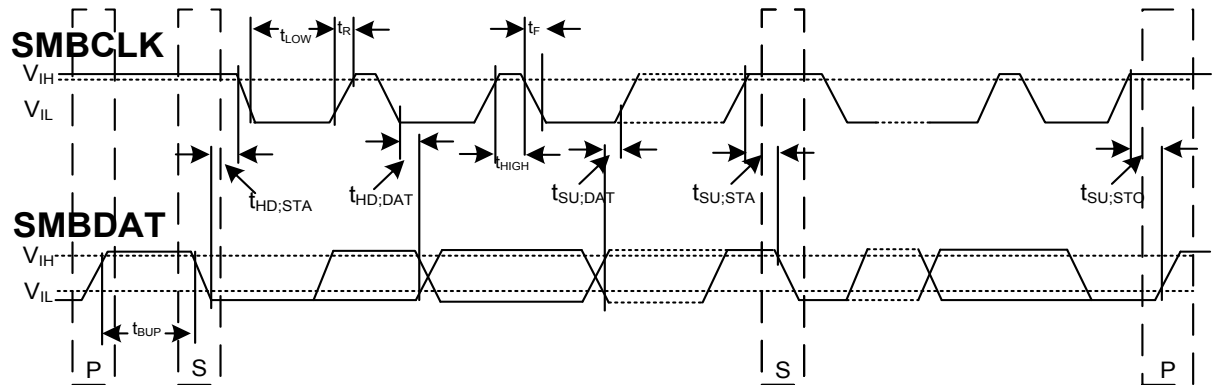


Figure 4: SMBus Common AC Specification

I²C Programming (Cont.)

Register Map

Register Address	Register Name	Read/Write/ Read Only State	Bits								Default Value
			D7	D6	D5	D4	D3	D2	D1	D0	
00	CONTROL0	Read/Write	0	0	0	1	1	1	1	0	1E
01	CONTROL1	Read/Write	0	1	0	1	0	1	0	0	54
02	CONTROL2	Read/Write	0	1	0	1	1	0	0	1	59
03	CHGCONFIG0	Read/Write	1	0	1	0	0	0	0	0	A0
05	CHGCONFIG2	Read/Write	0	0	1	0	0	0	0	0	20
06	CHGCONFIG3	Read/Write	1	0	1	0	1	0	0	1	A9
07	BUCKCONFIG0	Read/Write	0	0	1	1	0	0	1	1	33
08	BUCKCONFIG1	Read/Write	0	0	1	1	0	0	1	1	33
09	LDOCONFIG0	Read/Write	0	0	0	0	1	0	0	1	09
0A	LDOCONFIG1	Read/Write	0	0	0	0	0	1	1	0	06
0B	TIME LAPSE2	Read/Write	0	0	0	0	0	0	0	0	00
0C	TIME LAPSE1	Read/Write	0	0	0	0	0	0	0	0	00
0D	TIME LAPSE0	Read/Write	0	0	0	0	0	0	0	0	00
0E	SEQ0	Read/Write	0	0	0	0	0	0	1	0	02
0F	SEQ1	Read/Write	0	0	0	1	0	0	1	1	13
10	SEQ2	Read/Write	0	0	1	0	0	0	1	1	23
11	SEQ3	Read/Write	0	0	0	0	0	0	0	0	00
12	DLY0	Read/Write	0	0	0	1	0	0	0	1	11
13	DLY1	Read/Write	0	0	0	1	0	0	0	1	11
14	DLY2	Read/Write	0	0	0	1	0	0	0	1	11
15	DLY3	Read/Write	0	0	0	1	0	1	1	1	17
16	INT MASK	Read/Write	1	0	0	0	0	0	0	0	80
17	CHIPID	Read Only	0	0	1	0	0	x	x	x	2x
19	INT FLAG	Read Only	0	0	0	0	0	0	0	0	00
1A	WAKEUP	Read Only	0	0	0	0	0	0	0	0	00

I²C Programming (Cont.)

REG00

Bit	7	6	5	4	3	2	1	0
Name	WDT_RST	RESERVED	OFF	RSTTMR_EN	USB_EN	IUSB		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	1	1	1	1	0
Name	Description							
WDT_RST	Watchdog timer reset bit. Write "1" to reset the watchdog timer when WDT_EN bit is enabled. 0 – Read 0 as usual, write 1 no effect 1 – Write 1 to reset the watchdog timer. (auto clear)							
RESERVED	No Used							
OFF	0 – Normal status 1 – Trigger a power-down sequence. Note: When set this bit to 1 to trigger a power-down sequence. Bit is automatically reset to 0. During power down sequence, if the STBYON bit set to "1", the channel will still on.							
RSTTMR_EN	Push-button(Wakeup0) reset function enable-disable bit 0 – Disabled 1 – Enabled							
USB_EN	USB power path enable 0 – USB power input is turned off (USB suspend mode) 1 – USB power input is turned on							
IUSB	USB input current limit 000 – 100mA 001 – 500mA 010 – 900mA 011 – 1300mA 100 – 1700mA 101 – 2100mA 110 – 2500mA 111 – No Used							

I²C Programming (Cont.)

REG01

Bit	7	6	5	4	3	2	1	0
Name	RESERVED	RESERVED	RESERVED	RESERVED	TL_EN	RSTTMR	RESERVED	RESERVED
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	1	0	1	0	1	0	0
Name	Description							
RESERVED	No Used							
TL_EN	Time lapse function enabled bit 0 – time lapse function disable 1 – time lapse function enable							
RSTTMR	Push-button(Wakeup0) reset time constant 0 – 8s 1 – 16s NOTE: Device enters RESET if wakeup0 is held high pulse width for >8s or >16s(default), depending on RSTTMR bit.							

REG02

Bit	7	6	5	4	3	2	1	0
Name	WDT_EN	WDTMR			VDET_EN	RESERVED	RESERVED	RESERVED
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	1	0	1	1	0	0	1
Name	Description							
WDT_EN	Watchdog timer function enabled bit 0 – watchdog timer function disable 1 – watchdog timer function enable Note: When WDT_EN is enabled, write “1” to reset WDT_RST bit to reset watchdog timer, if watchdog timer is timeout, the PMIC will reset all registers and auto reboot.							
WDTMR	Watchdog timer setting bit. 000 – 1s 001 – 2s 010 – 4s 011 – 8s 110 – 16s 101 – 32s 110 – 64s 111 – 128s							
VDET_EN	VDET detect function enable bit. 0 – VDET detect function disable 1 – VDET detect function enable							
RESERVED	No Used							

I²C Programming (Cont.)

REG03

Bit	7	6	5	4	3	2	1	0
Name	TIMER		TMR_EN	RESERVED	RESERVED	RESERVED	RESERVED	CHG_EN
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1	0	1	0	0	0	0	0
Name	Description							
TIMER	Charge safety timer setting (fast charge timer) 00 – 4h 01 – 6h 10 – 8h 11 – 10h							
TMR_EN	Safety timer enable 0 –Fast charge timer is disabled 1 –Fast charge timer is enabled							
RESERVED	No Used							
CHG_EN	Charger enable 0 – charger is disabled 1 – charger is enabled							

REG05

Bit	7	6	5	4	3	2	1	0
Name	ICHG			RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	1	0	0	0	0	0
Name	Description							
ICHG	Charge current setting 000 – 100mA 001 – 255mA 010 – 440mA 011 – 640mA 100 ~ 111 – No use							

REG06

Bit	7	6	5	4	3	2	1	0
Name	VSUPC			RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1	0	1	0	1	0	0	1
Name	Description							
VSUPC	Supercap charger regulation voltage 000 – 4.08V 001 – 4.208V 010 – 4.272V 011 – 4.592V 100 – 4.72V 101 – 5.040V 110 – 5.232V 111 – 5.424V							
RESERVED	No Used							

I²C Programming (Cont.)

REG07

Bit	7	6	5	4	3	2	1	0
Name	STBYON_DC1	VFB_DC1			STBYON_DC2	VFB_DC2		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	1	1	0	0	1	1
Name	Description							
STBYON_DC1	Off mode DC1 regulator enabled bit 0 – power off as sequence 1 – still enable in OFF mode							
VFB_DC1	VFB_DC1 voltage setting 000 – 0.555V 001 – 0.570V 010 – 0.585V 011 – 0.600V 100 – 0.615V 101 – 0.630V 110 – 0.645V 111 – 0.660V							
STBYON_DC2	Off mode DC2 regulator enabled bit 0 – power off as sequence 1 – still enable in OFF mode							
VFB_DC2	VFB_DC2 voltage setting 000 – 0.555V 001 – 0.570V 010 – 0.585V 011 – 0.600V 100 – 0.615V 101 – 0.630V 110 – 0.645V 111 – 0.660V							

I²C Programming (Cont.)

REG08

Bit	7	6	5	4	3	2	1	0
Name	STBYON_DC3	VFB_DC3			STBYON_DC4	VFB_DC4		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	1	1	0	0	1	1
Name	Description							
STBYON_DC3	Off mode DC3 regulator enabled bit 0 – power off as sequence 1 – still enable in OFF mode							
VFB_DC3	VFB_DC3 voltage setting 000 – 0.555V 001 – 0.570V 010 – 0.585V 011 – 0.600V 100 – 0.615V 101 – 0.630V 110 – 0.645V 111 – 0.660V							
STBYON_DC4	Offmode DC4 regulator enabled bit 0 – power off as sequence 1 – still enable in OFF mode							
VFB_DC4	VFB_DC4 voltage setting 000 – 0.555V 001 – 0.570V 010 – 0.585V 011 – 0.600V 100 – 0.615V 101 – 0.630V 110 – 0.645V 111 – 0.660V							

I²C Programming (Cont.)

REG09

Bit	7	6	5	4	3	2	1	0
Name	RESERVED	RESERVED	RESERVED	RTCLDO				
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	0	1	0	0	1
Name	Description							
RESERVED	No Used							
RTCLDO	RTCLDO output voltage setting 00000 – 1.5V 00001 – 1.55V 00010 – 1.6V 00011 – 1.65V 00100 – 1.7V 00101 – 1.75V 00110 – 1.8V 00111 – 1.85V 01000 – 1.9V 01001 – 1.95V 01010 – 2.0V 01011 – 2.05V 01100 – 2.1V 01101 – 2.15V 01110 – 2.2V 01111 – 2.25V 10000 – 2.3V 10001 – 2.35V 10010 – 2.4V 10011 – 2.45V 10100 – 2.5V 10101 – 2.55V 10110 – 2.6V 10111 – 2.65V 11000 – 2.7V 11001 – 2.75V 11010 – 2.8V 11011 – 2.85V 11100 – 2.9V 11101 – 2.95V 11110 – 3.0V 11111 – 3.05V							

REG0A

Bit	7	6	5	4	3	2	1	0
Name	STBYON_ LDO1	STBYON_ LDO2	RESERVED	LDO2				
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	0	0	1	1	0
Name	Description							
STBY_ON_ LDO1	Standby mode regulator enabled bit 0 – power off as sequence 1 – still enable in OFF mode							
STBY_ON_ LDO2	Standby mode regulator enabled bit 0 – power off as sequence 1 – still enable in OFF mode							
RESERVED	No Used							
LDO2	LDO2 output voltage setting 0 0000 – 1.50V 0 0001 – 1.55V 0 0010 – 1.60V 0 0011 – 1.65V 0 0100 – 1.70V 0 0101 – 1.75V 0 0110 – 1.80V 0 0111 – 1.85V 0 1000 – 1.90V 0 1001 – 1.95V 0 1010 – 2.00V 0 1011 – 2.05V 0 1100 – 2.10V 0 1101 – 2.15V 0 1110 – 2.20V 0 1111 – 2.25V 1 0000 – 2.30V 1 0001 – 2.35V 1 0010 – 2.40V 1 0011 – 2.45V 1 0100 – 2.50V 1 0101 – 2.55V 1 0110 – 2.60V 1 0111 – 2.65V 1 1000 – 2.70V 1 1001 – 2.75V 1 1010 – 2.80V 1 1011 – 2.85V 1 1100 – 2.90V 1 1101 – 2.95V 1 1110 – 3.00V 1 1111 – 3.05V							

I²C Programming (Cont.)

REG0B

Bit	7	6	5	4	3	2	1	0
Name	T23	T22	T21	T20	T19	T18	T17	T16
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	0	0	0	0	0
Name	Description							
T23~T0	Time lapse length setting in second 00000000 00000000 00000000 - 1sec 11111111 11111111 11111111 -16777216sec (194D 4H 20M 16S)							

REG0C

Bit	7	6	5	4	3	2	1	0
Name	T15	T14	T13	T12	T11	T10	T09	T08
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	0	0	0	0	0
Name	Description							
T23~T0	Time lapse length setting in second 00000000 00000000 00000000 - 1sec 11111111 11111111 11111111 - 16777216sec (194D 4H 20M 16S)							

REG0D

Bit	7	6	5	4	3	2	1	0
Name	T07	T06	T05	T04	T03	T02	T01	T00
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	0	0	0	0	0
Name	Description							
T23~T0	Time lapse length setting in second 00000000 00000000 00000000 - 1sec 11111111 11111111 11111111 - 16777216sec (194D 4H 20M 16S)							

I²C Programming (Cont.)

REG0E

Bit	7	6	5	4	3	2	1	0
Name	DC1_SEQ				DC2_SEQ			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	0	0	0	1	0
Name	Description							
DC1_SEQ	DC1 enable STROBE 0000 – enable at STROBE0 0001 – enable at STROBE1 0010 – enable at STROBE2 0011 – enable at STROBE3 0100 – enable at STROBE4 0101 – enable at STROBE5 0110 – enable at STROBE6 0111 – enable at STROBE7							
DC2_SEQ	DC2 enable STROBE 0000 – enable at STROBE0 0001 – enable at STROBE1 0010 – enable at STROBE2 0011 – enable at STROBE3 0100 – enable at STROBE4 0101 – enable at STROBE5 0110 – enable at STROBE6 0111 – enable at STROBE7							

REG0F

Bit	7	6	5	4	3	2	1	0
Name	DC3_SEQ				DC4_SEQ			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	1	0	0	1	1
Name	Description							
DC3_SEQ	DC3 enable STROBE 0000 – enable at STROBE0 0001 – enable at STROBE1 0010 – enable at STROBE2 0011 – enable at STROBE3 0100 – enable at STROBE4 0101 – enable at STROBE5 0110 – enable at STROBE6 0111 – enable at STROBE7							
DC4_SEQ	DC4 enable STROBE 0000 – enable at STROBE0 0001 – enable at STROBE1 0010 – enable at STROBE2 0011 – enable at STROBE3 0100 – enable at STROBE4 0101 – enable at STROBE5 0110 – enable at STROBE6 0111 – enable at STROBE7							

I²C Programming (Cont.)

REG10

Bit	7	6	5	4	3	2	1	0
Name	LS1_EN_SEQ				LS2_EN_SEQ			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	1	0	0	0	1	1
Name	Description							
LS1_EN_SEQ	LS1_EN enable STROBE 0000 – enable at STROBE0 0001 – enable at STROBE1 0010 – enable at STROBE2 0011 – enable at STROBE3 0100 – enable at STROBE4 0101 – enable at STROBE5 0110 – enable at STROBE6 0111 – enable at STROBE7							
LS2_EN_SEQ	LS2_EN enable STROBE 0000 – enable at STROBE0 0001 – enable at STROBE1 0010 – enable at STROBE2 0011 – enable at STROBE3 0100 – enable at STROBE4 0101 – enable at STROBE5 0110 – enable at STROBE6 0111 – enable at STROBE7							

I²C Programming (Cont.)

REG11

Bit	7	6	5	4	3	2	1	0
Name	LDO1_SEQ				LDO2_SEQ			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	0	0	0	0	0
Name	Description							
LDO1_SEQ	LDO1 enable STROBE 0000 – enable at STROBE0 0001 – enable at STROBE1 0010 – enable at STROBE2 0011 – enable at STROBE3 0100 – enable at STROBE4 0101 – enable at STROBE5 0110 – enable at STROBE6 0111 – enable at STROBE7							
LDO2_SEQ	LDO2 enable STROBE 0000 – enable at STROBE0 0001 – enable at STROBE1 0010 – enable at STROBE2 0011 – enable at STROBE3 0100 – enable at STROBE4 0101 – enable at STROBE5 0110 – enable at STROBE6 0111 – enable at STROBE7							

I²C Programming (Cont.)

REG12

Bit	7	6	5	4	3	2	1	0
Name	DLY1				DLY2			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	1	0	0	0	1
Name	Description							
DLY1	Delay 1 time (Between STROBE0 and STROBLE1)							
	0000 – 12ms		0100 – 28ms		1000 – 44ms		1100 – 60ms	
	0001 – 16ms		0101 – 32ms		1001 – 48ms		1101 – 64ms	
	0010 – 20ms		0110 – 36ms		1010 – 52ms		1110 – 68ms	
	0011 – 24ms		0111 – 40ms		1011 – 56ms		1111 – 72ms	
DLY2	Delay 2 time (Between STROBE1 and STROBLE2)							
	0000 – 12ms		0100 – 28ms		1000 – 44ms		1100 – 60ms	
	0001 – 16ms		0101 – 32ms		1001 – 48ms		1101 – 64ms	
	0010 – 20ms		0110 – 36ms		1010 – 52ms		1110 – 68ms	
	0011 – 24ms		0111 – 40ms		1011 – 56ms		1111 – 72ms	

REG13

Bit	7	6	5	4	3	2	1	0
Name	DLY3				DLY4			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	1	0	0	0	1
Name	Description							
DLY3	Delay 3 time (Between STROBE2 and STROBLE3)							
	0000 – 12ms		0100 – 28ms		1000 – 44ms		1100 – 60ms	
	0001 – 16ms		0101 – 32ms		1001 – 48ms		1101 – 64ms	
	0010 – 20ms		0110 – 36ms		1010 – 52ms		1110 – 68ms	
	0011 – 24ms		0111 – 40ms		1011 – 56ms		1111 – 72ms	
DLY4	Delay 4 time (Between STROBE3 and STROBLE4)							
	0000 – 12ms		0100 – 28ms		1000 – 44ms		1100 – 60ms	
	0001 – 16ms		0101 – 32ms		1001 – 48ms		1101 – 64ms	
	0010 – 20ms		0110 – 36ms		1010 – 52ms		1110 – 68ms	
	0011 – 24ms		0111 – 40ms		1011 – 56ms		1111 – 72ms	

I²C Programming (Cont.)

REG14

Bit	7	6	5	4	3	2	1	0
Name	DLY5				DLY6			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	1	0	0	0	1
Name	Description							
DLY5	Delay 5 time (Between STROBE4 and STROBLE5)							
	0000 – 12ms		0100 – 28ms		1000 – 44ms		1100 – 60ms	
	0001 – 16ms		0101 – 32ms		1001 – 48ms		1101 – 64ms	
	0010 – 20ms		0110 – 36ms		1010 – 52ms		1110 – 68ms	
	0011 – 24ms		0111 – 40ms		1011 – 56ms		1111 – 72ms	
DLY6	Delay 6 time (Between STROBE5 and STROBLE6)							
	0000 – 12ms		0100 – 28ms		1000 – 44ms		1100 – 60ms	
	0001 – 16ms		0101 – 32ms		1001 – 48ms		1101 – 64ms	
	0010 – 20ms		0110 – 36ms		1010 – 52ms		1110 – 68ms	
	0011 – 24ms		0111 – 40ms		1011 – 56ms		1111 – 72ms	

REG15

Bit	7	6	5	4	3	2	1	0
Name	DLY7				PGDLY			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	1	0	1	1	1
Name	Description							
DLY7	Delay 7 time (Between STROBE6 and STROBLE7)							
	0000 – 12ms		0100 – 28ms		1000 – 44ms		1100 – 60ms	
	0001 – 16ms		0101 – 32ms		1001 – 48ms		1101 – 64ms	
	0010 – 20ms		0110 – 36ms		1010 – 52ms		1110 – 68ms	
	0011 – 24ms		0111 – 40ms		1011 – 56ms		1111 – 72ms	
PGDLY	Power Good Delay time							
	0000 – 10ms		0100 – 40ms		1000 – 72ms		1100 – 104ms	
	0001 – 16ms		0101 – 48ms		1001 – 80ms		1101 – 112ms	
	0010 – 24ms		0110 – 56ms		1010 – 88ms		1110 – 120ms	
	0011 – 32ms		0111 – 64ms		1011 – 96ms		1111 – 128ms	
Note PGDLY applies to PGOOD pin.								

I²C Programming (Cont.)

REG16

Bit	7	6	5	4	3	2	1	0
Name	RESERVED	VDETM	WKUPxM	RESERVED	TEMPM	RESERVED	OVPM	USBM
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1	0	0	0	0	0	0	0
Name	Description							
RESERVED	No Used							
VDETM	VDET status change interrupt mask 0 – interrupt is issued when VDET status changes 1 – no interrupt is issued when VDET status changes							
WKUP0M	Wakeup status change interrupt mask 0 – interrupt is issued when wakeup0 status changes (WAKEUP0 changed low to high) 1 – no interrupt is issued when wakeup0 status changes							
TEMPM	Chip temperature alarm status change interrupt mask 0 – interrupt is issued when chip temperature is over 130°C 1 – no interrupt is issued when chip temperature is over 130°C							
OVPM	USB power overvoltage status change interrupt mask 0 – interrupt is issued when USB input is overvoltage 1 – no interrupt is issued when USB input is overvoltage							
USBM	USB power status change interrupt mask 0 – interrupt is issued when power to USB input is applied or removed 1 – no interrupt is issued when power to USB input is applied or removed							

REG17

Bit	7	6	5	4	3	2	1	0
Name	RESERVED	CHIPID			RESERVED	REV		
Read/Write	R	R	R	R	R	R	R	R
Default Value	0	0	1	0	0	x	x	x
Name	Description							
RESERVED	No Used							
CHIP ID	Chip ID 010– APW7702							
REV	Revision 000 – revision 1.0 001 – revision 1.1 010 – revision 1.2 011 – revision 1.3 ... 111 - Future Use							

I²C Programming (Cont.)

REG19

Bit	7	6	5	4	3	2	1	0
Name	RESERVED	VDET_H	VDET_L	WKUP0	RESERVED	TEMPI	OVPI	USBI
Read/Write	R	R	R	R	R	R	R	R
Default Value	0	0	0	0	0	0	0	0
Name	Description							
RESERVED	No Used							
VDET_H	VDET status rising changed flag 0 – no change in VDET rising threshold 1 – VDET rising threshold has been detected							
VDET_L	VDET status falling changed flag 0 – no change in VDET falling threshold 1 – VDET falling threshold has been detected							
WKUP0	Wakeup0 status changed flag 0 – no change in status 1 – wakeup0 status change (WAKEUP0 changed low to high)							
TEMPI	Chip temperature alarm status changed flag 0 – no change in status 1 – Chip temperature is over 130°C							
OVPI	USB power overvoltage status changed flag 0 – no change in status 1 – USB input is overvoltage							
USBI	USB power status changed flag 0 – no change in status 1 – USB power status change (power to USB pin has either been applied or removed) NOTE: Status information is available in STATUS register							

I²C Programming (Cont.)

REG1A

Bit	7	6	5	4	3	2	1	0
Name	RESERVED	RESERVED	RESERVED	WKUP0	RESERVED	RESERVED	RESERVED	RESERVED
Read/Write	R	R	R	R	R	R	R	R
Default Value	0	0	0	0	0	0	0	0
Name	Description							
RESERVED	No Used							
WKUP0	WAKEUP0 status changed bit. (Alto clear when readout) 0 – no change in WAKEUP0 status 1 – WAKEUP0 status change							

REG1D

Bit	7	6	5	4	3	2	1	0
Name	DC1_OCP	DC1_OVP	DC1_UVP	DC2_OCP	DC2_OVP	DC2_UVP	DC3_OCP	DC3_OVP
Read/Write	R	R	R	R	R	R	R	R
Default Value	0	0	0	0	0	0	0	0
Name	Description							
DC1_OCP	0 : No OCP 1: OCP Occur							
DC1_OVP	0 : No OVP 1: OVP Occur							
DC1_UVP	0 : No UVP 1: UVP Occur							
DC2_OCP	0 : No OCP 1: OCP Occur							
DC2_OVP	0 : No OVP 1: OVP Occur							
DC2_UVP	0 : No UVP 1: UVP Occur							
DC3_OCP	0 : No OCP 1: OCP Occur							
DC3_OVP	0 : No OVP 1: OVP Occur							

I²C Programming (Cont.)

REG1E

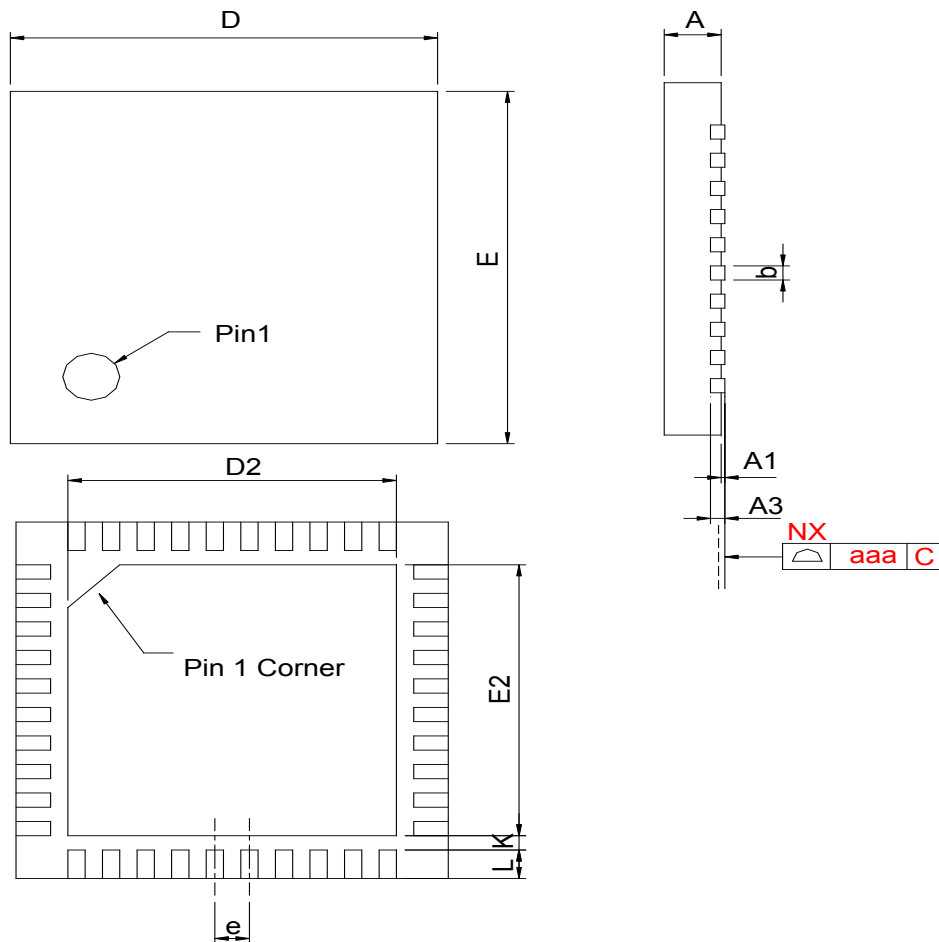
Bit	7	6	5	4	3	2	1	0
Name	DC3_UVP	DC4_OCP	DC4_OVP	DC4_UVP	LDO1_OVP	LDO1_UVP	LDO2_OVP	LDO2_UVP
Read/Write	R	R	R	R	R	R	R	R
Default Value	0	0	0	0	0	0	0	0
Name	Description							
DC3_UVP	0 : No UVP 1: UVP Occur							
DC4_OCP	0 : No OCP 1: OCP Occur							
DC4_OVP	0 : No OVP 1: OVP Occur							
DC4_UVP	0 : No UVP 1: UVP Occur							
LDO1_OVP	0 : No OVP 1: OVP Occur							
LDO1_UVP	0 : No UVP 1: UVP Occur							
LDO2_OVP	0 : No OVP 1: OVP Occur							
LDO2_UVP	0 : No UVP 1: UVP Occur							

REG2F

Bit	7	6	5	4	3	2	1	0
Name	FAULT_CLEAR							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	0	0	0	0	0
Name	Description							
FAULT_CLEAR	Write any value to this address will Clear Fault							

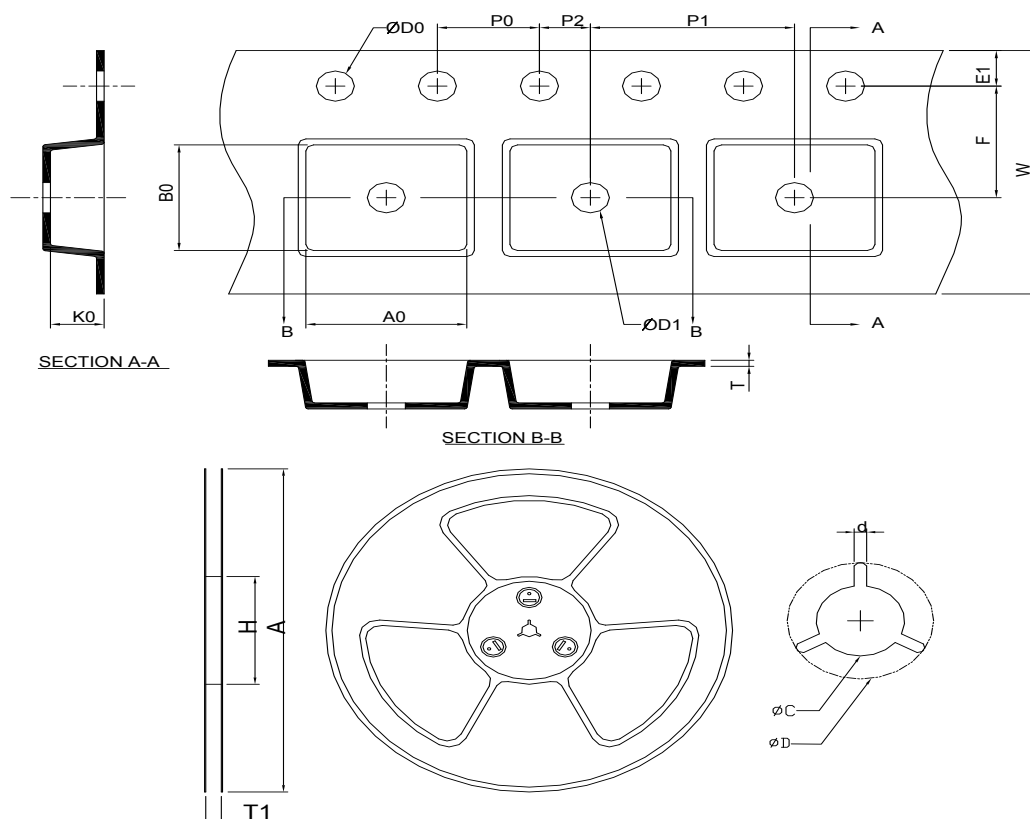
Package Information

TQFN5x5-40A



SYMBOL	TQFN5*5-40A			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.15	0.25	0.006	0.010
D	4.90	5.10	0.193	0.201
D2	3.70	3.90	0.146	0.154
E	4.90	5.10	0.193	0.201
E2	3.70	3.90	0.146	0.154
e	0.40 BSC		0.016 BSC	
L	0.30	0.40	0.012	0.016
K	0.20		0.008	
aaa	0.08		0.003	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN 5x5	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.10
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	8.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	5.35±0.20	5.35±0.20	1.00±0.20

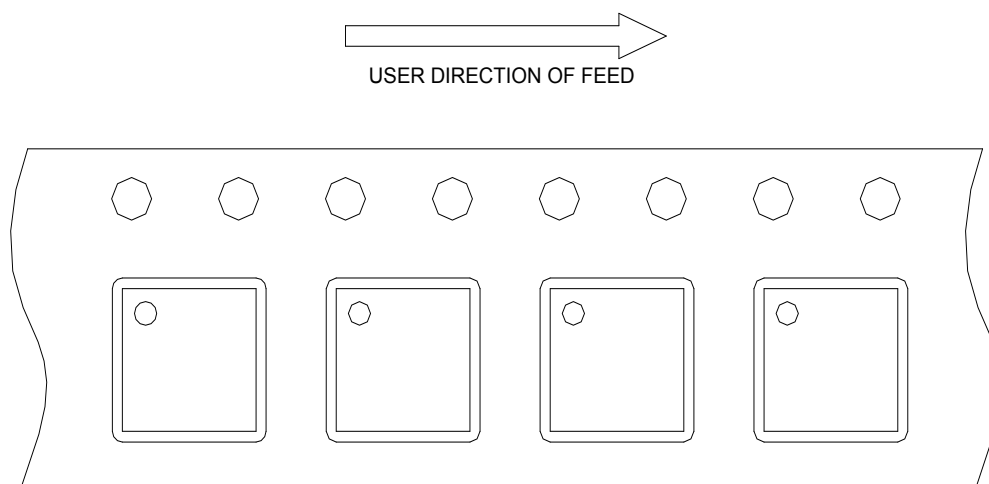
(mm)

Devices Per Unit

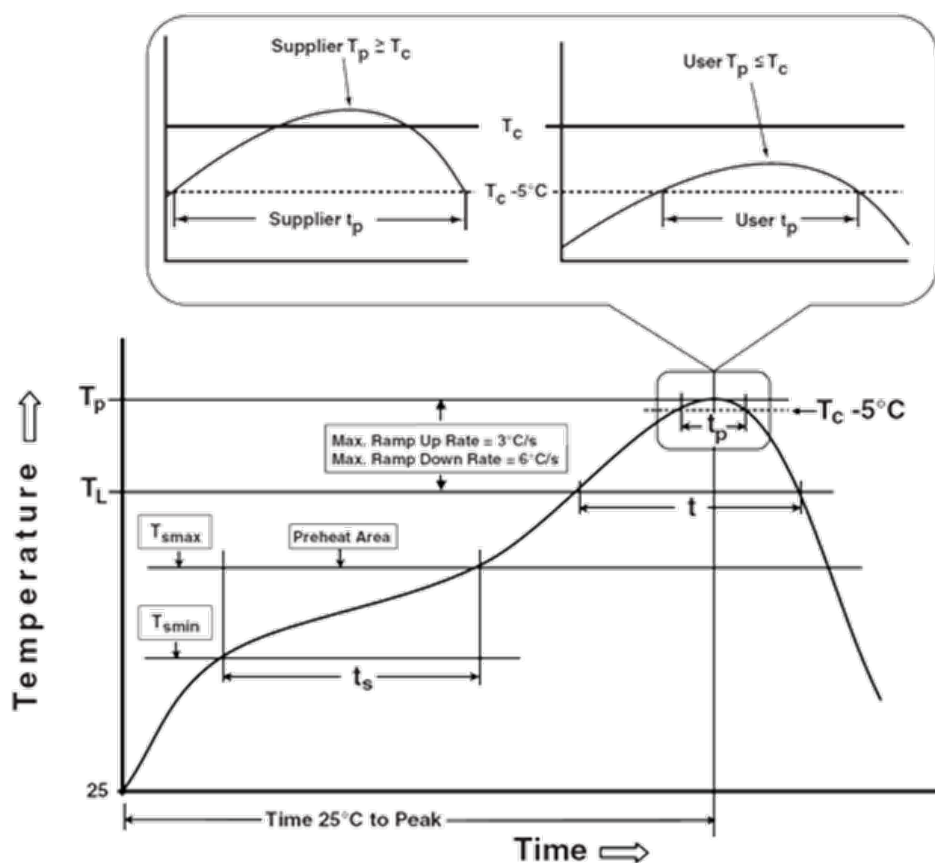
Package Type	Unit	Quantity
TQFN5x5-40A	Tape & Reel	2500

Taping Direction Information

TQFN5x5-40A



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak		
Temperature min (T_{smin})	100 °C	150 °C
Temperature max (T_{smax})	150 °C	200 °C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds	60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L)	183 °C	217 °C
Time at liquidous (t_L)	60-150 seconds	60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_p)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum.		
** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ 350-2000	Volume mm ³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j =125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≥ 2KV
MM	JESD-22, A115	VMM ≥ 200V
Latch-Up	JESD 78	10ms, $I_{tr} \geq 100mA$

Customer Service

Anpec Electronics Corp.

Head Office :

No.6, Dusing 1st Road, SBIP,

Hsin-Chu, Taiwan, R.O.C.

Tel : 886-3-5642000

Fax : 886-3-5642050

Taipei Branch :

2F, No. 11, Lane 218, Sec 2 Jhongsing Rd.,

Sindian City, Taipei County 23146, Taiwan

Tel : 886-2-2910-3838

Fax : 886-2-2917-3838