Dual-Phase COT Buck PWM Controller with Dynamic Voltage

Features

- **High Input Battery Voltages Range from 1.8V to 25V Input Power**
- **Multiform Purpose Input Voltage Collocation: VCC = 5V / VIN = 5.5V ~ 19V for NB MXM application**
- **Built in VREF voltage = 2.0V ±1% with all temperature range**
- **External reference input with PWM VID Dynamic voltage control**
- **Integrated Bootstrap Forward P-CH MOSFET**
- **Built in Adjustable Frequency by TON : 100KHz ~ 800KHz range**
- **Built in Constant On Time PWM Control with Current Sharing Operation**
- **Built in External Soft-Start & Soft-Stop functions for output voltage**
- **Support Single and Two phases PWM Control by LGATE2 & PSI voltage setting**
- **Built in Programmable OCP function by Sensing Low Side MOSFET**
- **Built in UVP (50%), OVP(145%) & Thermal Shutdown functions on PWM Channel**
- **Built in PGOOD indicator for output voltage**
- **Built in POR Control Scheme Implemented at 4.25V ~ 4.45V range**
- **Shutdown Control by EN using an External MOSFET**
- **TQFN 3x3-20 Package**

General Description

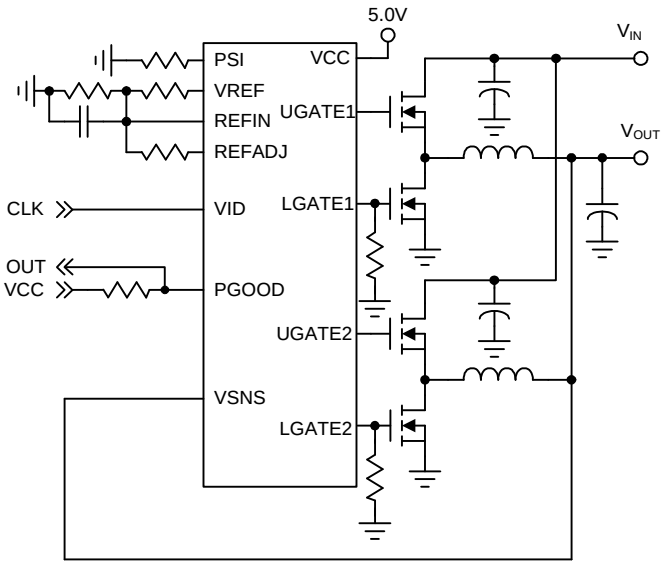
The APW8733 is a dual-phase PWM control IC which provides a precision voltage regulation system for advanced graphic card and motherboard applications. The integration of dual-phase power MOSFET drivers into the controller IC and reduces the number of external parts for a cost and space saving power management solution.

The APW8733 uses a constant on time architecture control, and results in excellent transient response and accurate DC voltage output in either PFM or PWM Mode. In Pulse Frequency Mode (PFM), the APW8733 provides very high efficiency over light to heavy loads with loading modulated switching frequencies. In PWM Mode, the converter works nearly at constant frequency for low-noise requirements. The device uses the voltage across the low side $R_{DS(ON)}$ for current sensing achieves high efficiency. The device integrates adjustable load line voltage positioning (droop) and adopts low side $R_{DS(ON)}$ for channel-current balance. The APW8733 also implement a VID control operation in which the feedback voltage is regulated and tracks external input reference voltage. This controller protection features include over-temperature (OTP), over-voltage (OVP), under-voltage (UVP) and over-current protections (OCP). The device also provides a power-on-reset function and a external programmable soft-start to prevent wrong operation and limit the input surge current during power-on or start-up. The APW8733 is available in TQFN 3x3-20 packages.

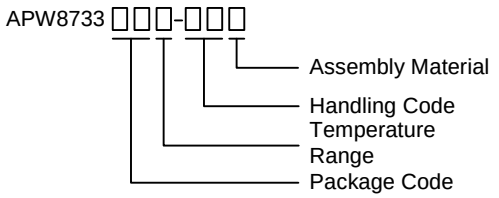
Applications

- **VGA**

Simplified Application Circuit



Ordering and Marking Information



Package Code
QB: TQFN3x3-20

Operating Ambient Temperature Range
I : -40 to 85°C

Handling Code
TR : Tape & Reel

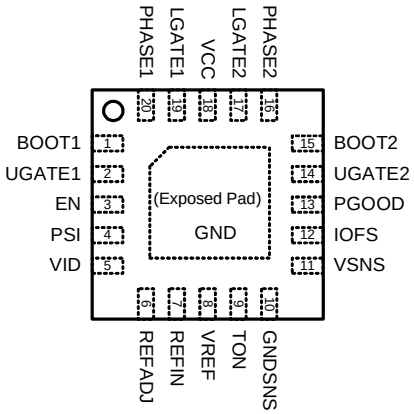
Assembly Material
G : Halogen and Lead Free Device

APW8733 QB:

XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Pin Configuration



TQFN3x3-20
Top View

= Thermal Pad (connected to GND plane for better heat dissipation)

Absolute Maximum Ratings (Note 1,2)

Symbol	Parameter		Rating	Unit
V_{CC}	VCC Supply Voltage (V_{CC} to GND)		-0.3 ~ 7	V
$V_{BOOT1/2}$	BOOT1/2 to PHASE1/2 Voltage		-0.3 ~ 7	V
	BOOT1/2 to GND Voltage		-0.3 ~ 44	V
$V_{UGATE1/2}$	UGATE1/2 to PHASE1/2 Voltage	> 400ns	-0.3 ~ $V_{BOOT1/2}$ + 0.3	V
		< 400ns	-5 ~ $V_{BOOT1/2}$ + 0.3	V
$V_{LAGTE1/2}$	LGATE1/2 to GND Voltage	> 400ns	-0.3 ~ V_{CC} + 0.3	V
		< 400ns	-5 ~ V_{CC} + 0.3	V
$V_{PHASE1/2}$	PHASE1/2 to GND Voltage	> 400ns	-1 ~ 28	V
		< 400ns	-5 ~ 35	V
	EN, PSI, VID, REFADJ, REFIN, VREF, TON, GNDSNS, VSNS, IOFS and PGOOD to GND Voltage		-0.3 ~ V_{CC} + 0.3	V
P_D	Power Dissipation		Internally Limited	W
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature		-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)		300	°C
V_{ESD}	Minimum ESD Rating (Human Body Mode)		±2	kV

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Note 2: The device is ESD sensitive. Handling precautions are recommended.

Thermal Characteristics (Note 3)

Symbol	Parameter		Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note3)	TQFN3x3-20	60	°C/W
θ_{JC}	Junction-to-Case Resistance	TQFN3x3-20	8	°C/W

Note 3: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 4)

Symbol	Parameter	Range	Unit
V_{IN}	Converter Input Voltage	1.8 ~ 25	V
V_{CC}	VCC Supply Voltage (V_{CC} to GND)	4.5 ~ 5.5	V
V_{OUT}	VOUT to GND	0.2 ~ 4	V
I_{OUT}	Converter Output Current	0 ~ 40	A
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 4: Refer to the typical application circuit.

Electrical Characteristics

Refer to Figure. 1 in the "Typical Application Circuits". These specifications apply over V_{IN} = 12V, V_{CC} = 5V, T_A = 25°C, unless otherwise noted. Typical values are at TA = 25°C.

Symbol	Parameter	Test Conditions	APW8733			Unit
			Min	Typ	Max	
SUPPLY CURRENT						
V_{cc}	VCC Supply Voltage Range		4.5	-	5.5	V
I_{VCC1}	VCC Supply Current	EN = high, V_{SNS} > V_{REFIN} = 1V, PSI = high, R_{LG2SET} = 4K Phase1 and Phase2 are both non-switching.	-	500	700	µA
I_{VCC2}	VCC Supply Current	EN = high, V_{SNS} > V_{REFIN} = 1V, PSI = high, R_{LG2SET} = 2K Phase1 is non-switching. Phase2 is shutdown.	-	300	500	µA
I_{VCC_SD}	VCC Shutdown Current	No switching, EN = GND		3	10	µA
POWER ON RESET (POR)						
V_{POR}	POR Threshold of VCC		4.25	4.35	4.45	V
V_{POR_HYST}	POR Hysteresis		-	0.1	-	V
PWM FREQUENCY SETTING						
T_{ON}	On Time	V_{IN}=19V, V_{OUT}=1V, R_{TON}=1MΩ	189	210	231	ns
$T_{ON(MIN)}$	Minimum On Time	Over all temperature & V_{CC}	80	110	140	ns
$T_{OFF(MIN)}$	Minimum Off Time	V_{REFIN} = 1V, V_{SNS} = 0.9V, V_{PHASE} = -0.1V	200	300	400	ns
BOOSTSTRAP SWITCH						
V_F	Forward Voltage	V_{CC} - $V_{BOOT1/2-GND}$, I_F = 10mA	-	0.3	0.4	V
I_R	Reverse Leakage current	$V_{BOOT1/2-GND}$ = 30V, $V_{PHASE1/2}$ = 25V, V_{CC}=5V	-	0.2	0.5	µA

Electrical Characteristics

Refer to Figure. 1 in the "Typical Application Circuits". These specifications apply over V_{IN} = 12V, V_{CC} = 5V, T_A = 25°C, unless otherwise noted. Typical values are at TA = 25°C.

Symbol	Parameter	Test Conditions	APW8733			Unit
			Min	Typ	Max	
CHIP ENABLE						
V_{ENH}	Chip Enable Threshold	EN Rising	1.2	-	-	V
V_{ENL}	Chip Shutdown Threshold	EN Falling	-	-	0.6	V
	EN_LCD Leakage Current	V_{CC} = EN = 5V	-	0.1	1	µA
POWER GOOD INDICATOR						
	PGOOD Leakage current	V_{PGOOD} = 5V	-	0.1	1.0	µA
	PGOOD output low voltage	I_{PGOOD_SINK} = 4mA		0.5	1.0	V
	PGOOD delay time	EN goes high to PGOOD goes high	-	300	350	us
	PGOOD Disable Debounce time	VSNS belows the Hysteresis of 85%V_{REFIN} to PGOOD goes low	-	20	-	us
POWER SAVING MODE						
V_{PSI_H}	PSI High Threshold Voltage	V_{PSI} Rising	0.9	1	1.1	V
V_{PSI_L}	PSI Low Threshold Voltage	V_{PSI} Falling	0.54	0.6	6.6	V
V_{LG2_1}	V_{LG2_1} Threshold Voltage	(Note5)	0.54	0.6	0.66	V
V_{LG2_2}	V_{LG2_2} Threshold Voltage	(Note5)	0.9675	1.075	1.1825	V
V_{LG2_3}	V_{LG2_3} Threshold Voltage	(Note5)	1.62	1.8	1.98	V
	Two-Phase with PWM to Single-Phase with PFM debounce time		-	300	-	us
	Two-Phase with PWM to Single-Phase with PWM debounce time		-	300	-	us
	Two-Phase with PWM to Single-Phase with Ultra-sonic PFM debounce time		-	300	-	us
	Switching Frequency of Ultra-sonic PFM	EN = high, PSI = low, R_{LG2SET}= 4K	25	30	35	kHz
I_{LG2SET}	Mode Setting Current	Source from LGATE2 Terminals	230	240	250	µA
REFERENCE VOLTAGE						
V_{REF}	Reference Voltage Accuracy	I_{REF}=100uA, T_A= -20°C ~ 85°C	1.98	2.00	2.02	V
I_{REF}	VREF Maximum Output Current	V_{REF} = GND	-	5	-	mA
ΔV_{REF}	Reference Voltage Load Regulation	I_{REF}=0~2mA	-5	-	5	mV
	VREF Discharge Resistance		-	-	100	Ω
	V_{REFIN} Operating Range		0.2	-	2	V
	REFIN Input Leakage Current		-	-	0.1	µA

Electrical Characteristics

Refer to Figure. 1 in the "Typical Application Circuits". These specifications apply over V_{IN} = 12V, V_{CC} = 5V, T_A = 25°C, unless otherwise noted. Typical values are at TA = 25°C.

Symbol	Parameter	Test Conditions	APW8733			Unit
			Min	Typ	Max	
SOFT-STOP						
R_{STOP}	Soft Stop Discharge Resistance	VSNS to GND Resistance	-	20	-	Ω
VID CONTROL INPUT						
V_{IH}	Logic High Threshold Level		1.2	-	-	V
V_{IL}	Logic Low Threshold Level		-	-	0.6	V
	VID Input Leakage Current	VID = 3.3V	-	-	1	μA
R_{REFADJ}	On Resistance of REFADJ MOSFET	VID = High	-	20	-	Ω
I_{REFADJ}	Leakage Current of REFADJ Pin	V_{REFADJ} = 2V, VID = GND	-	-	0.1	μA
REFADJ DRIVING						
T_R	REFADJ Rising Time	With 20pF Load	-	5	10	ns
T_F	REFADJ Falling Time	With 20pF Load	-	5	10	ns
	Rising and Falling Edge Delay	$\|T_R-T_F\|$	-0.5	-	0.5	ns
T_{PDR}	Rising Propagation Delay	50%VID to 50%V_{REFADJ} with 20pF Load	-	10	-	ns
T_{PDF}	Falling Propagation Delay	50%VID to 50%V_{REFADJ} with 20pF Load	-	10	-	ns
$\triangle T_{PD}$	Propagation Delay Error	$\|T_{PDR}-T_{PDF}\|$	-0.5	-	0.5	ns
T_U	Unit Pulse Width		-	27	-	ns
ZERO CURRENT DETECT						
V_{ZC}	Zero Current Detect	V_{PHASE1}-GND	-5	-	5	mV
PHASE CURRENT SENSE						
gm	Trans-conductance	Note5	-	1.0	-	mA/V
V_{OFFSET}	GM Amplifier Offset	Note5	-5	-	5	uV
V_{IOFS}	IOFS Voltage	100kΩ from IOFS to VREF	1.425	1.5	1.575	V
		100kΩ from IOFS to GND	0.475	0.5	0.525	V
GATE DRIVER						
R_{UG_SRC}	Upper Side Gate Sourcing	I_{UGATE}=100mA Sourcing	-	2.0	4.0	Ω
R_{UG_SNK}	Upper Side Gate Sinking	I_{UGATE}=100mA Sinking	-	1.5	3.0	Ω
R_{LG_SRC}	Low Side Gate Sourcing	I_{LGATE}=100mA Sourcing	-	2.0	4.0	Ω
R_{LG_SNK}	Low Side Gate Sinking	I_{LGATE}=100mA Sinking	-	1.0	2.0	Ω
T_{DT}	Dead-time		-	30	-	ns
I_{VSNS}	VSNS Input Bias Current	V_{SNS} = 2V	-0.5	-	0.5	μA
	VSNS Discharge Resistance		-	-	20	Ω

Electrical Characteristics

Refer to Figure. 1 in the "Typical Application Circuits". These specifications apply over V_{IN} = 12V, V_{CC} = 5V, T_A = 25°C, unless otherwise noted. Typical values are at TA = 25°C.

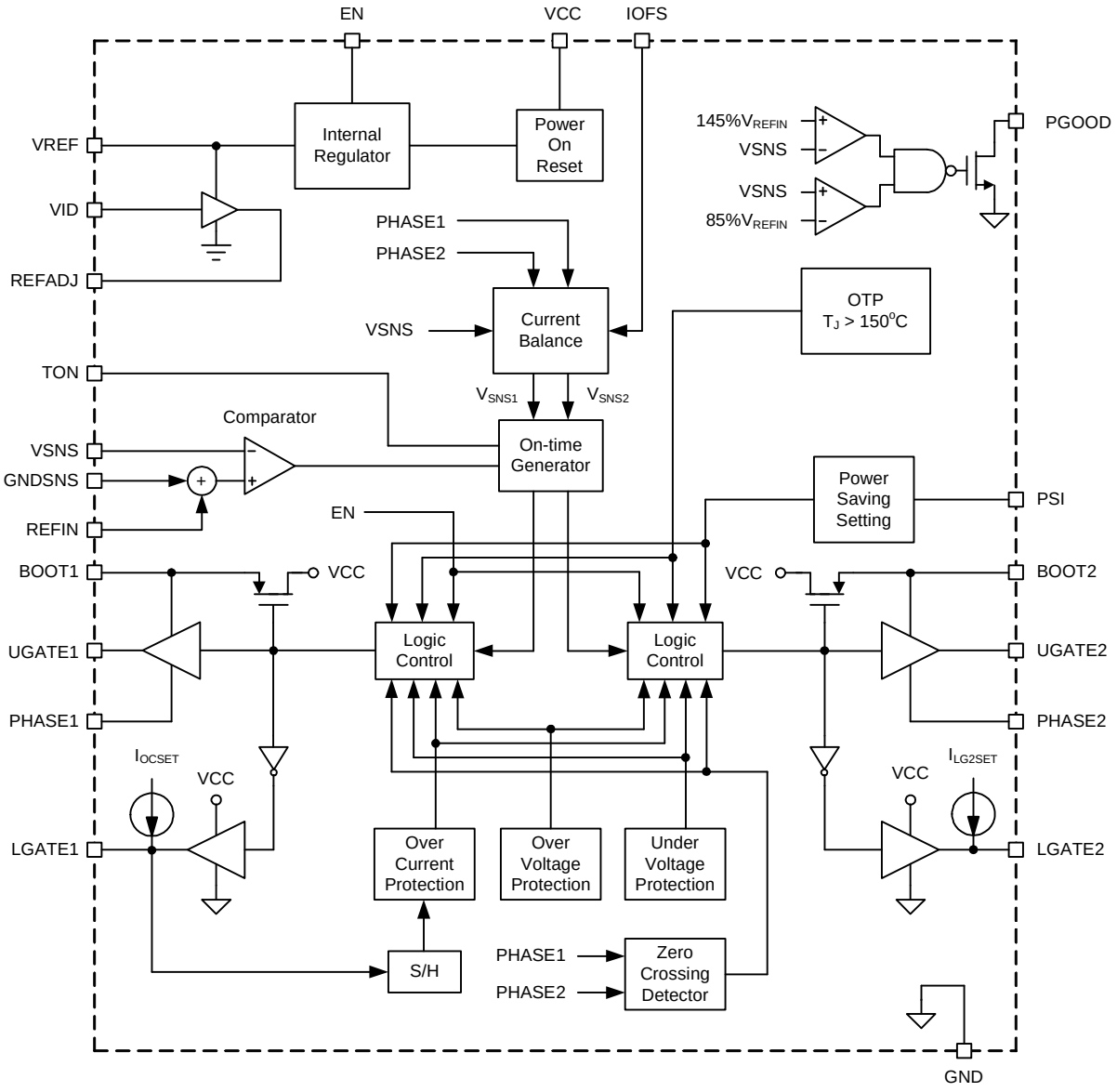
Symbol	Parameter	Test Conditions	APW8733			Unit
			Min	Typ	Max	
PROTECTION						
	Over Voltage Protection (OVP)	$V_{SNS-GNDSNS}/V_{REFIN-GND}$	140	145	150	%
	OVP Debounce time		-	2	-	us
	Under Voltage Protection (UVP)	$V_{SNS-GND}/V_{REFIN-GND}$	40	50	60	%
	UVP Debounce time		-	2	-	us
I_{OCSET}	OCP Setting Current	Source from LGATE1 Terminals	110	120	130	µA
	OCP Debounce time		-	2	-	us
	Maximum V_{OCSET} Threshold		0.55	0.6	-	V
	OCP DAC Sample Delay Time	(Note5)	-	50	-	us
	OCP DAC Maximum Sample Time	(Note5)	-	70	-	us
	Over Temperature Protection (OTP)		-	150	-	°C
	Over Temperature Hysteresis		-	30	-	°C

Note 5: Guarantee by design, not production test.

Pin Description

PIN	NAME	FUNCTION
1	BOOT1	Bootstrap Supply for the floating high-side gate driver of channel 1. Connect the Bootstrap capacitor between the BOOT1 pin and the PHASE1 pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the high-side MOSFET. Typical values for C_{BOOT1} range from 0.1µF to 1µF. Ensure that C_{BOOT1} is placed near the IC.
2	UGATE1	Upper Gate Driver Output for channel 1. Connect this pin to the gate of high-side MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the high-side MOSFET has turned off.
3	EN	Enable input.
4	PSI	Power Saving Mode. Connect a resistor from PSI to GND to set the power saving mode threshold current level. Connect this pin to VREF and R_{LG2SET} >= 4K for always two phases operation. Short this pin to ground for always single-phase operation. (refer to Table.1)
5	VID	VID Input. This pin is used to adjust reference voltage.
6	REFADJ	Reference adjustment output.
7	REFIN	External Reference Input. This is input pin of external reference voltage. Connect a voltage divider from VREF to REFIN to GND to set the reference voltage.
8	VREF	Reference Voltage Output. This is the output pin of high precision 2V reference voltage. Bypass this pin with a 1uF ceramic capacitor to GND.
9	TON	The Pin is Allowed to Adjust the Switching Frequency. Connect a resistor R_{TON} from TON pin to V_{IN}.
10	GNDSNS	GND Sense. Negative node of the remote voltage sense.
11	VSNS	Feedback Voltage. Output Voltage Feedback Pin. This pin is connected to the output voltage. The PGOOD, UVP, and OVP circuits detect this signal to report output voltage status.
12	IOFS	Current Balance Adjustment. Connect a resistor from this pin to VREF or GND to adjust the current sharing.
13	PGOOD	Open drain power good output.
14	UGATE2	Upper Gate Driver Output for channel 2. Connect this pin to the gate of high-side MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the high-side MOSFET has turned off.
15	BOOT2	Bootstrap Supply for the floating high-side gate driver of channel 2. Connect the Bootstrap capacitor between the BOOT2 pin and the PHASE2 pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the high-side MOSFET. Typical values for C_{BOOT2} range from 0.1µF to 1µF. Ensure that C_{BOOT2} is placed near the IC.
16	PHASE2	Switch Node for Channel 2. Connect this pin to the source of high-side MOSFET and the drain of the low-side MOSFET. This pin is used as sink for UGATE2 driver. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the high-side MOSFET has turned off.
17	LGATE2	Low-side Gate Driver Output for Channel 2. Connect this pin to the gate of low-side MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the low-side MOSFET has turned off.
18	VCC	Supply Voltage. This pin provides current for internal control circuit. Bypass this pin with a minimum 1uF ceramic capacitor next to the IC.
19	LGATE1	Low-side Gate Driver Output for Channel 1. Connect this pin to the gate of low-side MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the low-side MOSFET has turned off.
20	PHASE1	Switch Node for Channel 1. Connect this pin to the source of high-side MOSFET and the drain of the low-side MOSFET. This pin is used as sink for UGATE1 driver. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the high-side MOSFET has turned off.
Exposed Pad	GND	Ground. Tie this pin to the ground island/plane through the lowest impedance connection available.

Block Diagram



Typical Application Circuit

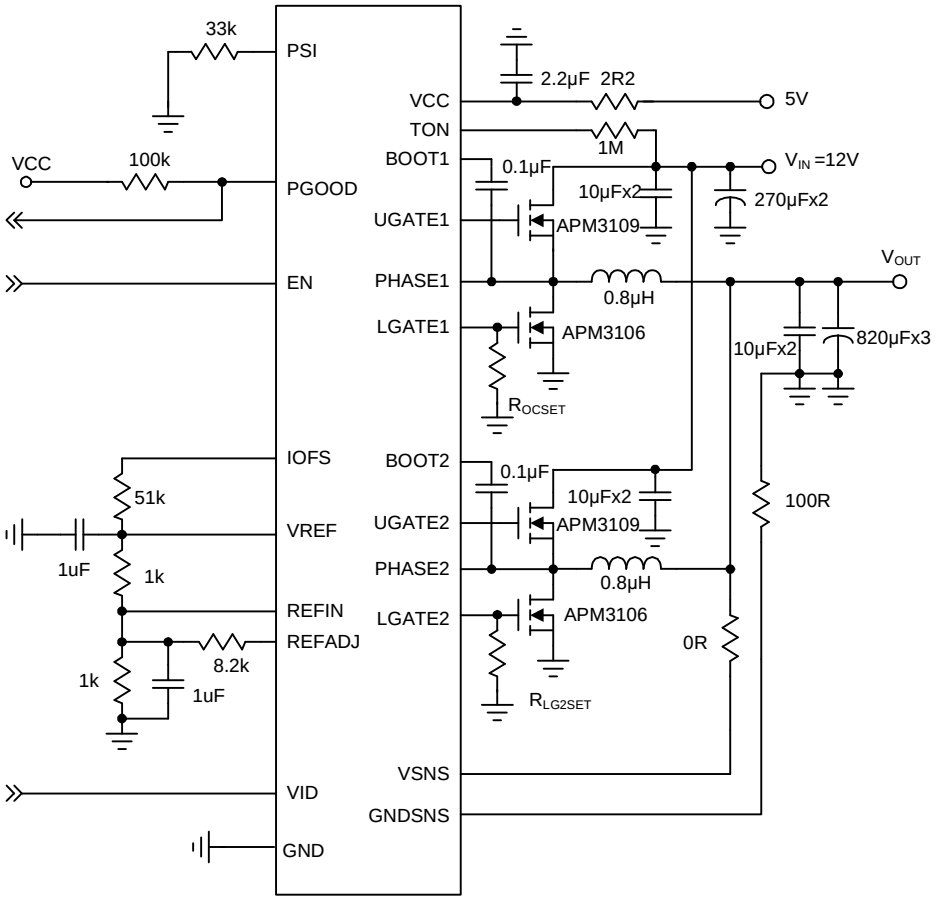


Figure.1 Typical Application Circuit

Function Description

Constant-On-Time PWM Controller with Input Feed-Forward

The constant-on-time control architecture is a pseudo fixed frequency with input voltage feed-forward. This architecture relies on the output filter capacitor's effective series resistance (ESR) to act as a current-sense resistor so the output ripple voltage provides the PWM ramp signal. In PFM operation, the high-side switch on-time is controlled by the on-time generator is determined solely by a one-shot whose pulse width is inversely proportional to the input voltage and directly proportional to the output voltage. In PWM operation, the high-side switch on-time is determined by a switching frequency control circuit in the on-time generator block. The switching frequency control circuit senses the switching frequency of the high-side switch and keeps regulating it at a constant frequency in PWM mode. The design improves the frequency variation and is more outstanding than a conventional constant-on-time controller, which has large switching frequency variation over input voltage, output current, and temperature. Both in PFM and PWM, the on-time generator, which senses input voltage on TON pin, provides very fast on-time response to input line transients. Another one-shot sets a minimum off-time (typical: 300ns). The on-time one-shot is triggered if the error comparator is high, the low-side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

Pulse-Frequency Modulation (PFM)

In PFM mode, an automatic switchover to pulse-frequency modulation (PFM) takes place at light loads. This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current zero crossing. This mechanism causes the threshold between PFM and PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the critical conduction point). The on-time of PFM is given by:

$$T_{ON-PFM} = \frac{1}{F_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

Where F_{SW} is the nominal switching frequency of the converter in PWM mode. The load current at handoff from PFM to PWM mode is given by:

$$T_{LOAD(PFM-PWM)} = \frac{1}{2} \times \frac{V_{OUT} - V_{OUT}}{L} \times T_{ON-PFM}$$

$$= \frac{V_{IN} - V_{OUT}}{2L} \times \frac{1}{F_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

Forced-PWM Mode

The Forced-PWM mode disables the zero-crossing comparator, which truncates the low-side switch on-time at the inductor current zero crossing. This causes the low-side gate-drive waveform to become the complement of the high-side gate-drive waveform. This in turn causes the inductor current to reverse at light loads while UGATE maintains a duty factor of $V_{OUT/VIN}$. The benefit of Forced-PWM mode is to keep the switching frequency fairly constant. The Forced-PWM mode is most useful for reducing audio frequency noise, improving load-transient response, and providing sink-current capability for dynamic output voltage adjustment.

VCC Power-On-Reset (POR)

The Power-On-Reset (POR) circuit compares the input voltage at VCC with the POR threshold (4.35V rising, typical) to ensure the input voltage is high enough for reliable operation. The 0.1V (typ.) hysteresis prevents supply transients from causing a restart. Once the input voltage exceeds the POR rising threshold, startup begins. When the input voltage falls below the POR falling threshold, the controller turns off the converter.

VREF

This is the output pin of high precision 2V reference voltage. Bypass this pin with a 1uF ceramic capacitor to GND. The VREF must have capability to drive 5mA output current.

Function Description (cont.)

Soft-start and Soft-stop

After the VCC voltage exceeds the POR voltage threshold and the EN threshold exceeds 1.6V, the device initials a start-up process and then ramps up the output voltage to the setting of output voltage. The external soft-start circuit is as shown in Figure. 2. The REFIN voltage is divided by the resistor R1 and R2. The soft-start duration is given by:

TSS = 5τ

Where $\tau = [(R1xR2) / (R1+R2)] \times C_{ADJ}$

Since the V_{REFIN} soft-start, to prevent PGOOD abnormal trigger during soft-start. For preventing wrong behavior or trigger some protections during soft start period, suggested the C_{ADJ} capacitance must be limited under 10nF and resistors R1 plus R2 is lower than 10kΩ. Moreover, consider the power sequence issue, suggested the V_{REFIN} established time is within 100μs(Typ.).After 300μs which EN goes high, the PGOOD is enabled. In the events of under-voltage, over-voltage, over-current, or shutdown, the chip enables the soft-stop function. The soft-stop function discharges the output voltages to the GND through an internal 20Ω switch.

VID

The VID pin adjusts from V_{BOOT} to V_{OUT} should be normal (Band-Width is large enough). The soft-start time from V_{BOOT} to V_{OUT} depend on R3 & C_{ADJ}, and the output ripple of VREFIN depend on C_{ADJ} & VID frequency.

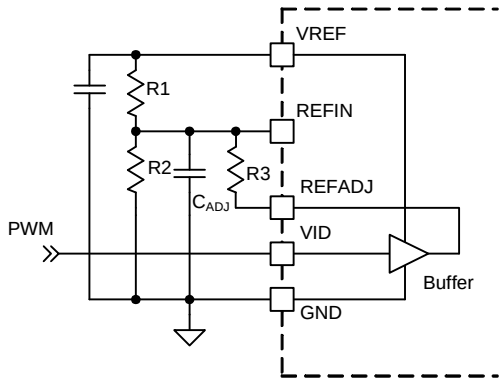


Figure.2 VID internal circuit.

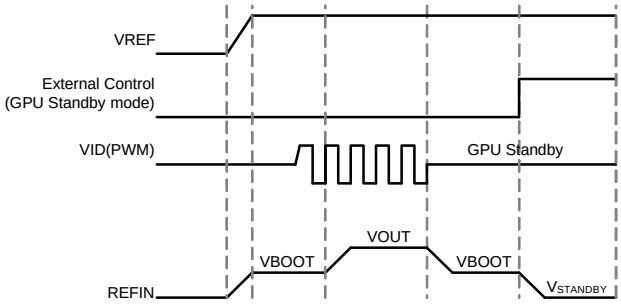


Figure. 3 Timing Diagram

Over Current Protection (OCP)

A resistor (R_{OCSET}), connected from the LGATE1 to GND, programs the over-current trip level. Before the IC initiates a start-up process, an internal current source, I_{OCSET} (120μA typical), flowing through the R_{OCSET} develops a voltage (V_{ROCSET}) across the R_{OCSET}. The device holds V_{OCP} and stops the current source, I_{OCSET}, during normal operation. When the voltage across the low-side MOSFET exceeds the V_{OCP}, the IC turns off both high-side and low-side MOSFETs. The APW8733 has an internal OCP voltage (V_{OCP_MAX}), and the value is 0.6V typical. When the $R_{OCSET\ x\ IOCSET}$ is exceeds 0.6V or the R_{OCSET} is floating or not connected, the over current threshold will be the internal default value 0.6V.

The threshold of the valley inductor current is therefore given by:

$$I_{OCP} = \frac{I_{OCSET} \times ROCSET}{R_{DS(ON)(LOW\ -\ Side)}}$$

$$I_{OCP} \times R_{OCSET} = I_{L1} \times R_{DS(ON)\_LG1} + I_{L2} \times R_{DS(ON)\_LG2}$$

$$\approx I_{OUT} \times R_{DS(ON)}$$

Function Description (cont.)

For the over-current is never occurred in the normal operating load range; the variation of all parameters in the above equation should be considered:

- The $R_{DS(ON)}$ of low-side MOSFET is varied by temperature and gate to source voltage. Users should determine the maximum $R_{DS(ON)}$ by using the manufacturer's datasheet.
- The minimum I_{OCSET} (120μA) and minimum R_{OCSET} should be used in the above equation.
- Note that the I_{OCP} is the current flow through the low-side MOSFET; I_{OCP} must be greater than valley inductor current which is output current minus the half of inductor ripple current.

$$L_{OCP} > I_{OUT} - \frac{\Delta I}{2}$$

Where ΔI = output inductor ropple current

Current Sharing

The APW8733 extracts phase currents for current balance by parasitic on-resistance of the lower switches when turned on as shown in Figure. 4. The GM amplifier senses the voltage drop across the lower switch and converts it into current signal each time it turns on. The sampled and held current is expressed as:

$$I_{SENx}=Gm \times \Delta V = (GND-V_{PHASE}) / R_X + V_{OFFSET} / R_X$$

$$=I_{LX} \times R_{DS(ON)} / R_X + V_{OFFSET} / R_X$$

The differential current of the current sharing control circuit (I_{SEN1}-I_{SEN2}) is used to generate two current parts, I1 and I2. The V_{SNS1} and V_{SNS2} will increase or decrease because of these two currents. For example, when I_{SEN1} > I_{SEN2}, the V_{SNS1} will decrease and the V_{SNS2} will increase. Therefore, the on-time of PWM1 will decrease and the on-time of PWM2 will increase. Then, the device will reduce I_{L1} current and increase I_{L2} current for current sharing, vice verse.

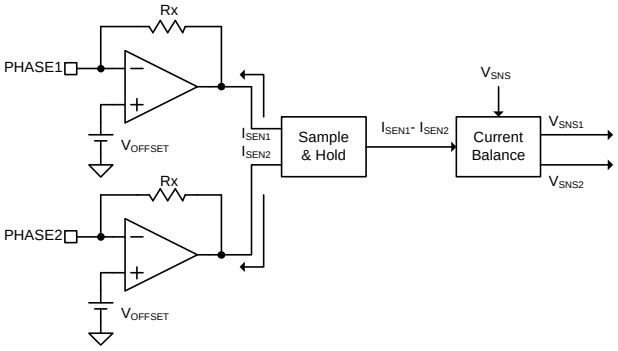


Figure. 4 Illustration of Current Balance Circuit

Offset Current Adjust

The APW8733 integrated IOFS allows the offset current to adjust phase current. The IOFS pin voltage is nominal 0.5V when connecting a resistor to GND and 1.5V when connecting a resistor to VREF. Connecting a resistor from IOFS pin to GND generate a current source as:

$$I_{OFS} = 0.5V / R_{IOFS}$$

This current is added to phase1 current signal I_{SEN1} for current balance. Consequently, phase2 will share more percentage of output current. Connecting a resistor from IOFS pin to VREF generates a current source as:

$$I_{OFS} = (V_{REF} - 1.5V) / R_{IOFS}$$

This current is added to phase2 current signal I_{SEN2} for current balance. Consequently, phase1 will share more percentage of output current.

Automatic Phase Reduction (PSI)

The APW8733 features automatic phase reduction that turns off phase2 driver signal at light load condition and reduces both switching and conduction losses. The automatic phase reduction maintains high power conversion efficiency over the output current range. The output current is sensed and mirrored to PSI pin as:

$$V_{PSI} = [(I_{L1} \times R_{DS(ON)\_LG1} + I_{L2} \times R_{DS(ON)\_LG2}) / 800] \times R_{PSI}$$
$$V_{PSI} \sim= (I_{OUT} \times R_{DS(ON)} / 800) \times R_{PSI}$$

Function Description (cont.)

A resistor (R_{LG2SET}), connected from the L_{GATE2} to GND, programs the V_{LG2} voltage. Before the IC initiates a start-up process, an internal current source, I_{LG2SET} (240µA typical), flowing through the R_{LG2SET} develops a voltage (V_{LG2}) across the R_{LG2SET}. The device holds V_{LG2} and stops the current source, I_{LG2SET}, during normal operation. The V_{LG2} is therefore given by:

$V_{LG2SET} = I_{LG2SET} \times R_{LG2SET}$

Noted that, the setting time must be ready with 120µs (Typ.) for correct mode setting in different output power MOSFET application.Select case1 to set the R_{LG2SET} is no connected. Select case2 to set the V_{LG2SET} which is ranged between V_{LG2_3}(1.8V) and V_{LG2_2}(1.075V). Select case3 to set the V_{LG2SET} which is ranged between V_{LG2_2}(1.075V) and V_{LG2_1}(0.6V). Select case3 to set the V_{LG2SET} which is lower than V_{LG2_1}(0.6V).

The APW8733 operation mode is as follows:

Table.1

Case	R_{LG2SET}	V_{PSI} > 1	V_{PSI} < 0.6	Debounce Time (us)	
1	NC	A	B	A à B	B à A
				300	0
2	5.6k		C	A à C	C à A
				300	0
3	3.3k		D	A à D	D à A
				300	0
4	1.8k	E	F	E à F	F à E
				0	0

Where:
A: Two Phases with PWM
B: Single Phase with PFM
C: Single Phase with PWM
D: Single Phase with Ultra-sonic PFM
E: Single Phase with PWM
F: Single Phase with PFM

Power-Good Output

PGOOD is an open-drain output and the PGOOD comparator continuously monitors the output voltage. PGOOD is actively held low in shutdown, and standby. When PWM converter's output voltage is greater than 85% (typ.) of its target value, the internal open-drain device will be pulled low and the PGOOD will go high. The When the output voltage V_{OUT} outruns 145% (typ.) or falls down 85% (typ.) of the target voltage, PGOOD signal will be pulled low and latched immediately.

Over-Temperature Protection (OTP)

The over-temperature circuit limits the junction temperature of the APW8733. When the junction temperature exceeds 150°C, a thermal sensor pulls UGTAE and LGATE low, allowing the devices to cool. The thermal sensor allows the converters to start a soft-start process and regulate the output voltage again after the junction temperature cools by 30°C. The OTP is designed with a 30°C hysteresis to lower the average Junction Temperature (T_J) during continuous thermal overload conditions, increasing the lifetime of the device.

Over Voltage Protection (OVP)

The over-voltage protection (OVP) circuit monitors the VSNS (V_{SNS}) voltage to prevent the output from over-voltage. When the V_{SNS} rises above 145% (typ.) of the setting reference voltage, the APW8733 turns off high-side and low-side MOSFETs, and through an internal 20Ω switch to sink the output voltage (V_{OUT}). The converter shuts down and the output is latched to be floating after PGOOD goes high. Cycling the EN enable signal, VCC power-on-reset signal can reset the latch. The OVP function is not latched before PGOOD goes high.

Function Description (cont.)

Under Voltage Protection (UVP)

The under-voltage protection circuit monitors the voltage on VSNS (V_{SNS}) by Under-Voltage (UV) comparator to protect the PWM converter against short-circuit conditions. When the V_{SNS} falls below the falling UVP threshold (50% of the setting reference voltage), a fault signal is generated and the device turns off high-side and low-side MOSFETs. The converter shuts down and the output is latched to be floating after PGOOD goes high. Cycling the EN enable signal, VCC power-on-reset signal can reset the latch. The UVP function doesn't active before PGOOD goes high.

Programming the On-Time Control and PWM Switching Frequency

The APW8733 does not use a clock signal to produce PWM. The device uses the constant-on-time control architecture to produce pseudo-fixed frequency with input voltage feed-forward. The on-time pulse width is proportional to output voltage V_{OUT} and inverses proportional to input voltage V_{IN}. In PWM, the on-time calculation is written as below:

$$T_{ON} = 3.85 \times 10^{-12} \times R_{TON} \times \frac{V_{OUT}}{V_{IN} - 0.5}$$

Where:

R_{TON} is the resistor connected from TON pin to VIN. Furthermore, the approximate PWM switching frequency is written as:

$$T_{ON} = \frac{D}{F_{SW}} \Rightarrow F_{SW} = \frac{V_{OUT} / V_{IN}}{T_{ON}}$$

Where:

F_{SW} is the PWM switching frequency. APW8733 doesn't have VIN pin to calculate on-time pulse width. Therefore, monitoring V_{TON} voltage as input voltage to calculate on-time. And then, use the relationship between on-time and duty cycle to obtain the switching frequency.

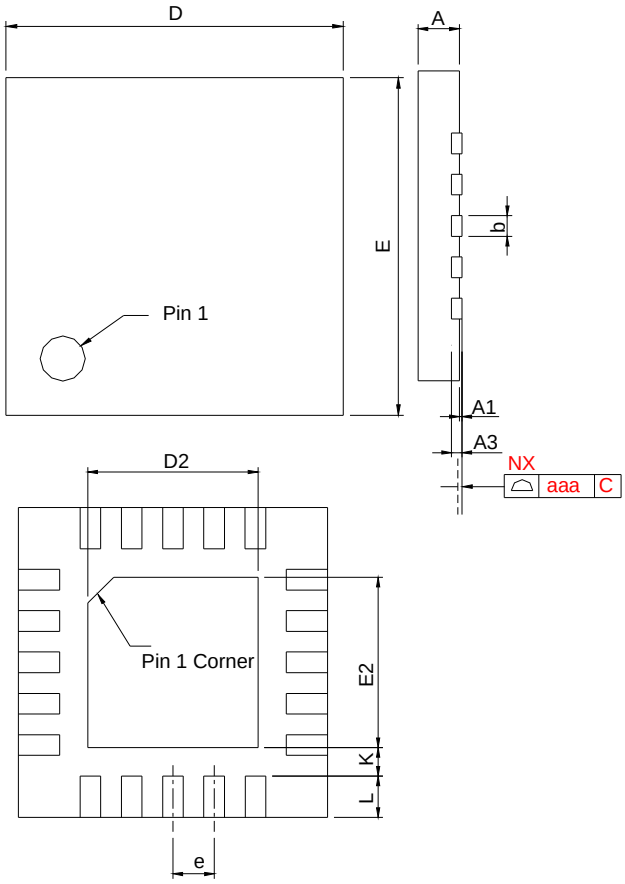
Layout Consideration

For all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

1. The input capacitor should be placed close to the VIN/VCC and GND. Connecting the capacitor and VIN/VCC/GND with short and wide trace without any via holes for good input voltage filtering. The distance between VIN/VCC and GND to capacitor less than 2mm respectively is recommended.
2. To minimize copper trace connections that can inject noise into the system, the inductor should be placed as close as possible to the PHASE1/PHASE2 pin to minimize the noise coupling into other circuits.
3. The output capacitor should be place closed to converter VOUT and GND.
4. Since the feedback pin and network is a high impedance circuit the feedback network should be routed away from the inductor. The feedback pin and feedback network should be shielded with a ground plane or trace to minimize noise coupling into this circuit.

Package Information

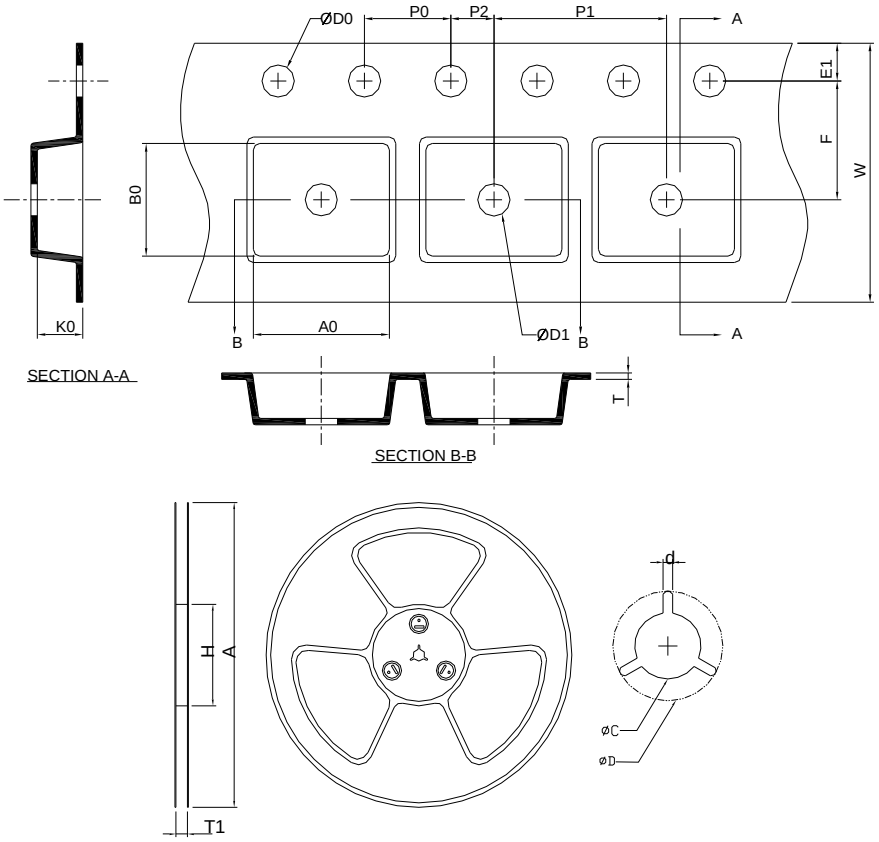
TQFN3x3-20



SYMBOL	TQFN3x3-20			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.15	0.25	0.006	0.010
D	2.90	3.10	0.114	0.122
D2	1.50	1.80	0.059	0.071
E	2.90	3.10	0.114	0.122
E2	1.50	1.80	0.059	0.071
e	0.40 BSC		0.016 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	
aaa	0.08		0.003	

Note : 1. Followed from JEDEC MO-220 WEEE

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN3x3-20	330±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.00±0.20

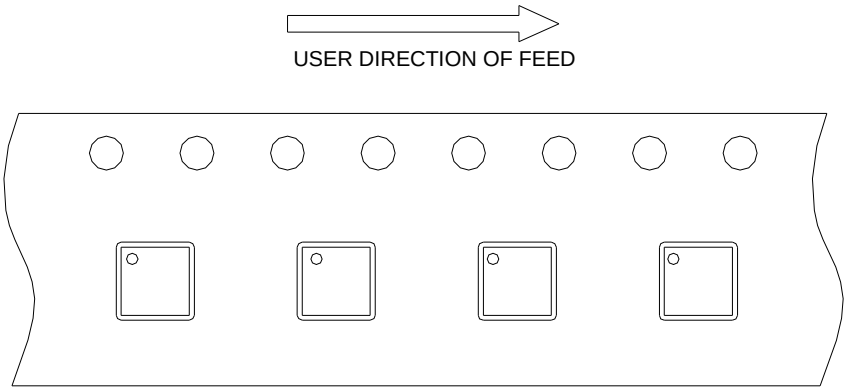
(mm)

Devices Per Unit

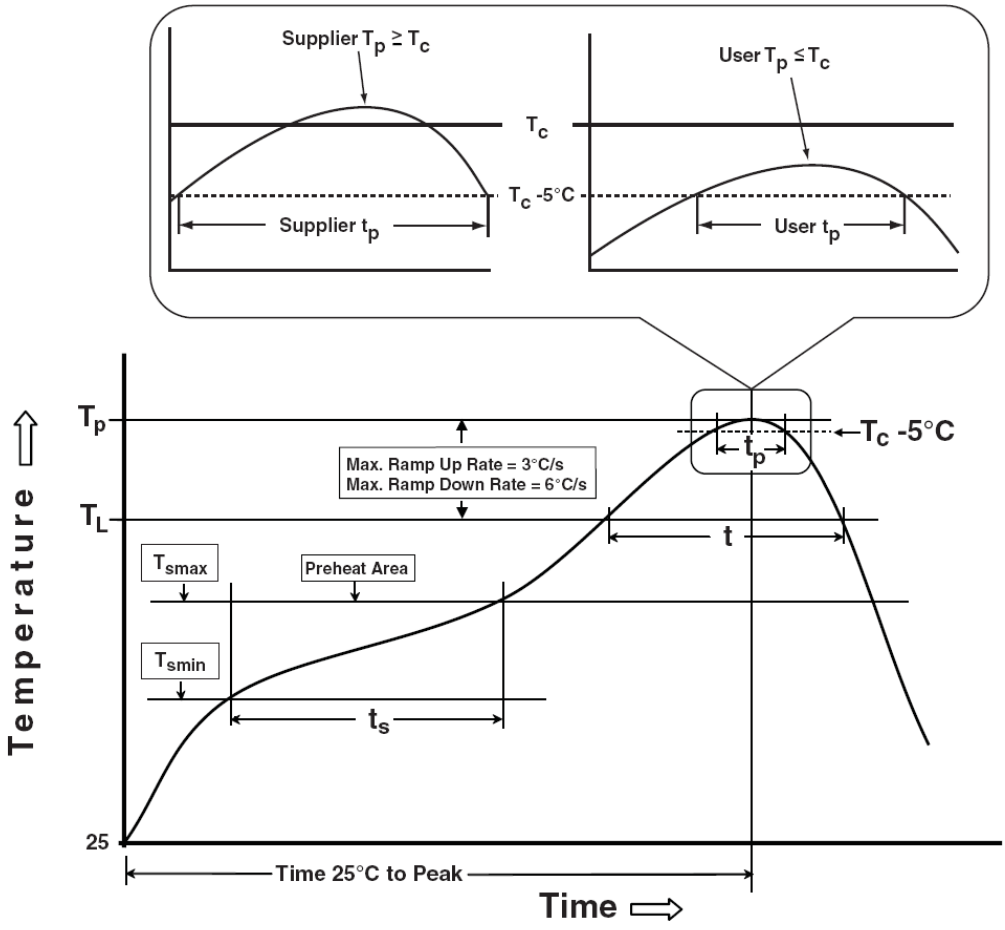
Package Type	Unit	Quantity
TQFN3x3-20	Tape & Reel	3000

Taping Direction Information

TQFN3x3-20



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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