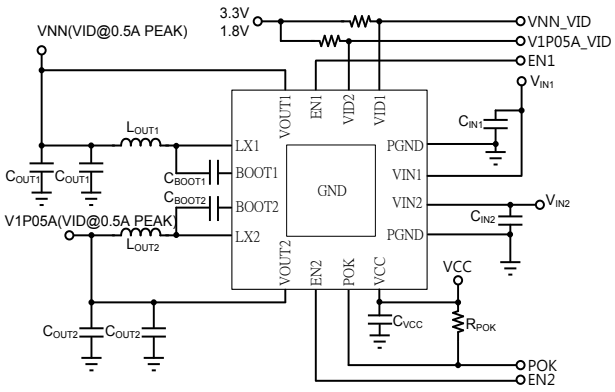
HV Dual Channels POL for Intel TGL VNN & V1P05A

Features

- **Support wide input voltage range from 4.5V to 24V**
- **1 high efficiency COT Mode with 0.5A output current capability for VNN_BYP**
- **1 high efficiency COT Mode with 0.5A output current capability for V1P05A_BYP**
- **Fixed 500KHz Switching Frequency for each channel**
- **Automatic switch over PWM/PFM Control**
- **Stable with low ESR Ceramic output capacitors**
- **Built VIN and VCC POR Control**
- **Built in Current Limit Protection with Latch off Mode**
- **Built in Under Voltage Protection with Latch off Mode**
- **Built in Over Voltage Protection with Latch off Mode**
- **Built in Over Temperature Protection**
- **Built in Individual EN Control for VNN_BYP & V1P05A_BYP**
- **Built in One POK signal indicator for VNN_BYP & V1P05A_BYP**
- **Built in Individual VID Control for VNN_BYP & V1P05A_BYP**
- **TQFN 3x3-16B package**

Simplified Application Circuit

APW8743C/D/E



General Description

The APW8743C/D/E is a HV Dual Channels switching converter designed to provide supply voltages for Intel Tiger Lake(TGL)* VNN and V1P05A application. The device is specially designed to provide high efficiency at lighter loads in the range of 4 to 50mA as the application requires while providing peak currents of up to 500mA.

The APW8743C/D/E is equipped with an automatic PFM/PWM mode operation. At light load, the converter operates in the PFM mode to reduce the switching losses and provide high efficiency. At heavy load, the converter works in PWM mode and operates nearly at constant frequency for low-noise requirements.

The converter is also equipped with some practical protections include over-temperature(OTP), over-voltage (OVP), under-voltage (UVP) and accurate over-current protections (OCP) for various applications. The poweronreset function and soft-start used to prevent wrong operation and limit the input surge current during poweron or start-up. A soft-stop function actively discharges the output capacitors by built-in integrated output discharge method.

This device, available TQFN 3x3-16B for APW8743C/D/E, provides a very compact system solution external components and PCB area.

(*) Tiger Lake is trade mark of Intel Corp

Applications

- **Notebook**
- **Graphic card**
- **Motherboard**

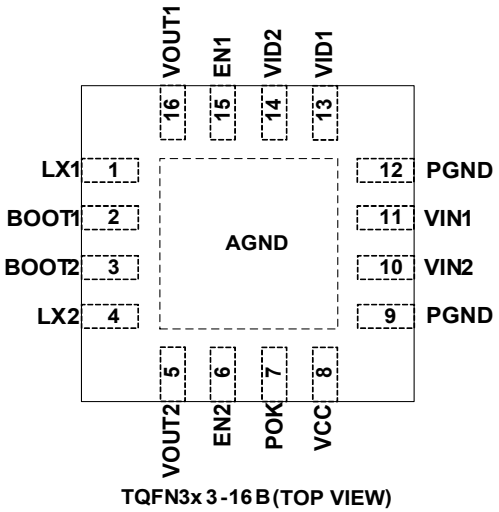
Ordering and Marking Information (Note 1)

<table>
<tr>
<td>APW8743 □□□□-□□□
Assembly Material
Handling Code
Temperature Range
Package Code
Product Code</td>
<td>Product Code
C, D or E, see below table for details
Package Code
QB: TQFN3x3-16B
Operating Ambient Temperature Range
I : -40 to 85 °C
Handling Code
TR : Tape & Reel
Lead Free Code
L : Lead Free Device G : Halogen and Lead Free Device</td>
</tr>
<tr>
<td>APW8743CQBI : APW 8743C XXXXX XXXXX - Date Code</td>
<td>APW8743DQBI : APW 8743D XXXXX XXXXX - Date Code</td>
</tr>
<tr>
<td>APW8743EQBI : APW 8743E XXXXX XXXXX - Date Code</td>
<td></td>
</tr>
</table>

Note1: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Part Number	VID=0(VNN)	VID=1(VNN)	VID=0(V1P05A)	VID=1(V1P05A)
APW8743CQBI	1.05V	0.78V	1.05V	0.96V
APW8743DQBI	0.78V	0.7V	1.05V	0.96V
APW8743EQBI	1.05V	0.7V	1.05V	0.96V

Pin Configuration



TQFN3x3-16B (TOP VIEW)

Absolute Maximum Ratings (Note 2)

Symbol	Parameter		Rating	Unit
V_{CC}	VCC Supply Voltage (VCC to AGND)		-0.3 ~ 7	V
V_{IN1}	VNN VIN Supply Voltage (VIN to AGND) <20ns pulse width >20ns pulse width		-0.3 ~ 26 -0.3 ~ 24	V
V_{IN2}	V1P05A VIN Supply Voltage (VIN to AGND) <20ns pulse width >20ns pulse width		-0.3 ~ 26 -0.3 ~ 24	V
$V_{BOOT1-GND}$	VNN BOOT Supply Voltage (BOOT to AGND)		-0.3 ~ 31	V
$V_{BOOT2-GND}$	V1P05A BOOT Supply Voltage (BOOT to AGND)		-0.3 ~ 31	V
V_{BOOT1}	VNN BOOT Supply Voltage (BOOT to LX)		V_{LX} -0.3 ~ V_{LX} +7	V
V_{BOOT2}	V1P05A BOOT Supply Voltage (BOOT to LX)		V_{LX} -0.3 ~ V_{LX} +7	V
V_{GND}	AGND to PGND		-0.3 ~ +0.3	V
	All Other Pins (POK, EN1, EN2, VOUT1, VOUT2, VID1, VID2)		-0.3 ~ 7	V
V_{LX1}	VNN LX Voltage (LX1 to GND) <20ns pulse width >20ns pulse width		-5 ~ 30 -1 ~ 24	V
V_{LX2}	V1P05A LX Voltage (LX2 to GND) <20ns pulse width >20ns pulse width		-5 ~ 30 -1 ~ 24	V
$V_{IN1-LX1}$	VIN1 to LX1 Voltage <20ns pulse width >20ns pulse width		-5 ~ 29 -1 ~ 24	V
$V_{IN2-LX2}$	VIN2 to LX2 Voltage <20ns pulse width >20ns pulse width		-5 ~ 29 -1 ~ 24	V
P_D	Power Dissipation		Internally Limited	W
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature		-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature(10 Seconds)		260	°C
V_{ESD}	Minimum ESD Rating (Note 3)	Human Body Mode	±2	kV
		MM Mode	0.2	kV

Note 2: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Note 3: The device is ESD sensitive. Handling precautions are recommended.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance (Note 4)	50	°C/W
θ_{JC}	Junction-to-case(top) Thermal Resistance	34.5	°C/W

Note 4: θ_{JA},θ_{JC} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operation Conditions (Note 5)

Symbol	Parameter	Range	Unit
V_{CC}	VCC Supply Voltage	4.5 ~ 5.5	V
V_{IN1}	VNN Converter Input Voltage	4.5 ~ 24	V
V_{IN2}	V1P05A Converter Input Voltage	4.5 ~ 24	V
I_{OUT1}	VNN Converter Output Current	0 ~ 0.5	A
I_{OUT2}	V1P05A Converter Output Current	0 ~ 0.5	A
L_{OUT1}	VNN Converter Output Inductor	0.68~1	μH
L_{OUT2}	V1P05A Converter Output Inductor	10 ~ 22	μH
C_{IN1}	VNN Converter Input Capacitor (MLCC)	4.7 ~ 20	μF
C_{IN2}	V1P05A Converter Input Capacitor (MLCC)	4.7 ~ 20	μF
C_{OUT1}	VNN Converter Output Capacitor (MLCC)	20 ~ 50	μF
C_{OUT2}	V1P05A Converter Output Capacitor (MLCC)	20 ~ 50	μF
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 5: Refer to the typical application circuit

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=8.4V, V_{EN}=5V and T_A= -40 to 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
INPUT VOLTAGE (for VNN and V1P05A)						
V_{IN1}	VNN VIN POR Voltage Threshold	V_{IN} Rising	3.5	3.7	3.9	V
	VNN VIN POR Hysteresis		-	0.2	-	V
V_{IN2}	V1P05A VIN POR Voltage Threshold	V_{IN} Rising	3.5	3.7	3.9	V
	V1P05A VIN POR Hysteresis		-	0.2	-	V
SWITCHING FREQUENCY (for VNN and V1P05A)						
F_{OSC}	Switching Frequency		-	0.5	-	MHz
OUTPUT VOLTAGE (for VNN and V1P05A)						
V_{OUT1}	VNN Output Voltage	VID = 0 (APW8743C Only)	-	1.05	-	V
		VID = 1 (APW8743C Only)	-	0.78	-	V
	VNN Output Voltage Accuracy	T_A = 25 °C	-0.6	-	+0.6	%
		T_A = -40 ~ 85 °C	-1	-	+1	%
	VNN Load Transient Drop (VVNN=1.05V)	I_{OUT1} = 0mA ~ 350mA	-4	-	+4	%
		I_{OUT1} = 150mA ~ 500mA	-4	-	+4	%
	VNN Load Transient Drop (V_{VNN}=0.70V)	I_{OUT1} = 0mA ~ 350mA	-4	-	+4	%
		I_{OUT1} = 150mA ~ 500mA	-4	-	+4	%
V_{OUT2}	V1P05A Output Voltage	VID = 0	-	1.05	-	V
		VID = 1	-	0.96	-	V
	V1P05A Output Voltage Accuracy	T_A = 25 °C	-0.6	-	+0.6	%
		T_A = -40 ~ 85 °C	-1	-	+1	%
	V1P05A Transient Drop (V_{OUT2} = 1.05V)	I_{OUT2} = 0mA ~ 350mA	-4	-	+4	%
		I_{OUT2} = 150mA ~ 500mA	-4	-	+4	%
	V1P05A Transient Drop	I_{OUT2} = 0mA ~ 350mA	-4	-	+4	%
	(V_{OUT2} = 0.96V)	I_{OUT2} = 150mA ~ 500mA	-4	-	+4	%
$R_{\_DIS1}$	VNN VOUT Discharge Resistance		-	10	-	Ω
$R_{\_DIS2}$	V1P05A VOUT Discharge Resistance		-	10	-	Ω
VCC POR THRESHOLD (for VNN and V1P05A)						
V_{CC}	VCC POR Voltage Threshold	V_{IN} Rising	-	4.2	-	V
	VCC POR Hysteresis		-	0.2	-	V

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=8.4V, V_{EN}=5V and T_A= -40 to 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY CURRENT (for VNN and V1P05A)						
I_{VCC}	VCC Supply Current	V_{OUT1} = 0.8V & V_{OUT2} = 1.1V , SW is no switching	-	65	80	uA
I_{VCC_SD}	VCC Shutdown Current	V_{EN1}= 0V & V_{EN2}= 0V.	-	3	5.5	uA
I_{VIN1}	VNN VIN Supply Current	V_{OUT1} = 1.2V, SW is no switching	1	17	20	uA
I_{VIN1_SD}	VNN VIN Shutdown Current	V_{EN1}= 0V.	-	3	5.5	uA
I_{VIN2}	V1P05A VIN Supply Current	V_{OUT2}=1.2V, SW is no switching	1	17	20	uA
I_{VIN2_SD}	V1P05A VIN Shutdown Current	V_{EN2}= 0V.	-	3	5.5	uA
CONTROL (ENx , VIDx)						
V_H	High Level Input Threshold Voltage	For ENx, VIDx	1.5	-	-	V
V_L	Low Level Input Threshold Voltage	For ENx, VIDx	-	-	0.4	V
I_{LKG}	Input Leakage Current at ENx, VIDx	V_{ENx} = VIDx = 5V	-	1.0	-	uA
$T_{\_EN}$	ENx Turn on delay time		-	20	-	us
	ENx Turn off delay time		-	10	-	us
POWER-OK INDICATOR (for VNN and V1P05A)						
POK	POK Threshold (OTP occur, POK always go low)	$V_{OUT / VREF}$, POK go high from Lower	85	90	95	%
		Hysteresis	-	5	-	%
		$V_{OUT / VREF}$, POK go low from Normal	1.155	1.26	1.365	V
	POK Sink Current	V_{POK}=0.5V	-	3	-	mA
	POK Impedance		-	-	400	Ω
$T_{\_DELAY}$	POK Enable Delay time	EN1 and EN2 are all High to POK High	-	1.5	-	ms
	POK Disable Delay time	EN1 or EN2 goes low or VOUT1 or VOUT2 down to 85% or up to 1.26V	-	5	-	us
CURRENT SENSE (for VNN and V1P05A)						
$I_{\_LIM1\_N}$	VNN Low side Current Limit		0.8	1.2	1.6	A
$I_{\_LIM2\_N}$	V1P05A Low side Current Limit		0.9	1.2	1.5	A
	Current Limit response time		-	2	-	us
SOFT START (for VNN and V1P05A)						
T_{SS}	Soft-Start slew rate	EN1 = H, VIN is higher than POR	-	10	-	mV/us
	VOUT1 Transition slew rate	V_{OUT1} from 1.05V to 0.78V to 1.05V	-	10	20	mV/us
	VOUT2 Transition slew rate	V_{OUT2} from 1.05V to 0.96V to 1.05V	-	10	20	mV/us

Electrical Characteristics

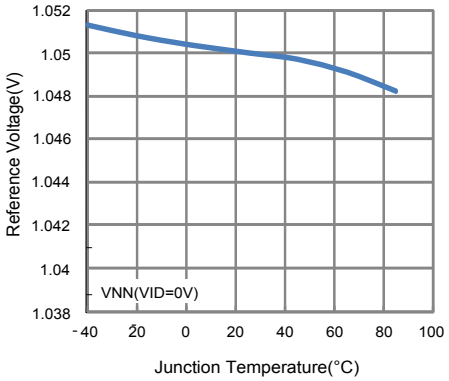
Unless otherwise specified, these specifications apply over V_{IN}=8.4V, V_{EN}=5V and T_A= -40 to 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
PROTECTION (for VNN and V1P05A)						
V_{OVP_VNN}	Over Voltage Protection	$V_{OUT}/V_{OUT(MON)}$	1.155	1.26	1.365	V
	Over Voltage Protection delay time		-	8	-	us
V_{OVP_V1P05A}	Over Voltage Protection	$V_{OUT}/V_{OUT(MON)}$	1.155	1.26	1.365	V
	Over Voltage Protection delay time		-	8	-	us
V_{UVP}	Under Voltage Protection	$V_{OUT}/V_{OUT(MON)}$	-	70	-	%
	Under Voltage Protection delay time		-	5	-	us
T_{OTP}	OTP Rising Threshold	Guaranteed by Design	-	145	-	°C
	OTP Hysteresis	Guaranteed by Design	-	45	-	°C
INTERNAL POWER SWITCH (for VNN and V1P05A)						
$R_{DS1(ON)H}$	VNN NMOS_HI ON Resistance	V_{CC}=5V	-	210	-	mΩ
$R_{DS1(ON)L}$	VNN NMOS_LO ON Resistance	V_{CC}=5V	-	90	-	mΩ
$R_{DS2(ON)H}$	V1P05A NMOS_HI ON Resistance	V_{CC}=5V	-	430	-	mΩ
$R_{DS2(ON)L}$	V1P05A NMOS_LO ON Resistance	V_{CC}=5V	-	160	-	mΩ
BOOTSTRAP SWITCH Resistance (for VNN and V1P05A)						
$R_{\_BOOT1}$	VNN Bootstrap Switch On Resistance		-	5	-	Ω
$R_{\_BOOT2}$	V1P05A Bootstrap Switch On Resistance		-	5	-	Ω

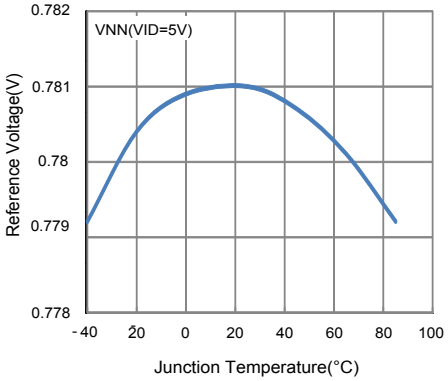
Typical Operating Characteristics

Refer to the typical application circuit. The test condition is V_{IN}=8.4V, L_{OUT1}=1μH, L_{OUT2} =10μH,C_{OUT}(VNN)=22μF*2, C_{OUT}(V1.05A)=22μF*2, T_A= 25°C unless otherwise specified.

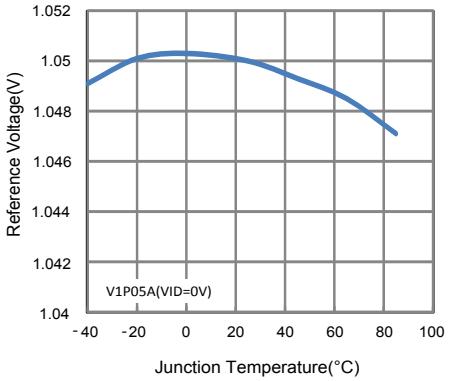
Reference Voltage vs. Junction Temperature



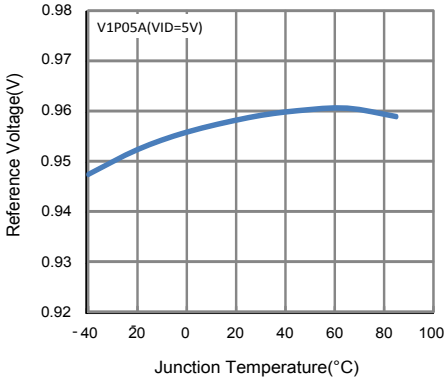
Reference Voltage vs. Junction Temperature



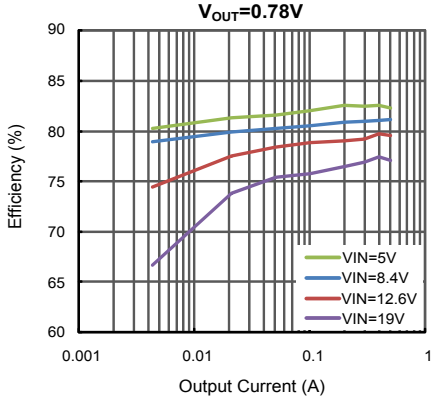
Reference Voltage vs. Junction Temperature



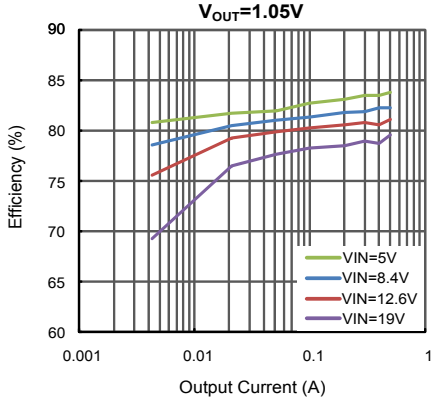
Reference Voltage vs. Junction Temperature



VNN Efficiency vs. Output Current
V_{OUT}=0.78V

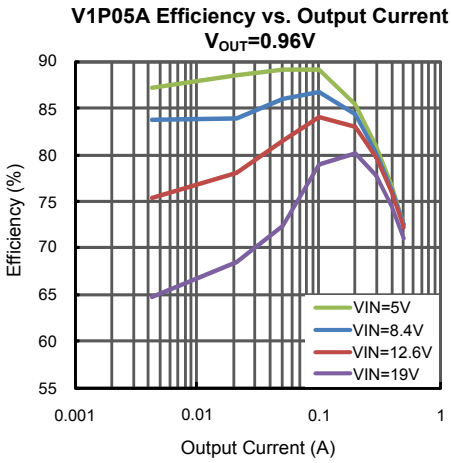


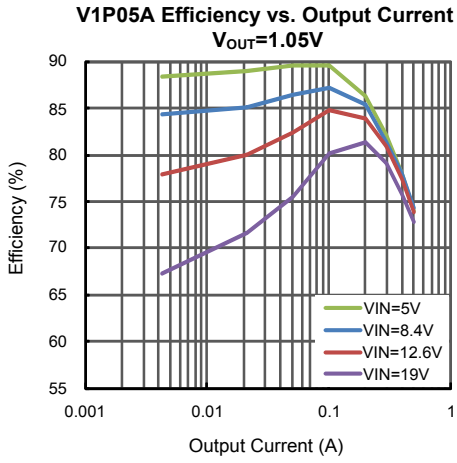
VNN Efficiency vs. Output Current
V_{OUT}=1.05V



Typical Operating Characteristics (Cont.)

Refer to the typical application circuit. The test condition is V_{IN}=8.4V, L_{OUT1}=1μH, L_{OUT2} =10μH,C_{OUT}(VNN)=22μF*2, C_{OUT}(V1.05A)=22μF*2, T_A= 25°C unless otherwise specified.

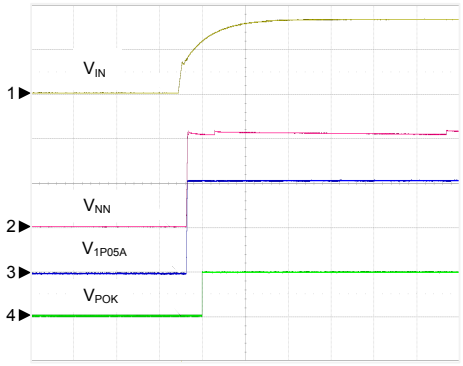




Operating Waveforms

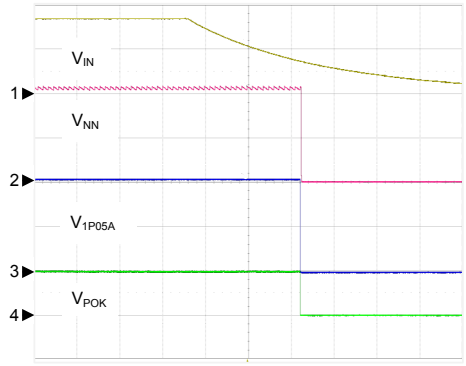
Refer to the typical application circuit. The test condition is V_{IN}=8.4V, L_{OUT1}=1μH, L_{OUT2} =10μH,C_{OUT}(VNN)=22μF*2, C_{OUT}(V1.05A)=22μF*2, T_A= 25°C unless otherwise specified.

Power On



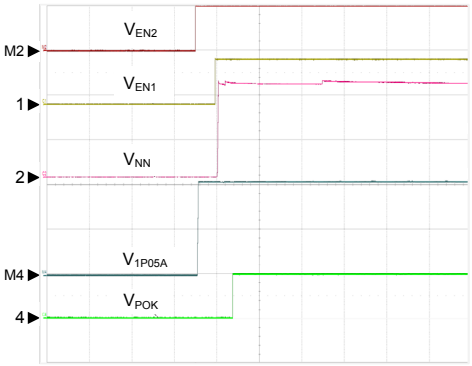
CH1: V_{IN}, 5V/Div, DC
CH2: V_{NN}, 500mV/Div, DC
CH3: V_{1P05A}, 500mV/Div, DC
CH4: V_{POK}, 5V/Div, DC
TIME: 5ms/Div

Power Off



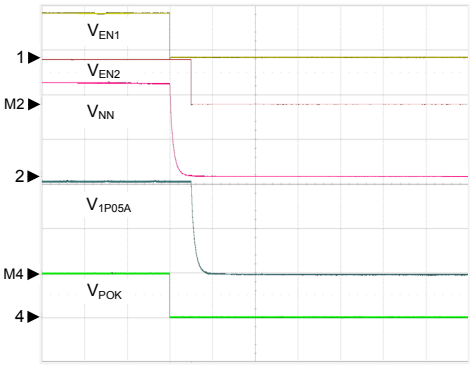
CH1: V_{IN}, 5V/Div, DC
CH2: V_{NN}, 500mV/Div, DC
CH3: V_{1P05A}, 500mV/Div, DC
CH4: V_{POK}, 5V/Div, DC
TIME: 500ms/Div

Enable



CH1: V_{EN1}, 5V/Div, DC
CH2: V_{NN}, 500mV/Div, DC
CH4: V_{POK}, 5V/Div, DC
CHM2: V_{EN2}, 5V/Div, DC
CHM4: V_{1P05A}, 500mV/Div, DC
TIME: 5ms/Div

Shutdown

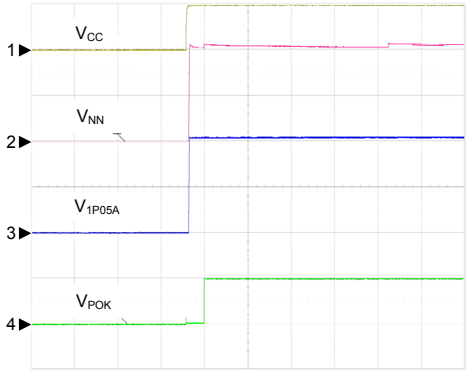


CH1: V_{EN1}, 5V/Div, DC
CH2: V_{NN}, 500mV/Div, DC
CH4: V_{POK}, 5V/Div, DC
CHM2: V_{EN2}, 5V/Div, DC
CHM4: V_{1P05A}, 500mV/Div, DC
TIME: 5ms/Div

Operating Waveforms (Cont.)

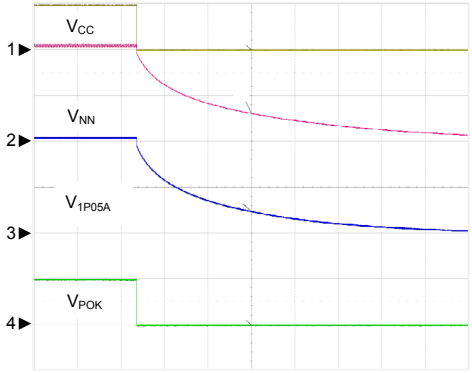
Refer to the typical application circuit. The test condition is V_{IN}=8.4V, L_{OUT1}=1μH, L_{OUT2} =10μH,C_{OUT}(VNN)=22μF*2, C_{OUT}(V1.05A)=22μF*2, T_A= 25°C unless otherwise specified.

VCC Power On



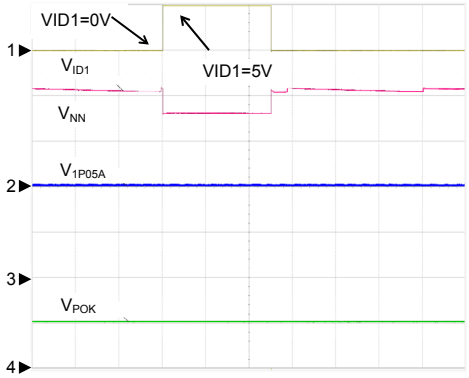
CH1: V_{CC}, 5V/Div, DC
CH2: V_{NN}, 500mV/Div, DC
CH3: V_{1P05A}, 500mV/Div, DC
CH4: V_{POK}, 5V/Div, DC
TIME: 5ms/Div

VCC Power Off



CH1: V_{CC}, 5V/Div, DC
CH2: V_{NN}, 500mV/Div, DC
CH3: V_{1P05A}, 500mV/Div, DC
CH4: V_{POK}, 5V/Div, DC
TIME: 2s/Div

VNN Dynamic Voltage Change



CH1: V_{ID1}, 5V/Div, DC
CH2: V_{NN}, 500mV/Div, DC
CH3: V_{1P05A}, 500mV/Div, DC
CH4: V_{POK}, 5V/Div, DC
TIME: 20ms/Div

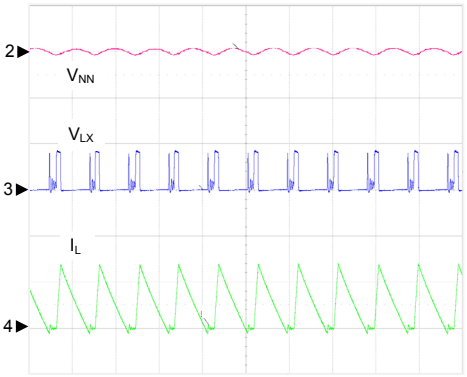
V1P05A Dynamic Voltage Change

CH1: V_{ID2}, 5V/Div, DC
CH2: V_{NN}, 500mV/Div, DC
CH3: V_{1P05A}, 500mV/Div, DC
CH4: V_{POK}, 5V/Div, DC
TIME: 20ms/Div

Operating Waveforms (Cont.)

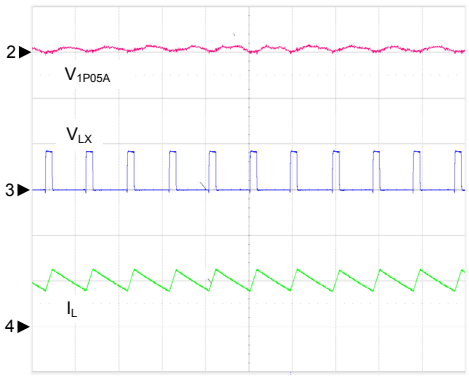
Refer to the typical application circuit. The test condition is V_{IN}=8.4V, L_{OUT1}=1μH, L_{OUT2} =10μH,C_{OUT}(VNN)=22μF*2, C_{OUT}(V1.05A)=22μF*2, T_A= 25°C unless otherwise specified.

Normal Operation



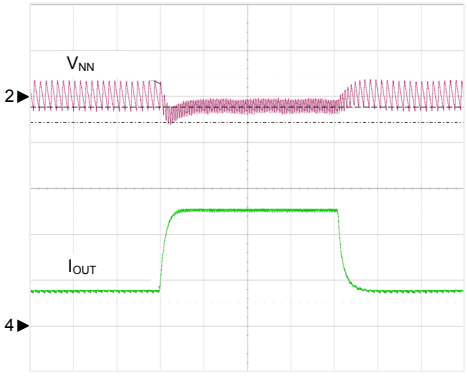
CH2: V_{NN}, 100mV/Div, DC offset 1.05V
CH3: V_{LX}, 10V/Div, DC
CH4: I_L, 1A/Div, DC
TIME: 2μs/Div

Normal Operation



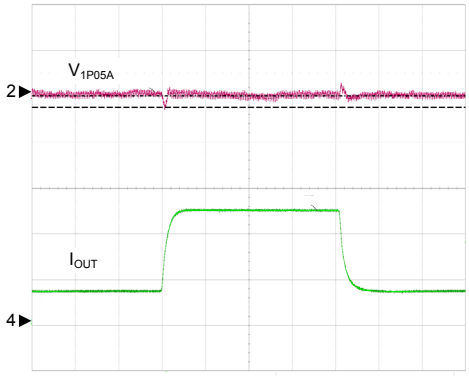
CH2: V_{1P05A}, 20mV/Div, DC offset 1.05V
CH3: V_{LX}, 10V/Div, DC
CH4: I_L, 500mA/Div, DC
TIME: 2μs/Div

Load Transition Response



I_{OUT},=0.15A to 0.5A to 0.15A
CH1: V_{NN}, 50mV/Div, DC offset 1.05V
CH2: I_{OUT}, 200mA/Div, DC
TIME: 50μs/Div

Load Transition Response

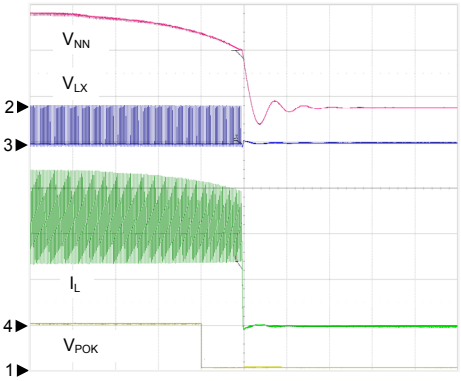


I_{OUT},=0.15A to 0.5A to 0.15A
CH1: V_{1P05A}, 20mV/Div, DC offset 1.05V
CH2: I_{OUT}, 200mA/Div, DC
TIME: 50μs/Div

Operating Waveforms (Cont.)

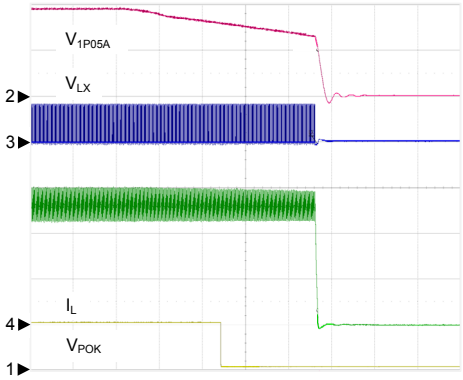
Refer to the typical application circuit. The test condition is V_{IN}=8.4V, L_{OUT1}=1μH, L_{OUT2} =10μH,C_{OUT}(VNN)=22μF*2, C_{OUT}(V1.05A)=22μF*2, T_A= 25°C unless otherwise specified.

OCP



CH1: V_{POK}, 5V/Div, DC
CH2: V_{NN}, 500mV/Div, DC
CH3: V_{LX}, 10V/Div, DC
CH4: I_L, 1A/Div, DC
TIME: 50μs/Div

OCP

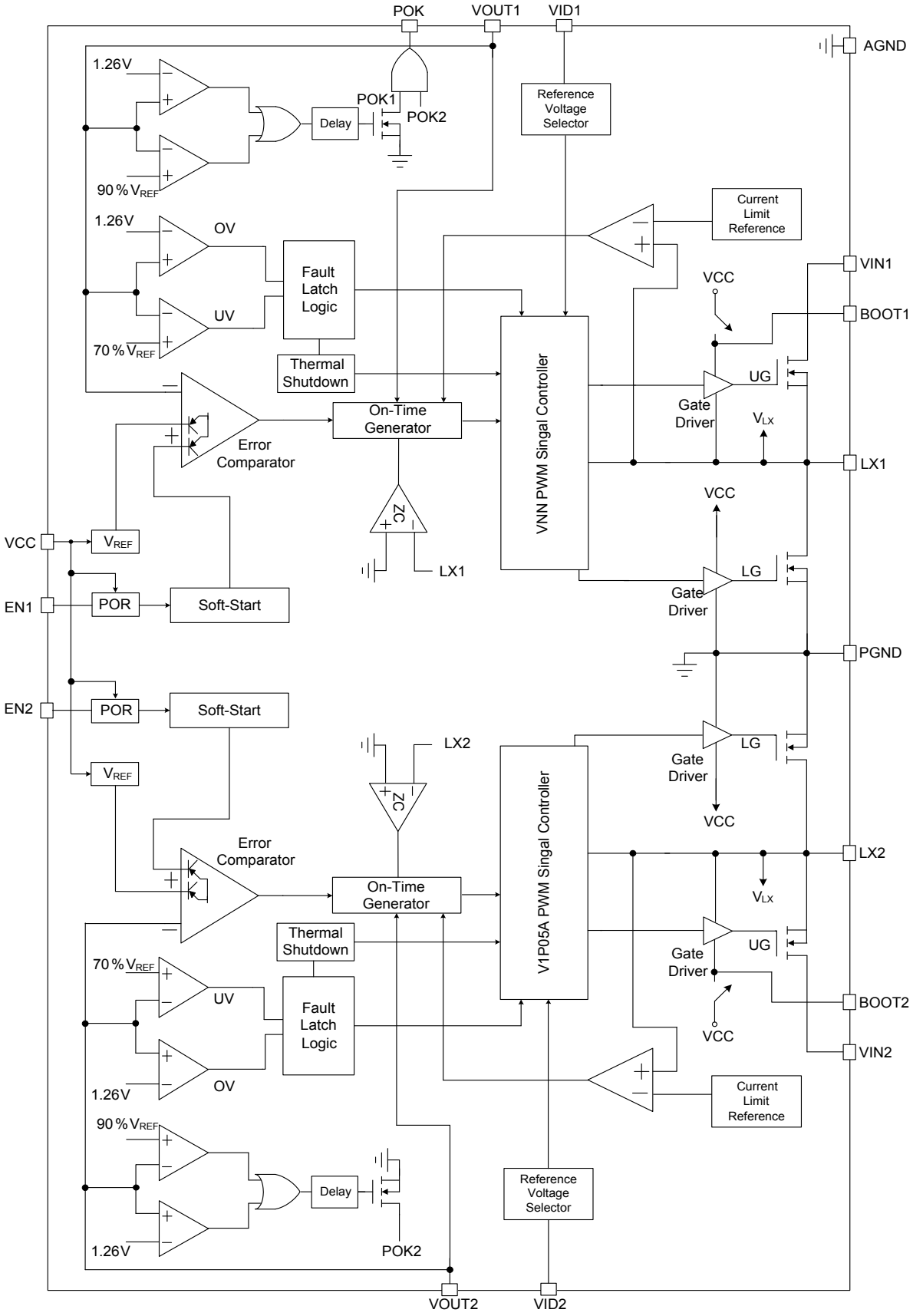


CH1: V_{POK}, 5V/Div, DC
CH2: V_{1P05A}, 500mV/Div, DC
CH3: V_{LX}, 10V/Div, DC
CH4: I_L, 500mA/Div, DC
TIME: 100μs/Div

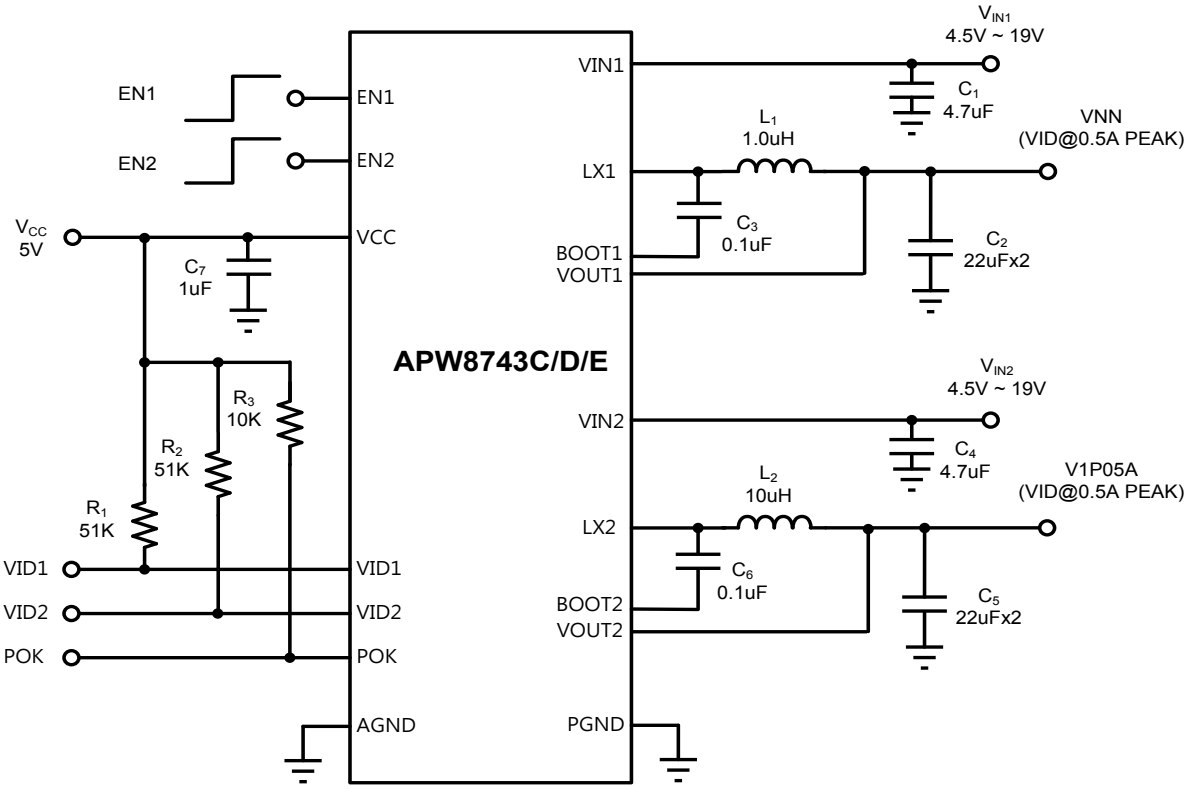
Pin Descriptions

PIN		FUNCTION
NO.	NAME	
1	LX1	Junction point of the High-Side MOSFET source, output filter inductor and the Low-Side MOSFET drain for VNN channel PWM. LX serves as the lower supply rail for the UGATE High-side gate driver. LX is the current-sense input for the PWM.
2	BOOT1	Supply Input for the VNN Channel UGATE gate driver and an internal level-shift circuit. Connect to an external capacitor to create a boosted voltage suitable to drive a logic-level N-channel MOSFET.
3	BOOT2	Supply Input for the V1P05A channel UGATE gate driver and an internal level-shift circuit. Connect to an external capacitor to create a boosted voltage suitable to drive a logic-level N-channel MOSFET.
4	LX2	Junction point of the High-Side MOSFET source, output filter inductor and the Low-Side MOSFET drain for V1P05A channel PWM. LX serves as the lower supply rail for the UGATE High-side gate driver. LX is the current-sense input for the PWM.
5	VOUT2	Output Voltage of V1P05A channel. VOUT2 pin is used to sense the output voltage of the V1P05A channel in order to keep the switching freq fixed when VID2 changes state
6	EN2	V1P05A channel PWM Enable. PWM is enabled when EN=1. When EN=0, PWM is in shutdown. EN pin can't be floate. It must be connected to high level or low level.
7	POK	Power-Good Output Pin of two channel. POK is valid when VNN & V1P05A is ready , and it is an open-drain output used to indicate the status of the PWM output voltage. Connect the POK in to VCC.
8	VCC	Supply voltage input pin for control circuitry, connect +5V from the VCC pin to the GND pin. Decoupling at least 1µF of a MLCC capacitor from the VCC pin to the AGND pin.
9	PGND	Power Ground of The LGATE Low-Side MOSFET Drivers. Connect directly to the GND plane.
10	VIN2	Battery Voltage Input Pin. The APW8743C/D/E V1P05A channel operates from a +4.5V to +24V input rail. Must be closely decoupled to GND with 4.7µF or greater ceramic capacitor.
11	VIN1	Battery Voltage Input Pin. The APW8743C/D/E VNN channel operates from a +4.5V to +24V input rail. Must be closely decoupled to GND with 4.7µF or greater ceramic capacitor.
12	PGND	Power Ground of The LGATE Low-Side MOSFET Drivers. Connect directly to the GND plane.
13	VID1	VID1 control input to get different reference voltage for different output rails on VNN channel.
14	VID2	VID2 control input to get different reference voltage for different output rails on V1P05A channel.
15	EN1	VNN channel PWM Enable. PWM is enabled when EN=1. When EN=0, PWM is in shutdown. EN pin can't be floate. It must be connected to high level or low level.
16	VOUT1	Output Voltage of VNN channel. VOUT1 pin is used to sense the output voltage of the VNN channel in order to keep the switching freq fixed when VID1 changes state
Exposed Pad	AGND	The pin is the Analog GND pin and must be connected directly via the exposed pad to the GND plane.

Block Diagram



Typical Application Circuit



VNN_BYPASS VID Table

VID1	Voltage(APW8743C)	Voltage(APW8743D)	Voltage(APW8743E)	Slew Rate
0	1.05V	0.78V	1.05V	10mV/us ~ 20mV/us
1	0.78V	0.7V	0.7V	10mV/us ~ 20mV/us

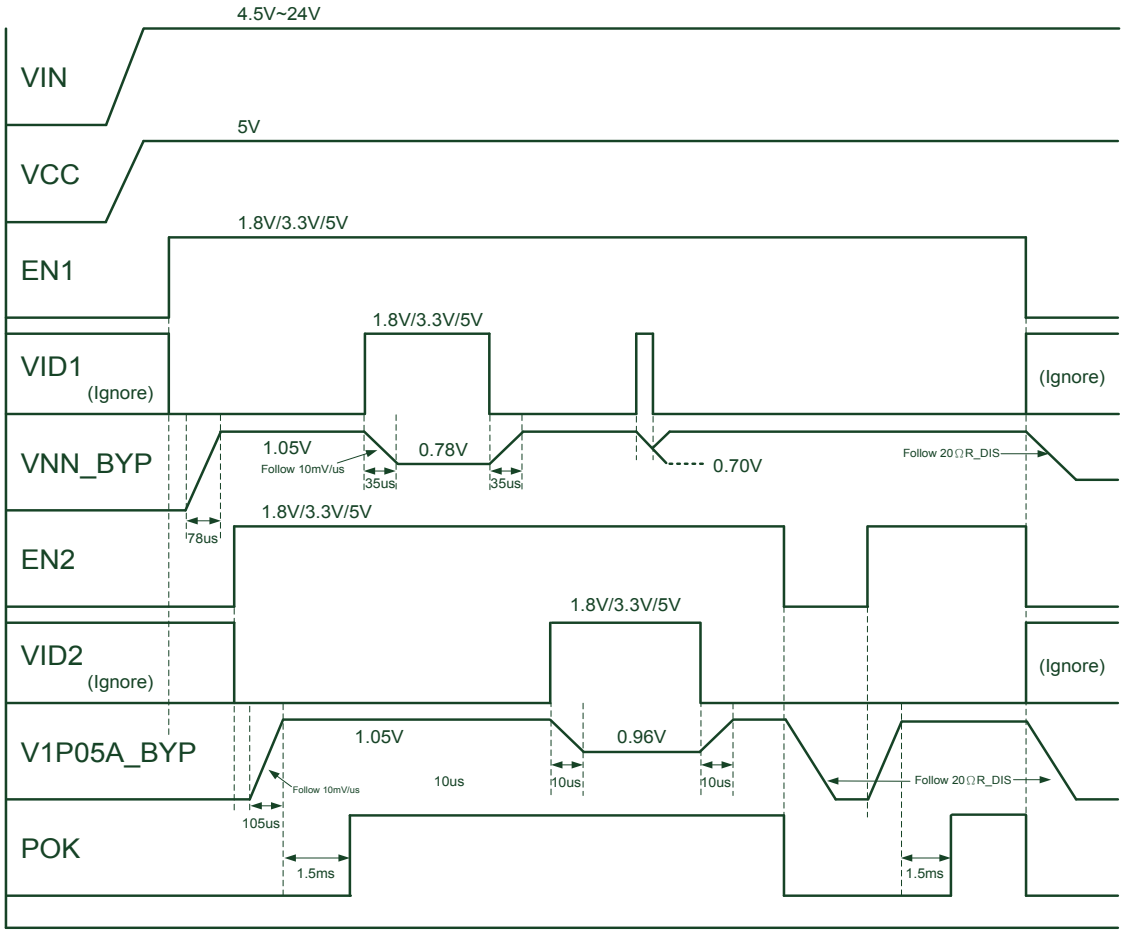
V1P05A_BYPASS VID Table

VID2	Voltage(APW8743C/D/E)	Slew Rate
0	1.05V	10mV/us ~ 20mV/us
1	0.96V	10mV/us ~ 20mV/us

Suggested BOM List

Designation	Manufacturer	Part No.	Description
C1, C4	Viking	MC06KTB500475	4.7μF, 50V, X7R, 1206
C2, C5	MuRata	GRM219R60J226ME47D	22μF, 6.3V, X5R, 0805
C3, C6	MuRata	GRM21BR71H104KA01L	0.1μF, 10V, X7R, 0805
C7	Viking	MC05KTB500105	1μF, 10V, X7R, 0805
L1	MuRata	DFE252012F-1R0M=P2	1μH, 2.5mmx2.0mm
L2	MuRata	1239AS-H-100M=P2	10μH, 2.5mmx2.0mm
R1,R2	Walsin	WR08X513	51KΩ, 0805
R3	Walsin	WR08X103	10kΩ, 0805

Power Sequence



Function Descriptions

Constant-On-Time PWM Controller with Input Feed-Forward

The APW8743C/D/E uses a pseudo fixed frequency constant on time architecture with internal ramp compensation allowing it to use ceramic type output capacitors. The ON time is inversely proportional with the input voltage and directly with output voltage of VNN and V1P05A such that switching freq is set to 500Khz if Vin changes or the VNN changes with the VID1 setting or the V1P05A changes with the VID2 setting . When IC enters the PFM mode, the fixed ON time ramps the output voltage above the error comparator threshold and once the ON time is finished the load discharges the output capacitor below the threshold and cycle continues. Another one-shot sets a minimum off-time (typical:250ns). The on-time one-shot is triggered if the error comparator is high, the low-side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

Pulse-Frequency Modulation (PFM) Mode

In PFM mode, an automatic switchover to pulse-frequency modulation (PFM) takes place at light loads. This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current zero crossing. This mechanism causes the threshold between PFM and PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the critical conduction point). The on-time of PFM is given by:

$$T_{ON-PFM} = \frac{1}{F_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

Where FSW is the nominal switching frequency of the converter in PWM mode.
The load current at handoff from PFM to PWM mode is given by:

$$I_{LOAD(PFM\ to\ PWM)} = \frac{1}{2} \times \frac{V_{IN} - V_{OUT}}{L} \times T_{ON-PFM}$$
$$= \frac{V_{IN} - V_{OUT}}{2L} \times \frac{1}{F_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

Power-On-Reset

A Power-On-Reset (POR) function is designed to prevent wrong logic controls when the VCC voltage is low. The POR function continually monitors the bias supply voltage on the VCC pin if at least one of the enable pins is set high. When the rising VCC voltage reaches the rising POR voltage threshold (4.2V, typical), the POR signal goes high and the chip initiates soft-start operations. Should this voltage drop lower than 4.0V (typical), the POR disables the chip.

EN Pin Control

When VEN is above the EN high threshold (1.5V, minimum), the converter is enabled. When VEN is below the EN low threshold (0.4V, maximum), the chip is in the shutdown and only low leakage current is taken from VCC.

Soft-Start

The APW8743C/D/E integrates soft-start circuits to ramp up the output voltage of the converter to the programmed regulation set point at a predictable slew rate. The slew rate of output voltage is internally controlled to limit the inrush current through the output capacitors during soft-start process. When the EN pin is pulled above the rising EN threshold voltage, the device initiates a soft-start process to ramp up the output voltage. During soft-start stage before the POK pin is ready, the under voltage protection is prohibited. The over voltage and current limit protection functions are enabled. If the output capacitor has residue voltage before startup, both low-side and high-side MOSFETs are in off-state until the soft start voltage equal the VOUT voltage. This will ensure the output voltage starts from its existing voltage level. In the event of under-voltage, over-voltage, over-temperature or shutdown, the chip enables the soft-stop function. The soft-stop function discharges the output voltages by low side turns MOSFET on linearly.

Power OK Indicator

In the soft-start process, the POK is an open-drain. When the soft-start is finished, the POK is released. In normal operation, POK is valid when VNN & V1P05A is ready, the POK window is greater than 90% of the converter reference voltage or less than 1.26V. When the VNN or V1P05A has to stay within this window, POK signal will become high. When the VNN or V1P05A outruns 90% of the target voltage or higher than 1.26V, POK signal will be pulled low immediately. In order to prevent false POK drop, capacitors need to parallel at the output to confine the voltage deviation with severe load step transient.

Under-Voltage Protection (UVP)

In the process of operation, if a short circuit occurs, the output voltage will drop quickly. When load current is bigger than current limit threshold value, the output voltage will fall out of the required regulation range. The under-voltage protection circuit continually monitors the VOUT voltage after soft-start is completed. If a load step is strong enough to pull the output voltage lower than the under voltage threshold, the under voltage threshold is 70% of the nominal output voltage, the internal UVP delay counter starts to count. After 3us de-bounce time, the device turns off both high side and low-side MOSEFET with latched. Toggling EN pin to low or recycling VIN will clear the latch and bring the chip back to operation.

Function Descriptions (Cont.)

Over-Voltage Protection (OVP)

The VNN Channel over voltage function monitors the output voltage by VOUT1 pin and V1P05A Channel over voltage function monitors the VOUT2 pin. VNN Channel should the VOUT1 increase over 1.26V due to the high-side MOSFET failure or for other reasons, V1P05A Channel should the VOUT2 increase over 1.26V due to the high-side MOSFET failure or for other reasons, the over voltage protection comparator designed with a 8μs noise filter will force the low-side MOSFET gate driver fully turn on and latch high. This action actively pulls down the output voltage.

This OVP scheme only clamps the voltage overshoot, and does not invert the output voltage when otherwise activated with a continuously high output from low-side MOSFET driver. It's a common problem for OVP schemes with a latch. Once an over-voltage fault condition is set, it can only be reset by toggling EN or VIN power-on-reset signal.

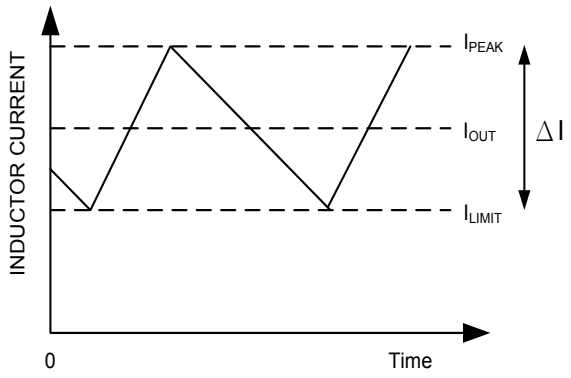
Current Limit

The current limit circuit employs a "valley" current-sensing algorithm (See Figure 1). The APW8743C/D/E uses the low-side MOSFET's $R_{DS(ON)}$ of the synchronous rectifier as a current-sensing element.

If the magnitude of the current-sense signal at LX pin is above the current-limit threshold 0.8A(minimum), the PWM is not allowed to initiate a new cycle. The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the sense resistance, inductor value, and input voltage.

The PWM controller uses the low-side MOSFETs on-resistance $R_{DS(ON)}$ to monitor the current for protection against shorted outputs. The MOSFET's $R_{DS(ON)}$ is varied by temperature and gate to source voltage, the user should determine the maximum $R_{DS(ON)}$ in manufacture's datasheet.

The PCB layout guidelines should ensure that noise and DC errors do not corrupt the current-sense signals at LX. Place the hottest power MOSEFTs as close to the IC as possible for best thermal coupling. When combined with the under-voltage protection circuit, this current-limit method is effective in almost every circumstance.



Over-Temperature Protection (OTP)

When the junction temperature increases above the rising threshold temperature T_{OTP}, the IC will enter the over temperature protection state that suspends the PWM, which forces the UG and LG gate drivers output low. The thermal sensor allows the converters to start a start-up process and regulate the output voltage again after the junction temperature cools by 45°C. The OTP designed with a 45°C hysteresis lowers the average T_J during continuous thermal overload conditions, which increases lifetime of the APW8743C/D/E.

Application Information

Output Inductor Selection

The duty cycle (D) of a buck converter is the function of the input voltage and output voltage. Once an output voltage is fixed, it can be written as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

The inductor value (L) determines the inductor ripple current, IRIPPLE, and affects the load transient response. Higher inductor value reduces the inductor's ripple current and induces lower output ripple voltage. The ripple current and ripple voltage can be approximated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{F_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Where F_{SW} is the switching frequency of the regulator. Although the inductor value and frequency are increased and the ripple current and voltage are reduced, a tradeoff exists between the inductor's ripple current and the regulator load transient response time.

A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current. Increasing the switching frequency (F_{SW}) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFETs and the power dissipation of the converter. The maximum ripple current occurs at the maximum input voltage.

The inductors in this application are selected such that it offers best overall efficiency while maintaing a good transient response. Once the inductance value has been chosen, selecting an inductor that is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This results in a larger output ripple voltage.

Besides, the inductor needs to have low DCR to reduce the loss of efficiency.

Output Capacitor Selection

Output voltage ripple and the transient voltage deviation are factors that have to be taken into consideration when selecting an output capacitor. Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, selecting high performance low ESR capacitors is recommended for switching regulator applications. In addition to high frequency noise related to MOSFET turn-on and turnoff, the output voltage ripple includes the capacitance voltage drop ΔV_{COUT} and ESR voltage drop ΔV_{ESR} caused by the AC peak-to-peak inductor's current. These two voltages can be represented by:

$$\Delta C_{OUT} = \frac{I_{RIPPLE}}{8 \times C_{OUT} \times F_{SW}}$$

$$\Delta V_{ESR} = I_{RIPPLE} \times R_{ESR}$$

Output Capacitor Selection (Cont.)

These two components constitute a large portion of the total output voltage ripple. In some applications, multiple capacitors have to be paralleled to achieve the desired ESR value. If the output of the converter has to support another load with high pulsating current, more capacitors are needed in order to reduce the equivalent ESR and suppress the voltage ripple to a tolerable level. A small decoupling capacitor (1µF) in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors are also must be considered.

To support a load transient that is faster than the switching frequency, more capacitors are needed for reducing the voltage excursion during load step change. Another aspect of the capacitor selection is that the total AC current going through the capacitors has to be less than the rated RMS current specified on the capacitors in order to prevent the capacitor from over-heating.

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, selecting the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage. The maximum RMS current rating requirement is approximately $I_{OUT}/2$, where IOUT is the load current. During power-up, the input capacitors have to handle great amount of surge current. For low-duty notebook applications, ceramic capacitor is recommended. The capacitors must be connected between the drain of high-side MOSFET and the source of low-side MOSFET with very low-impedance PCB layout.

Thermal Consideration

Because the APW8743C/D/E build-in high-side and low-side MOSFET, the heat dissipated may exceed the maximum junction temperature of the part in applications. If the junction temperature reaches approximately 150°C, both power switches will be turned off and the LX node will become high impedance. To avoid the APW8743C/D/E from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The main power dissipated by the part is approximated:

$$P_{UPPER} = I_{OUT}^2 (1+TC)(R_{DS(ON)})D + 0.5(I_{OUT})(V_{IN})(t_{SW})F_{SW}$$

$$P_{LOWER} = I_{OUT}^2 (1+TC)(R_{DS(ON)})(1-D)$$

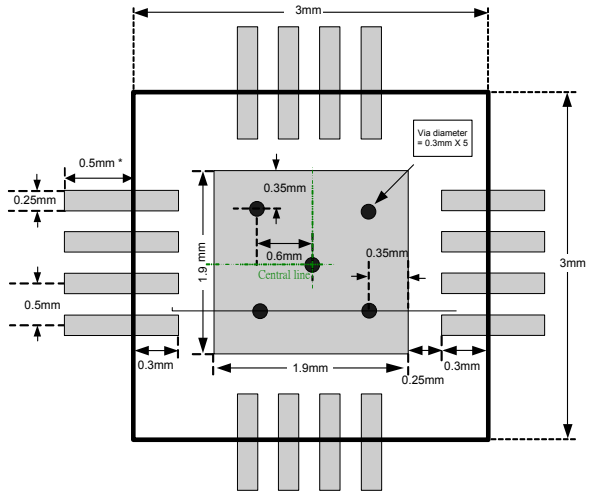
I_{OUT} is the load current
TC is the temperature dependency of $R_{DS(ON)}$
F_{SW} is the switching frequency
t_{SW} is the switching interval
D is the duty cycle

Note that both internal MOSFETs have conduction losses while the upper MOSFET include an additional transition loss. The switching internal, t_{SW}, is the function of the reverse transfer capacitance C_{RSS}. The (1+TC) term factors in the temperature dependency of the $R_{DS(ON)}$ and can be extracted from the "$R_{DS(ON)}$ vs. Temperature" curve of the power MOSFET.

Application Information (Cont.)

Recommended Minimum Footprint

TQFN3x3-16B (For APW8743C/D/E)



* Just Recommend

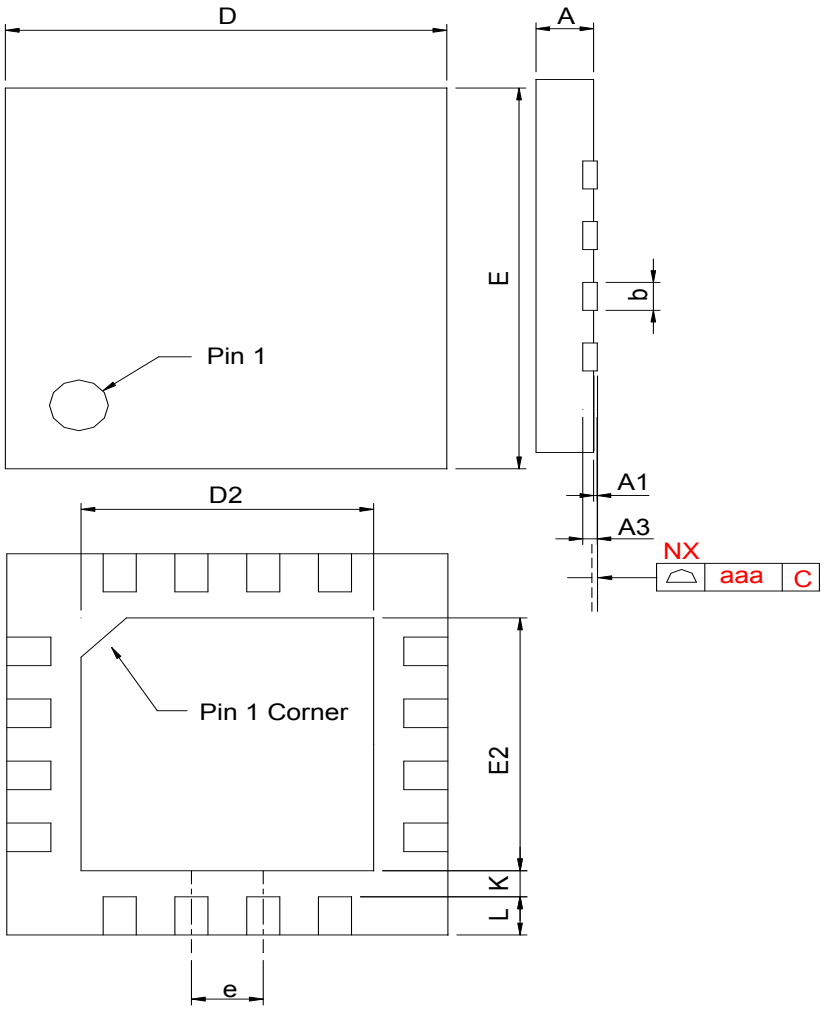
Thermal Consideration

In any high switching frequency converter, a correct layout Is important to ensure proper operation of the regulator. In general, using short and wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike. In addition, signal and power grounds are to be kept separating And finally combined using ground plane construction Or single point rounding. The signal ground and the power ground is at the negative Side of the output capacitor on each channel, where there is less noise. Noisy traces beneath the IC are not recommended. Below is a checklist for your layout:

1. Keep the switching nodes (BOOT, and LX) away from sensitive small signal nodes(VOUT) since these nodes are fast moving signals. Therefore, keep traces to these nodes as short as possible and there should be no other weak signal traces in parallel with theses traces on any layer.
2. Place the high-current paths (VIN, GND and LX) very close to the device and wide traces. The PGND trace should be as wide as possible (It should be the top priority).
3. Decoupling capacitors, the resistor-divider, and boot capacitor should be close to their pins. (For example, place the decoupling ceramic capacitor close to the drain of the high-side MOSFET as close as possible and on the same layer as the IC.)
4. The input bulk capacitors should be close to the drain of the high-side MOSFET, and the output bulk capacitors should be close to the loads. the input capacitor's ground should be close to the grounds of the output capacitors and low-side MOSFET.
5. VOUT pin traces can't be close to the switching signal traces (BOOT, and LX).
6. A 4-layer layout is strongly recommended to achieve better thermal performance.

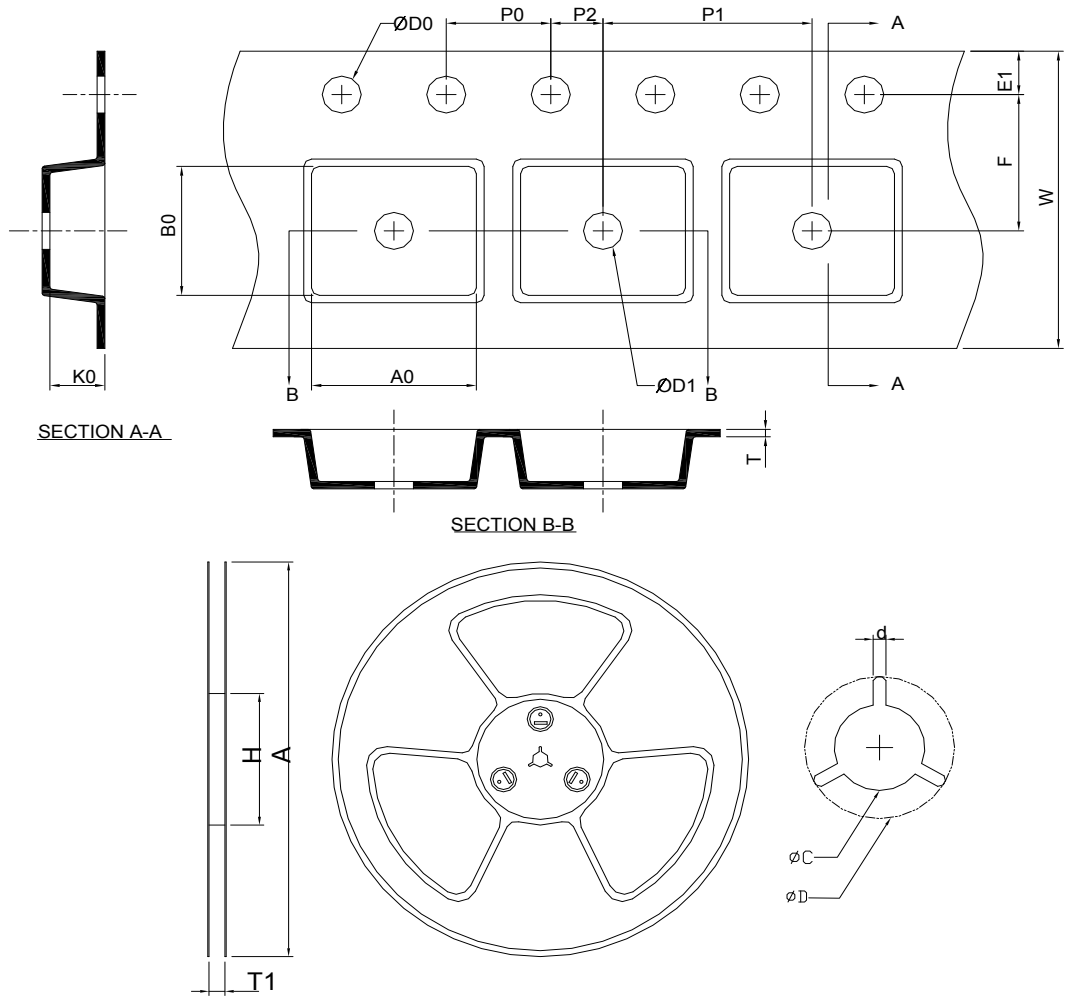
Package Information

TQFN3x3-16B



SYMBOL	TQFN3*3-16B			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.20	0.30	0.008	0.012
D	2.90	3.10	0.114	0.122
D2	1.80	2.00	0.071	0.079
E	2.90	3.10	0.114	0.122
E2	1.80	2.00	0.071	0.079
e	0.50 BSC		0.020 BSC	
L	0.25	0.35	0.010	0.014
K	0.20		0.008	
aaa	0.08		0.003	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN3x3	330±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.00±0.20

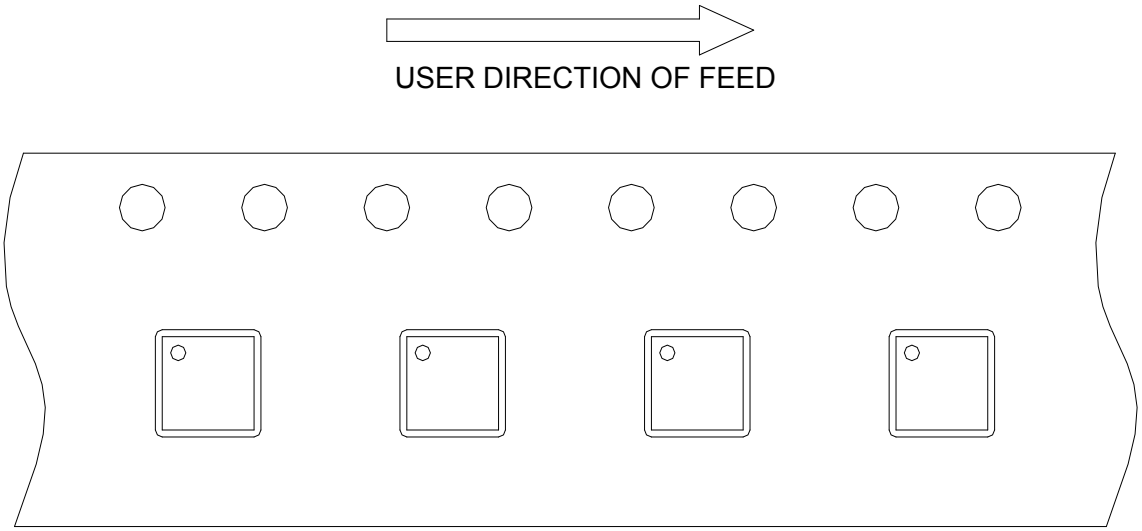
(mm)

Devices Per Unit

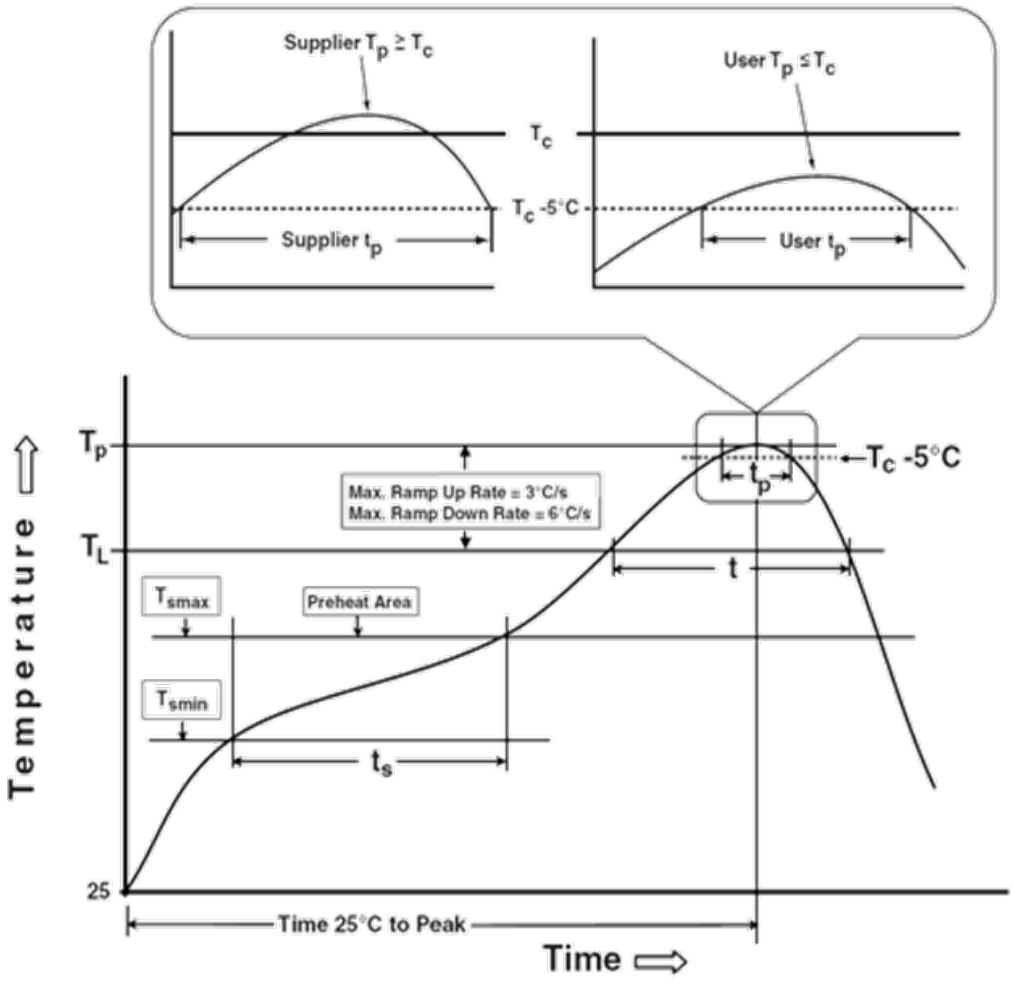
Package Type	Unit	Quantity
TQFN3x3	Tape & Reel	3000

Taping Direction Information

TQFN3x3-16B



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≧ 2KV
MM	JESD-22, A115	VMM ≧ 200V
Latch-Up	JESD 78	10ms, 1_{tr} ≧ 100mA

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