APW8830

3A 5V 1MHz Synchronous Buck Converter

Features

- **High Efficiency up to 95%**
  - Automatic Skip/PWM Mode Operation
- **Integrated 75mΩ High Side / 65mΩ Low Side MOSFETs**
- **Stable with Low ESR Ceramic Capacitors**
- **Power-On-Reset Detection on VDD and PVDD**
- **Integrated Soft-Start and Soft-Stop**
- **Over-Temperature Protection**
- **Over-Voltage Protection**
- **Under-Voltage Protection**
- **High/ Low Side Current Limit**
- **Power Good Indication**
- **Enable/Shutdown Function**
- **TDFN3x3-10 Package**
- **Lead Free and Green Devices Available (RoHS Compliant)**

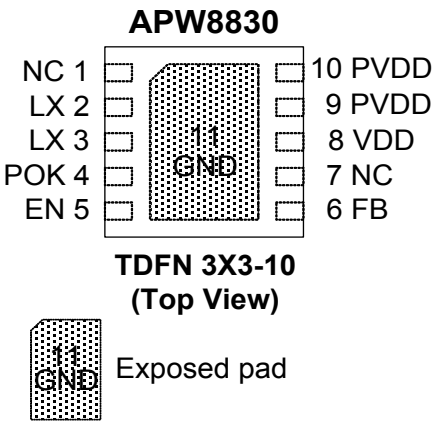
Applications

- **Notebook Computer & UMPC**
- **LCDMonitor/TV**
- **Set-Top Box**
- **DSL, Switch HUBr**
- **Portable Instrument**

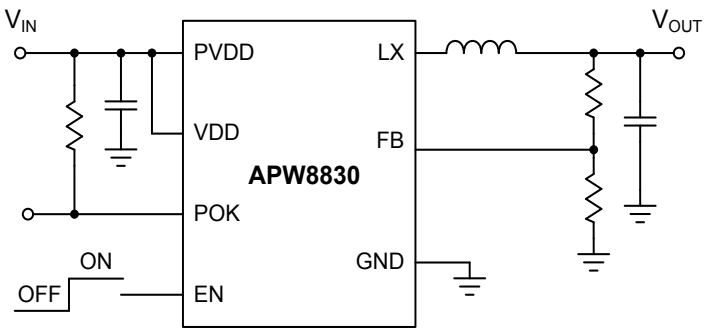
General Description

APW8830 is a 3A synchronous buck converter with integrated 75mΩ high side and 65mΩ low side power MOSFETs. The APW8830, design with a current-mode control scheme, can convert wide input voltage of 2.9V to 5.5V to provide excellent output voltage regulation.
The APW8830 is equipped with an automatic Skip/PWM mode operation. At light load , the IC operates in the Skip mode to reduce the switching losses. At heavy load, the IC works in PWM mode.
The APW8830 is also equipped with Power-on-reset, softstart, soft-stop, and whole protections (under-voltage, over-voltage, over-temperature and current-limit) into a single package.
This device, available TDFN3x3-10 , provides a very compact system solution external components and PCB area.

Pin Configuration



Simplified Application Circuit



ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information

APW8830 □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QB : TDFN3x3-10 Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW8830 QB : APW 8830 XXXXX	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter		Rating	Unit
V_{PVDD}, V_{VDD}	Input Supply Voltage		-0.3 ~ 6.5	V
V_{LX}	LX to GND Voltage	<50ns pulse width	-3 ~V_{PVDD}+3	V
		>50ns pulse width	-1 ~V_{PVDD}+0.3	V
	POK, FB, EN to GND Voltage		-0.3 ~ 6.5	V
P_D	Power Dissipation		2	W
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature		-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds		260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter		Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air (Note 2)	TDFN3x3-10	50	°C/W
θ_{JC}	Junction-to-Case Resistance in Free Air	TDFN3x3-10	10	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of TDFN3x3-10 is soldered directly on the PCB.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{VDD}	Control and Driver Supply Voltage	2.9~ 5.5	V
V_{PVDD}	Input Supply Voltage	2.9~5.5	V
I_{OUT}	Converter Output Current	0~3	A
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the typical application circuit.

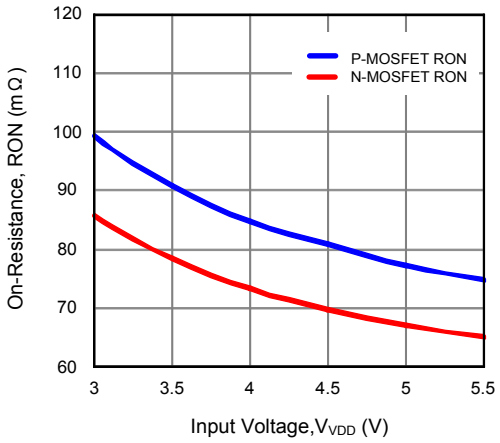
Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{VDD}=V_{PVDD}=5V, T_A=25°C.

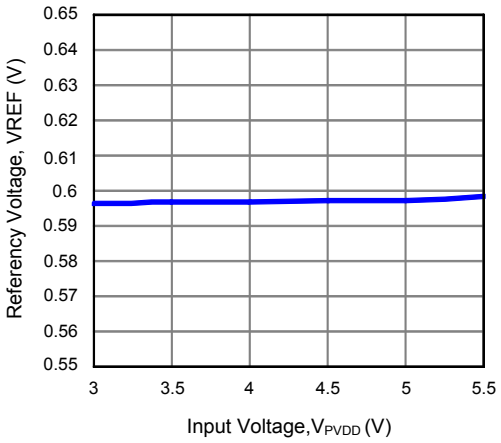
Symbol	Parameter	Test Conditions	APW8830			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
I_{VDD}	VDD Supply Current	V_{FB}=0.7V	-	65	-	μA
I_{VDD_SDH}	VDD Shutdown Supply Current	EN=GND	-	-	1	μA
POWER-ON-RESET (POR)						
	VDD POR Voltage Threshold	V_{VDD} Rising	2.3	2.4	2.5	V
	VDD POR Hysteresis		-	0.2	-	V
	PVDD POR Voltage Threshold		1.6	1.7	1.8	V
	PVDD POR Hysteresis		-	0.2	-	V
REFERENCE VOLTAGE						
V_{REF}	Reference Voltage		-	0.6	-	V
		All temperature	-1	-	+1	%
	Output Accuracy	I_{OUT}=10mA~3A, V_{PVDD}=2.9~5.5V	-1.5	-	+1.5	%
OSCILLATOR AND DUTY CYCLE						
F_{OSC}	Oscillator Frequency		0.85	1	1.15	MHz
	Minimum on Time		-	70	-	ns
POWER MOSFET						
	High Side P-MOSFET Resistance	V_{VDD}=5V, I_{LX}=0.5A, T_A=25°C	-	75	100	mΩ
	Low Side N-MOSFET Resistance	V_{VDD}=5V, I_{LX}=0.5A, T_A=25 °C	-	65	85	mΩ
	High/Low Side MOSFET Leakage Current		-	-	1	μA
PROTECTIONS						
I_{LIM}	High Side MOSFET current-limit	Peak Current, V_{VDD}=2.9~5.5V T_A= -40 ~125 °C	4	5	6	A
T_{OTP}	Over-temperature Trip Point (Resoft start after OTP)		-	160	-	°C
	Over-temperature Hysteresis		-	50	-	°C
	Over- Voltage Protection threshold	V_{OUT} Rising	120	125	130	%V_{REF}
	Under-Voltage Protection threshold		57	66	75	%V_{REF}
	Over-Voltage Protection debounce time		-	25	-	μs
	Low Side Switch Current-Limit	From Drain to Source	-	-1	-	A
SOFT-START, ENABLE, AND INPUT CURRENTS						
	Soft-Start Time		-	0.8	-	ms
	EN Enable Input High Voltage	V_{EN} rising voltage to enable device	1.4	-	-	V
	EN Shutdown Input Low Voltage	V_{EN} falling voltage to shutdown device	-	-	0.5	V
	EN Pull Low Current		-	0.5	1	μA
	POK Threshold	POK in from Lower (POK Goes High)	82.5	87.5	92.5	%V_{OUT}
		POK Low Hysteresis (POK Goes Low)	-	5	-	%V_{OUT}
		POK in from Higher (POK Goes High)	120	125	130	%V_{OUT}
	Power Good Pull Low Resistance		-	-	30	Ω
	Power Good Debounce	High to low	-	20	-	us

Typical Operating Characteristics

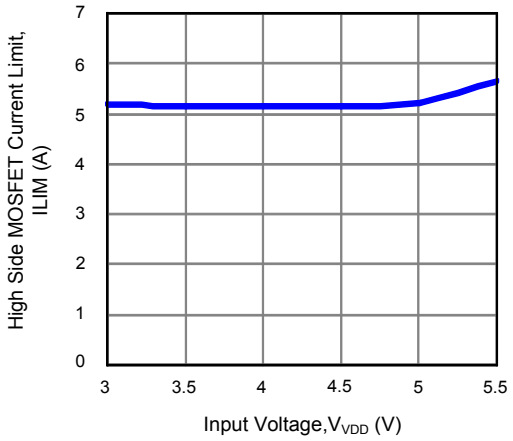
On-Resistance vs. Input Voltage



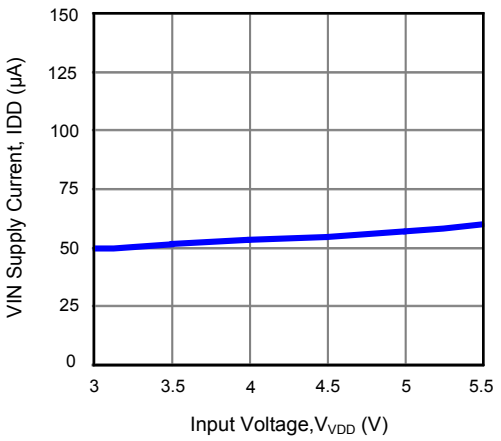
Referency Voltage vs. Input Voltage



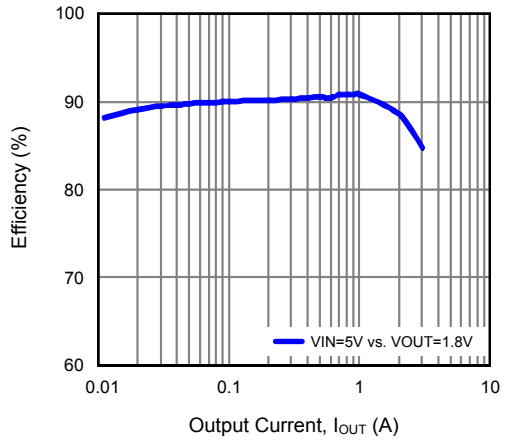
High Side MOSFET Current Limit vs. Input Voltage



VIN Supply Current vs. Input Voltage



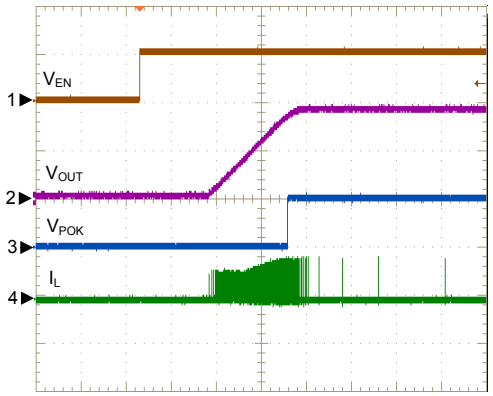
Efficiency vs. Load Current



Operating Waveforms

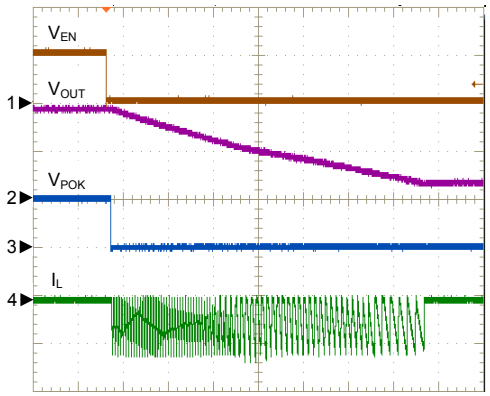
Refer to the typical application circuit. The test condition is V_{VDD}=V_{PVDD}=5V, V_{OUT}=1.8V, T_A= 25°C unless otherwise specified.

Enable without Loading



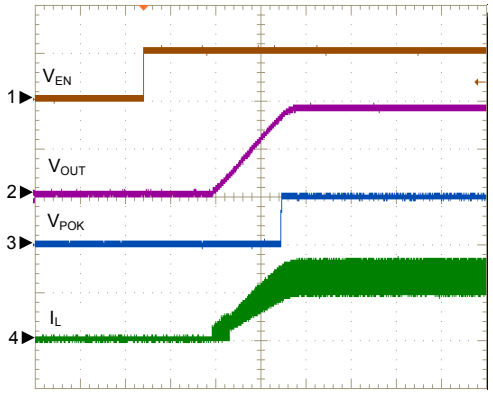
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 1V/Div, DC
CH3: V_{POK}, 5V/Div, DC
CH4: I_L, 1A/Div, DC
TIME: 400us/Div

Shutdown without Loading



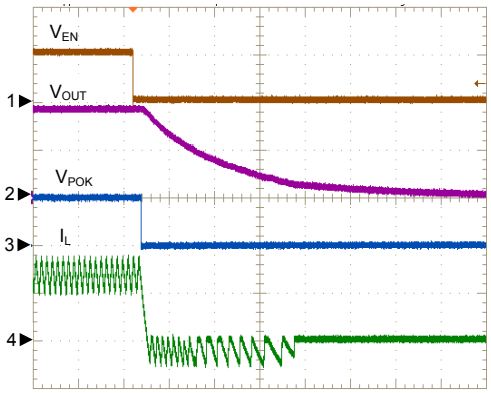
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 1V/Div, DC
CH3: V_{POK}, 5V/Div, DC
CH4: I_L, 1A/Div, DC
TIME: 20us/Div

Enable with 3A Loading



CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 1V/Div, DC
CH3: V_{POK}, 5V/Div, DC
CH4: I_L, 2A/Div, DC
TIME: 400us/Div

Shutdown with 3A Loading

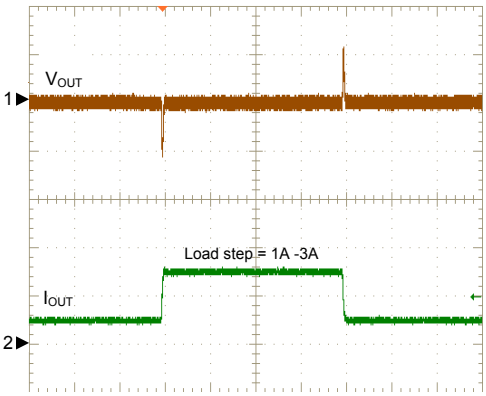


CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 1V/Div, DC
CH3: V_{POK}, 5V/Div, DC
CH4: I_L, 2A/Div, DC
TIME: 10us/Div

Operating Waveforms (Cont.)

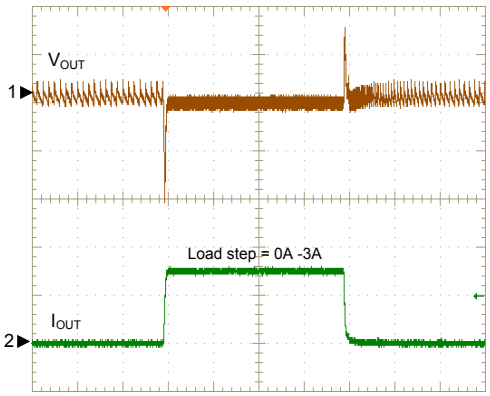
Refer to the typical application circuit. The test condition is V_{VDD}=V_{PVDD}=5V, V_{OUT}=1.8V, T_A= 25°C unless otherwise specified.

Load Transient



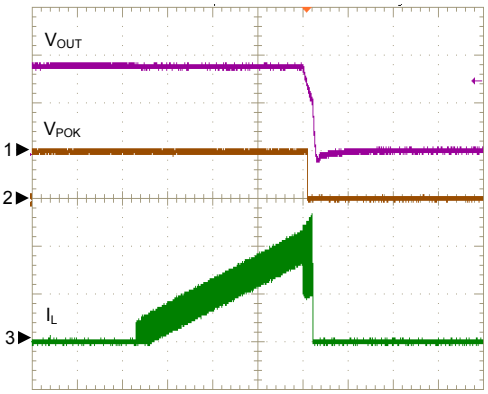
CH1: V_{OUT}, 100mV/Div, DC, Offset=1.8V
CH2: I_{OUT}, 2A/Div, DC
TIME: 200us/Div

Load Transient



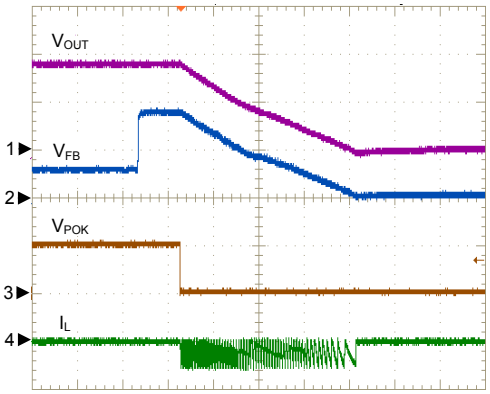
CH1: V_{OUT}, 100mV/Div, DC, Offset=1.8V
CH2: I_{OUT}, 1A/Div, DC
TIME: 200us/Div

Current Limit



CH1: V_{OUT}, 1V/Div, DC
CH2: V_{POK}, 5V/Div, DC
CH3: I_L, 2A/Div, DC
TIME: 200us/Div

Over Voltage Protection

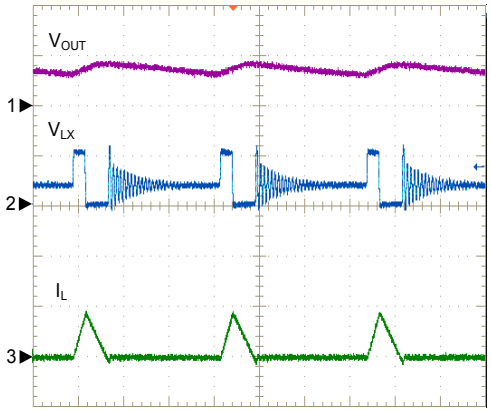


CH1: V_{OUT}, 1V/Div, DC
CH2: V_{FB}, 1V/Div, DC
CH3: V_{POK}, 5V/Div, DC
CH4: I_L, 2A/Div, DC
TIME: 40us/Div

Operating Waveforms (Cont.)

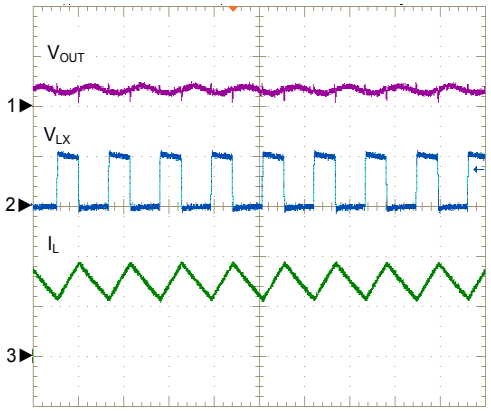
Refer to the typical application circuit. The test condition is V_{VDD}=V_{PVDD}=5V, V_{OUT}=1.8V, T_A= 25°C unless otherwise specified.

Normal Operation in Light Load



I_{OUT} =100mA
CH1: V_{OUT}, 50mV/Div, DC, Offset=1.8V
CH2: V_{LX}, 5V/Div, DC
CH3: I_L, 1A/Div, DC
TIME: 1us/Div

Normal Operation in Heavy Load

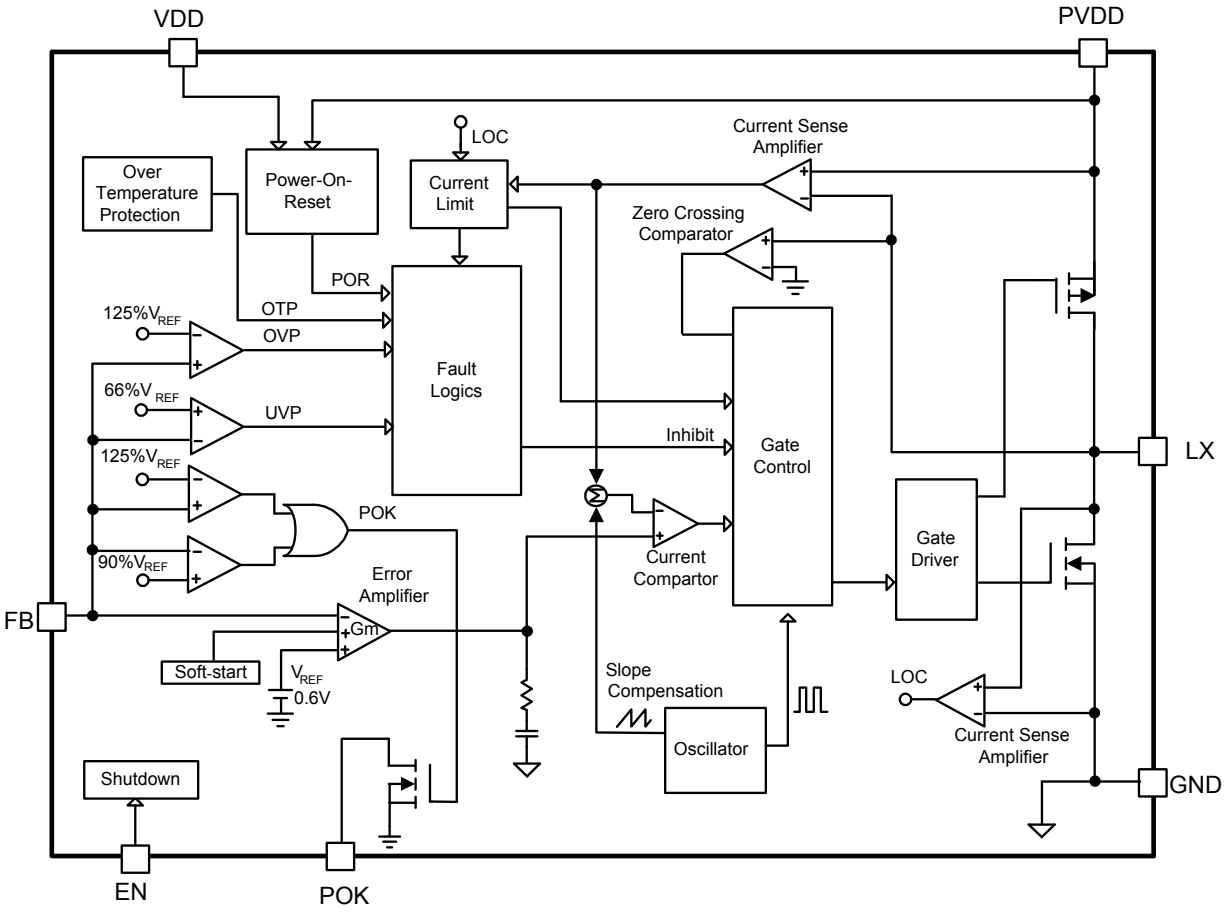


I_{OUT} = 3A
CH1: V_{OUT}, 50mV/Div, DC, Offset=1.8V
CH2: V_{LX}, 5V/Div, DC
CH3: I_L, 2A/Div, DC
TIME: 1us/Div

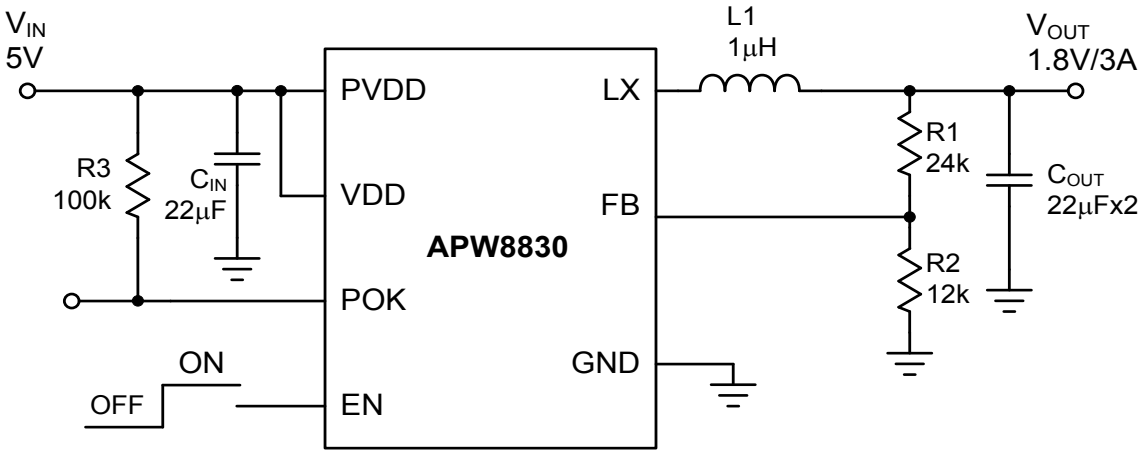
Pin Descriptions

PIN		FUNCTION
NO.	NAME	
1	NC	No Connection.
2,3	LX	Power Switching Output. LX is the Junction of the high-side and low-side Power MOSFETs to supply power to the output LC filter.
4	POK	Power Good Output. This pin is open-drain logic output that is pulled to the ground when the output voltage is out of regulation point.
5	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator, drive it low to turn it off.
6	FB	Output Feedback Input. The APW8830 senses the feedback voltage via FB and regulates the voltage at 0.6V. Connecting FB with a resistor-divider from the converter's output sets the output voltage.
7	NC	No connection.
8	VDD	Signal Input. VDD supplies the control circuitry, gate drivers. Connecting a ceramic bypass capacitor from VDD to GND to eliminate switching noise and voltage ripple on the input to the IC.
9,10	PVDD	Power Input. PVDD supplies the step-down converter switches. Connecting a ceramic bypass capacitor from PVDD to GND to eliminate switching noise and voltage ripple on the input to the IC.
11	GND (Exposed Pad)	Ground and Exposed pad. Connect the exposed pad to the system ground plan with large copper area for dissipating heat into the ambient air.

Block Diagram



Typical Application Circuit



Recommended Component Values

V_{IN} (V)	V_{OUT} (V)	R_{TOP} (Ω)	R_{BOT} (Ω)	L (H)	C_{OUT} (F)
5	3.3	45.3k	10k	1 μ	22 μ x 2
5	0.95	6.65k	11.3k	1 μ	10 μ x 1

Function Descriptions

VDD and PVDD Power-On-Reset (POR)

The APW8830 keeps monitoring the voltage on VDD and PVDD pins to prevent wrong logic operations which may occur when VDD or PVDD voltage is not high enough for internal control circuitry to operate. The VDD POR rising threshold is 2.4V (typical) with 0.2V hysteresis and PVDD POR rising threshold is 1.7V with 0.2V hysteresis.
During start-up, the VDD and PVDD voltage must exceed the POR threshold. Then, the IC starts a start-up process and ramps up the output voltage to the voltage target.

Output Under-Voltage Protection (UVP)

In the operational process, if a short-circuit occurs, the output voltage will drop quickly. Before the current-limit circuit responds, the output voltage will fall out of the required regulation range. The under-voltage continually monitors the FB voltage after soft-start is completed. If a load step is strong enough to pull the output voltage lower than the under-voltage threshold, the IC shuts down converter's output.
The under-voltage threshold is 66% of the nominal output voltage. APW8830 will be latched after under-voltage protection.

Over-Voltage Protection (OVP)

The over-voltage function monitors the output voltage by FB pin. When the FB voltage increases over 125% of the reference voltage due to the high-side MOSFET failure or for other reasons, the over-voltage protection comparator will trigger soft-stop function and shutdown the converter output.

Over-Temperature Protection (OTP)

The over-temperature circuit limits the junction temperature of the APW8830. When the junction temperature exceeds T_J=+160°C, a thermal sensor turns off the both power MOSFETs, allowing the devices to cool. The thermal sensor allows the converters to start a start-up process and to regulate the output voltage again after the junction temperature cools by 50°C. The OTP is designed with a 50°C hysteresis to lower the average T_J during continuous thermal overload conditions, increasing lifetime of the APW8830.

Current-Limit Protection

The APW8830 monitors the output current, flows through he high-side and low-side power MOSFETs, and limits the current peak at current-limit level to prevent the IC from damaging during overload, short-circuit and overvoltage conditions. Typical high side power MOSFET current limit is 5A, and low side MOSFET current limit is -1A.

Soft-Start

The APW8830 has a built-in soft-start to control the rise rate of the output voltage and limit the input current surge during start-up. During soft-start, an internal voltage ramp connected to one of the positive inputs of the error amplifier, rises up to replace the reference voltage (0.6V) until the voltage ramp reaches the reference voltage. During soft-start without output over-voltage, the APW8830 converter's sinking capability is disabled until the output voltage reaches the voltage target.

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Soft-Stop

At the moment of shutdown controlled by EN signal or over-voltage event, the APW8830 initiates a soft-stop process to discharge the output voltage in the output capacitors. Certainly, the load current also discharges the output voltage. During soft-stop, the low side MOSFET turns on each cycle to discharge the output voltage.
Therefore, the output voltage falls down slowly at the light load. After the soft-stop interval elapses, the soft-stop process ends and the IC turns off.

Enable and Shutdown

Driving EN to ground places the APW8830 in shutdown.
In shutdown mode, the internal power MOSFETs turn off, all internal circuitry shuts down and the quiescent supply current reduces to less than 1μA.

Power Good Indicator

POK is actively held low in shutdown and soft-start status. In the soft-start process, the POK is an open-drain. When the soft-start is finished, the POK is released. In normal operation, the POK window is from 87.5% to 125% of the converter reference voltage.When the output voltage stays within this window, POK signal will become high. When the output voltage outruns 82.5% or 125% of the target voltage, POK signal will be pulled low immediately. In order to prevent false POK drop, capacitors need to parallel at the output to confine the voltage deviation with severe load step transient.

Application Information

Input Capacitor Selection

Because buck converters have a pulsating input current, a low ESR input capacitor is required. This results in the best input voltage filtering, minimizing the interference with other circuits caused by high input voltage spikes.
Also, the input capacitor must be sufficiently large to stabilize the input voltage during heavy load transients. For good input voltage filtering, usually a 22µF input capacitor is sufficient. It can be increased without any limit for better input-voltage filtering. Ceramic capacitors show better performance because of the low ESR value, and they are less sensitive against voltage transients and spikes compared to tantalum capacitors. Place the input capacitor as close as possible to the input and GND pin of the device for better performance.

Inductor Selection

For high efficiencies, the inductor should have a low DC resistance to minimize conduction losses. Especially at high-switching frequencies, the core material has a higher impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. A reasonable starting point for setting ripple current, DIL, is 40% of maximum output current. The recommended inductor value can be calculated as below:

$$L \geq \frac{V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right)}{F_{SW}\cdot \Delta I_L}$$

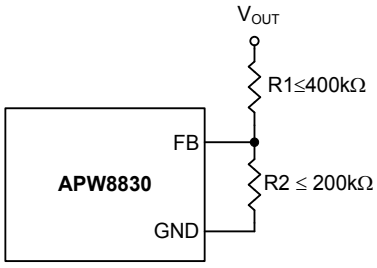
$$I_{L(MAX)} = I_{OUT(MAX)} + 1/2 \times \Delta I_L$$

To avoid the saturation of the inductor, the inductor should be rated at least for the maximum output current of the converter plus the inductor ripple current.

Output Voltage Setting

In the adjustable version, the output voltage is set by a resistive divider. The external resistive divider is connected to the output, allowing remote voltage sensing as shown in “Typical Application Circuits”. A suggestion of maximum value of R2 is 200kW to keep the minimum current that provides enough noise rejection ability through the resistor divider. The output voltage can be calculated as below:

$$V_{OUT} = V_{REF}\cdot\left(1+\frac{R1}{R2}\right) = 0.6\cdot\left(1+\frac{R1}{R2}\right)$$

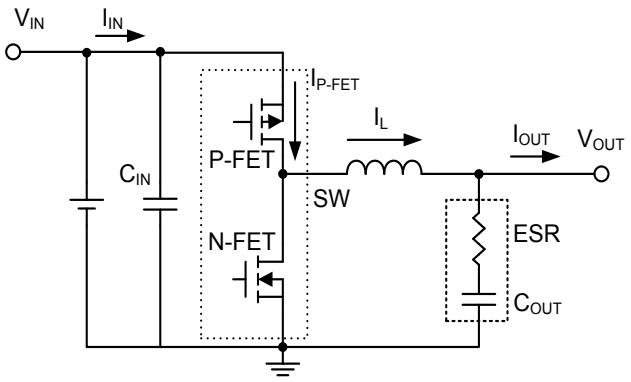


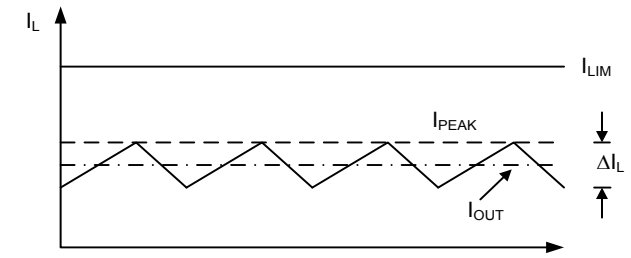
Output Capacitor Selection

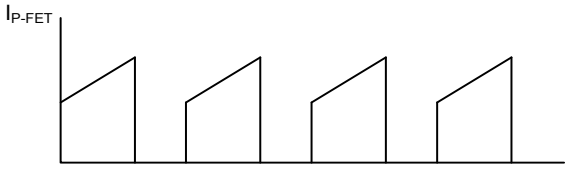
The current-mode control scheme of the APW8830 allows the use of tiny ceramic capacitors. The higher capacitor value provides the good load transients response.
Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. If required, tantalum capacitors may be used as well. The output ripple is the sum of the voltages across the ESR and the ideal output capacitor.

$$\Delta V_{OUT} \cong \frac{V_{OUT}\cdot\left(1-\frac{V_{OUT}}{V_{IN}}\right)}{F_{SW}\cdot L}\cdot\left(ESR+\frac{1}{8\cdot F_{SW}\cdot C_{OUT}}\right)$$

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.





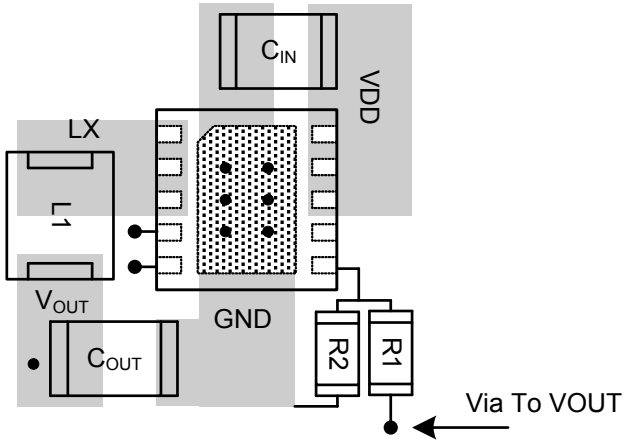


Application Information (Cont.)

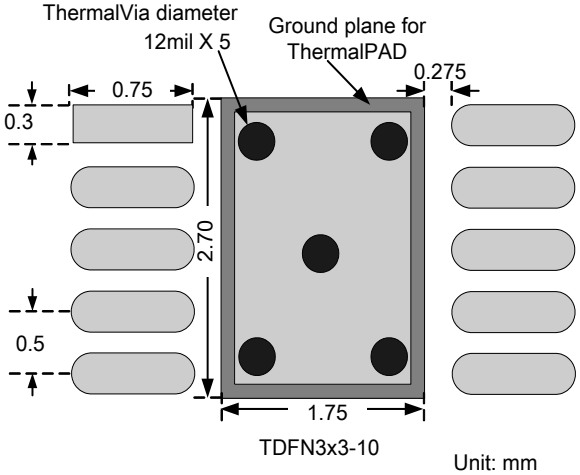
Layout Consideration

For all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

1. The input capacitor should be placed close to the PVDD and GND. Connecting the capacitor and PVDD/GND with short and wide trace without any via holes for good input voltage filtering. The distance between VIN/GND to capacitor less than 2mm respectively is recommended.
2. To minimize copper trace connections that can inject noise into the system, the inductor should be placed as close as possible to the LX pin to minimize the noise coupling into other circuits.
3. The output capacitor should be place closed to LX and GND.
4. Since the feedback pin and network is a high impedance circuit the feedback network should be routed away from the inductor. The feedback pin and feedback network should be shielded with a ground plane or trace to minimize noise coupling into this circuit.
5. A star ground connection or ground plane minimizes ground shifts and noise is recommended.



TDFN3x3-10
APW8830 Layout Consideration

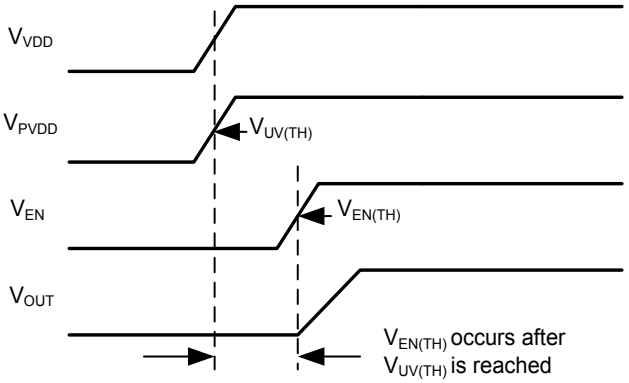


APW8830 Recommended Footprint

Input Power Sequence

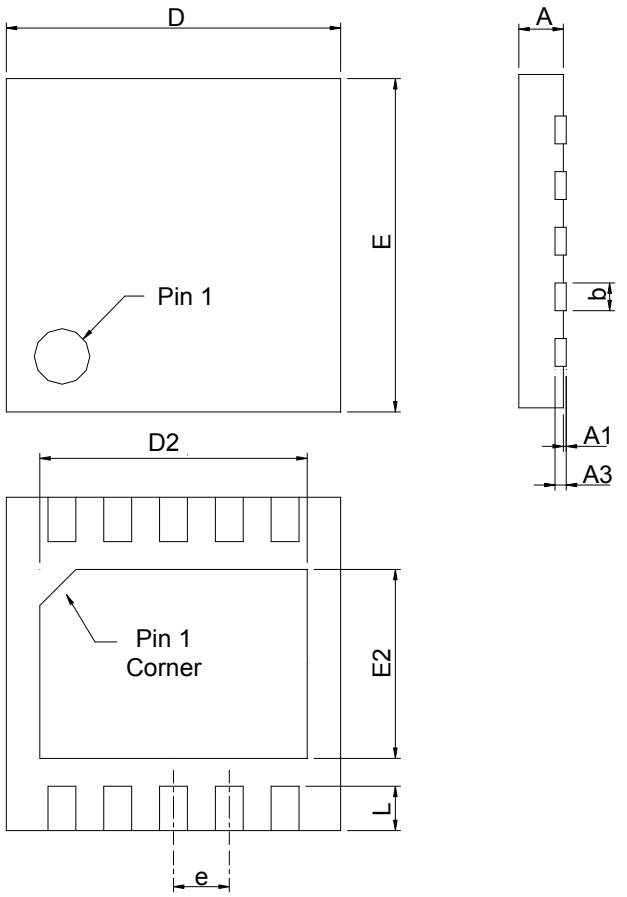
The APW8830 has three power-on control pins, PVDD, VDD and EN input pins. It is recommended that the three inputs should have a standard sequence. The VDD and PVDD input powers should be present to their respective pins regardless of input sequence. After VDD and PVDD powers are ready, the enable signal can be present to EN pin and the IC will be enabled.

Figure 1 shows the VDD and PVDD comes up before the VEN. Recommended power on sequence is shown in Figure1.



Package Information

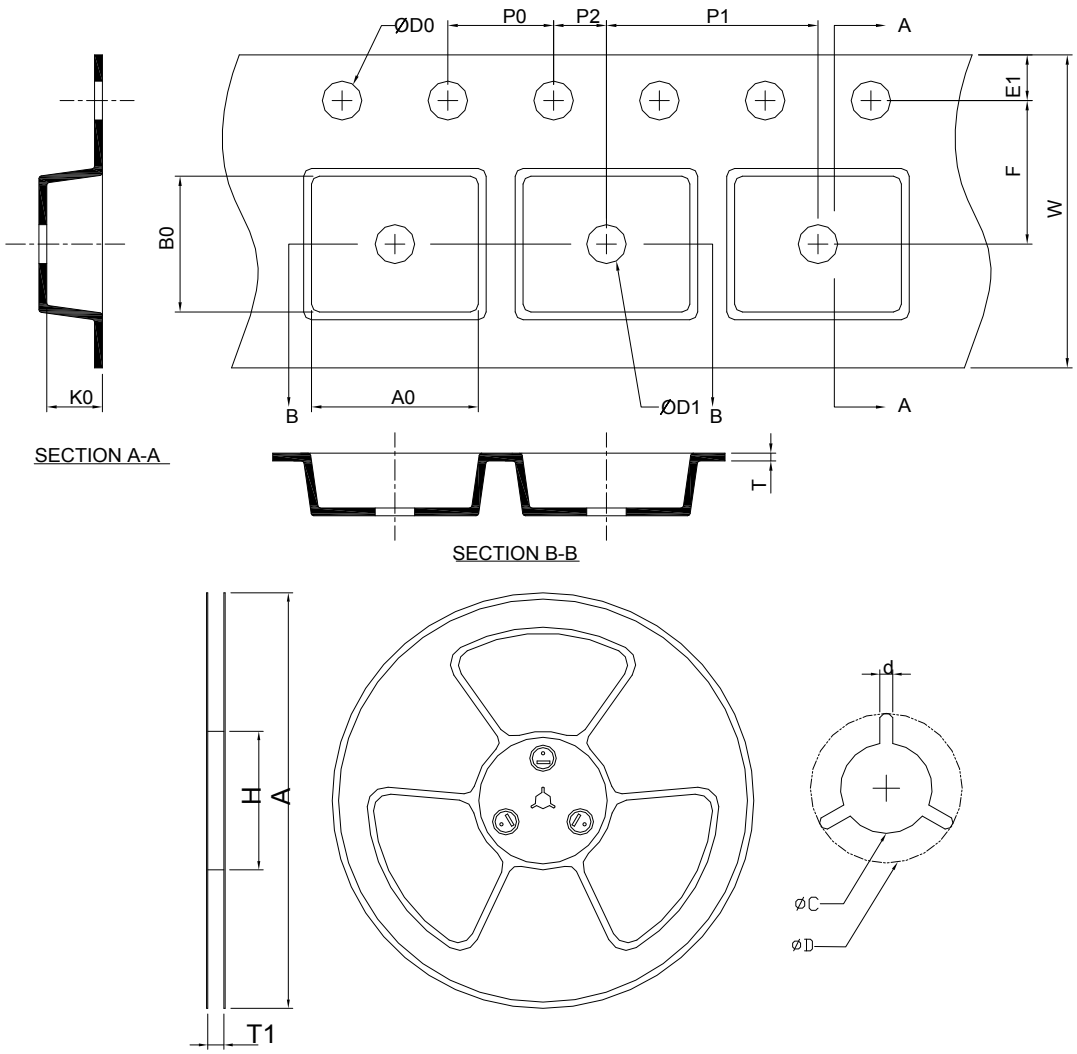
TDFN3x3-10



SYMBOL	TDFN3x3-10			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
D2	2.20	2.70	0.087	0.106
E	2.90	3.10	0.114	0.122
E2	1.40	1.75	0.055	0.069
e	0.50 BSC		0.020 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	

Note : 1. Followed from JEDEC MO-229 VEED-5.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TDFN3x3-10	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.30±0.20

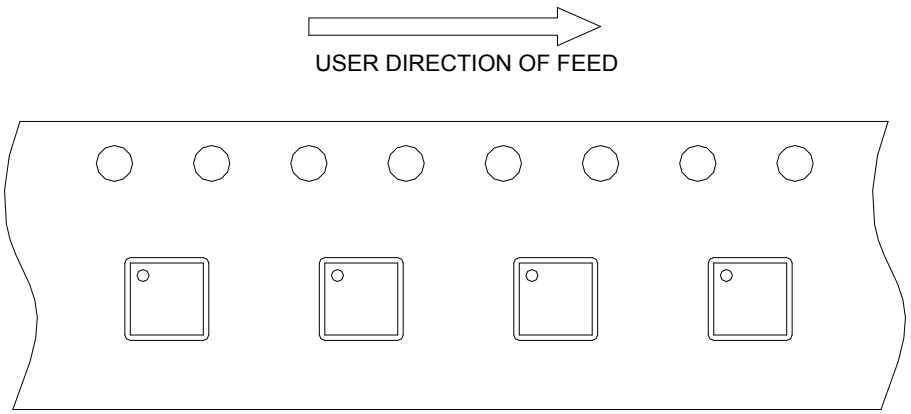
(mm)

Devices Per Unit

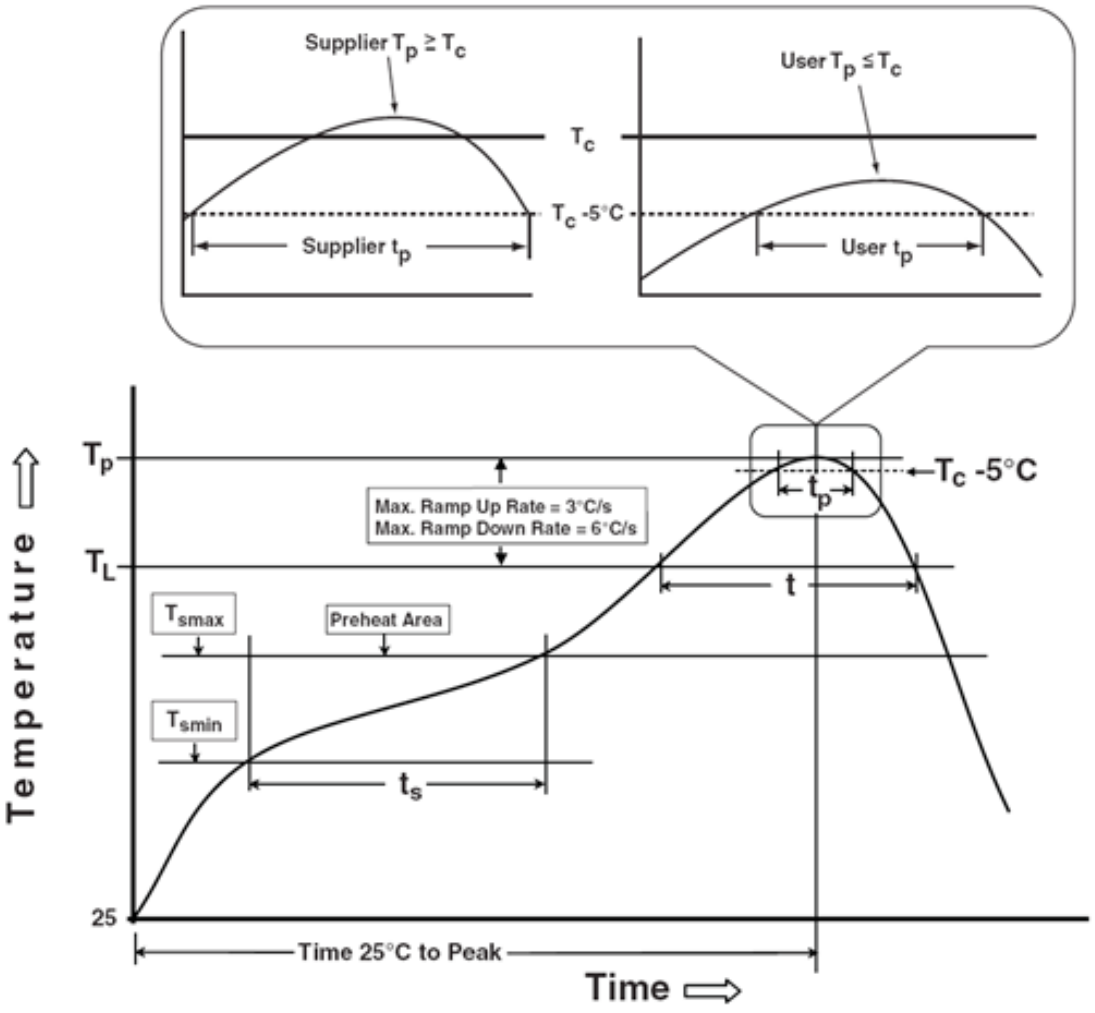
Application	Packing	Devices Per Reel
TDFN3x3	Tape & Reel	3000

Taping Direction Information

TDFN3x3-10



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≧ 2KV
MM	JESD-22, A115	VMM ≧ 200V
Latch-Up	JESD 78	10ms, 1_{tr} ≧ 100mA

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