High Current, High Frequency 7 Outputs Voltage Regulator and Power Management IC for High Performance Tablet and Ultra Notebook Applications

1.General Description

The APW8855 is a Power Management IC (PMIC) designed to provide 7 Voltage regulators for AMD's Stoney Ridge APU with ability to communicate via an I2C interface. The IC operates from a wide input voltage of 5.5V to 20V. There are 5 Switching Buck regulators and 2 low power LDOs that are all controlled and sequenced via the serial interface. The Buck PWM regulators consists of 3 switching controller driving external power stage such as APW8703 which is capable of supplying up to 8A supply, 2 single phase switching regulators supplying up to 3A supply.

The IC is equipped with all the standard protection features such as over current, over voltage and internal under voltage lock out protection. The serial interface is an I2C communication interface which allows supply sequencing as well as controlled supply ramp up and ramp down of all supplies except for the always on 1.5V LDO supplying to RTC load. The IC is offered in TQFN4x4-32A package.

2.Applications

- **High Performance Tablet PCs**
- **Ultra Notebook PCs**
- **Netbook PCs**
- **High Performance Digital Signage**
- **Medical Devices**
- **Smart phones**

3.Features

Voltage Rail

- **Provide 3 Buck PWM Controllers with High Accuracy over Temperature**
  -VR1 provides 5V, 4A continuous output current.
  -VR2 provides 3.3V, 8A continuous output current.
  -VR5 provides 0.95V, 8A continuous output current.
- **Provide 2 Buck PWM Converters with High Accuracy over Temperature**
  -VR3 provides 1.8V, 2.5A continuous output current.
  -VR3 provides 1.5V, 2.5A continuous output current.
- **Provide 2 LDO Outputs with High Accuracy over Temperature**
  -VR6 provides a low quiescent LDO output for RTC.
  -VR7 provides a 0.65V to1.35V, 0.2A LDO output.
- **Built in Current limit, Over Voltage protection and Over temperature protection**

Serial Interface

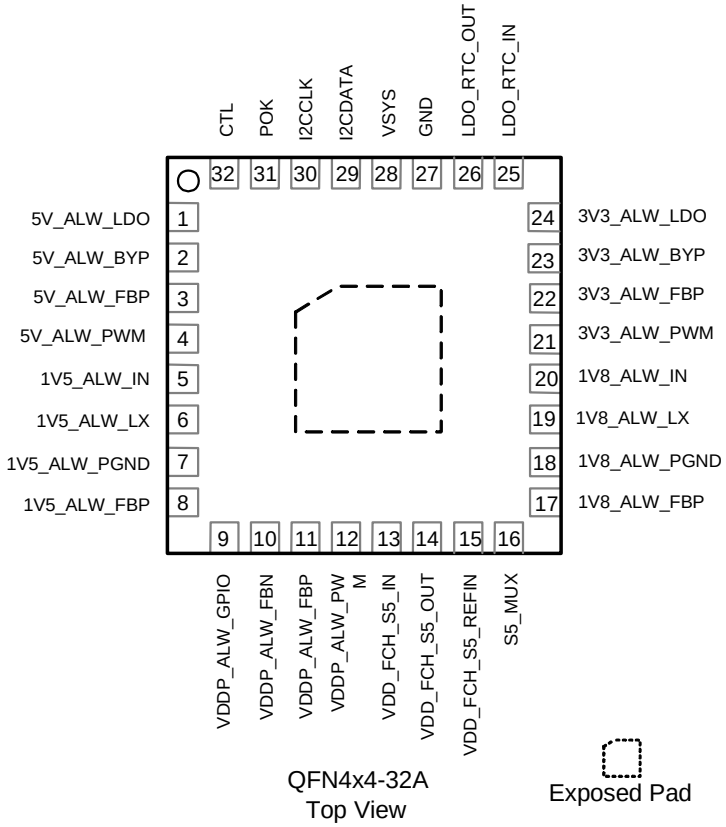
- **I2C communication Interface for SoC Access**
- **Support Bit Rate 0.4MBit/s, 1MBit/s and 3.4MBit/s**
- **Power Sequence Control by CTL**
- **Built-in Thermal Diode and I2C Reading Function for Temperature Sensing**
- **POK Signal for VR power state.**
- **4x4 TQFN-32A Package.**

4.Ordering and Marking Information

APW8855 □□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QB : TQFN4x4-32A Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW8855 QB: 	X - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

5.Pin Configuration



6.Absolute Maximum Ratings (Note 1)

Pin or Symbol	Parameter	Rating	Unit
VSYS	VSYS to GND	-0.3~28	V
1V8_ALW_LX, 1V5_ALW_LX 1V8_ALW_IN, 1V5_ALW_IN	1V8_ALW_LX to 1V8_ALW_PGND 1V5_ALW_LX to 1V5_ALW_PGND 1V8_ALW_IN to 1V8_ALW_PGND 1V5_ALW_IN to 1V5_ALW_PGND	-0.3 to 6.5	V
5V_ALW_BYP, 3V3_ALW_BYP	5V_ALW_BYP, 3V3_ALW_BYP to GND	-0.3 to 6.5	V
5V_ALW_PWM, 3V3_ALW_PWM, VDDP_ALW_PWM	5V_ALW_PWM, 3V3_ALW_PWM, VDDP_ALW_PWM to GND	-0.3 to 6.5	V
1V8_ALW_PGND, 1V5_ALW_PGND	PGND to GND	-0.3 to 0.3	V
All Other Pins	All Other Pins to GND	-0.3 to 6.5	V
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature(10 Seconds)	260	°C

Note 1: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)		°C/W

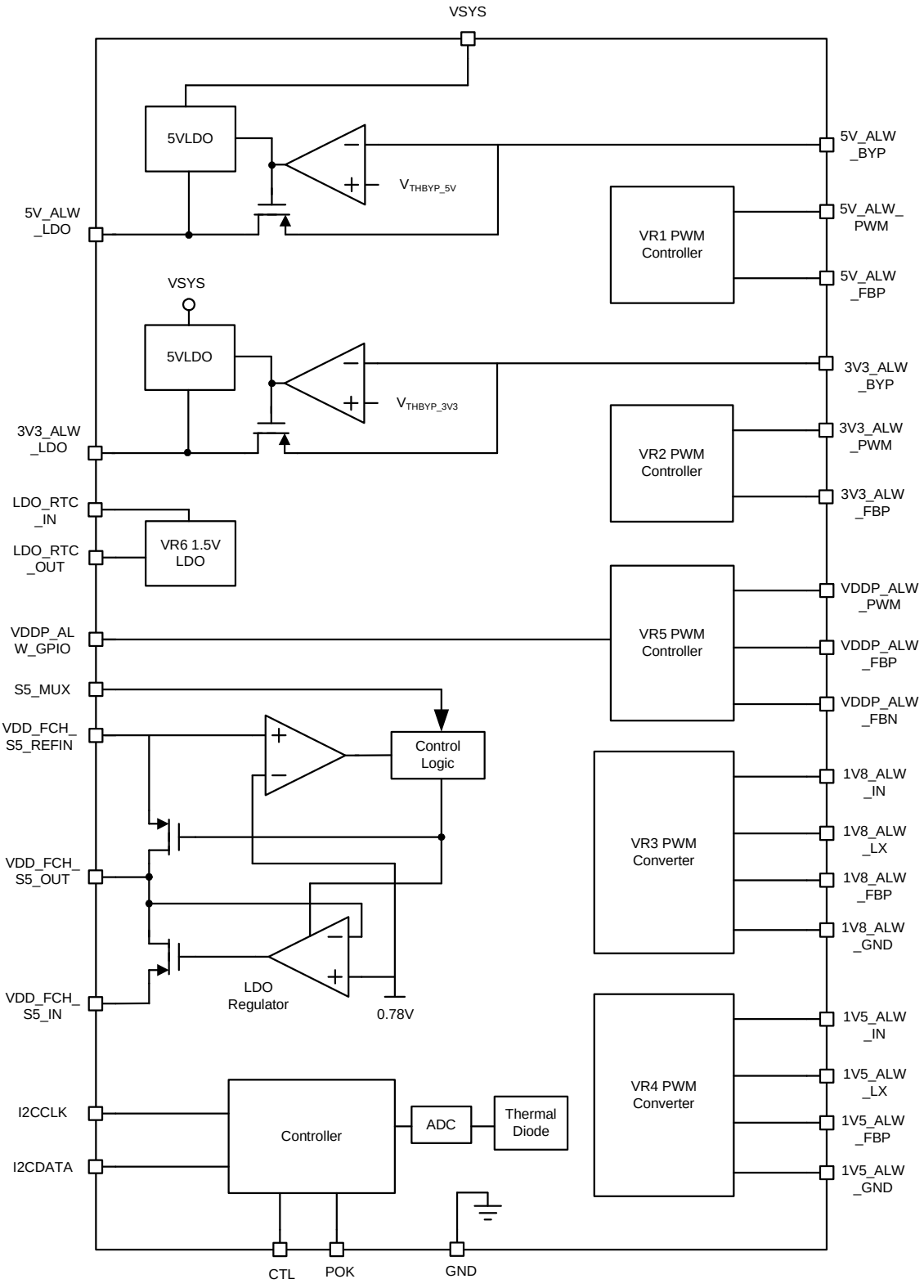
Note2: θ_{JA} is measured with the component mounted on a JESD-51-7 high effective thermal conductivity test board in free air.

8.Recommended Operating Conditions(Note3)

Symbol	Parameter	Range	Unit
V_{VSYS}	System Rail From Battery Management Unit	5.5 ~ 20	V
$V_{1V8\_ALW\_IN}$	1V8_ALW Regulator Input Voltage	3 ~ 5.5	V
$V_{1V5\_ALW\_IN}$	1V5_ALW Regulator Input Voltage	3 ~ 5.5	V
$V_{VDD\_FCH\_S5\_IN}$	VDD_FCH_S5 Regulator Input Voltage	0.5~1.5	V
$V_{VDD\_FCH\_S5\_REFIN}$	VDD_FCH_S5 Regulator Reference Input Voltage	0.65 ~ 1.35	V
V_{CTL_L}	CTL Input Low Voltage	0 ~ 0.6	V
V_{CTL_H}	CTL Input High Voltage	1.2 ~ 5.5	V
V_{POK}	POK Pull High Voltage	~ 5.5	V
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

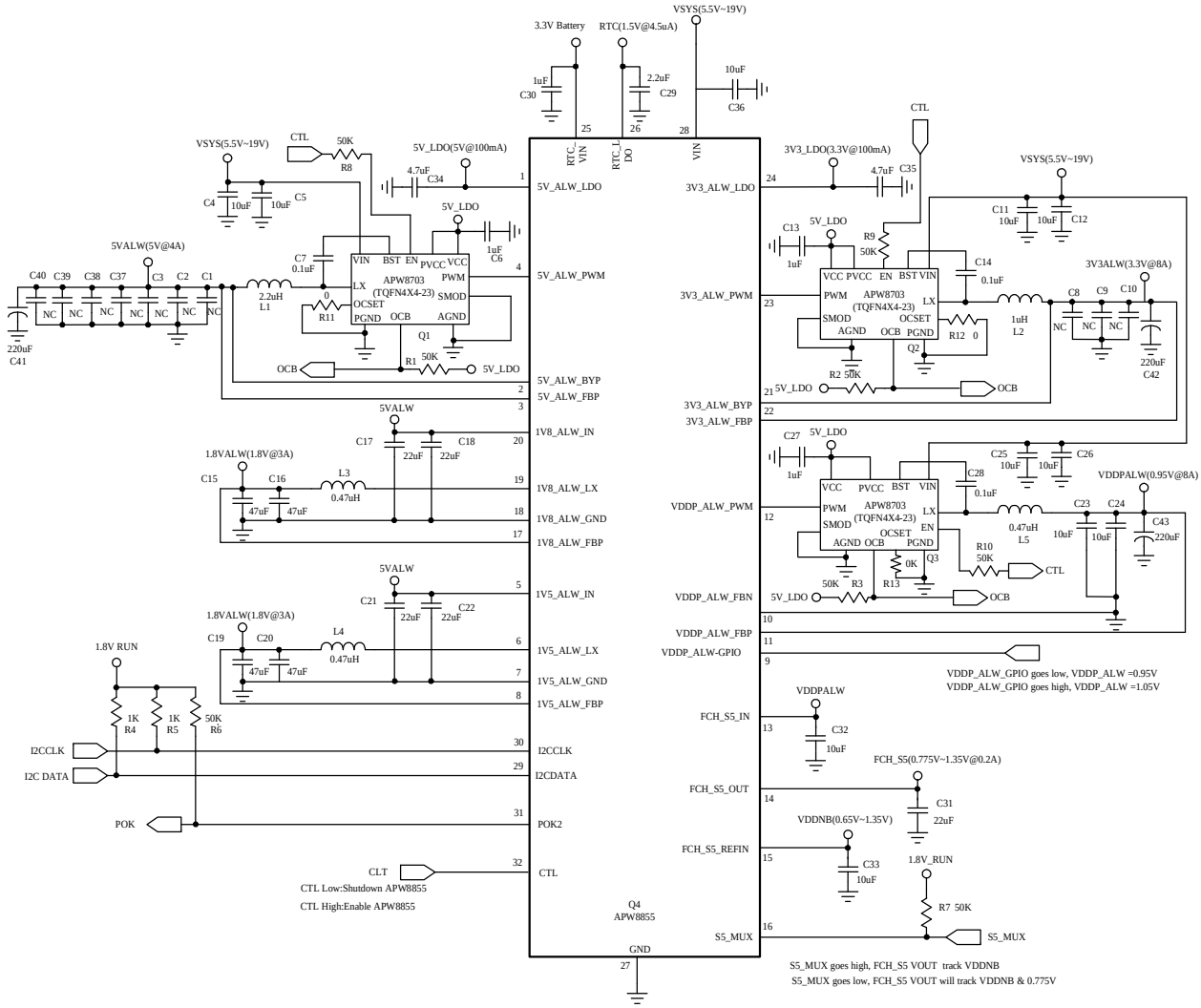
Note 3: Refer to the typical application circuit.

9.Block Diagram



10.Typical Application Circuit

10.1 Typical Application Circuit



10.2 Bill of Materials

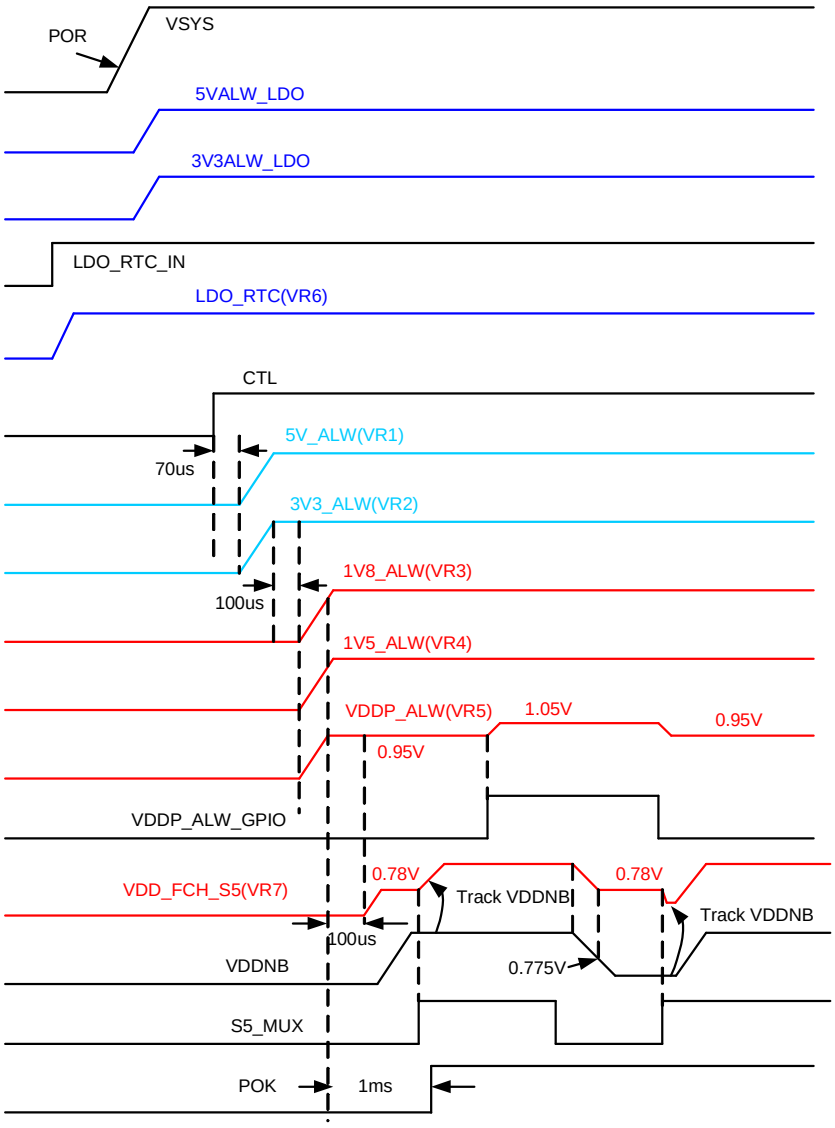
Designator	Quantity	Value	Description	Package Reference	Part Number	MFR
C1, C2, C3, C8, C9, C10, C17, C18, C21, C22, C37, C38, C39, C40	14	22uF	Cap, Ceramic, 10V, X5R, 10%	1206	GRM31CR61A226KE19#	Murata
C31	1	22uF	Cap, Ceramic, 6.3V, X7R, 10%	1206	GRM31CR70J226KE19#	Murata
C4, C5, C11, C12, C25, C26, C36	7	10uF	Cap, Ceramic, 35V, X5R, 10% ,	1206	GRM31CR6YA106KA12#	Murata
C23,C24,C32,C33	4	10uF	Cap, Ceramic, 6.3V, X5R, 10%	1206	GRM319R60J106KE19#	Murata
C15,C16,C19,C20	4	47uF	Cap, Ceramic, 6.3V, X5R, 20%	1206	GRM31CR60J476ME19#	Murata
C6, C13,C27	3	1uF	Cap, Ceramic, 10V, X5R, 10%	0805	GRM219R61A105KA01#	Murata
C7,C14,C28	3	0.1uF	Cap, Ceramic, 10V, X7R, 20%	0603	LLL185R71A104MA01#	Murata
C30	1	1uF	Cap, Ceramic, 35V, X7R, 10%	0805	GRM219R7YA105KA12#	Murata
C29	1	1uF	Cap, Ceramic, 6.3V, X5R, 10%	0603	GRM188R60J105KA01#	Murata
C34, C35	2	4.7uF	Cap, Ceramic, 10V, X5R, 10%	1206	GRM319R61A475KA01#	Murata
C41, C42, C43	3	220uF	Cap, POSCAP, 10V, 20%	1812	10TPE220MIL	Panasonic
L1	1	2.2uH	Inductor, SMD Flat Wire Coils-SDB, shielding, 13.97mOhm	0630, 6.76mm x 6.56mm x 3.1mm	XAL6030-222MEB	Coilcraft
L2	1	1.0uH	Inductor, SMD Flat Wire Coils-SDB, shielding, 6.18mOhm	0630, 6.76mm x 6.56mm x 3.1mm	XAL6030-102MEB	Coilcraft
L3,L4, L5	3	0.47uH	Inductor, SMD Flat Wire Coils-SDB, shielding, 6.38mOhm	0630, 7.5mm x 7.5mm x 1.5mm	XFL7015-471MEB	Coilcraft
R1, R2, R3, R6, R7, R8, R9, R10	8	50kOhm	RES, 5%,	0402		
R4, R5	2	1kOhm	RES, 5%,	0402		
R11,R12,R13	3	0Ohm	RES, 5%,	0402		
Q1, Q2, Q3	3	-	Power Stage	TQFN4x4-23	APW8703	ANPEC
Q4	1	-	PMIC	TDFN4x4-32	APW8855	ANPEC

11.Pin Description

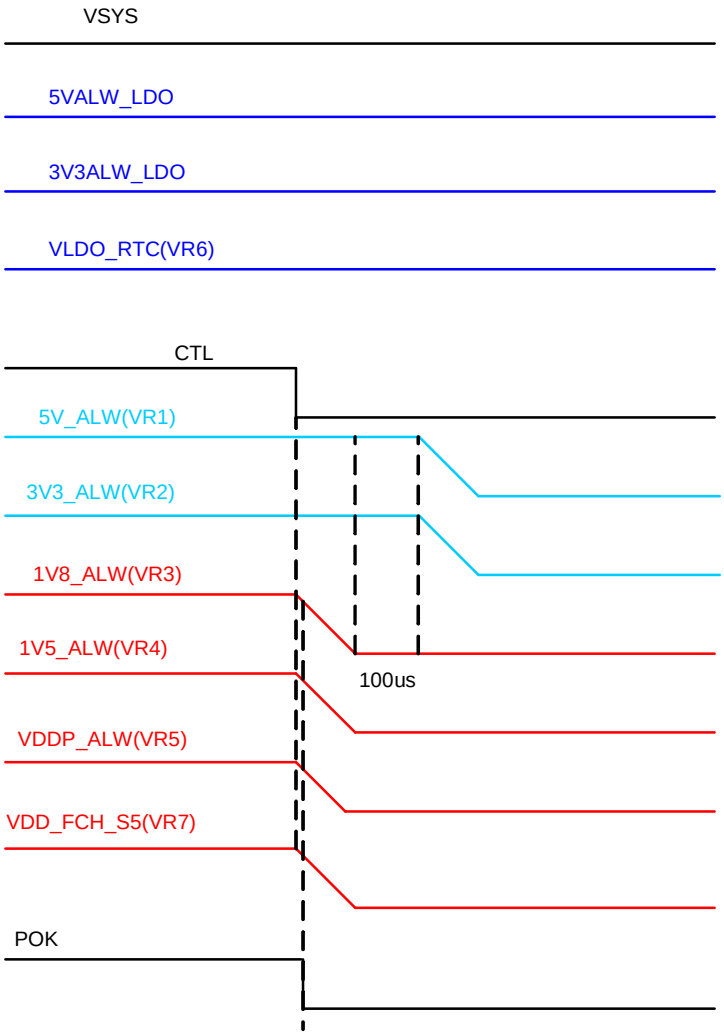
PIN		FUNCTION
NO.	NAME	
1	5V_ALW_LDO	5V_ALW_LDO Output Pin.
2	5V_ALW_BYP	5V_ALW_LDO Input Pin. Connect to 5V_ALW Output Voltage.
3	5V_ALW_FBP	5V_ALW Output Voltage Feedback Pin.
4	5V_ALW_PWM	5V_ALW PWM Signal Output Pin. Connect to External power stage's PWM input pin.
5	1V5_ALW_IN	1V5_ALW PWM Regulator Input Pin.
6	1V5_ALW_LX	1V5_ALW PWM Regulator LX Pin. Connect to external inductor for output LC filter.
7	1V5_ALW_PGND	1V5_ALW PWM Regulator PGND Pin.
8	1V5_ALW_FBP	1V5_ALW PWM Regulator Output Voltage Feedback Pin.
9	VDDP_ALW_GPIO	VDDP_ALW Output Select Pin. Pull high for VPPD_ALW=1.05V, pull low for VDDP_ALW=0.95V.
10	VDDP_ALW_FBN	VDDP_ALW Negative Output Feedback Pin. Connect to VR5's ground.
11	VDDP_ALW_FBP	VDDP_ALW Positive Output Feedback Pin. Connect to VR5's output voltage.
12	VDDP_ALW_PWM	VDDP_ALW PWM Signal Output Pin. Connect to External power stage's PWM input pin.
13	VDD_FCH_S5_IN	VDD_FCH_S5 LDO Regulator Input Pin.
14	VDD_FCH_S5 _OUT	VDD_FCH_S5 Output Pin.
15	VDD_FCH_S5_REFIN	VDD_FCH_S5 Track Voltage Input Pin.
16	S5_MUX	VDD_FCH_S5 Track Select Pin. When S5_MUX=high, VDD_FCH_S5 fully track VDD_FCH_S5_REFIN voltage; S5_MUX=low, VDD_FCH_S5 partially track VDD_FCH_S5_REFIN voltage.
17	1V8_ALW_FBP	1V8_ALW PWM Regulator Output Voltage Feedback Pin.
18	1V8_ALW_PGND	1V8_ALW PWM Regulator Output PGND Pin.
19	1V8_ALW_LX	1V8_ALW PWM Regulator Output LX Pin. Connect to external inductor for output LC filter.
20	1V8_ALW_IN	1V8_ALW PWM Regulator Input Pin.
21	3V3_ALW_BYP	3V3_ALW_LDO Input Pin. Connect to 3V3_ALW Output Voltage.
22	3V3_ALW_FBP	3V3_ALW Output Voltage Feedback Pin.
23	3V3_ALW_PWM	3V3_ALW PWM Signal Output Pin. Connect to External power stage's PWM input pin.
24	3V3_ALW_LDO	3V3_ALW_LDO Output Pin.
25	LDO_RTC_IN	LDO_RTC Input Voltage Pin. Provide a 3.3V power into this pin to enable LDO_RTC Output.
26	LDO_RTC_OUT	LDO_RTC Output Voltage Pin.
27	GND	IC Analog Ground.
28	VSYS	IC Power Input Pin.
29	I2CDATA	I2C Data Connection Pin.
30	I2CCLK	I2C Clock Signal Pin.
31	POK	Power Good Indicator. Connect a resistor from POK to a pull-high voltage.
32	CTL	System Power State Control Pin. Pull CTL high to enable VR1/2/3/4/5/7.
Exposed Pad	PGND	IC Power Ground

12.Power Sequence

12.1 Power-on Sequence



12.2 Power-off Sequence



13.Electrical Characteristics

13.1 Regulator Table

Table 1. PWM Controllers VR1, VR2,VR5

Symbol	Parameter	VR1(5VALW)	VR2(3VALW)	VR5(VDDPALW)	Unit
V_{IN}	Input Voltage	V_{VSYS}	V_{VSYS}	V_{VSYS}	V
V_{OUT}	Default Output Voltage	5.06	3.3	0.95	V
	Output Voltage Range	4.5~5.5	2.6~4	0.5~1.5	
I_{OUT}	Continuous Output Current	4	8	8	A
I_{PEAK}	Peak Output Current	8	-	-	A
C_{IN}	Input Capacitor	>2 x 10	>2 x 10	>2x 10	µF
C_{OUT}	Output Capacitor	>1 x 220	>1 x 220	>2 x 10+1x220	µF
ESR	Output Capacitor ESR	6	6	6	mΩ
L	Output Inductor	2.2	1.0	0.47	µH
DCR	Output Inductor DCR	<10	<10	<10	mΩ

Table 2. PWM Converters VR3, VR4

Symbol	Parameter	VR3(1V8ALW)	VR4(1V5ALW)	Unit
V_{IN}	Input Voltage	V_{5V_ALW}	V_{5V_ALW}	V
V_{OUT}	Default Output Voltage	1.8	1.5	V
	Output Voltage Range	1.45~2.25	0.8~2	
I_{OUT}	Continuous Output Current	2.5	2.5	A
I_{PEAK}	Peak Output Current	3	3	A
C_{IN}	Input Capacitor	>2x 22	>2 x 22	µF
C_{OUT}	Output Capacitor	>2 x 47	>2 x 47	µF
ESR	Output Capacitor ESR	6	6	mΩ
L	Output Inductor	0.47	0.47	µH
DCR	Output Inductor DCR	<15	<15	mΩ

Table 3. LDO Regulators VR6, VR7

Symbol	Parameter	VR6(LDO_RTC)	VR7(VDD_FCH_S5)	Unit
V_{IN}	Input Voltage	$V_{LDO\_RTC\_IN}$ (3.3V Battery)	V_{VDDP_ALW} or $V_{VDD\_FCH\_S5\_REFIN}$(VDDNB)	V
V_{OUT}	Default Output Voltage	1.5	0.78	V
	Output Voltage Range	-	0.5~1.5	
I_{OUT}	Continuous Output Current	4.5µ	0.2(LDO)/0.9(Switch)	A
C_{IN}	Input Capacitor	1	10	µF
C_{OUT}	Output Capacitor	2 .2	22	µF

13.1 Regulator Table

Table 4. LDO Regulators 5V_ALW_LDO, 3V3_ALW_LDO

Symbol	Parameter	5V_ALW_LDO	3V3_ALW_LDO	Unit
V_{IN}	Input Voltage	V_{VSYS}	V_{VSYS}	V
V_{OUT}	Default Output Voltage	5.06	3.3	V
	Output Voltage Range	4.5~5.5	2.9~4	
I_{OUT}	Continuous Output Current	100	100	mA
C_{IN}	Input Capacitor	10	10	µF
C_{OUT}	Output Capacitor	4.7	4.7	µF

13.2 VR1 Electrical Characteristics

These specifications apply over V_{VSYS} = 12V, V_{5V_ALW} = 5.06V, TA = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8855(VR1)			Unit
			Min	Typ	Max	
PWM OUTPUT VOLTAGE						
	Output Voltage Accuracy	T_A = 25°C	-	-	±0.8	%
	Output Voltage Line/Load Regulation	Vin=7.5V to 20V, I_{OUT}=1.08A to 4A			±0.2	%
	Load Transient Drop Voltage	Tr=200ns, I_{OUT}=1.08A to 4A, Refer to the typical circuit			-4	%
	Load Transient Overshoot Voltage	Tf=200ns, I_{OUT}=4A to 1.08A, Refer to the typical circuit			+4	%
	Output Step Ramp Rate Accuracy		-10		+10	%
	Output Voltage Soft-start Rate		9	10	11	mV/µs
	Output Discharge Resistance			10		Ω
	Feedback Leakage Current	$V_{5V\_ALW\_FBP}$ = 5.5V	-	-	100	nA
PWM GATE DRIVER						
	Switching Frequency Accuracy	V_{VSYS} =7.5 to 20V, V_{OUT}=4V to 5.5V	-	-	±15	%
	Switching Frequency	V_{VSYS} =5.5V, V_{OUT}= 5.06V			300	kHz
	Minimum Off Time			200		ns
	Minimum Controllable On Time			60	80	ns
	PWM Sink Resistance			15	20	Ω
	PWM Source Resistance			15	20	Ω
	PWM Leakage Current	$V_{5V\_ALW\_PWM}$=5.5V			100	nA
PROTECTION						
	Under-voltage Protection (UVP)		65	70	75	%
	UVP Debounce Time		-	2	-	µs
	Over-voltage Protection (OVP)		125	130	135	%
	OVP Debounce Time			2	-	µs

13.2 VR1 Electrical Characteristics

These specifications apply over V_{VSYS} = 12V, V_{5V_ALW} = 5.06V, TA = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8855(VR1)			Unit
			Min	Typ	Max	
LDO REGULATOR						
V_{SYS_UVLO}	VSYS Under-voltage Lockout (UVLO)	V_{VSYS} Rising, enable 5V_LDO	3.85	4.0	4.15	V
		Hysteresis	0.1	0.15	0.2	V
$V_{5V\_LDO\_POR}$	LDO Regulator Under-voltage Lockout (UVLO)	V_{5V_LDO} Rising, enable other VRs	4.15	4.3	4.45	V
		Hysteresis	0.1	0.15	0.2	V
V_{5V_LDO}	LDO Regulator Output Voltage Accuracy	V_{VSYS}=5.5V to 20V, 10mA	-2		+2	%
	LDO Dropout Voltage	I_{OUT}=100mA, V_{5V_LDO}=5.06V			0.4	V
	LDO Current Limit		150	200	250	mA
	LDO Discharge Resistance			10		Ω
	LDO Power-on Delay	V_{SYS}>V_{SYS_POR} to 5V_LDO soft-start starting		20		µs
V_{THBYP_5V}	Bypass Threshold	PWM Voltage Rising	91	94	97	%VR1
		Hysteresis	2	3	4	%VR1
	Bypass Switch On Resistance		-	1.5	3	Ω
	LDO Soft-start Time	C_{OUT}=4.7uF		100		us
	Bypass Leakage Current	$V_{5V\_ALW\_BYP}$=5.5V, V_{VSYS}=0V	-	-	100	nA
EFFICIENCY						
	Efficiency (Refer to the typical circuit)	VOUT=5V, IOUT=5mA to 50mA, DCR<10mΩ		93		%
		VOUT=5V, IOUT=50mA to 500mA, DCR<10mΩ		93		%
		VOUT=5V, IOUT=2A, DCR<10mΩ		92		%
		VOUT=5V, IOUT=4A, DCR<10mΩ		90		%

13.3 VR2 Electrical Characteristics

These specifications apply over V_{VSYS} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8855(VR2)			Unit
			Min	Typ	Max	
PWM OUTPUT VOLTAGE						
	Output Voltage Accuracy	T_A = 25°C	-	-	±0.8	%
	Output Voltage Line/Load Regulation	Vin=7.5V to 20V, I_{OUT}=2.16A to 8A			±0.2	%
	Load Transient Drop Voltage	Tr=200ns, IOUT=2.16A to 8A, Refer to the typical circuit			-4	%
	Load Transient Overshoot Voltage	Tf=200ns, IOUT=8A to 2.16A, Refer to the typical circuit			+4	%
	Output Step Ramp Rate Accuracy		-10		+10	%
	Output Voltage Soft-start Rate		9	10	11	mV/µs
	Output Discharge Resistance			10		Ω
	Feedback Leakage Current	$V_{3V3\_ALW\_FBP}$ = 5.5V	-	-	100	nA

13.3 VR2 Electrical Characteristics

These specifications apply over V_{VSYS} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8855(VR2)			Unit
			Min	Typ	Max	
PWM GATE DRIVER						
	Switching Frequency Accuracy	V_{VSYS} =5.5 to 20V, V_{OUT}=2.6V to 4V		-	±15	%
	Minimum Off Time			200		ns
	Minimum Controllable On Time			60	80	ns
	PWM Sink Resistance			15	20	Ω
	PWM Source Resistance			15	20	Ω
	PWM Leakage Current	$V_{3V3\_ALW\_PWM}$=5.5V			100	nA
PROTECTION						
	Under-voltage Protection (UVP)		65	70	75	%
	UVP Debounce Time		-	2	-	µs
	Over-voltage Protection (OVP)		125	130	135	%
	OVP Debounce Time			2	-	µs
LDO REGULATOR						
	LDO Regulator Under-voltage Lockout (UVLO)	V_{VSYS} Rising, enable 3V3_LDO	3.8	4.0	4.2	%
		Hysteresis	0.1	0.15	0.2	V
V_{3V3_LDO}	LDO Regulator Output Voltage Accuracy		-1		+1	%
	LDO Dropout Voltage	I_{OUT}=100mA, $V_{3V3\_ALW\_PWM}$=4V			1.5	V
	LDO Current Limit		150	200	250	mA
	LDO Discharge Resistance			10		Ω
	LDO Soft-start Time			100		us
V_{THBYP_3V3}	Bypass Threshold	PWM Voltage Rising	91	94	97	%VR2
		Hysteresis	2	3	4	%VR2
	Bypass Switch On Resistance		-	1.5	3	Ω
	Bypass Leakage Current	$V_{3V3\_ALW\_BYP}$=5.5V, V_{VSYS}=0V	-	-	100	nA
EFFICIENCY						
	Efficiency (Refer to the typical circuit)	VOUT=3.3V, IOUT=5mA to 50mA, DCR<10mΩ		93		%
		VOUT=3.3V, IOUT=50mA to 500mA, DCR<10mΩ		93		%
		VOUT=3.3V, IOUT=3A, DCR<10mΩ		88		%
		VOUT=3.3V, IOUT=8A, DCR<10mΩ		93		%

13.4 VR3 Electrical Characteristics

These specifications apply over V_{VSYS} = 12V, V_{OUT} = 1.8V, TA = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8855(VR3)			Unit
			Min	Typ	Max	
PWM CONTROLLER						
	Switching Frequency Accuracy	Default is 2MHz		-	±10	%
	Maximum Duty Cycle		90	93	96	%
	Minimum Controllable On Time		-	60	100	ns
	High-side MOSFET On Resistance	$V_{1V8\_ALW\_IN}$=5V		55		mΩ
	Low-side MOSFET On Resistance	$V_{1V8\_ALW\_IN}$=5V		40		mΩ
	Input Leakage Current	VR3 is off, $V_{1V8\_ALW\_IN}$=5.5V			1	μA
	LX Leakage Current	$V_{1V8\_ALW\_LX}$ =5.5V, $V_{1V8\_ALW\_IN}$=5.5V			1	μA
	Zero Current Offset		-5		5	mV
PWM OUTPUT VOLTEGE						
	Output Voltage Accuracy	T_A = 25°C		-	±0.8	%
	Output Voltage Load Regulation				±0.2	%
	Load Transient Drop Voltage	Tr=200ns, I_{OUT}=0.81A to 3A, Refer to the typical circuit			-3	%
	Load Transient Overshoot Voltage	Tf=200ns, I_{OUT}=3A to 0.81A, Refer to the typical circuit			+3	%
	Output Step Ramp Rate Accuracy		-10		+10	%
	Output Voltage Soft-start Rate		9	10	11	mV/μs
	Output Discharge Resistance	CTL=0V		10		Ω
	Feedback Leakage Current	$V_{1V8\_ALW\_FBP}$ = 5.5V	-	-	100	nA
PROTECTION						
	Under-voltage Protection (UVP)		65	70	75	%
	UVP Debounce Time		-	2	-	μs
	Over-voltage Protection (OVP)		125	130	135	%
	OVP Debounce Time			2	-	μs
I_{OCP3}	High-side MOSFET Over-current-Protection(OCP)		4	5	6	A
	OCP Debounce TIme			2		μs
	Thermal Shutdown Protection	T_J Rising		150		?

13.4 VR3 Electrical Characteristics

These specifications apply over V_{VSYS} = 12V, V_{OUT} = 1.8V, TA = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8855(VR3)			Unit
			Min	Typ	Max	
EFFICIENCY						
	Efficiency (Refer to the typical circuit)	VOUT=1.8V, IOUT=5mA to 50mA, DCR<25mΩ		88		%
		VOUT=1.45V, IOUT=0.1A to 3A, DCR<25mΩ		82		%
		VOUT=1.8V, IOUT=0.1A to 3A, DCR<25mΩ		85		%
		VOUT=2.25V, IOUT=3A, DCR<25mΩ		87		%

13.5 VR4 Electrical Characteristics

These specifications apply over V_{VSYS} = 12V, V_{OUT} = 1.5V, TA = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8855(VR4)			Unit
			Min	Typ	Max	
PWM CONTROLLER						
	Switching Frequency Accuracy	Default is 2MHz		-	±10	%
	Maximum Duty Cycle		70	80	90	%
	Minimum Controllable On Time		-	70	-	ns
	High-side MOSFET On Resistance	$V_{1V5\_ALW\_IN}$=5V		55		mΩ
	Low-side MOSFET On Resistance	$V_{1V5\_ALW\_IN}$=5V		40		mΩ
	Input Leakage Current	VR4 is off, $V_{1V5\_ALW\_IN}$=5.5V			1	µA
	LX Leakage Current	$V_{1V5\_ALW\_LX}$=5.5V, $V_{1V5\_ALW\_IN}$=5.5V			1	µA
	Zero Current Offset		-5		5	mV
PWM OUTPUT VOLTEGE						
	Output Voltage Accuracy	T_A = 25°C		-	±0.8	%
	Output Voltage Load Regulation				±0.2	%
	Load Transient Drop Voltage	Tr=200ns, I_{OUT}=0.81A to 3A, Refer to the typical circuit			-3	%
	Load Transient Overshoot Voltage	Tf=200ns, I_{OUT}=3A to 0.81A, Refer to the typical circuit			+3	%
	Output Step Ramp Rate Accuracy		-10		+10	%
	Output Voltage Soft-start Rate		9	10	11	mV/µs
	Output Discharge Resistance	CTL=0V		10		Ω
	Feedback Leakage Current	$V_{1V5\_ALW\_FBP}$ = 5.5V	-	-	100	nA

13.5 VR4 Electrical Characteristics

These specifications apply over V_{VSYS} = 12V, V_{OUT} = 1.5V, TA = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8855(VR4)			Unit
			Min	Typ	Max	
PROTECTION						
	Under-voltage Protection (UVP)		65	70	75	%
	UVP Debounce Time		-	2	-	µs
	Over-voltage Protection (OVP)		125	130	135	%
	OVP Debounce Time			2	-	µs
I_{OCP}	High-side MOSFET Over-current-Protection(OCP)		4	5	6	A
	OCP Debounce Time			2		µs
	Thermal Shutdown Protection	T_J Rising		150		?
EFFICIENCY						
	Efficiency (Refer to the typical circuit)	VOUT=1.5V, IOUT=5mA to 50mA, DCR<25mΩ		85		%
		VOUT=1.45V, IOUT=0.1A to 3A, DCR<25mΩ		82		%
		VOUT=1.5V, IOUT=0.1A to 3A, DCR<25mΩ		85		%
		VOUT=2.0V, IOUT=3A, DCR<25mΩ		86		%

13.6 VR5 Electrical Characteristics

These specifications apply over V_{VSYS} = 12V, V_{OUT} = 0.95V, TA = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8855(VR5)			Unit
			Min	Typ	Max	
PWM OUTPUT VOLTAGE						
	Output Voltage Accuracy	T_A = 25°C	-	-	±10	mV
	Output Voltage Line/Load Regulation				5	mV
	Load Transient Drop Voltage	Tr=200ns, I_{OUT}=2.16A to 8A, Refer to the typical circuit			-35	mV
	Load Transient Overshoot Voltage	Tf=200ns, I_{OUT}=8A to 2.16A, Refer to the typical circuit			+35	mV
	Output Step Ramp Rate Accuracy		-10		+10	%
	Output Voltage Soft-start Rate		9	10	11	mV/µs
	Output Discharge Resistance			10		Ω
	Feedback Leakage Current	$V_{VDDP\_ALW\_FBP}$ = 5.5V	-	-	100	nA
	VDDP_ALW_GPIO Threshold	VDDP_ALW_GPIO rising		1.0	1.2	V
		VDDP_ALW_GPIO falling	0.6	0.8		V
	VDDP_ALW_GPIO Input Leakage Current	$V_{VDDP\_ALW\_GPIO}$=5V			1	uA
	VDDP_ALW_GPIO Debounce Time	High to low and low to high		2		us

13.6 VR5 Electrical Characteristics

These specifications apply over V_{VSYS} = 12V, V_{OUT} = 0.95V, TA = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8855(VR5)			Unit
			Min	Typ	Max	
PWM GATE DRIVER						
	Switching Frequency Accuracy	V_{IN}=5.5 to 20V, V_{OUT}=2.6V to 4V		-	±15	%
	Minimum Off Time			200		ns
	Minimum Controllable On Time			60	80	ns
	PWM Sink Resistance			15	20	Ω
	PWM Source Resistance			15	20	Ω
	PWM Leakage Current	$V_{VDDP\_ALW\_PWM}$=5.5V			100	nA
PROTECTION						
	Under-voltage Protection (UVP)		65	70	75	%
	UVP Debounce Time		-	2	-	µs
	Over-voltage Protection (OVP)		125	130	135	%
	OVP Debounce Time			2	-	µs
EFFICIENCY						
	Efficiency (Refer to the typical circuit)	VOUT=0.95V, IOUT=5mA to 10mA, DCR<10mΩ		87		%
		VOUT=0.95V, IOUT=50mA to 500mA, DCR<10mΩ		87		%
		VOUT=0.95V, IOUT=3A, DCR<10mΩ		86		%
		VOUT=0.95V, IOUT=8A, DCR<10mΩ		86		%

13.7 VR6 Electrical Characteristics

These specifications apply over $V_{LDO\_RTC\_IN}$ = 3.3V, TA = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8855(VR6)			Unit
			Min	Typ	Max	
SUPPLY VOLTAGE						
	Input Bias Current		-	1	2	µA
REGULATOR OUTPUT						
	Output Voltage	I_{OUT}=4.5µA	1.425	1.500	1.575	V
	Output Current Capability		4.5			µA
	Output Noise	f=100 to 100kHz		100		μV_{RMS}
	Power-Supply Rejection Ration (PSRR)	f=10kHz	40			dB
	Output Voltage Soft-start Time			1		ms

13.8 VR7 Electrical Characteristics

These specifications apply over V_{5V_ALW} = 5.06V, $V_{VDD\_FCH\_S5}$ = 0.78V, TA = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8855(VR7)			Unit
			Min	Typ	Max	
REGULATOR OUTPUT						
	Output Voltage Accuracy	T_A = 25°C	-	-	±1	%
	Output Voltage Load Regulation	IOUT=0.06A to 0.2A			±0.5	%
	Output Load Transient Drop Voltage	Tr=1us, IOUT=0.06A to 0.2A, Refer to the typical circuit			-8.5	%
	Output Load Transient Overshoot Voltage	Tf=1us, IOUT=0.2A to 0.06A, Refer to the typical circuit			+8.5	%
	Dropout Voltage	I_{OUT}=200mA		25	50	mV
	Output Discharge Resistance			10		Ω
	Output Noise	f=100 to 100kHz		100		μV_{RMS}
	Power-Supply Rejection Ration (PSRR)	f=10kHz	40			dB
	Current Limit		300	400	500	mA
	Under Voltage Protection (UVP)		45	50	55	%
	Output Voltage Soft-start Rate		9	10	11	mV/µs
SWITCH OUTPUT						
	Switch On Resistance			10	20	mΩ
	Over Current-Protection		2	2.5		A
	Input Leakage Current	$V_{VDD\_FCH\_S5\_REFN}$=5.5V			1	µA
CONTROL LOGIC						
	S5_MUX Input Logic Threshold	Rising		1.0	1.2	V
		Falling	0.6	0.8		
	Transition Threshold from Switch to LDO	From switch to LDO		0.78		V
		From LDO to switch		0.8		
	S5_MUX Input Leakage Current	V_{S5_MUX}=5V			1	uA

13.9 VSYS&POK&CTL Electrical Characteristics

These specifications apply over V_{5V_ALW} = 5.06V, TA = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8855(POK)			Unit
			Min	Typ	Max	
VSYS SUPPLY CCURRENT						
	VSYS Supply Current	VSYS=19V, CTL=Low, only 5V_LDO, 3V3_LDO, LDO_RTC are on		110		µA
		CTL=High, all VR are on, VR1/2/3/4/5 are no switching		TBD		µA
POK						
	POK Threshold	POK in from Lower (POK goes high) Monitor VR1~5 and VR7(LDO Output or Switch OCP)	87	90	93	%
		POK out to normal (POK goes low) Monitor VR1~5 and VR7(LDO Output or Switch OCP)	125	130	135	%
		POK Hysteresis		3		%
	POK Leakage Current	VPOK = 5V	-	0.1	1	? µA?
	POK Low Voltage	I_{POK_sink} =4mA	-	0.5	1	V
	POK Enable Blanking Time	From VR1~VR5,VR7 rising to 90% of their set point to POK goes High	-	1320	-	µs
	POK Disable Blanking Time	From VR1~VR5, VR7 falling to 87% of their set point to POK goes Low		2		µs
CTL						
	CTL Input Logic Threshold	V_{CTL} rising		1.0	1.2	V
		V_{CTL} falling	0.6	0.8		V
	CTL Leakage Current	V_{CTL}=5V			1	? µA
t_{DCTL}	CTL Debounce Time	CTL high to 5V_ALW start soft-start		70		? µs
		CTL low to 5V_ALW start soft-stop		2		? µs
t_{D1}	5V_ALW and 3V3_ALW Timing	5V_ALW ready to 1V8_ALW soft-start		100		? µs
		VR1~5 ready to VR7 soft-start		100		? µs
t_{D2}		1V8_ALW off to 5V_ALW soft-stop		100		? µs

13.10 I2C Electrical Characteristics

Timing characteristics for I2C Interface signals over recommended operating conditions (unless otherwise noted)

Symbol	Parameter	High Speed		Fast Speed Plus		Fast Speed		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCL}	Frequency, SCL		3.4		1		0.4	MHz
$t_{W(H)}$	Pulse Duration, SCL High	60		260		600		ns
$t_{W(L)}$	Pulse Duration, SCL Low	160		500		1300		ns
t_r	Rise Time, SCL and SDA	10	40		120	20+0.1 C_L(pF)	300	ns
tf	Fall Time, SCL and SDA	10	80		120	20+0.1 C_L(pF)	300	ns
t_{setup1}	Setup Time, SCL to SDA	10				100		ns
t_{hold1}	Hold Time, SCL to SDA	0				0		ns
$t_{(buf)}$	Bus Free Time Between Stop and Start Condition			500		1300		ns
t_{setup2}	Setup Time, SCL to Start Condition	160				600		
t_{hold2}	Hold Time, Start condition to SCL	160				600		
t_{setup3}	Setup Time, SCL to Stop Condition	160				600		
C_L	Load Capacitance for Each Bus Line		100				400	pF

14.Register Description

14.1 Register Map

Channel	Register Name	Register Address	Read/Write/Read Only State	Default Value
VR1	5V_ALW DAC	0x01	R/W	0x6d
	5V_ALW Control	0x02	R/W	0x08
VR2	3V3_ALW DAC	0x03	R/W	0x15
	3V3_ALW Control	0x04	R/W	0x08
VR3	1V8_ALW DAC	0x05	R/W	0x24
	1V8_ALW Control	0x06	R/W	0x04
VR4	1V5_ALW DAC	0x07	R/W	0x47
	1V5_ALW Control	0x08	R/W	0x04
VR5	VDDP_ALW DAC	0x09	R/W	0x2e
	VDDP_ALW Control	0x0A	R/W	0x08
VR7	VDD_FCH_S5 DAC	0x0B	R/W	0x1d
	VDD_FCH_S5 Control	0x0C	R/W	0x00
Thermal	Thermal Report	0x2C	R	-
POK	POK Blanking Time	0x26	R/W	0x7d
ID	Version ID	0xF0	R	0x00

14.2 VR1 Register Table

Address	0x01							
Field Name	5V_ALW DAC [7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	5V_ALW_VSEL							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	1	1	0	1	1	0	1
Bit Name	**Bit Definition**							
5V_ALW_VSEL	00h : shutdown 51h : VR1&$V_{5V\_ALW\_LDO}$ Voltage = 4500mV. 52h : VR1&$V_{5V\_ALW\_LDO}$ Voltage = 4520mV. 53h : VR1&$V_{5V\_ALW\_LDO}$ Voltage = 4040mV. … 6dh : VR1&$V_{5V\_ALW\_LDO}$ Voltage = 5060mV (Default) …. 83h : VR1&$V_{5V\_ALW\_LDO}$ Voltage = 5500mV. 84h ~ ffh: Reserved.							

Address	0x02							
Field Name	5V_ALW CONTROL [7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reserved		5V_ALW_SLEW		5V_ALW_FSW _SEL		5V_ALW__SEL	5V_ALW__EN
Read/Write			R/W	R/W	R/W	R/W	R/W	R/W
Power On Default			0	0	1	0	0	0
Bit Name	**Bit Definition**							
5V_ALW__EN	0: VR1 off (Default) 1: VR1 on							
5V_ALW__SEL	0: VR1 on/off is controlled by CTL (Default) 1: VR1 on/off is controlled by 5V_ALW_EN State							
5V_ALW_FSW_SEL	00 : FSW = 1.0MHz at PWM mode. 01 : FSW = 0.6MHz at PWM mode. 10 : FSW = 0.8MHz at PWM mode. (Default) 11 : FSW = 1.2MHz at PWM mode.							
5V_ALW_SLEW	00 : Transition slew rate = 10mV/us. (Default) 01 : Transition slew rate = 15mV/us. 10 : Transition slew rate = 20mV/us. 11: Transition slew rate = 25mV/us							

14.3 VR2 Register Table

Address	0x03							
Field Name	3V3_ALW DAC [7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	3V3_ALW_VSEL							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	1	0	1	0	1
Bit Name	**Bit Definition**							
3V3_ALW_VSEL	00h : shutdown 01h : VR2&$V_{3V3\_ALW\_LDO}$ Voltage = 2900mV. 02h : VR2&$V_{3V3\_ALW\_LDO}$ Voltage = 2920mV. 03h : VR2&$V_{3V3\_ALW\_LDO}$ Voltage = 2940mV. … 15h : VR2&$V_{3V3\_ALW\_LDO}$ Voltage = 3300mV (Default) …. 38h : VR2&$V_{3V3\_ALW\_LDO}$ Voltage = 4000mV.							

Address	0x04							
Field Name	3V3_ALW CONTROL [7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reserved		3V3_ALW_SLEW		3V3_ALW_FSW _SEL		3V3_ALW_ _SEL	3V3_ALW_ _EN
Read/Write			R/W	R/W	R/W	R/W	R/W	R/W
Power On Default			0	0	1	0	0	0
Bit Name	**Bit Definition**							
3V3_ALW__EN	0: VR2 off (Default) 1: VR2 on							
3V3_ALW__SEL	0: VR2 on/off is controlled by CTL (Default) 1: VR2 on/off is controlled by 3V3_ALW_EN State							
3V3_ALW_FSW_SEL	00 : FSW = 1.0MHz at PWM mode. 01 : FSW = 0.6MHz at PWM mode. 10 : FSW = 0.8MHz at PWM mode. (Default) 11 : FSW = 1.2MHz at PWM mode.							
3V3_ALW_SLEW	00 : Transition slew rate = 10mV/us. (Default) 01 : Transition slew rate = 15mV/us. 10 : Transition slew rate = 20mV/us. 11: Transition slew rate = 25mV/us							

14.4 VR3 Register Table

Address	0x05							
Field Name	1V8_ALW DAC [7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	1V8_ALW_VSEL							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	1	0	0	1	0	0
Bit Name	**Bit Definition**							
1V8_ALW_VSEL	00h : shutdown 01h : VR3 Voltage = 1450mV. 02h : VR3 Voltage = 1460mV. 03h : VR3 Voltage = 1470mV. … 24h : VR3 Voltage = 1800mV (Default) …. 51h : VR3 Voltage = 2250mV. 52h~ffh : Reserved							

Address	0x06							
Field Name	1V8_ALW CONTROL [7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reserved		1V8_ALW_SLEW		1V8_ALW_FSW _SEL		1V8_ALW_ _SEL	1V8_ALW_ _EN
Read/Write			R/W	R/W	R/W	R/W	R/W	R/W
Power On Default			0	0	0	1	0	0
Bit Name	**Bit Definition**							
1V8_ALW__EN	0: VR3 off (Default) 1: VR3 on							
1V8_ALW__SEL	0: VR3 on/off is controlled by CTL (Default) 1: VR3 on/off is controlled by 1V8_ALW_EN State							
1V8_ALW_FSW_SEL	00 : FSW = 3.0MHz at PWM mode. 01 : FSW = 2.0MHz at PWM mode. (Default) 10 : FSW = 1.0MHz at PWM mode. 11 : FSW = 4.0MHz at PWM mode.							
1V8ALW_SLEW	00 : Transition slew rate = 10mV/us. (Default) 01 : Transition slew rate = 15mV/us. 10 : Transition slew rate = 20mV/us. 11: Transition slew rate = 25mV/us							

14.5 VR4 Register Table

Address	0x07							
Field Name	**1V5_ALW DAC [7:0]**							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	1V5_ALW_VSEL							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	1	0	0	0	1	1	1
Bit Name	**Bit Definition**							
1V5_ALW_VSEL	00h : shutdown 01h : VR4 Voltage = 800mV. 02h : VR4 Voltage = 810mV. 03h : VR4 Voltage = 820mV. … 47h : VR4 Voltage = 1500mV (Default) …. 79h : VR4 Voltage = 2000mV. 80h~ffh : Reserved							

Address	0x08							
Field Name	**V1V5_ALW CONTROL [7:0]**							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reserved		1V5_ALW_SLEW		1V5_ALW_FSW _SEL		1V5_ALW_ _SEL	1V5_ALW_ _EN
Read/Write			R/W	R/W	R/W	R/W	R/W	R/W
Power On Default			0	0	0	1	0	0
Bit Name	**Bit Definition**							
1V5_ALW__EN	0: VR4 off (Default) 1: VR4 on							
1V5_ALW__SEL	0: VR4 on/off is controlled by CTL (Default) 1: VR4 on/off is controlled by 1V5_ALW_EN State							
1V5_ALW_FSW_SEL	00 : FSW = 3.0MHz at PWM mode. 01 : FSW = 2.0MHz at PWM mode. (Default) 10 : FSW = 1.0MHz at PWM mode. 11 : FSW = 4.0MHz at PWM mode.							
1V5_ALW_SLEW	00 : Transition slew rate = 10mV/us. (Default) 01 : Transition slew rate = 15mV/us. 10 : Transition slew rate = 20mV/us. 11: Transition slew rate = 25mV/us							

14.6 VR5 Register Table

Address	0x09							
Field Name	VDDP_ALW DAC [7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	VDDP_ALW_VSEL							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	1	0	1	1	1	0
Bit Name	**Bit Definition**							
VDDP_ALW_VSEL	00h : shutdown 01h : VR5 Voltage = 500mV. 02h : VR5 Voltage = 510mV. 03h : VR5 Voltage = 520mV. … 2eh : VR5 Voltage = 950mV (Default) …. 65h : VR5 Voltage = 1500mV. 66h~ffh : Reserved							

Address	0x0A							
Field Name	VDDP_ALW CONTROL [7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reserved		VDDP_ALW_SLEW		VDDP_ALW_FSW_SEL		VDDP_ALW__SEL	VDDP_ALW__EN
Read/Write			R/W	R/W	R/W	R/W	R/W	R/W
Power On Default			0	0	1	0	0	0
Bit Name	**Bit Definition**							
VDDP_ALW_EN	0: VR5 off (Default) 1: VR4 on							
VDDP_ALW_SEL	0: VR5 on/off is controlled by CTL, and output voltage is control by VDDP_ALW_GPIO. (Default) 1: VR5 on/off is controlled by VDDP_ALW_EN State and output voltage is control by VDDP_ALW_VSEL.							
VDDP_ALW_FSW_SEL	00 : FSW = 0.3MHz at PWM mode. 01 : FSW = 0.6MHz at PWM mode. 10 : FSW = 0.5MHz at PWM mode. (Default) 11 : FSW = 0.8MHz at PWM mode.							
VDDP_ALW_SLEW	00 : Transition slew rate = 10mV/us. (Default) 01 : Transition slew rate = 15mV/us. 10 : Transition slew rate = 20mV/us. 11: Transition slew rate = 25mV/us							

14.7 VR6 Register Table

Address	0x0B							
Field Name	**VDD_FCH_S5 DAC [7:0]**							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	VDD_FCH_S5_VSEL							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	1	1	1	0	1
Bit Name	**Bit Definition**							
VDD_FCH_S5_VSEL	00h : shutdown 01h : VR7 Voltage = 500mV. 02h : VR7 Voltage = 510mV. 03h : VR7 Voltage = 520mV. … 1dh : VR7 Voltage = 780mV (Default) …. 65h : VR7 Voltage = 1500mV. 66h~ffh : Reserved							

Address	0x0C							
Field Name	**VDD_FCH_S5 CONTROL [7:0]**							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reserved		Reserved				VDD_FCH_S5_SEL	VDD_FCH_S5_EN
Read/Write							R/W	R/W
Power On Default							0	0
Bit Name	**Bit Definition**							
VDD_FCH_S5_EN	0: VR7 off (Default) 1: VR7 on							
VDD_FCH_S5_SEL	0: VR7 on/off is controlled by CTL. (Default) 1: VR7 on/off is controlled by VDD_FCH_S5_EN State.							

14.8 Thermal Report Register Table

Address	0x2C							
Field Name	THERMAL REPORT[7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reserved			THERMAL REPORT				
Read/Write				R	R	R	R	R
Power On Default				-	-	-	-	-
Bit Name	**Bit Definition**							
Thermal Report	00000 : -10℃ 00001 : -5℃ 00010 : 0℃ … 01000 : 30℃ … 11110 : 140℃ 11111 : 145℃							

14.9 POK BLANKING Time Register Table

Address	0x26							
Field Name	POK BLANKING TIME [7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	POK BLANKING TIME							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	1	1	1	1	1	0	1
Bit Name	**Bit Definition**							
POK Blanking Time	00h : 320us 01h : 328us 02h : 336us … 7dh : 1320us (Default) …. ffh : 2360us							

14.10 Version ID Register

Address	0xF0							
Field Name	VERSION ID [7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	VERSION ID [7:0]							
Read/Write	R	R	R	R	R	R	R	R
Version A Default	0	0	0	0	0	0	0	0
Bit Name	**Bit Definition**							
VERSION ID	VERSION ID 00h:Verson A							

15.Function Description

15.1 VR Function Description

Soft-Start

All VRs are equipped soft-start function, when enable signal of each VR is activated, an internal soft start ramps the output voltage at a rate of 10mV/usec. This allows the output voltage to ramp up gradually, eliminating overshoot and excessive in rush current.

Over Voltage Protection (OVP) for VR3 and VR4

The over voltage protection circuitry monitors the feedback voltage to prevent the output from accidently exceeding the desired set point. Once the feedback voltage exceeds typically 130% of the set point voltage, the high side MOSFET turn off, Low side MOSFET turns off and internal latch circuitry is activated. This insures protection of the load damage and circuit reset is only achieved either by internal reset via the I2C, CTL or by cycling the power.

Over Current Protection (OCP) and Under Voltage Protection (UVP) for VR3 and VR4

The switching converter is protected against gradual over current or sudden short on its output. When inductor current peak value exceeds the set threshold an internal over-current protection is activated which turns off the high side and low side MOSFETs.

Once the output voltage drops below a typical threshold of 70% of the output set point value, both high side and low side MOSFETs turn off and an internal latch circuit is initiated.

When any of OCP or UVP is activated, the IC will be latch off, need reset via the I2C, CTL or by cycling the power.

Over Voltage Protection (OVP) and Under Voltage Protection (UVP) for VR1, VR2 and VR5

Once the output voltage drops below a typical threshold of 70% of set point value or the output voltage exceeds typically 130% of the set point voltage, the PWM signal will be latched low to turn off the converter and discharge the output voltage.

When any of UVP or OVP is activated, need reset via CTL or by cycling the power.

Soft-Stop

When VR3 or VR4 is shut down by CTL or I2C, both Upper and Lower MOSFETs will be turned off and an internal MOSFET with about 10ohm (Typ.) Rds-on discharges the output via the FBP pin. The VR7 also discharges the output via the output pin.

When VR1, VR2, VR5 is shut down by CTL or I2C, the PWM signal pin will be low level to discharge the output voltage via the low-side MOSFET of APW8703.

VDD_FCH_S5 Output Voltage

The VDD_FCH_S5 output voltage level will be changed between internal fixed LDO regulator and external REFIN input voltage, and it depends on S5_MUX signal and the REFIN voltage level. When MUX_S5 is high, the FCH_S5 output voltage will follow the REFIN input voltage. When MUX_S5 is low, REFIN input voltage is below 0.78mV, FCH_S5 output voltage will change to internal LDO regulator. When MUX_S5 is low, and REFIN input voltage is above 0.78mV, FCH_S5 output voltage will follow the REFIN input voltage. Below table shows the FCH_S5 output voltage operation.

MUX_S5	REFIN	VDD_FCH_S5 Output
H	X	Track REFIN Voltage
L	<0.78V	Internal LDO regulator Output
L	≧0.78V	Track REFIN Voltage

15.1 VR Function Description(Cont.)

POK Output

The POK circuitry monitors the VR1-VR5 via the FB pins of each regulator to make sure that the output of each regulator has reached its desired set point during the start up. When all these voltages have reached 90% of their set point, then POK will switch from a low state to high after a 1 ms delay time. The POK pin is an open drain output that will switch high via an external pull up resistor. It can be pulled up to a maximum voltage of up to 5.5V.

The POK also monitors the FB voltage for any over voltage that may happen during the operation. This threshold is typically set at 130% of the desired set point. If any of the voltages exceeds this threshold and satisfied the blanking time the POK switches low and after a short delay of about 2usec or so, the outputs latch off and system returns to G3 state.

During the power down or at any point either of these VR1-VR5, output voltages drop below 90% typical set point and continue over blanking time, the POK pin switches to low state again.

15.2 I2C Function Description

I2C Overview

APW8855 is a slave-only device that is mastered by the SoC. It resides off the SoC's I2C. The slave device implemented on APW8855 side is an asynchronous implementation and will support the high speed mode (3.4MHz). Some of the main features for the I2C slave are:

- APW8855 is accessed using a 7-bit addressing scheme.
- I2C slave is not allowed to stretch the clock, and must be capable of being multi-mastered in a debug environment.
- The interface draws as minimum power when not actively reading/writing registers.
- The slave adapts to the incoming frequency without any communication as the protocol for fast mode and high speed mode is the same.
- Interface implementation is asynchronous.

Slave Address

APW8855 supports the standard I2C read and write functions. The configuration register space is divided to 59-byte partitions. APW8855 supports five 7-bit device addresses to access each of the 59 byte partitions.

Slave Address
1101110

Table 5. I2C Slave Addresses

The slave addresses need to be locked in order to avoid that software can overwrite them and disable the communication.

15.2 I2C Function Description(Cont.)

Protocol

Reads from PMIC registers follow the “combined protocol” as described in the I2C specification, in which the first byte written is the register offset to be read, and the first byte read (after a repeat START condition) is the data from that register offset. See the figures below for details. The following diagrams capture the different high-speed and fast-speed transaction format/protocol.

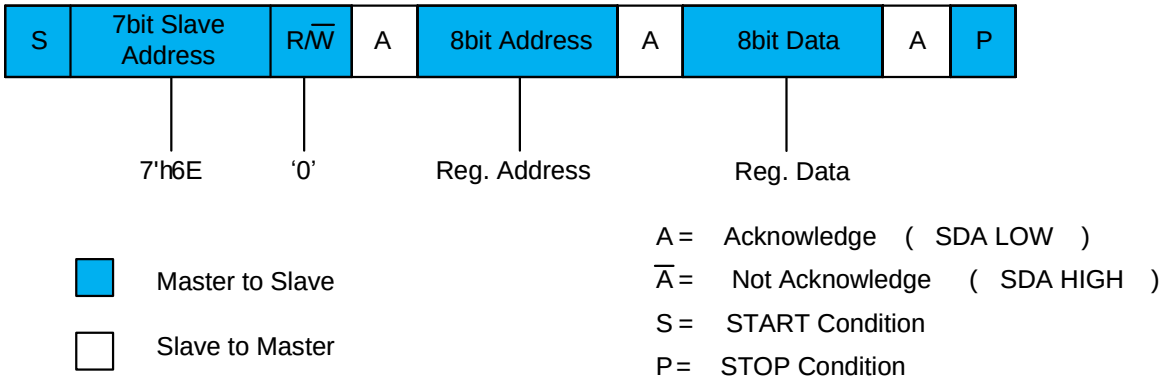


Figure 1. I2C Fast Speed / Fast Speed Plus Single Byte Write

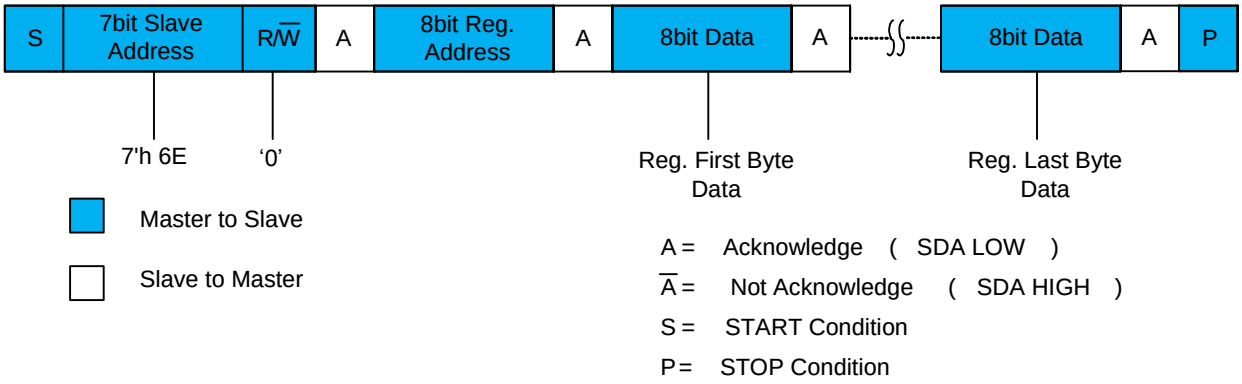


Figure 2. I2C Fast Speed / Fast Speed Plus Multiple Byte Write

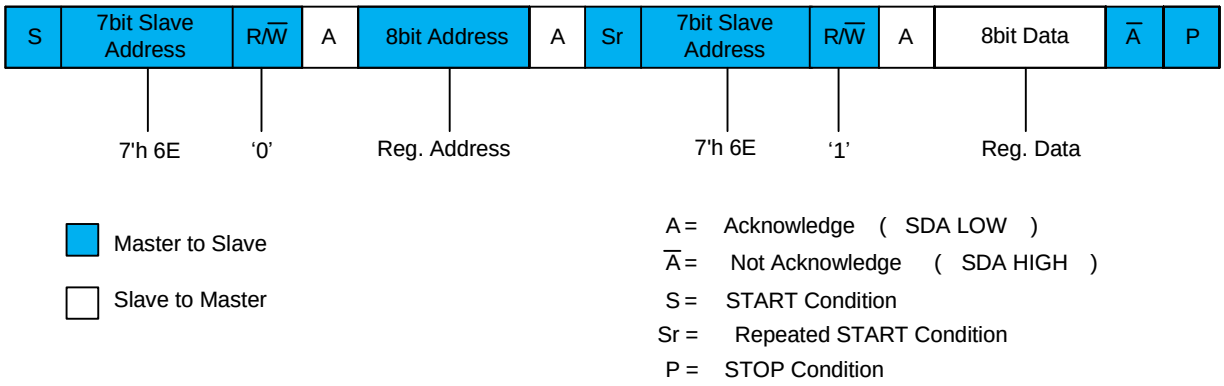


Figure 3. I2C Fast Speed / Fast Speed Plus Single Byte Read

15.2 I2C Function Description(Cont.)

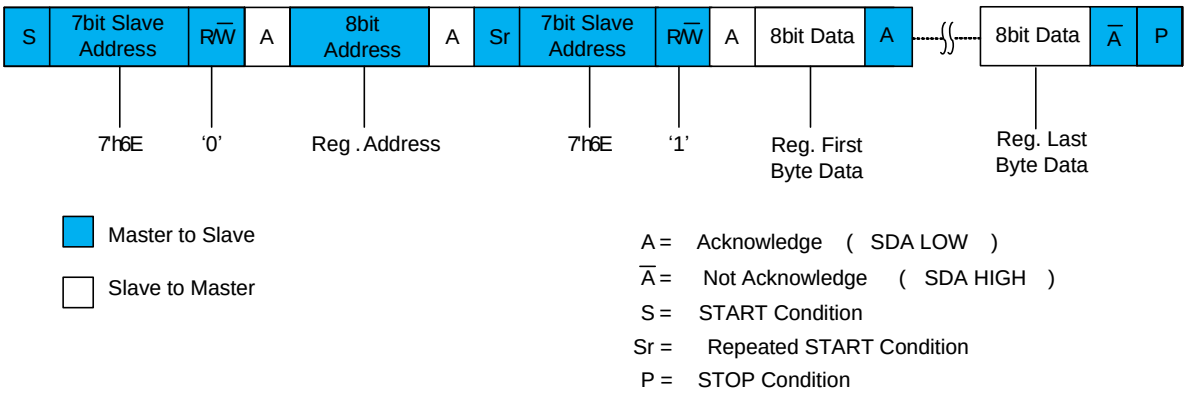


Figure 4. I2C Fast Speed / Fast Speed Plus Multiple Byte Read

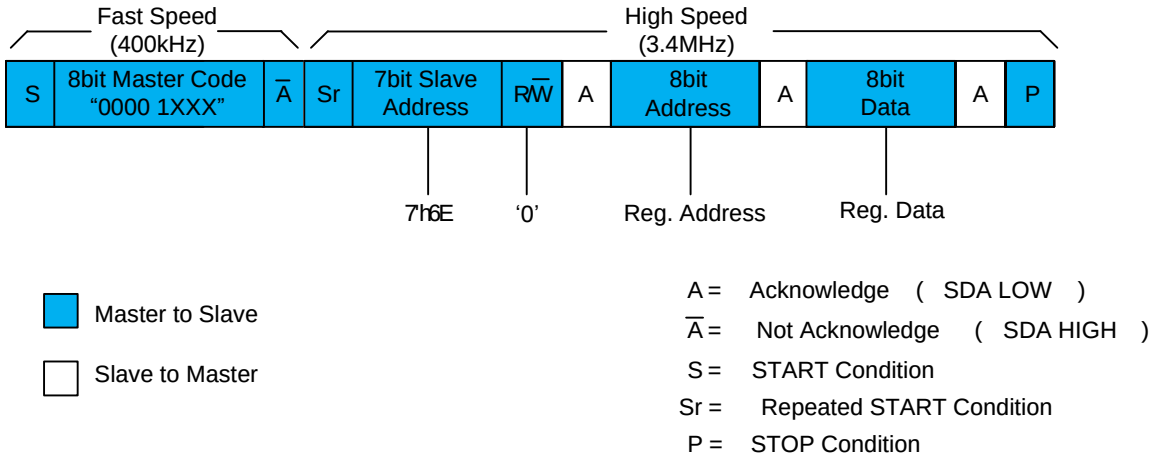


Figure 5. I2C High Speed Single Byte Write

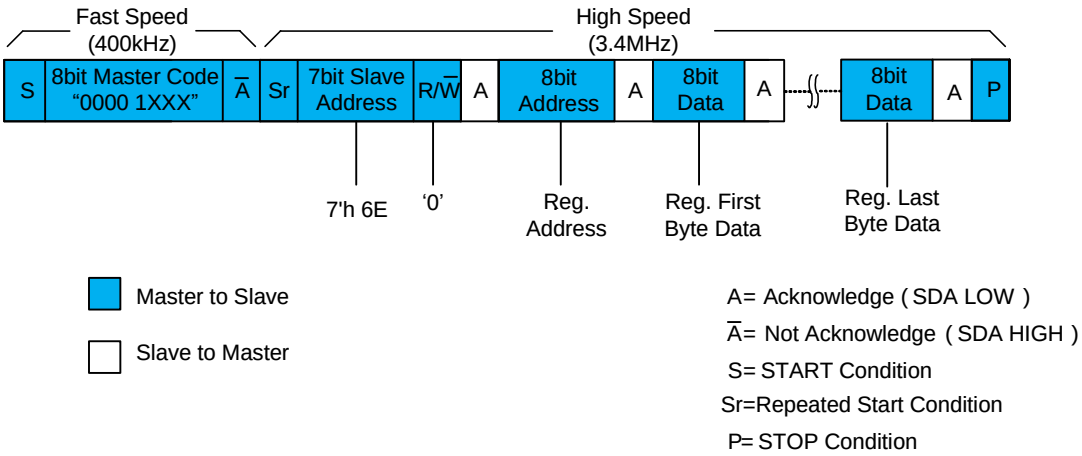


Figure 6. I2C High Speed Multiple Byte Write

15.2 I2C Function Description(Cont.)

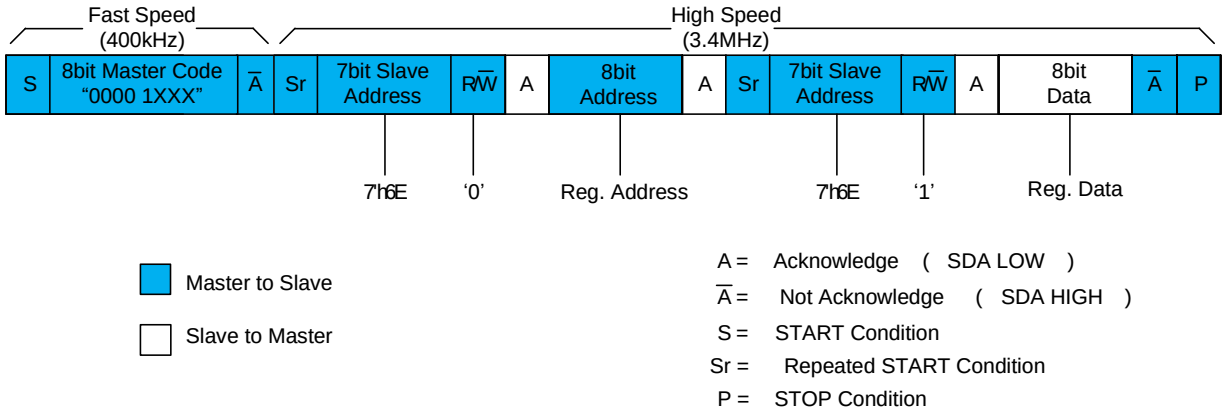


Figure 7. I2C High Speed Single Byte Read

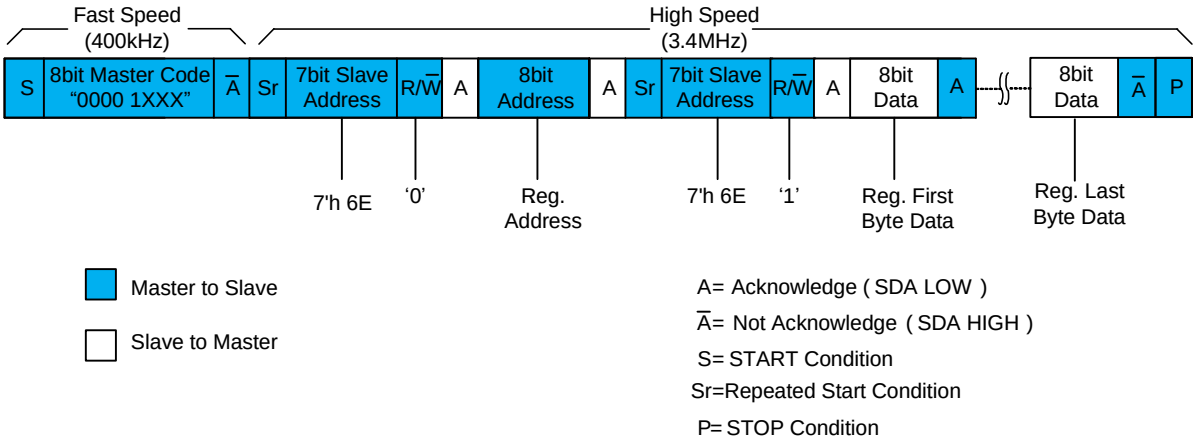


Figure 8. I2CHigh Speed Multiple Byte Read

16.Application Information

Output Voltage Selection

The duty cycle (D) of a buck converter is the function of the input voltage and output voltage. Once an output voltage is fixed, it can be written as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

For PWM converter, the inductor value (L) determines the sum of the inductor ripple currents ΔI_{P-P}, and affects the load transient response. Higher inductor value reduces the output capacitors¡¦ ripple current and induces lower output ripple voltage. The ripple current can be approximated by:

$$\Delta I_{P-P} = \frac{V_{IN} - V_{OUT}}{F_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Where F_{SW} is the switching frequency of the regulator, although the inductor value and frequency are increased and the ripple current and voltage are reduced, a tradeoff exists between the inductor¡¦s ripple current and the regulator load transient response time. A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current. Increasing the switching frequency (F_{SW}) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFETs and the power dissipation of the converter. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current. Once the inductance value has been chosen, select an inductor that is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This results in a larger output ripple voltage.

Output Capacitor Selection

Output voltage ripple and the transient voltage deviation are factors that have to be taken into consideration when selecting output capacitors. Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, selecting high performance low ESR capacitors is recommended for switching regulator applications. In addition to high frequency noise related to MOSFET turn-on and turn-off, the output voltage ripple includes the capacitance voltage drop ΔV_{COUT} and ESR voltage drop ΔV_{ESR} caused by the AC peak-to-peak sum of the inductor's current. The ripple voltage of output capacitors can be represented by:

$$\Delta V_{COUT} = \frac{\Delta I_{P-P}}{8 \times C_{OUT} \times F_{SW}}$$

$$\Delta V_{ESR} = \Delta I_{P-P} \times R_{ESR}$$

These two components constitute a large portion of the total output voltage ripple. In some applications, multiple capacitors have to be paralleled to achieve the desired ESR value. If the output of the converter has to support another load with high pulsating current, more capacitors are needed in order to reduce the equivalent ESR and suppress the voltage ripple to a tolerable level. A small decoupling capacitor in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors are also must be considered. To support a load transient that is faster than the switching frequency, more capacitors are needed for reducing the voltage excursion during load step change. For getting same load transient response, another aspect of the capacitor selection is that the total AC current going through the capacitors has to be less than the rated RMS current specified on the capacitors in order to prevent the capacitor from overheating.

16.Application Information(Cont.)

Input Capacitor Selection

Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the surge current needed each time high-side MOSFET turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of high-side MOSFET and the source of low-side MOSFET. The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The maximum RMS current rating requirement is approximately $I_{OUT/2}$, where I_{OUT} is the load current.

Layout Consideration

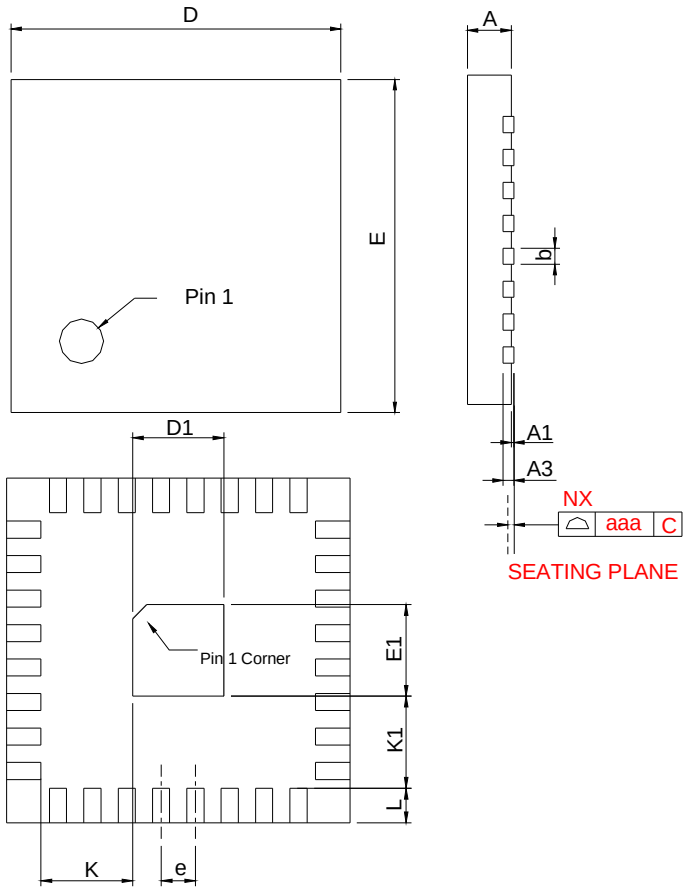
Signal Name	Description	Layout Guidelines
GND	IC's analog ground.	Connect the GND pin to GND plane through several vias directly.
1V5_ALW_PGND,and 1V8_ALW_PGND	IC's power ground pins of VR3 and VR4.	Use a ground plane or a short and wide trace to connect the ground terminals of input capacitors and output capacitors, and 1Vx_ALW_PGND pins on top layer.
Each of VR's Input Pins (VSYS, 1V8_ALW_IN...)	All VR's input voltage pins.	Place the input capacitors on each of the VR's input pins with low impedance to GND and low impedance to the each of VR's input pins.
Each of PWM VR's LX pins (5V_ALW_LX1, 1V8_ALW_LX…)	These are the connections to the mid point of the power stage consisting of the high- and low-side switch. The output inductor is connected here.	Connect to the output inductor with a short wire. For higher efficiency requirement, the inductor and LX pins should be as close as possible, and the trace resistance from LX pin to inductor should be less than 10mOhm is recommended. Ideally, route the high current path like LX pins to inductors and inductors to output capacitors on the top layer is recommended.
Each of PWM VR's output voltage feedback pins (5V_ALW_FBP, 1V8_ALW_FBP…)	Voltage feedback pin for each of VR.	The pins are high impedance and sensible to noise from the switch node. The positive feedback signal should be tied to the V+ pad of the output capacitor directly. The feedback pin could be routed to the input capacitor on the load side for remote sense. Coupling from fast switching signals must be avoided.
VSYS	APW8855 input supply voltage	Connect the input capacitors from VSYS to GND for noise decoupling. The capacitors and VSYS pins should be as close as possible.
5V_ALW_PWM, 3V3_ALW_PWM, VDDP_ALW_PWM	The gate driver outputs of 5V_ALW, 3V3_ALW and VDDP_ALW	The traces of PWM signal from the gate driver output pins to the APW8703 should be short to eliminate the parasitical capacitance; the parasitical capacitance less than 80pF is recommended.

17.Revision History

Version	Date	Revision History	
		Chapter	Description
A1	-	-	Initial description

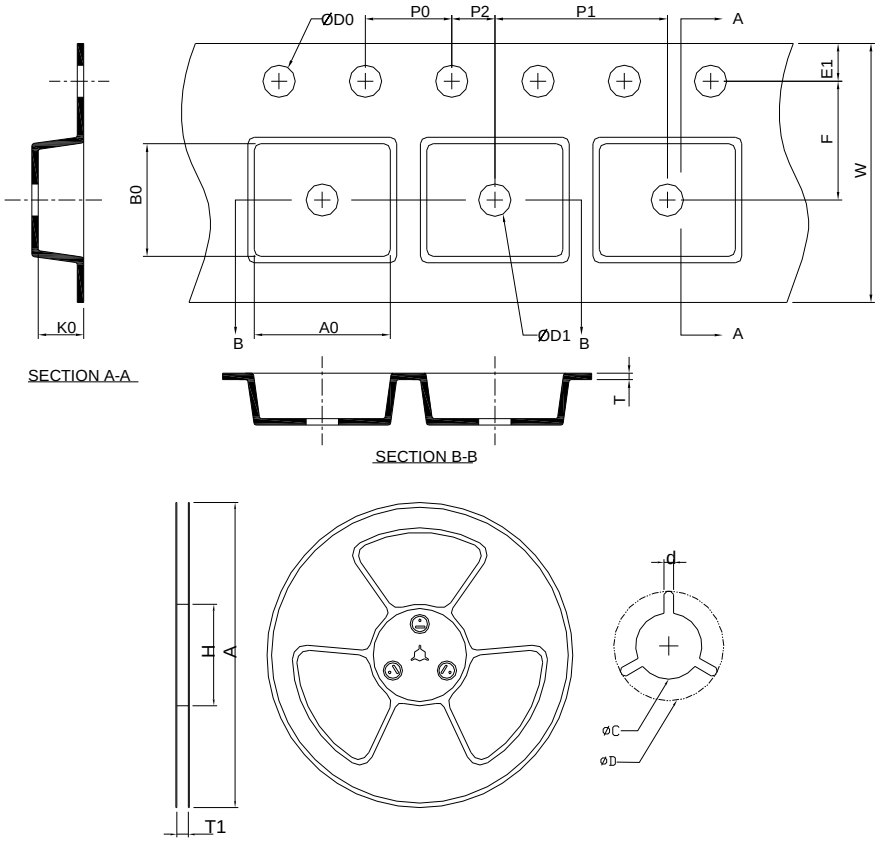
18.Package Information

TQFN4x4-32A



SYMBOL	TQFN4*4-32A			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.15	0.25	0.006	0.010
D	3.90	4.10	0.154	0.161
D1	1.20	1.50	0.047	0.059
E	3.90	4.10	0.154	0.161
E1	1.30	1.60	0.051	0.063
e	0.40 BSC		0.016 BSC	
L	0.25	0.45	0.010	0.018
K	1.02 REF		0.040 REF	
K1	0.93 REF		0.037 REF	
aaa	0.08		0.003	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN4x4	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	4.30±0.20	4.30±0.20	1.30±0.20

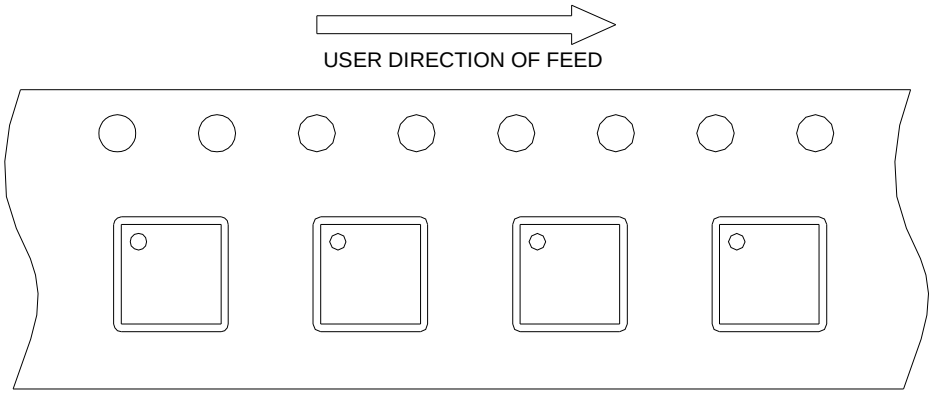
(mm)

Devices Per Unit

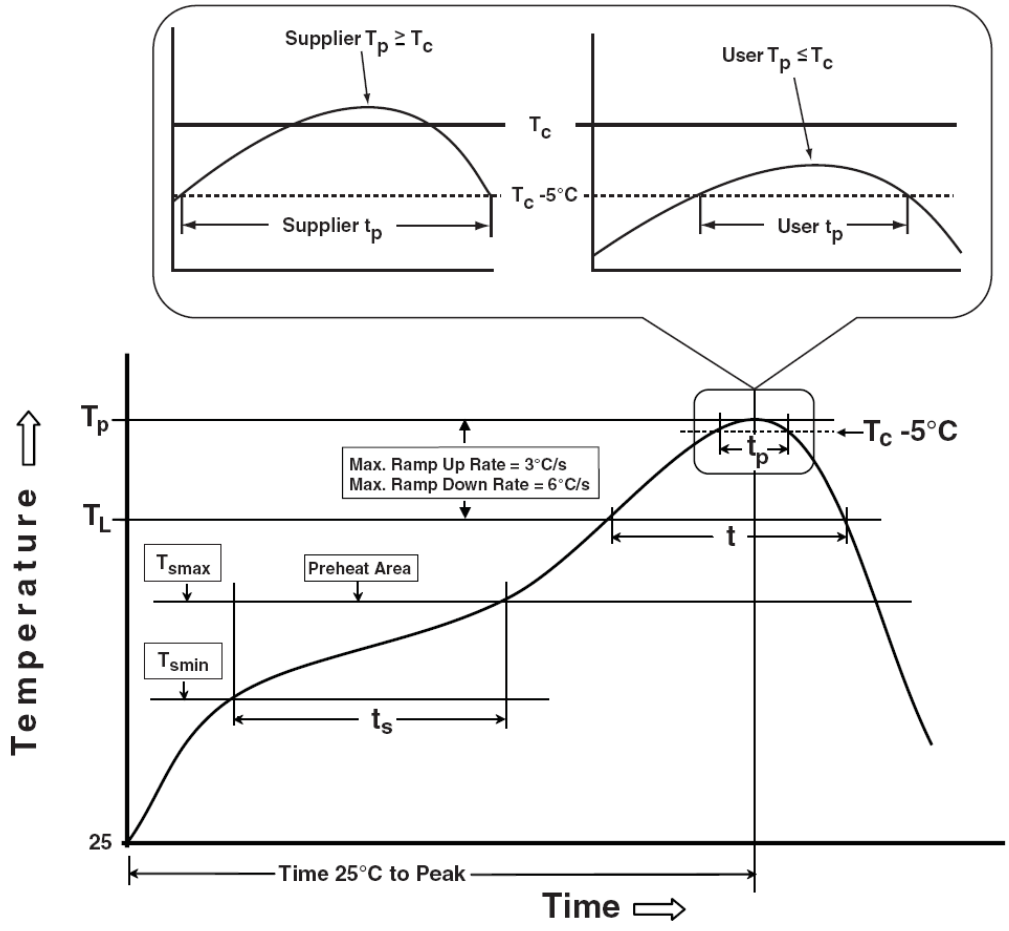
Package Type	Unit	Quantity
TQFN4x4	Tape & Reel	3000

Taping Direction Information

TQFN4x4-32



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.

* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum.
** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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