DDR4 TOTAL POWER SOLUTION (VPP/VDDQ/VTT)
SYNCHRONOUS DC/DC CONVERTER for NB/MB

## Features

**Provide 4 Independent Outputs for VPP, VDDQ, VTT LDO and VTTREF LDO**

**VDDQ Converter**

- **High Input Voltages Range from 4.5V to 25V Input Power**
- **Provide 1.2V (DDR4) or Adjustable Output Voltage Max to 1.8V by SMBus Control**
  **- ±1% Accuracy over Temperature**
- **High Efficiency Performance up to 90% scale & Low Shutdown Current <1uA**
- **Integrated High_Side N-Channel MOSFET 20mΩ and Low_Side N-Channel MOSFET 10mΩ @ VCC=5V**
- **Integrated Bootstrap Forward P-CH MOSFET**
- **Built in Internal Soft-Start: 0.4ms(typ.) and Soft-Stop Functions for PWM Output**
- **Built In Automatic PFM/PWM Mode Selection**
- **Fixed 800kHz Switching Frequency**
- **S3 and S5 Pins Control The Device in S0, S3 or S4/S5 State**
- **Built In PMAX Signal for Total Power Indicator**
- **Power Good Monitoring**
- **60% Under-Voltage Protection (UVP)**
- **125% Over-Voltage Protection (OVP)**
- **Built in Fixed Valley Current Limit Protection**
- **Built In Thermal Shutdown Function**

**VPP Converter**

- **Integrated High_Side P-Channel MOSFET 220mΩ and Low_Side N-Channel MOSFET 200mΩ @ VCC=5V**
- **Excellent Reference Voltage = 0.6V**
  **- ±1% Load/Line Regulations over all TC range**
- **Fixed 1MHz switching Frequency**
- **Built in Internal Soft-Start: 0.2ms(typ.) and Soft-Stop Functions for PWM Output**
- **60% Under-Voltage Protection (UVP)**
- **125% Over-Voltage Protection (OVP)**
- **Built in Fixed Valley Current Limit Protection**
- **Built In Thermal Shutdown Function**

**±0.75A LDO Section (VTT)**

- **Support Only 10μF MLCC for Stability on VTT LDO**
- **VTT and VTTREF Track at Half the VDDQ by internal divider**
- **Built In 0.75A Source/Sink Capability on VTT LDO and 10mA Source/Sink Capability on VTTREF LDO**
- **Independent Current Limit Protection**
- **Thermal Shutdown Protection**
- **4mmx4mm 26-pin package (TQFN-26)**
- **Halogen and Lead Free Available (RoHS Compliant)**

## General Description

The APW8871 integrates two synchronous buck PWM controller and high/low side power MOSFETs to generate VPP and VDDQ, two sourcing and sinking LDO linear regulator to generate VTT and VTTREF. It provides a complete power supply for DDR4 memory system. It offers the lowest total solution cost in system where space is at a premium.

The APW8871 provides excellent transient response and accurate DC voltage output in PFM Mode. In Pulse Frequency Mode (PFM), the APW8871 provides very high efficiency over light to heavy loads with loading-modulated switching frequencies.
The APW8871 has maximum power indicator function in order to prevent over load condition. The device also has single enable for VPP and VDDQ with JEDEC sequence implemented. Moreover, the APW8871 integrates SMBus controller to program VDDQ output voltage, VDDQ DAC voltage adjustment, VDDQ voltage slew rate setting, and VDDQ PWM converter frequency.

The APW8871 is equipped with accurate current-limit, output under-voltage, output over-voltage and over-temperature protections. A Power-On- Reset function monitors the voltage on VCC prevents wrong operation during power on.

## General Description (cont.)

The LDO is designed to provide a regulated voltage with bi-directional output current for DDR-SDRAM termination. The device integrates two power transistors to source or sink current up to 0.75A. It also incorporates current-limit and thermal shutdown protection.

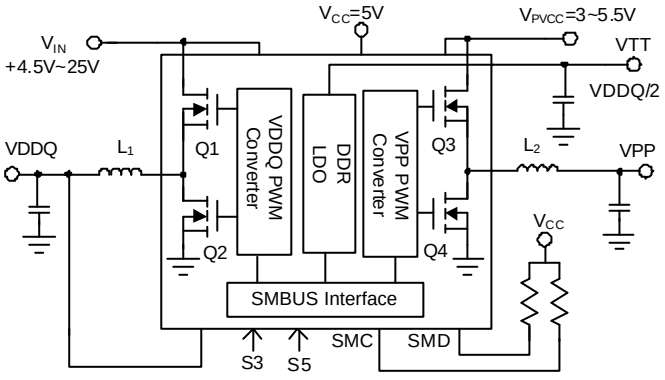
An internal resistor divider is used to provide a half voltage of VDDQ for VTTREF and VTT Voltage. The VTT output voltage is only requiring 10µF of ceramic output capacitance for stability and fast transient response. The S3 and S5 pins provide the sleep state for VTT (S3 state) and suspend state (S4/S5 state) for device, when S5 and S3 are both pulled low the device provides the soft-off for VTT and VTTREF.

The APW8871 is available in 4mmx4mm 26-pin Thin QFN package.

## Applications

- **DDR3 and DDR4 Memory Power Supplies**
- **NB/MB/Tablet**

## Simplified Application Circuit



## Ordering and Marking Information

APW8871 □□ – □□ □

- Lead Free Code
- Handling Code
- Temperature Range
- Package Code

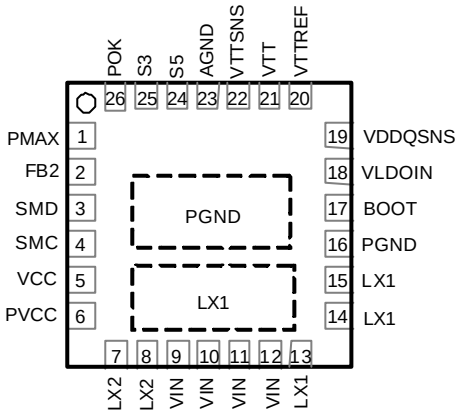
Package Code
QB : TQFN4x4-26
Operating Ambient Temperature Range
I : -40 to 85°C
Handling Code
TR : Tape & Reel
TY : Tray
Lead Free Code
L : Lead Free Device  Blank : Original Device

APW8871 QB :


XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

## Pin Configuration




**TQFN4x4-26 (Top View)**

= Thermal Pad (Include LX1 and PGND)

## Absolute Maximum Ratings (Note 1.2)

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| $V_{CC}$, $V_{PVCC}$ | VCC /PVCC Supply Voltage (VCC/PVCC to AGND) | -0.3 ~ 7 | V |
| $V_{IN}$ | VIN Supply Voltage (VIN to AGND) | -0.3 ~ 28 | V |
| $V_{BOOT}$ | BOOT Supply Voltage (BOOT to LX1) | -0.3 ~ 7 | V |
| $V_{BOOT-GND}$ | BOOT Supply Voltage (BOOT to GND) | -0.3 ~ 35 | V |
| $V_{LX1}$ | LX1 Voltage (LX1 to GND)<br><20ns pulse width<br>>20ns pulse width | <br>-5 ~ 35<br>-0.3 ~ 28 | V |
| $V_{LX2}$ | LX2 Voltage (LX2 to GND)<br><20ns pulse width<br>>20ns pulse width | <br>-5 ~ 9<br>-0.3 ~ 7 | V |
| | All Other Pins (FB2, S3, S5, VDDQSNS, SMD, SMC, POK, VLDOIN, VTTSNS, VTT, and VTTREF to AGND Voltage) | -0.3 ~ 7 | V |
| | PGND to AGND Voltage | -0.3 ~ 0.3 | V |
| $T_j$ | Maximum Junction Temperature | 150 | °C |
| $T_{STG}$ | Storage Temperature | -65 ~ 150 | °C |
| $T_{SDR}$ | Maximum Soldering Temperature, 10 Seconds | 260 | °C |

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Note 2: The device is ESD sensitive. Handling precautions are recommended.

## Thermal Characteristics (Note 3)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $\theta_{JA}$ | Thermal Resistance -Junction to Ambient | 40 | °C/W |
| $\theta_{JC}$ | Thermal Resistance -Junction to Case | 12 | |

Note3: $\theta_{JA}$ and $\theta_{JC}$ are measured with the component mounted on a high effective the thermal conductivity test board in free air. The exposed pad of package is soldered directly on the PCB.

## Recommended Operating Conditions

| Symbol | Parameter | Range | Unit |
|---|---|---|---|
| $V_{CC}$ | VCC Supply Voltage | 4.5 ~ 5.5 | V |
| $V_{IN}$ | Converter Input Voltage | 4.5 ~ 25 | V |
| $V_{PVCC}$ | PVCC Supply Voltage | 3 ~ 5.5 | V |
| $V_{VDDQ}$ | VDDQ Output Voltage | 1.0 ~ 1.7 | V |
| $V_{VPP}$ | VPP Output Voltage | 0.6 ~ 3.3 | V |
| $V_{VTT}$ | LDO Output Voltage | 0.5 ~ 0.9 | V |
| $I_{VPP}$ | VPP Output Current | 0 ~ 0.6 | A |
| $I_{VDDQ}$ | VDDQ Output Current | 0 ~ 8.5 | A |
| $I_{VTT}$ | LDO Output Current | -0.75 ~ +0.75 | A |
| $L_1$ | VDDQ Output Inductor | 0.5 ~ 4.7 | µH |

## Recommended Operating Conditions

| Symbol | Parameter | Range | Unit |
|---|---|---|---|
| $L_2$ | VPP Output Inductor | 2.2 ~ 4.7 | µH |
| $C_{VCC}$ | VCC Capacitance | 1~ | µF |
| $C_{VDDQ}$ | VDDQ Output Capacitance | 100~ | µF |
| $C_{VPP}$ | VPP Output Capacitance | 10 ~ | µF |
| $C_{VTT}$ | VTT Output Capacitance | 10 ~ | µF |
| $C_{VTTREF}$ | VTTREF Output Capacitance | 0.22 ~ 2.2 | µF |
| $T_A$ | Ambient Temperature | -40 ~ 85 | °C |
| $T_J$ | Junction Temperature | -40 ~ 125 | °C |

## Electrical Characteristics

Refer to the typical application circuits. These specifications apply over $V_{VCC}$=$V_{BOOT}$=5V, $V_{IN}$=19V and $T_A$= -40 ~ 85°C, unless otherwise specified. Typical values are at $T_A$=25°C.

| Symbol | Parameter | Test Conditions | APW8871 | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| **SUPPLY CURRENT** | | | | | | |
| $I_{VCC}$ | VCC Supply Current | $T_A$ = 25°C, $V_{S3}$ = $V_{S5}$ = 5V, no load | - | 270 | 320 | µA |
| $I_{VCCSTB}$ | VCC Standby Current | $T_A$ = 25°C, $V_{S3}$ = 0V, $V_{S5}$ = 5V, no load | - | 245 | 295 | µA |
| $I_{VCCSDN}$ | VCC Shutdown Current | $T_A$ =25°C, $V_{S3}$ = $V_{S5}$ = 0V, no load | - | 0.1 | 1 | µA |
| $I_{LDOIN}$ | LDOIN Supply Current | $T_A$ = 25°C, $V_{S3}$ = $V_{S5}$ = 5V, no load | 0.3 | 0.6 | 1 | mA |
| $I_{LDOINSTB}$ | LDOIN Standby Current | $T_A$ = 25°C, $V_{S3}$ = 0V, $V_{S5}$ = 5V, no load, | - | 0.1 | 1 | µA |
| $I_{LDOINSDN}$ | LDOIN Shutdown Current | $T_A$ = 25°C, $V_{S3}$ = $V_{S5}$ = 0V, no load | - | 0.1 | 1 | µA |
| **POWER-ON-RESET** | | | | | | |
| | VCC POR Threshold | VCC Rising | 4.1 | 4.3 | 4.45 | V |
| | VCC POR Hysteresis | | - | 100 | - | mV |
| **VTT OUTPUT** | | | | | | |
| $V_{VTT}$ | VTT Output Voltage | $V_{LDOIN}$ = $V_{VDDQ}$ = 1.2V | - | 0.6 | - | V |
| $V_{VTT}$ | VTT Output Tolerance | $V_{LDOIN}$ = $V_{VDDQ}$ = 1.2V, $V_{VDDQ}$/2 - $V_{VTT}$, $I_{VTT}$ = 0A | -20 | - | 20 | mV |
| | | $V_{LDOIN}$ = $V_{VDDQ}$ = 1.2V, $V_{VDDQ}$/2 - $V_{VTT}$, $I_{VTT}$ = ±0.75A | -30 | - | 30 | |
| $I_{LIM}$ | Current-Limit | Sourcing Current ($V_{LDOIN}$ =1.2V) | 0.8 | 1 | 1.3 | A |
| | | Sinking Current ($V_{LDOIN}$ =1.2V) | -0.8 | -1 | -1.3 | |
| $I_{VTTLK}$ | VTT Leakage Current | $V_{VTT}$ = 1.25V, $V_{S3}$ = 0V, $V_{S5}$ = 5V, $T_A$ = 25°C | -1.0 | - | 1.0 | µA |
| $I_{VTTSNSLK}$ | VTTSNS Leakage Current | $V_{VTT}$ = 1.25V, $T_A$ = 25°C | -1.00 | 0.01 | 1.00 | µA |
| $I_{VTTDIS}$ | VTT Discharge Current | $V_{VTT}$ = 0.5V, $V_{S3}$ = $V_{S5}$ = 0V, $T_A$ = 25°C | - | 5 | - | mA |

## Electrical Characteristics

Refer to the typical application circuits. These specifications apply over $V_{VCC}$=$V_{BOOT}$=5V, $V_{IN}$=19V and $T_A$= -40 ~ 85°C, unless otherwise specified. Typical values are at $T_A$=25°C.

| Symbol | Parameter | Test Conditions | APW8871 | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| **VTTREF OUTPUT** | | | | | | |
| $V_{VTTREF}$ | VTTREF Output Voltage | $V_{LDOIN}$ = $V_{VDDQ}$ = 1.2V, $V_{VDDQ}$/2 | - | 0.6 | - | V |
| | VTTREF Tolerance | -10mA < $I_{VTTREF}$ < 10mA, $V_{VDDQ}$/2 - $V_{VTTREF}$<br>$V_{LDOIN}$ = $V_{VDDQ}$ = 1.2V | -12 | - | +12 | mV |
| $I_{VTTREF}$ | VTTREF Source Current | $V_{VTTREF}$ = 0V | -10 | -20 | -40 | mA |
| $I_{VTTREF}$ | VTTREF Sink Current | $V_{VTTREF}$ = 1.2V | 10 | 20 | 40 | mA |
| $I_{VTTREFDIS}$ | VTTREF Discharge Current | $T_A$=25 °C, S3=S5=0V, VTTREF=0.5V | - | 2 | - | mA |
| **VDDQ OUTPUT** | | | | | | |
| $V_{VDDQ}$ | VDDQ Sense Voltage | VDDQ Initial Setting = 1.2V | - | 1.2 | - | V |
| | VDDQ Regulation Voltage Tolerance to SMBus Setting | $T_A$=25 °C | -3 | - | 3 | mV |
| $I_{VDDQ}$ | VDDQSNS Input Current | $V_{VDDQSNS}$=2V | -0.5 | - | 0.5 | uA |
| | VDDQSNS Discharge Current | $V_{S3}$ = $V_{S5}$ = 0V, $V_{VDDQ}$ = 0.5V, VDDQSNS to GND MOSFET turns on | - | 12 | 25 | mA |
| | LDOIN Discharge Current | $V_{S3}$ = $V_{S5}$ = 0V, $V_{VDDQSNS}$ = 0.5V, (Tracking) | - | 700 | - | mA |
| **VDDQ PWM CONTROLLERS** | | | | | | |
| $F_{SW}$ | Operating Frequency | $V_{CC}$=4.5V~5.5V | 720 | 800 | 880 | kHz |
| $T_{SS\_VDDQ}$ | Internal Soft Start Time | $V_{VPP}$ is High to $V_{VDDQ}$ Regulation | 0.3 | 0.4 | 0.5 | ms |
| $T_{OFF(MIN)}$ | Minimum off time | | 200 | 300 | 400 | ns |
| $T_{ON(MIN)}$ | Minimum on time | Over all temperature and $V_{CC}$ | 80 | 110 | 140 | ns |
| | Zero-Crossing Threshold | | -5 | 0.5 | 5 | mV |
| **VDDQ POWER MOSFET** | | | | | | |
| $R_{ON\_HS\_VDDQ}$ | High-Side N-MOSFET Resistance | | - | 20 | 30 | mΩ |
| $R_{ON\_LS\_VDDQ}$ | Low-Side N-MOSFET Resistance | | - | 10 | 15 | mΩ |
| **VDDQ PROTECTIONS** | | | | | | |
| $V_{OCL}$ | Current Limit Threshold | Sensing Valley Current | 11 | 12 | 13 | A |
| $V_{NOCL}$ | Negative Current Limit Threshold | | - | -5 | - | A |
| | VDDQ OVP Trip Threshold | $V_{VDDQ}$ Rising | 120 | 125 | 130 | % |
| | VDDQ OVP Debounce Delay | $V_{VDDQ}$ Rising, DV=10mV | - | 2 | - | µs |
| | VDDQ UVP Trip Threshold | $V_{VDDQ}$ Falling | 55 | 60 | 65 | % |
| | VDDQ UVP Debounce | | - | 2 | - | µs |
| | VDDQ UVP Enable Delay | From S5=H to POK goes high | - | 0.7 | - | ms |

## Electrical Characteristics

Refer to the typical application circuits. These specifications apply over $V_{VCC}$=$V_{BOOT}$=5V, $V_{IN}$=19V and $T_A$= -40 ~ 85°C, unless otherwise specified. Typical values are at $T_A$=25°C.

| Symbol | Parameter | Test Conditions | APW8871 | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| **VPP PWM CONTROLLER** | | | | | | |
| $V_{VREF\_PP}$ | VPP Reference Voltage | | - | 0.6 | - | V |
| $I_{FB2}$ | $V_{FB2}$ Input Current | $V_{FB2}$=2V | -50 | - | 50 | nA |
| | Reference Voltage Accuracy | Over All Temperature Range | -0.5 | - | 0.5 | % |
| | | Load and Line Regulation, $I_{VPP}$< 0.6A, 3V < PVCC< 5.5V | -0.5 | - | 0.5 | % |
| $F_{SW}$ | Operating Frequency | $V_{CC}$=4.5V~5.5V | 850 | 1000 | 1150 | kHz |
| $T_{SS\_VPP}$ | Internal Soft Start Time | S5 is High to $V_{VPP}$ Regulation | 0.1 | 0.2 | 0.3 | ms |
| $T_{OFF(MIN)}$ | Minimum off time | | 200 | 300 | 400 | ns |
| $T_{ON(MIN)}$ | Minimum on time | Over All Temperature and $V_{CC}$ | 80 | 110 | 140 | ns |
| | Zero-Crossing Threshold | | -5 | 0.5 | 5 | mV |
| | LX2 Discharge Resistance | $V_{S3}$ = $V_{S5}$ = 0V | - | - | 100 | Ω |
| **VPP POWER MOSFET** | | | | | | |
| $R_{ON\_HS\_PP}$ | High-Side P-MOSFET Resistance | | - | - | 220 | mΩ |
| $R_{ON\_LS\_PP}$ | Low-Side N-MOSFET Resistance | | - | - | 200 | mΩ |
| $T_D$ | Dead Time | Internal Design Spec. | 2 | 3 | 5 | ns |
| **VPP PROTECTIONS** | | | | | | |
| $V_{OCL}$ | Current Limit Threshold | Sensing Valley Current | 2.5 | 3 | 3.5 | A |
| $V_{NOCL}$ | Negative Current Limit Threshold | | - | -0.6 | - | A |
| | VPP OVP Trip Threshold | $V_{VPP}$ Rising | 120 | 125 | 130 | % |
| | VPP OVP Debounce Delay | $V_{VPP}$ Rising, DV=10mV | - | 2 | - | µs |
| | VPP UVP Trip Threshold | $V_{VPP}$ Falling | 55 | 60 | 65 | % |
| | VPP UVP Debounce | | - | 2 | - | µs |
| | VPP UVP Enable Delay | | - | 0.7 | - | ms |
| **POK** | | | | | | |
| $V_{POK}$ | POK Threshold | POK in from Lower (POK Goes High) | 87 | 90 | 93 | % |
| | | POK Out from Normal (POK Goes Low) | 120 | 125 | 130 | % |
| $I_{POK}$ | POK Leakage Current | $V_{POK}$=5V | - | 0.1 | 1.0 | µA |
| | POK Output Low Voltage | $V_{CC}$=5V, $I_{POK\_SINK}$=4mA | - | 0.5 | 1 | V |
| | POK Enable Delay Time | S5 High to POK High | - | 0.7 | - | ms |
| | POK Delay Time | Delay for POK Rise Up/ Fall Down | - | 20 | - | µs |
| **BOOTSTRAP DIODE** | | | | | | |
| $V_F$ | Forward Voltage | $V_{VCC}$ – $V_{BOOT}$=5V, $I_F$ = 10mA, $T_A$ = 25 °C | - | 0.15 | 0.25 | V |
| $I_F$ | Reverse Leakage | $V_{BOOT}$ = 30V, $V_{LX}$ = 25V, $V_{VCC}$=5V, $T_A$ = 25 °C | - | 0.2 | 0.5 | µA |

## Electrical Characteristics

Refer to the typical application circuits. These specifications apply over $V_{VCC}$=$V_{BOOT}$=5V, $V_{IN}$=19V and $T_A$= -40 ~ 85°C, unless otherwise specified. Typical values are at $T_A$=25°C.

| Symbol | Parameter | Test Conditions | APW8871 | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| **LOGIC THRESHOLD** | | | | | | |
| $V_{IH}$ | S3, S5 High Threshold Voltage | S3, S5 Rising | 1.6 | - | - | V |
| $V_{IL}$ | S3, S5 Low Threshold Voltage | S3, S5 Falling | - | - | 0.6 | V |
| $I_{ILEAK}$ | Logic Input Leakage Current | $V_{S3}$ = $V_{S5}$ = 5V, $T_A$ =25°C | -1 | - | 1 | µA |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{SD}$ | Thermal Shutdown Temperature | $T_J$ Rising | - | 150 | - | °C |
| | Thermal Shutdown Hysteresis | | - | 40 | - | °C |

Note4 : Guaranteed by design.

## SMBus Serial Control Port Operation

Timing characteristics for SMBus Interface signals over recommended operating conditions (unless otherwise noted)

| Symbol | Parameter | Test Conditions | APW8871 | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| | Input High Voltage Threshold | | 1.6 | - | - | V |
| | Input Low Voltage Threshold | | - | - | 0.9 | V |
| $f_{SMC}$ | Frequency, SMC | | 10 | - | 100 | kHz |
| $t_{HIGH}$ | Pulse Duration, SMC High | | 4 | - | 50 | µs |
| $t_{LOW}$ | Pulse Duration, SMC Low | | 4.7 | - | - | |
| $t_R$ | Rise Time, SMC and SMD | | - | - | 1 | µs |
| $t_F$ | Fall Time, SMC and SMD | VCC=4.5V to 5.5V | - | - | 300 | ns |
| $t_{SU\_DAT}$ | Data Setup Time | | 250 | - | - | ns |
| $t_{HD\_DAT}$ | Data Hold Time | | 300 | - | - | ns |
| $t_{BUF}$ | Bus Free Time Between Stop and Start Condition | | 4.7 | - | - | µs |
| $t_{SU\_STA}$ | Setup Time for Start Condition | | 4.7 | - | - | |
| $t_{HD\_STA}$ | Start Condition Hold Time after Which First Clock Pulse Is Generated | | 4 | - | - | |
| $t_{SU\_STO}$ | Setup Time for Stop Condition | | 4 | - | - | µs |
| $t_{TIMEOUT}$ | SMBus Bus Release Timeout | | 25 | - | 35 | ms |

## SMBus Serial Control Port Operation(cont.)

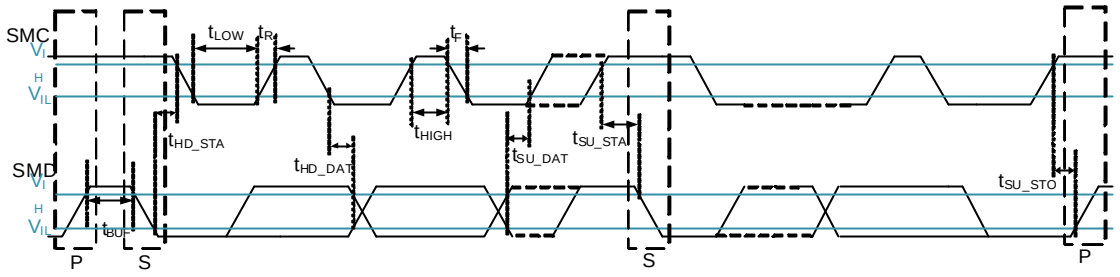


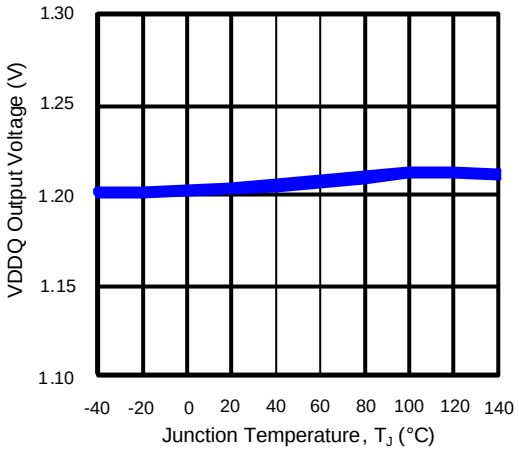

Figure1. SMC and SMD Timing

## Pin Description

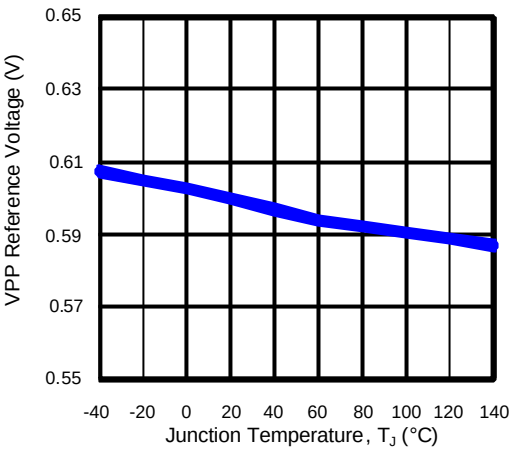
| NO. | NAME | FUNCTION |
|---|---|---|
| 1 | PMAX | Open drain indicator. When total power is larger than setting values, then this pin will assert to PCH or CPU. |
| 2 | FB2 | VPP PWM output voltage feedback pin. This pin is connected the resistor divider to set the desired output voltage. |
| 3 | SMD | Serial data. This pin must be connected to AGND if not used. |
| 4 | SMC | Serial clock. This pin must be connected to AGND if not used. |
| 5 | VCC | Filtered 5V power supply input for internal control circuitry. |
| 6 | PVCC | VPP Power input stage pin. This pin supply voltage for internal high side power MOSFET. |
| 7, 8 | LX2 | VPP Junction point of the high-side MOSFET Source, output filter inductor and the low-side MOSFET Drain for VPP PWM Converter. |
| 9 ~12 | VIN | VDDQ Power input stage pin. This pin supply voltage for internal high side power MOSFET. |
| 13~15 | LX1 | Junction point of the high-side MOSFET Source, output filter inductor and the low-side MOSFET Drain for VDDQ PWM Converter. |
| 16 | PGND | Power ground for internal low side power MOSFET source. |
| 17 | BOOT | Supply Input for the internal UGATE gate driver and an internal level-shift circuit. Connect to an external capacitor and diode to create a boosted voltage suitable to drive an internal logic-level N-channel MOSFET. |
| 18 | LDOIN | Supply voltage input for the VTT LDO. |
| 19 | VDDQSNS | Reference input for VTT and VTTREF. Power supply for the VTTREF. Discharge current sinking terminal for VDDQ discharge. Output voltage feedback input for VDDQ output if VDDQSET pin is connected to VCC or GND. |
| 20 | VTTREF | VTTREF buffered reference output. |
| 21 | VTT | Power output for the VTT LDO. |
| 22 | VTTSNS | Voltage sense input for the VTT LDO. Connect to plus terminal of the VTT LDO output capacitor. |
| 23 | AGND | Signal ground for PWM controller and VTT LDO. |
| 24 | S5 | S5 signal input. |
| 25 | S3 | S3 signal input. |
| 26 | POK | Power-okay output pin. POK is an open drain output used to Indicate the status of the output voltage. When VDDQ/VPP output voltage is within the target range, it is in high state. |

## Typical Operating Characteristics

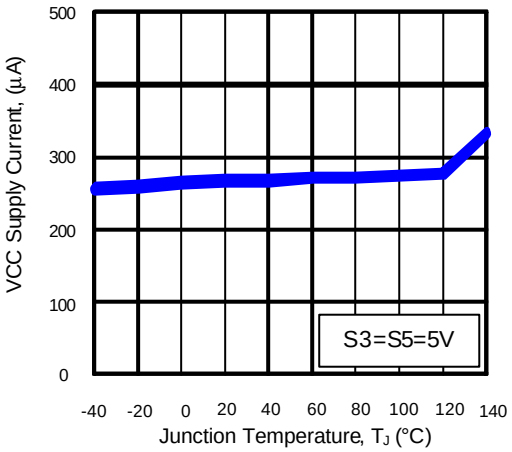
$I^2C$ Setting $V_{VDDQ}$=1.2V



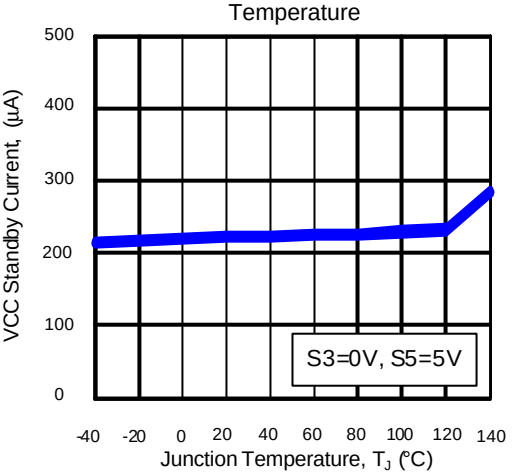

VPP Reference Voltage




Supply Current vs. Junction Temperature

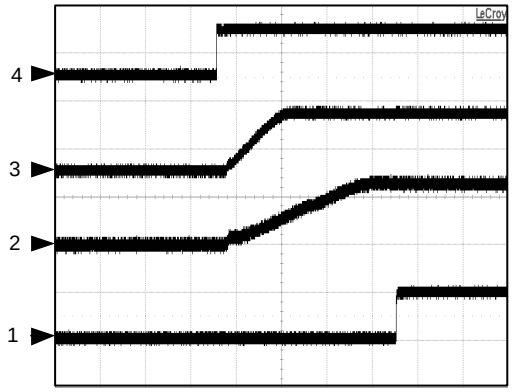



VCC Standby Current vs. Junction Temperature



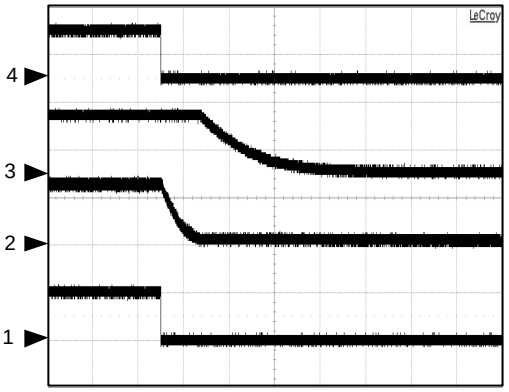
## Operating Waveforms

**S5=S3 Enable, No Load**



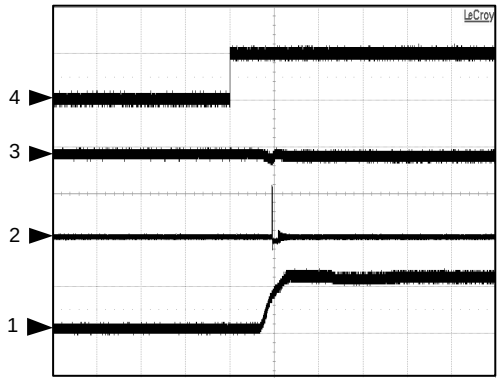

CH1: $V_{POK}$ (5V/div)
CH2: $V_{VDDQ}$ (1V/div)
CH3: $V_{VPP}$ (2V/div)
CH4: $V_{S5}$ (5V/div)
Time: 200µs/div

**S5=S3 Shutdown - No Load**



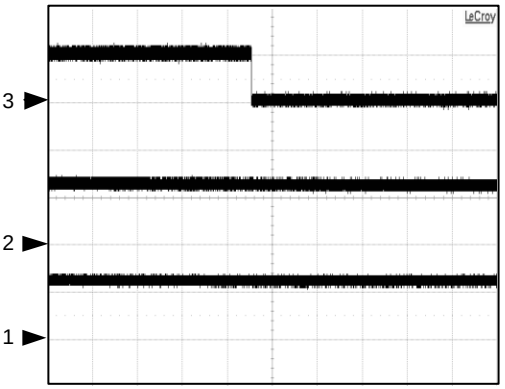

CH1: $V_{POK}$ (5V/div)
CH2: $V_{VDDQ}$ (1V/div)
CH3: $V_{VPP}$ (2V/div)
CH4: $V_{S5}$ (5V/div)
Time: 200µs/div

**S3 Enable**




CH1: $V_{VTT}$ (500mV/div)
CH2: $V_{LX1}$ (20V/div)
CH3: $V_{VDDQ}$ (1V/div)
CH4: $V_{S3}$ (5V/div)
Time: 20µs/div

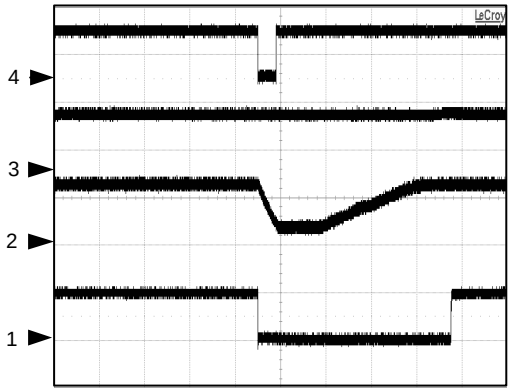
**S3 Shutdown ➔ HZ Mode**




CH1: $V_{VTT}$ (500mV/div)
CH2: $V_{VDDQ}$ (1V/div)
CH3: $V_{S3}$ (5V/div)
Time: 5ms/div

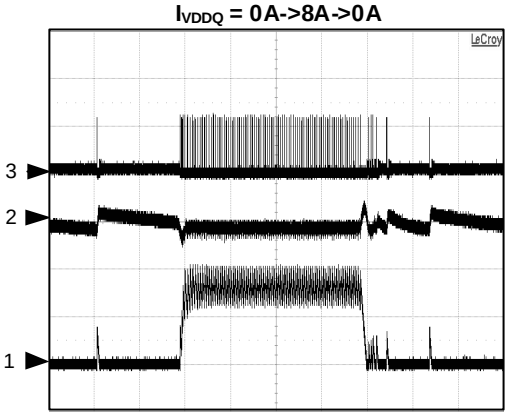
## Operating Waveforms

**S5 Shutdown-Enable, Non-Zero VDDQ**



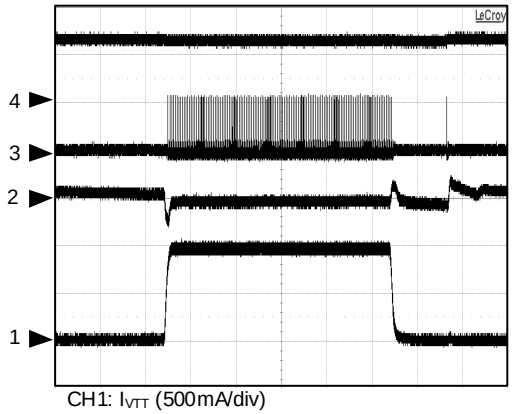

CH1: $V_{POK}$ (5V/div)
CH2: $V_{VDDQ}$ (1V/div)
CH3: $V_{VPP}$ (2V/div)
CH4: $V_{S5}$ (5V/div)
Time: 200µs/div

**VDDQ Load Transient,**
**$I_{VDDQ}$ = 0A->8A->0A**



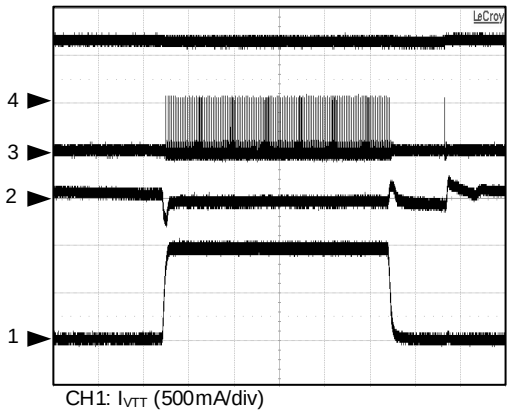

CH1: $I_{L1}$ (5A/div)
CH2: $V_{VDDQ}$ (AC,200mV/div)
CH3: $V_{LX1}$ (20V/div)
Time: 50µs/div

**VTT Source Load Transient,**
**$I_{VTT}$ = 0A->1A->0A**




CH1: $I_{VTT}$ (500mA/div)
CH2: $V_{VTT}$ (AC,100mV/div)
CH3: $V_{LX1}$ (20V/div)
CH4: $V_{VDDQ}$ (1V/div)
Time: 100µs/div

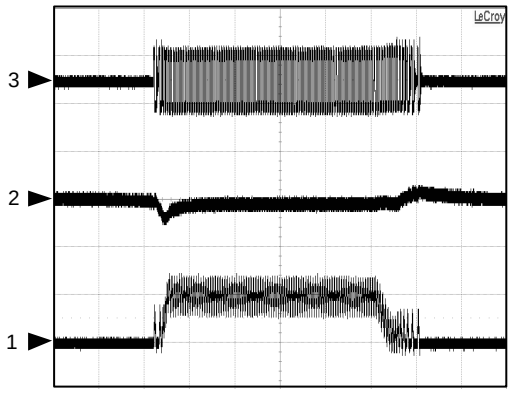
**VTT Source Load Transient,**
**$I_{VTT}$ = 0A->1A->0A**




CH1: $I_{VTT}$ (500mA/div)
CH2: $V_{VTT}$ (AC,100mV/div)
CH3: $V_{LX1}$ (20V/div)
CH4: $V_{VDDQ}$ (1V/div)
Time: 100µs/div

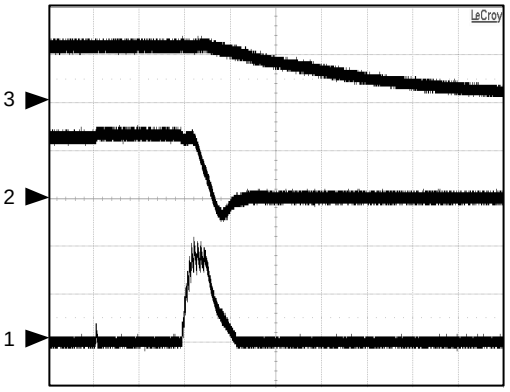
## Operating Waveforms

**VPP Load Transient,**
**$I_{VPP}$ = 0A->1A->0A**



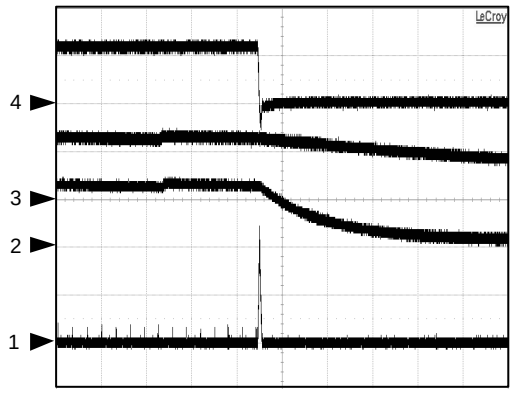

CH1: $I_{L2}$ (1A/div)
CH2: $V_{VPP}$ (AC,500mV/div)
CH3: $V_{LX2}$ (5V/div)
Time: 20µs/div

**Short Circuit Test to VDDQ Terminal**



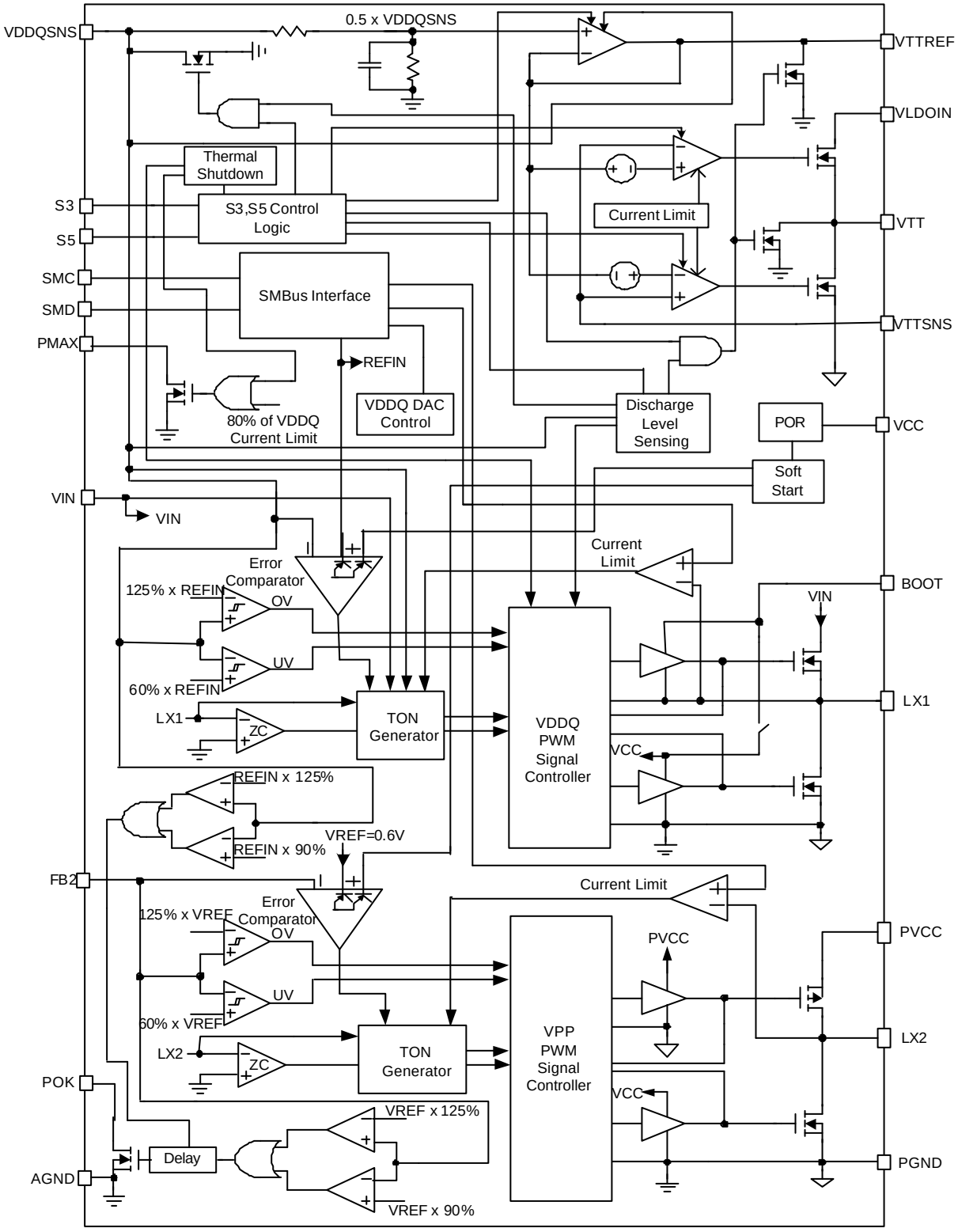

CH1: $I_{L1}$ (10Adiv)
CH2: $V_{VDDQ}$ (1V/div)
CH3: $V_{VPP}$ (2V/div)
Time: 50µs/div

**Short Circuit Test to VPP Terminal**

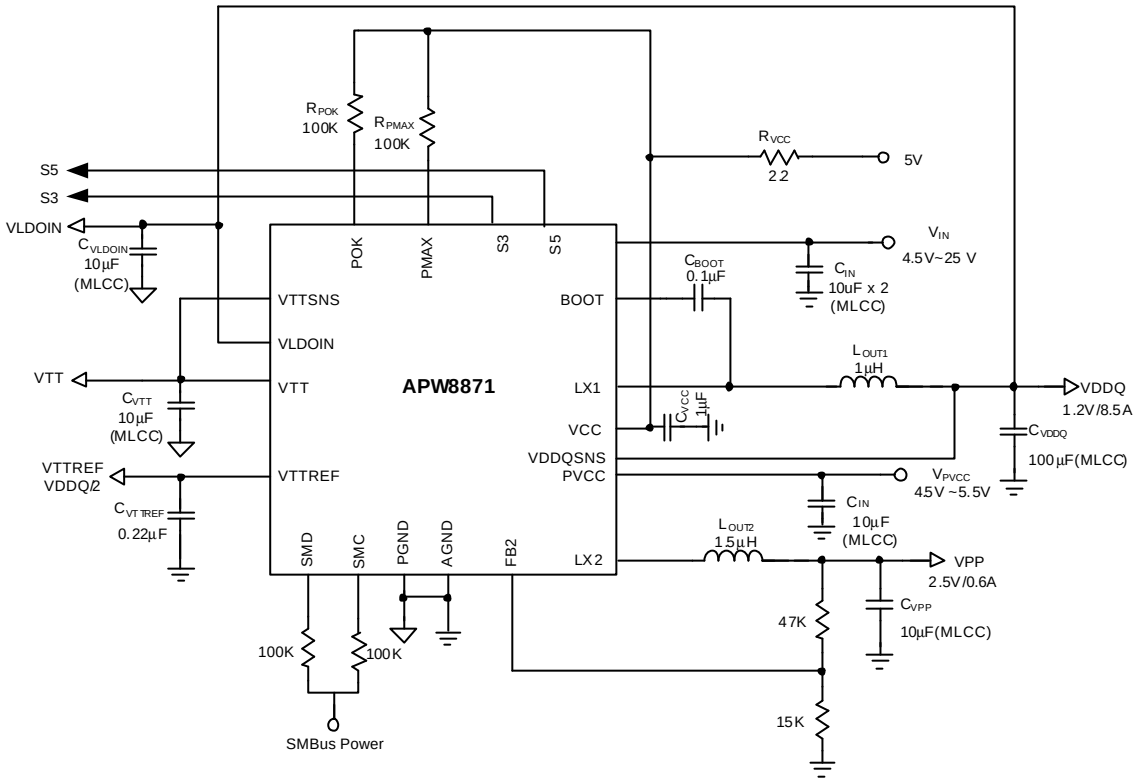



CH1: $I_{L2}$ (2A/div)
CH2: $V_{VTT}$ (500mV/div)
CH3: $V_{VDDQ}$ (1V/div)
CH4: $V_{VPP}$ (2V/div)
Time: 200µs/div

## Block Diagram



## Typical Application Circuit




DDR4 Total Power Solution Application Circuit

## Function Description

The APW8871 integrates two synchronous buck PWM controller and high/low side power MOSFETs to generate VPP and VDDQ, two sourcing and sinking LDO linear regulator to generate VTT and VTTREF. It provides a complete power supply for DDR4 memory system in 26-pin TQFN package. User defined output voltage is also possible and can be adjustable from 0.6V to 3.3V for VPP terminal and SMBus 2 bits programmable 1.0V/1.1V/1.2V/0V with maximum 500mV DAC dynamic adjustable. Input voltage range of the VDDQ PWM converter is 4.5V to 25V and for VPP PWM converter is 3V to 5.5V. The converter runs an adaptive on-time PWM operation at high-load condition and automatically reduces frequency to keep excellent efficiency down to several mA.

The VTT LDO can source and sink up to 0.75A peak current with only 10µF ceramic output capacitor. VTTREF tracks VDDQ/2 within 1% of VDDQ. VTT output tracks VTTREF within 20 mV at no load condition while 30 mV at full load. The LDO input can be separated from VDDQ and optionally connected to a lower voltage by using VLDOIN pin. This helps reducing power dissipation in sourcing phase. The APW8871 is fully compatible to JEDEC DDR4 specifications at S3/S5 sleep state (see Table 1). When VPP, VDDQ and VTT are disabled, the part has output tracking discharge function. The tracking discharge mode discharges VDDQ and VTT outputs through the internal LDO transistors and then VTT output tracks half of VDDQ voltage during discharge. When VDDQ voltage has been discharged to about 200mV, the internal discharge MOSFETs that are connected to VDDQ and VTT are turned on. The current capability of these discharge MOSFETs are limited and discharge occurs more slowly than the tracking discharge. Furthermore, the device discharges VPP Voltage by the internal resistor through LX2 to PGND.

### Constant-On-Time PWM Controller with Input Feed-Forward

The constant on-time control architecture is a pseudo-fixed frequency with input voltage feed-forward. This architecture relies on the output filter capacitor's effective series resistance (ESR) to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal.

In PFM operation, the high-side switch on-time controlled by the on-time generator is determined solely by a one-shot whose pulse width is inversely proportional to input voltage and directly proportional to output voltage. In PWM operation, the high-side switch on-time is determined by a switching frequency control circuit in the on-time generator block. The switching frequency control circuit senses the switching frequency of the high-side switch and keeps regulating it at a constant frequency in PWM mode. The design improves the frequency variation and be more outstanding than a conventional constant on-time controller which has large switching frequency variation over input voltage, output current and temperature. Both in PFM and PWM, the on-time generator, which senses input voltage on VIN and PVCC pins, provides very fast on-time response to input line transients.

Another one-shot sets a minimum off-time (typical: 300ns). The on-time one-shot is triggered if the error comparator is high, the low-side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

### Power-On-Reset

A Power-On-Reset (POR) function is designed to prevent wrong logic controls when the VCC voltage is low. The POR function continually monitors the bias supply voltage on the VCC pin if at least one of the enable pins is set high. When the rising VCC voltage reaches the rising POR voltage threshold (4.3V typical), the POR signal goes high and the chip initiates soft-start operations. There is almost no hysteresis to POR voltage threshold (about 100mV typical). When VCC voltage drop lower than 4.2V (typical), the POR disables the chip.

### Power Sequence and Soft- Start

The APW8871 conforms to JEDEC DDR4 sequence specification. VPP must ramp at the same time or earlier than VDDQ and VPP terminal voltage must equal to or higher than VDDQ at all time. APW8871 integrates digital soft-start circuits to ramp up the output voltage of the converter to the programmed regulation setpoint at a predictable slew rate. The slew rate of output voltage is internally controlled to limit the inrush current through the output capacitors during soft-start process.

## Function Description (Cont.)

**Power Sequence and Soft- Start (cont.)**

The figure 2 shows VPP/VDDQ soft-start sequence. When the S5 pin is pulled above the rising S5 threshold voltage, the device initiates a soft-start process to ramp up the output voltage. In normal operation, the VDDQ voltage starts to rise up after VPP voltage has been established. The VPP PWM converter soft-start interval is 0.2ms (max.); VDDQ PWM converter soft-start interval is 0.4ms (max.) and independent of the switching frequency.

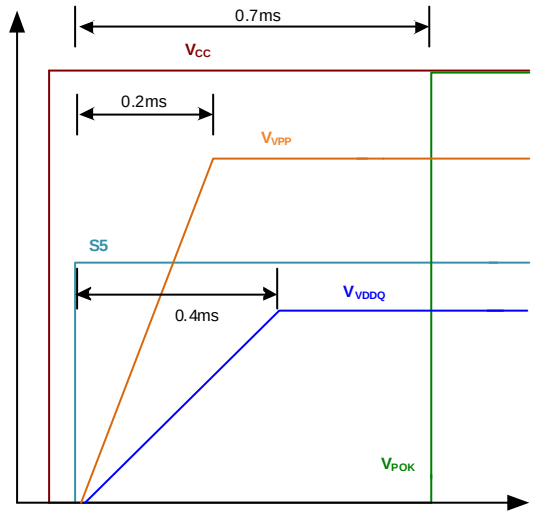



Figure 2. Soft-Start Sequence.

During soft-start stage before the POK pin is ready, the under voltage protection is prohibited. The over voltage and current limit protection functions are enabled. If the output capacitor has residue voltage before startup, both internal low-side and high-side MOSFETs are in off-state until the internal individual digital soft start voltage equal the $V_{VPP}$/$V_{VDDQ}$ voltages. This will ensure the output voltage starts from its existing voltage level.

The VTT LDO part monitors the output current, both sourcing and sinking current, and limits the maximum output current to prevent damages during current overload or short circuit (shorted from VTT to GND or VLDOIN) conditions.

The VTT LDO provides a soft-start function, using the constant current to charge the output capacitor that gives a rapid and linear output voltage rise. If the load current is above the current limit start-up, the VTT cannot start successfully.

APW8871 has an independent counter for each output, but the POK signal indicates only the status of VPP and VDDQ and does not indicate VTT power good externally.

**Power-Good Output (POK)**

POK is an open-drain output and the POK comparator continuously monitors the output voltage. POK is actively held low in shutdown, and standby. When both PWM converters' output voltages are greater than 90% of their target value, the internal open-drain device will be pulled low. After 20µs debounce time, the POK goes high. When one of the output voltages VPP/VDDQ outrun 125% of the target voltage, POK signal will be pulled low with 20ms debounce time.

**Under Voltage Protection**

In the process of operation, if a short-circuit occurs, the output voltage will drop quickly. When load current is bigger than current limit threshold value, the output voltage will fall out of the required regulation range. The undervoltage continually monitors the setting output voltage after both PWM operations to ensure startup. If a load step is strong enough to pull the output voltage lower than the under voltage threshold (60% of normal output voltage), the internal UVP delay counter begins counting. After 2µs debounce time, the device turns off both internal high-side and low-side MOSFETs with latched and starts a soft-stop process to shut down the output gradually. Toggling enable pin to low or recycling VCC will clear the latch and bring the chip back to operation.

**Over Voltage Protection (OVP)**

The feedback voltage should increase over 125% of the reference voltage due to the high-side MOSFET failure or for other reasons, and the over voltage protection comparator designed with a 2µs noise filter will turn on the internal low-side MOSFET. If the inductor current triggers negative current limit, the device turns off Low-side MOSFET for 300ns (typ.) and repeats the OVP function action.This action actively pulls down the output voltage. When the OVP occurs, the POK pin will pull down and latch-off the converter. This OVP scheme only clamps the voltage overshoot, and does not invert the output voltage when otherwise activated with a continuously high output from the internal low-side MOSFET driver. It' s a common problem for OVP schemes with a latch. Once an overvoltage fault condition is set, toggling VCC power-on-reset signal can only reset it.

## Function Description (Cont.)

**PWM Converter Current Limit**

The current-limit circuit employs a "valley" current-sensing algorithm (See Figure 3). The APW8871 uses the internal low-side MOSFET' s $R_{DS(ON)}$ of the synchronous rectifier as a current-sensing element. If the magnitude of the current-sense signal at LX1/LX2 pin is above the current limit threshold individual, the PWM is not allowed to initiate a new cycle. The actual peak current is greater than the current limit threshold by an amount equals to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are the functions of the sense resistance, inductor value, and input voltage.

The PWM controller uses the internal low-side MOSFETs on-resistance $R_{DS(ON)}$ to monitor the current for protection against shortened outputs.

When the inductor valley current $I_{VALLEY}$ is bigger than device setting $I_{CL}$, the current limit function is triggered and internal LGATE turns on until current limit event released. $I_{VALLEY}$ can be expressed as $I_{OUT}$ minus half of peak-to-peak inductor current.

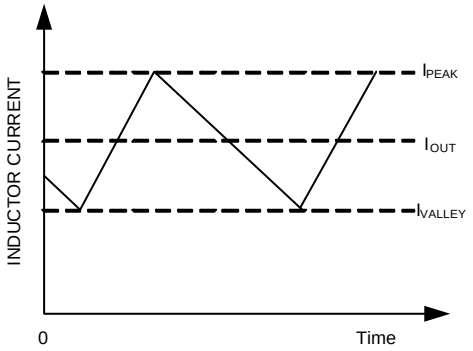



Figure 3. Current Limit Algorithm

**VTT Sink/Source Regulator**

The output voltage at VTT pin tracks the reference voltage applied at VTTREF pin. Two internal N-channel MOSFETs controlled by separate high bandwidth error amplifiers regulate the output voltage by sourcing current from VLDOIN pin or sinking current to GND pin. To prevent two pass transistors from shoot-through, a small voltage offset is created between the positive inputs of the two error amplifiers. The VTT with fast response feedback loop keeps tracking to the VTTREF within ±30 mV at all conditions including fast load transient.

**S3, S5 Control**

In the DDR4 memory application, it is important to keep VPP always higher than VDDQ and VDDQ always higher than VTT/VTTREF including both start-up and shutdown. The S3 and S5 signals control the VPP, VDDQ, VTT, VTTREF states and these pins should be connected to SLP_S3 and SLP_S5 signals respectively. The table1 shows the truth table of the S3 and S5 pins. When both S3 and S5 are above the logic threshold voltage, the VPP, VDDQ, VTT and VTTREF are turned on at S0 state. When S3 is low and S5 is high, the VPP, VDDQ and VTTREF are kept on while the VTT voltage is disabled and left high impedance in S3 state. When both S3 and S5 are low, the VDDQ, VTT and VTTREF are turned off and discharged to the ground according to the tracking discharge. When VDDQ voltage is lower than 200mV (typical), the discharge mode changes from tracking to non-tracking and at the same time, it sends a signal to enable VPP discharge during S4/S5 state.

Table1. The Truth Table of S3 and S5 pins

| STATE | S3 | S5 | VDDQ | VTTREF | VTT |
|---|---|---|---|---|---|
| S0 | H | H | 1 | 1 | 1 |
| S3 | L | H | 1 | 1 | 0 (high-Z) |
| S4/5 | L | L | 0 (discharge) | 0 (discharge) | 0 (discharge) |

**VPP, VDDQ and VTT Discharge Control**

APW8871 discharges VPP, VDDQ, VTTREF and VTT outputs during S3 and S5 are both low. First, when S3 and S5 are low, APW8871 discharges VDDQ output through the internal VTT regulator transistors and VTT output tracks half of VDDQ voltage during this tracking discharge. Note that VDDQ discharge current flows via

VLDOIN to VTTGND thus VLDOIN must be connected to VDDQ output. After VDDQ is discharged down to 0.2V, the internal LDO is turned off and the internal discharge MOSFETs that are connected to VDDQ and VTT are turned on. At the same time, APW8871 will send a signal to turn on VPP discharge device from LX2 to AGND. Therefore, in this design rule, VPP voltage could be always guaranteed bigger than VDDQ voltage.

## Function Description (Cont.)

**PMAX Indicator**

PMAX is an open-drain output and supports the PMAX signal for VDDQ PWM converter power indicator. If the inductor valley current is bigger than 80% of current limit threshold and counts four cycles continually, or the device temperature is over 120°C, the internal open-drain device will be turned on. The PMAX signal will go low to indicate that the PMAX condition has happened and passes message to the system. When inductor valley current is less than 80% of current limit threshold, or the device temperature is under 120°C, the PMAX signal will be pulled high immediately. Therefore, this indicator function is not latch up.

**Thermal Shutdown**

A thermal shutdown circuit limits the junction temperature of APW8871. When the junction temperature exceeds +150°C, both PWM converters, VTTLDO and VTTREF are shut off, allowing the device to cool down. The regulator regulates the output again through initiation of a new soft-start cycle after the junction temperature cools by 40°C, resulting in a pulsed output during continuous thermal overload conditions. The thermal shutdown designed with a 40°C hysteresis lowers the average junction temperature during continuous thermal overload conditions, extending life time of the device.
For normal operation, device power dissipation should be externally limited so that junction temperatures will not exceed +125°C.

The device slave address is defined as "00101010" (2AH) for APW8871.

| Register Address | Description | Read/Write | Power On Default Value |
|---|---|---|---|
| 01 | VDDQ Switching Frequency setting | Read/Write | 00h |
| 02 | VDDQ Initial Voltage setting | Read/Write | 02h |
| 03 | VDDQ DAC Voltage adjustable | Read/Write | 00h |
| 04 | VDDQ Voltage Slew Rate | Read/Write | 00h |

The below tables define the operation of each register bit. Default values are in **bold** text.

**REGISTER Address:01h**

| Bit | Name | Data | Read/Write | Description |
|---|---|---|---|---|
| [7:3] | Reserve | - | - | No Used |
| [2:0] | VDDQ FSW | **000** | **Read/Write** | **$V_{DDQ}$ $F_{SW}$ = 400KHz at PWM mode.** |
| | | 001 | Read/Write | $V_{DDQ}$ $F_{SW}$ = 600KHz at PWM mode. |
| | | 010 | Read/Write | $V_{DDQ}$ $F_{SW}$ = 800KHz at PWM mode. |
| | | 011 | Read/Write | $V_{DDQ}$ $F_{SW}$ = 1000KHz at PWM mode. |
| | | 100 | Read/Write | $V_{DDQ}$ $F_{SW}$ = 1200KHz at PWM mode. |
| | | 101 | Read/Write | $V_{DDQ}$ $F_{SW}$ = 1400KHz at PWM mode. |

**REGISTER Address:02h**

| Bit | Name | Data | Read/Write | Description |
|---|---|---|---|---|
| [7:2] | Reserve | - | - | No Used |
| [1:0] | VDDQ Initial Voltage | 00 | Read/Write | $V_{DDQ}$ Voltage = 1.0V. |
| | | 01 | Read/Write | $V_{DDQ}$ Voltage = 1.1V. |
| | | **10** | **Read/Write** | **$V_{DDQ}$ Voltage = 1.2V.** |
| | | 11 | Read/Write | $V_{DDQ}$ Voltage = 0V. |

**REGISTER Address:03h**

| Bit | Name | Data | Read/Write | Description |
|---|---|---|---|---|
| [7:6] | Reserved | - | - | No Used |
| [5:0] | VDDQ DAC | **000000** | **Read/Write** | **VDAC Voltage = 0mV** |
| | | 000001 | Read/Write | VDAC Voltage = 10mV |
| | | 000010 | Read/Write | VDAC Voltage = 20mV |
| | | 000011 | Read/Write | VDAC Voltage = 30mV |
| | | 000100 | Read/Write | VDAC Voltage = 40mV |
| | | 000101 | Read/Write | VDAC Voltage = 50mV |
| | | 000110 | Read/Write | VDAC Voltage = 60mV |
| | | 000111 | Read/Write | VDAC Voltage = 70mV |
| | | 001000 | Read/Write | VDAC Voltage = 80mV |
| | | 001001 | Read/Write | VDAC Voltage = 90mV |
| | | 001010 | Read/Write | VDAC Voltage = 100mV |
| | | 001011 | Read/Write | VDAC Voltage = 110mV |

**REGISTER Address:03h**

| Bit | Name | Data | Read/Write | Description |
|---|---|---|---|---|
| [5:0] | VDDQ DAC | 001100 | Read/Write | VDAC Voltage = 120mV |
| | | 001101 | Read/Write | VDAC Voltage = 130mV |
| | | 001110 | Read/Write | VDAC Voltage = 140mV |
| | | 001111 | Read/Write | VDAC Voltage = 150mV |
| | | 010000 | Read/Write | VDAC Voltage = 160mV |
| | | 010001 | Read/Write | VDAC Voltage = 170mV |
| | | 010010 | Read/Write | VDAC Voltage = 180mV |
| | | 010011 | Read/Write | VDAC Voltage = 190mV |
| | | 010100 | Read/Write | VDAC Voltage = 200mV |
| | | 010101 | Read/Write | VDAC Voltage = 210mV |
| | | 010110 | Read/Write | VDAC Voltage = 220mV |
| | | 010111 | Read/Write | VDAC Voltage = 230mV |
| | | 011000 | Read/Write | VDAC Voltage = 240mV |
| | | 011001 | Read/Write | VDAC Voltage = 250mV |
| | | 011010 | Read/Write | VDAC Voltage = 260mV |
| | | 011011 | Read/Write | VDAC Voltage = 270mV |
| | | 011100 | Read/Write | VDAC Voltage = 280mV |
| | | 011101 | Read/Write | VDAC Voltage = 290mV |
| | | 011110 | Read/Write | VDAC Voltage = 300mV |
| | | 011111 | Read/Write | VDAC Voltage = 310mV |
| | | 100000 | Read/Write | VDAC Voltage = 320mV |
| | | 100001 | Read/Write | VDAC Voltage = 330mV |
| | | 100010 | Read/Write | VDAC Voltage = 340mV |
| | | 100011 | Read/Write | VDAC Voltage = 350mV |
| | | 100100 | Read/Write | VDAC Voltage = 360mV |
| | | 100101 | Read/Write | VDAC Voltage = 370mV |
| | | 100110 | Read/Write | VDAC Voltage = 380mV |
| | | 100111 | Read/Write | VDAC Voltage = 390mV |
| | | 101000 | Read/Write | VDAC Voltage = 400mV |
| | | 101001 | Read/Write | VDAC Voltage = 410mV |
| | | 101010 | Read/Write | VDAC Voltage = 420mV |
| | | 101011 | Read/Write | VDAC Voltage = 430mV |
| | | 101100 | Read/Write | VDAC Voltage = 440mV |
| | | 101101 | Read/Write | VDAC Voltage = 450mV |
| | | 101110 | Read/Write | VDAC Voltage = 460mV |
| | | 101111 | Read/Write | VDAC Voltage = 470mV |
| | | 110000 | Read/Write | VDAC Voltage = 480mV |
| | | 110001 | Read/Write | VDAC Voltage = 490mV |
| | | 110010 | Read/Write | VDAC Voltage = 500mV |

**REGISTER Address:03h**

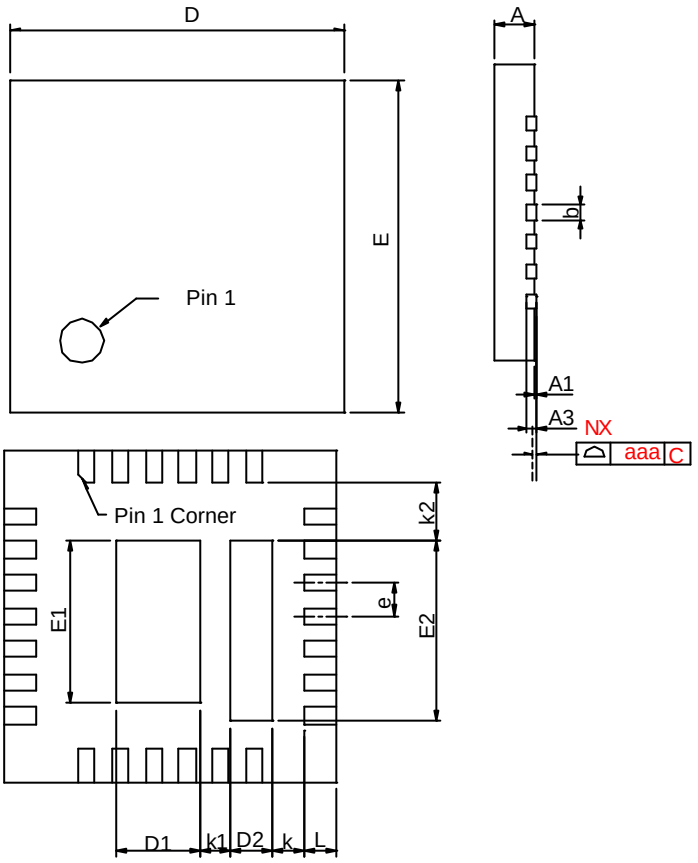
| Bit | Name | Data | Read/Write | Description |
|---|---|---|---|---|
| [5:0] | VDDQ DAC | 110011 | Read/Write | Reserved |
| | | 110100 | Read/Write | Reserved |
| | | 110101 | Read/Write | Reserved |
| | | 110110 | Read/Write | Reserved |
| | | 110111 | Read/Write | Reserved |
| | | 111000 | Read/Write | Reserved |
| | | 111001 | Read/Write | Reserved |
| | | 111010 | Read/Write | Reserved |
| | | 111011 | Read/Write | Reserved |
| | | 111100 | Read/Write | Reserved |
| | | 111101 | Read/Write | Reserved |
| | | 111110 | Read/Write | Reserved |
| | | 111111 | Read/Write | IC Shutdown |

**REGISTER Address:04h**

| Bit | Name | Data | Read/Write | Description |
|---|---|---|---|---|
| [7:2] | Reserve | - | - | No Used |
| [1:0] | VDDQ Slew Rate | **00** | **Read/Write** | **10mV/ms** |
| | | 01 | Read/Write | 15mV/µs |
| | | 10 | Read/Write | 20mV/µs |
| | | 11 | Read/Write | 25mV/µs |

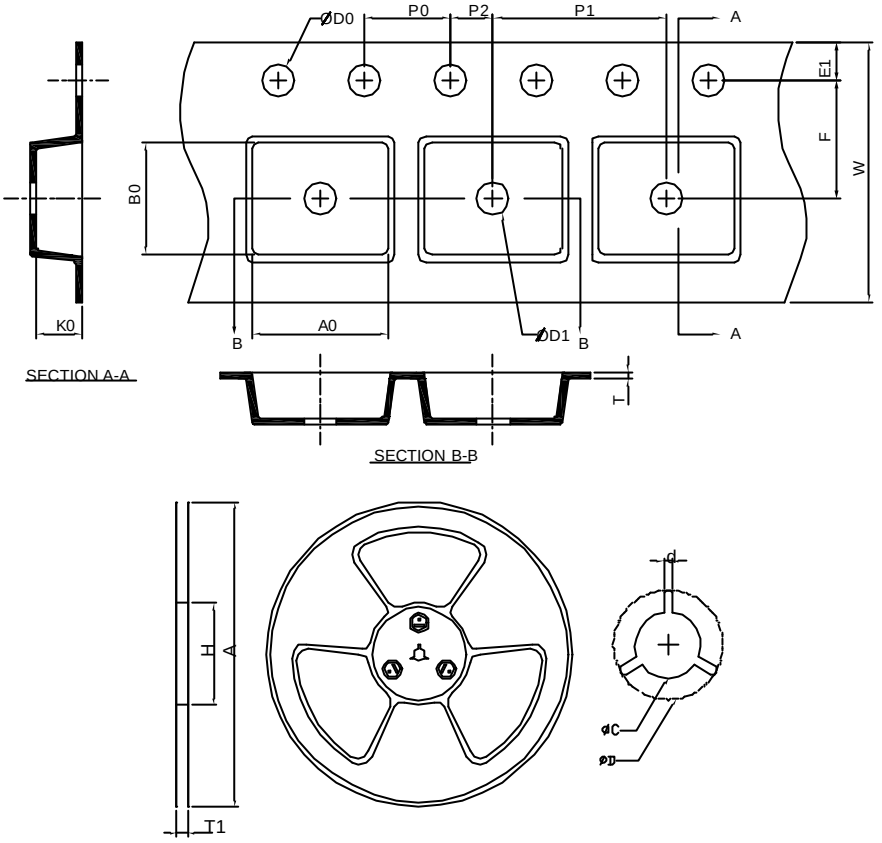
## Package Information

**TQFN4x4-26**




| SYMBOL | TQFN4x4-26 | | | |
|---|---|---|---|---|
| | MILLIMETERS | | INCHES | |
| | MIN. | MAX. | MIN. | MAX. |
| A | 0.70 | 0.80 | 0.028 | 0.031 |
| A1 | 0.00 | 0.05 | 0.000 | 0.002 |
| A3 | 0.11 REF | | 0.004 REF | |
| b | 0.15 | 0.25 | 0.006 | 0.010 |
| D | 3.90 | 4.10 | 0.154 | 0.161 |
| D1 | 0.90 | 1.10 | 0.035 | 0.043 |
| D2 | 0.40 | 0.60 | 0.016 | 0.024 |
| E | 3.90 | 4.10 | 0.154 | 0.161 |
| E1 | 1.85 | 2.05 | 0.073 | 0.081 |
| E2 | 2.07 | 2.27 | 0.081 | 0.089 |
| e | 0.40 BSC | | 0.016 BSC | |
| L | 0.35 | 0.45 | 0.014 | 0.018 |
| k | 0.327 | 0.427 | 0.013 | 0.017 |
| k1 | 0.317 | 0.417 | 0.012 | 0.016 |
| k2 | 0.66 | 0.76 | 0.026 | 0.030 |
| aaa | 0.08 | | 0.003 | |

## Carrier Tape & Reel Dimensions




| Application | A | H | T1 | C | d | D | W | E1 | F |
|---|---|---|---|---|---|---|---|---|---|
| TQFN4x4-26 | 330.0±2.00 | 50 MIN. | 12.4+2.00 -0.00 | 13.0+0.50 -0.20 | 1.5 MIN. | 20.2 MIN. | 12.0±0.30 | 1.75±0.10 | 5.5±0.05 |
| | **P0** | **P1** | **P2** | **D0** | **D1** | **T** | **A0** | **B0** | **K0** |
| | 4.0±0.10 | 8.0±0.10 | 2.0±0.05 | 1.5+0.10 -0.00 | 1.5 MIN. | 0.6+0.00 -0.40 | 4.30±0.20 | 4.30±0.20 | 1.30±0.20 |

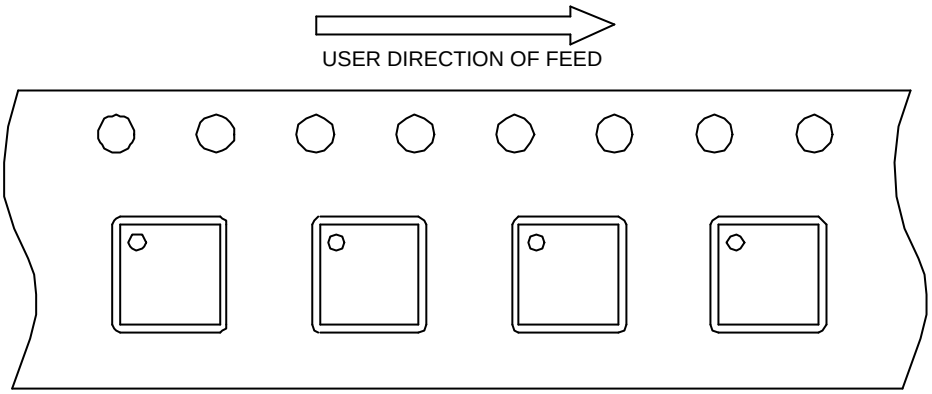
(mm)

## Devices Per Unit

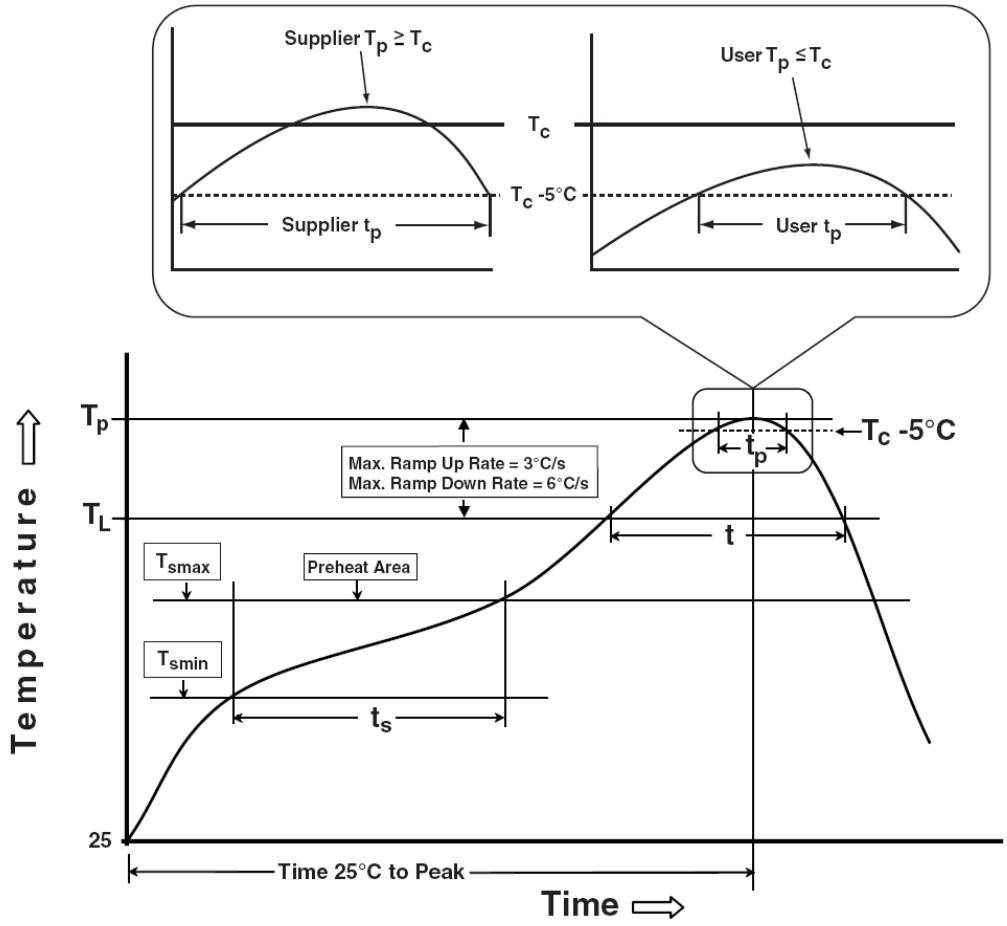
| Package Type | Unit | Quantity |
|---|---|---|
| **TQFN4x4-26** | Tape & Reel | 3000 |

## Taping Direction Information

**TQFN4x4-26**




## Classification Profile



## Classification Reflow Profiles

| Profile Feature | Sn-Pb Eutectic Assembly | Pb-Free Assembly |
|---|---|---|
| **Preheat & Soak**<br>Temperature min ($T_{smin}$)<br>Temperature max ($T_{smax}$)<br>Time ($T_{smin}$ to $T_{smax}$) ($t_s$) | 100 °C<br>150 °C<br>60-120 seconds | 150 °C<br>200 °C<br>60-120 seconds |
| Average ramp-up rate ($T_{smax}$ to $T_P$) | 3 °C/second max. | 3°C/second max. |
| Liquidous temperature ($T_L$)<br>Time at liquidous ($t_L$) | 183 °C<br>60-150 seconds | 217 °C<br>60-150 seconds |
| Peak package body Temperature ($T_p$)* | See Classification Temp in table 1 | See Classification Temp in table 2 |
| Time ($t_P$)** within 5°C of the specified classification temperature ($T_c$) | 20** seconds | 30** seconds |
| Average ramp-down rate ($T_p$ to $T_{smax}$) | 6 °C/second max. | 6 °C/second max. |
| Time 25°C to peak temperature | 6 minutes max. | 8 minutes max. |
| * Tolerance for peak profile Temperature ($T_p$) is defined as a supplier minimum and a user maximum.<br>** Tolerance for time at peak profile temperature ($t_p$) is defined as a supplier minimum and a user maximum. | | |

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

| Package Thickness | Volume $mm^3$ <350 | Volume $mm^3$ ³350 |
|---|---|---|
| <2.5 mm | 235 °C | 220 °C |
| ≥2.5 mm | 220 °C | 220 °C |

Table 2. Pb-free Process – Classification Temperatures (Tc)

| Package Thickness | Volume $mm^3$ <350 | Volume $mm^3$ 350-2000 | Volume $mm^3$ >2000 |
|---|---|---|---|
| <1.6 mm | 260 °C | 260 °C | 260 °C |
| 1.6 mm – 2.5 mm | 260 °C | 250 °C | 245 °C |
| ≥2.5 mm | 250 °C | 245 °C | 245 °C |

## Reliability Test Program

| Test item | Method | Description |
|---|---|---|
| SOLDERABILITY | JESD-22, B102 | 5 Sec, 245°C |
| HOLT | JESD-22, A108 | 1000 Hrs, Bias @ $T_J$=125°C |
| PCT | JESD-22, A102 | 168 Hrs, 100%RH, 2atm, 121°C |
| TCT | JESD-22, A104 | 500 Cycles, -65°C~150°C |
| HBM | MIL-STD-883-3015.7 | VHBM≧2KV |
| MM | JESD-22, A115 | VMM≧200V |
| Latch-Up | JESD 78 | 10ms, $1_{tr}$≧100mA |

## Customer Service

**Anpec Electronics Corp.**
Head Office :
No.6, Dusing 1st Road, SBIP,
Hsin-Chu, Taiwan, R.O.C.
Tel : 886-3-5642000
Fax : 886-3-5642050

Taipei Branch :
2F, No. 11, Lane 218, Sec 2 Jhongsing Rd.,
Sindian City, Taipei County 23146, Taiwan
Tel : 886-2-2910-3838
Fax : 886-2-2917-3838