

Three-Phase Full-wave Sine-wave Brushless Motor Driver

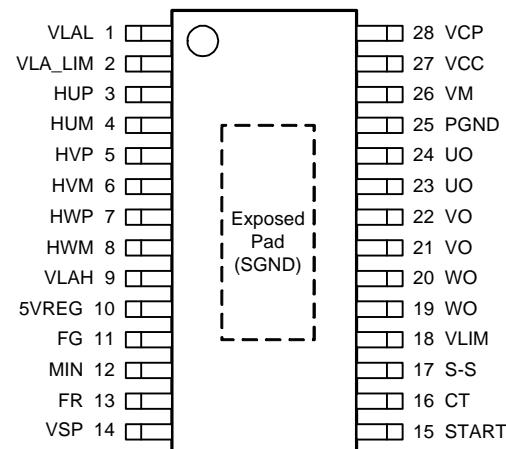
Features

- Three-Phase Full-Wave Sine-Wave Driver
- 1-Hall or 3-Hall Drive
- Wide Input Voltage: 6V to 30V
- VSP Pin Linear or Direct PWM input Speed Control
- Rotation Direction Selectable
- Built-in 5V LDO Regulator
- Built-in Charge Pump Circuit
- Built-in Current Limit Circuit
- Built-in Over Current Protection
- Built-in Lock Protection and Auto Restart Function
- Soft Start Function
- FG Output
- Built-in Thermal Shutdown Protection
- TSSOP-28P Package
- Lead Free and Green Device Available (RoHS Compliant)

General Description

The APX7320 is a three-phase full-wave sine-wave brushless motor drive by 1-hall or 3-hall (sensor or IC). This IC built-in linear or direct PWM input speed control, leading angle setting, current limit, over current protection and soft start features suitable for the three-phase brushless DC motors. The APX7320 is available in TSSOP-28P package (see Pin Configuration).

Pin Configuration

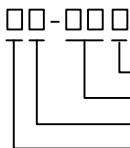


TSSOP-28P

 = Thermal Pad (SGND must connected to the GND plane for the IC circuit and better heat dissipation)

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information

APX7320  Assembly Material Handling Code Temperature Range Package Code	Package Code R: TSSOP - 28P Operating Ambient Temperature Range I : -40 to 90 °C Handling Code TR : Tape & Reel Assembly Material G: Halogen and Lead Free Device
APX7320 R : 	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note1)

Symbol	Parameter	Ratings	Unit
V _{CC}	VCC Pin Supply Voltage (VCC to SGND)	-0.3 to 34	V
V _M	VM Pin Supply Voltage (VM to PGND)	-0.3 to 34	V
V _{VCP}	VCP Pin Output Voltage (VCP to SGND)	-0.3 to V _{CC} +6V	V
I _{OUT}	UO, VO, WO Pin Maximum Output Peak Current	4.5	A
V _{UO, VO, WO}	UO, VO and WO Pins Output Voltage	V _{PGND} -0.3 to V _{CC}	V
V _{HUP, HUM}	HUP, HUM, HVP, HVM, HWP and HWM Pins Input Voltage	-0.3 to 6	V
V _{VLA (H, L, LIM)}	VLAH, VLAL and VLA_LIM Pins Input Voltage (to SGND)	-0.3 to 6	V
V _{VSP}	VSP Pin Input Voltage (VSP to SGND)	-0.3 to 6	V
V _{MIN}	MIN Pin Input Voltage (MIN to SGND)	-0.3 to 6	V
V _{FR}	FR Pin Input Voltage (FR to SGND)	-0.3 to 6	V
V _{VLIM}	VLIM Pin input Voltage (VLIM to SGND)	-0.3 to 6	V
I _{5VREG}	5VREG Pin Output Source Current	0 to -30	mA
V _{FG}	FG Pin Output Voltage	-0.3 to 34	V
I _{FG}	FG Pin Maximum Output Sink Current	10	mA
T _J	Maximum Junction Temperature	150	°C
T _{STG}	Storage Temperature	-65 to 150	°C
T _{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Thermal Resistance-Junction to Ambient ^(Note 3) TSSOP-28P	50	°C/W
θ_{JC}	Thermal Resistance-Junction to Case ^(Note 4) TSSOP-28P	20	°C/W
P_D	Power Dissipation, $T_A=25^\circ\text{C}$	2.5	W

Note 3: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of TSSOP-28P is soldered directly on the PCB.

Note 4: The case temperature is measured at the center on the top of the TSSOP-28P package.

Recommended Operation Conditions ^(Note3)

Symbol	Parameter	Range	Unit
V_{CC}	VCC Pin Supply Voltage Range	6 to 30	V
$V_{HP, HM (U, V, W)}$	HUP, HUM, HVP, HVM, HWP and HWM Pins Input Voltage	0 to V_{5VREG}	V
$V_{VLA (H, L, LIM)}$	VLAH, VLAL and VLA_LIM Pins Input Voltage	0 to V_{5VREG}	V
V_{VSP}	VSP Pin Input Voltage	0 to V_{5VREG}	V
V_{MIN}	MIN Pin Input Voltage	0 to V_{5VREG}	V
V_{VLIM}	VLIM Pin Input Voltage	0 to V_{5VREG}	V
V_{FR}	FR Pin Input Voltage Range	0 to V_{5VREG}	V
T_A	Ambient Temperature	-40 to 90	°C
T_J	Junction Temperature	-40 to 125	°C

Note 5: Refer to the typical application circuit.

Electrical Characteristics ($V_{CC} = 24\text{V}$, $T_A = 25^\circ\text{C}$, unless otherwise specified)

Symbol	Parameter	Test Conditions	APX7320			Unit
			Min	Typ	Max	
SUPPLY CURRENT						
V_{5VREG}	5VREG Pin Output Voltage	$I_{5VREG} = -25\text{mA}$	4.6	4.8	5.5	V
I_{cc}	Operating Current	Rotation Mode	5.5	7	8.5	mA
OUTPUT DRIVERS						
V_{OL}	Low-side Output Saturation Voltage	$V_{CC}=24\text{V}; I_{OUT}=1\text{A}$	-	0.12	0.18	V
V_{OH}	High-side Output Saturation Voltage	$V_{CC}=24\text{V}; I_{OUT}=1\text{A}$	-	0.12	0.18	V
V_{FG}	FG Pin Low Voltage	$I_{FG}=5\text{mA}$	-	0.2	0.3	V
I_{FGL}	FG Pin Off Leakage Current	$V_{FG}=24\text{V}$	-	0.1	1	μA
F_{OUT}	Output Switching Frequency		30	38	45	kHz

Electrical Characteristics ($V_{CC} = 24V$, $T_A = 25^\circ C$, unless otherwise specified)

Symbol	Parameter	Test Conditions	APX7320			Unit
			Min	Typ	Max	
HALL AMPLIFIER						
V_{ICM1}	HALL Common-mode Input Voltage 1	Hall element application	0.3	-	V_{5VREG} -2	V
V_{ICM2}	HALL Common-mode Input Voltage 2	Hall IC application	0	-	V_{5VREG}	V
V_{HYS}	HALL Input Hysteresis Voltage		± 1	± 7.5	± 15	mV
LOCK PROTECTION						
V_{CTH}	CT Pin High Level Voltage		2.7	3	3.3	V
V_{CTL}	CT Pin Low Level Voltage		0.9	1	1.1	V
I_{CT1}	CT Charge Current	$V_{CT}=0.5V$	1.5	2	2.5	μA
I_{CT2}	CT Discharge Current	$V_{CT}=3.5V$	0.3	0.4	0.5	μA
R_{CT}	CT Charge/Discharge Current Ratio		4	5	6	-
START UP OSCILLATOR						
V_{STARTH}	START Pin High Level Voltage		1.2	1.6	2	V
V_{STARTL}	START Pin Low Level Voltage		0.6	0.8	1	V
I_{START1}	START Pin Charge Current	$V_{START}=0V$	5.5	7	8.5	μA
I_{START2}	START Pin Discharge Current	$V_{START}=2V$	5.5	7	8.5	μA
SOFT START OSCILLATOR						
V_{S-SH}	S-S Pin High Level Voltage		1.2	1.6	2	V
V_{S-SL}	S-S Pin Low Level Voltage		0.6	0.8	1	V
I_{S-S1}	S-S Pin Charge Current	$V_{SS}=0V$	5.5	7	8.5	μA
I_{S-S2}	S-S Pin Discharge Current	$V_{SS}=2V$	5.5	7	8.5	μA
FR						
V_{FRH}	FR Pin High Level Voltage		2.5	-	V_{5VREG}	V
V_{FRL}	FR Pin Low Level Voltage		0	-	1	V
I_{FR}	FR Pin Bias Current	$V_{FR}=0V$	-	2.5	-	μA
VSP VOLTAGE MODE						
V_{SPH}	VSP Voltage of Maximum Output Duty		$5VREG^*$ 0.85	$5VREG^*$ 0.9	$5VREG^*$ 0.95	V
V_{SPL}	VSP Voltage of Minimum Output Duty		$5VREG^*$ 0.285	$5VREG^*$ 0.3	$5VREG^*$ 0.315	V
V_{SPSD}	VSP Voltage of Output Shut-down	$V_{MIN}>0V$, OUTPUT OFF	$5VREG^*$ 0.14	$5VREG^*$ 0.16	$5VREG^*$ 0.18	V
V_{SPPHYS}	V_{SPSD} Hysteresis		-	100	200	mV
VSP DIRECT PWM MODE (MIN=V_{5VREG})						
V_{PWMH}	VSP High Level Voltage for PWM Mode		2.5	-	5.5	V
V_{PWML}	VSP Low Level Voltage for PWM Mode		0	-	1	V
LEAD ANGLE						
T_{LAH1}	Lead Angle Correction	$V_{VLAH}=0V$	-	0	-	$^\circ$
T_{LAH2}	($VSP=V_{5VREG}, V_{VLA}=0V, V_{VLA_LIM}=$ floating)	$V_{VLAH}=1/2*V_{5VREG}$	26.5	30	33.5	$^\circ$
T_{LAH3}		$V_{VLAH}=V_{5VREG}$	54.5	58	61.5	$^\circ$

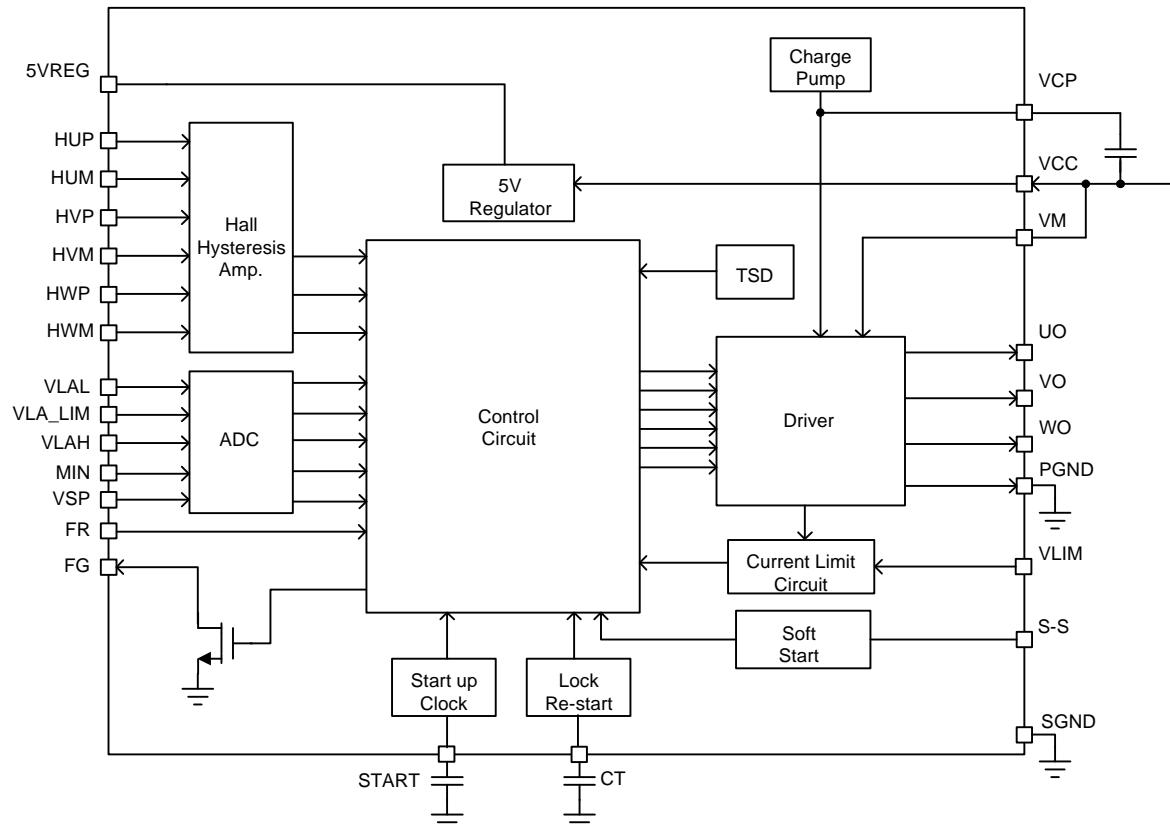
Electrical Characteristics ($V_{CC} = 24V$, $T_A = 25^\circ C$, unless otherwise specified)

Symbol	Parameter	Test Conditions	APX7320			Unit
			Min	Typ	Max	
CURRENT PROTECTION						
I_{LIM}	Current Limit Level	$V_{LIM} = 0V$ to $1V$	-	1	-	A
	Current Limit Level	$V_{LIM} = 3V$ to V_{5VREG}	-	3	-	A
I_{OCP}	Over Current Protection		-	4.5	-	A
THERMAL PROTECTION						
	Thermal Protection Temperature		-	165	-	$^\circ C$
	Thermal Protection Hysteresis		-	30	-	$^\circ C$

Pin Description

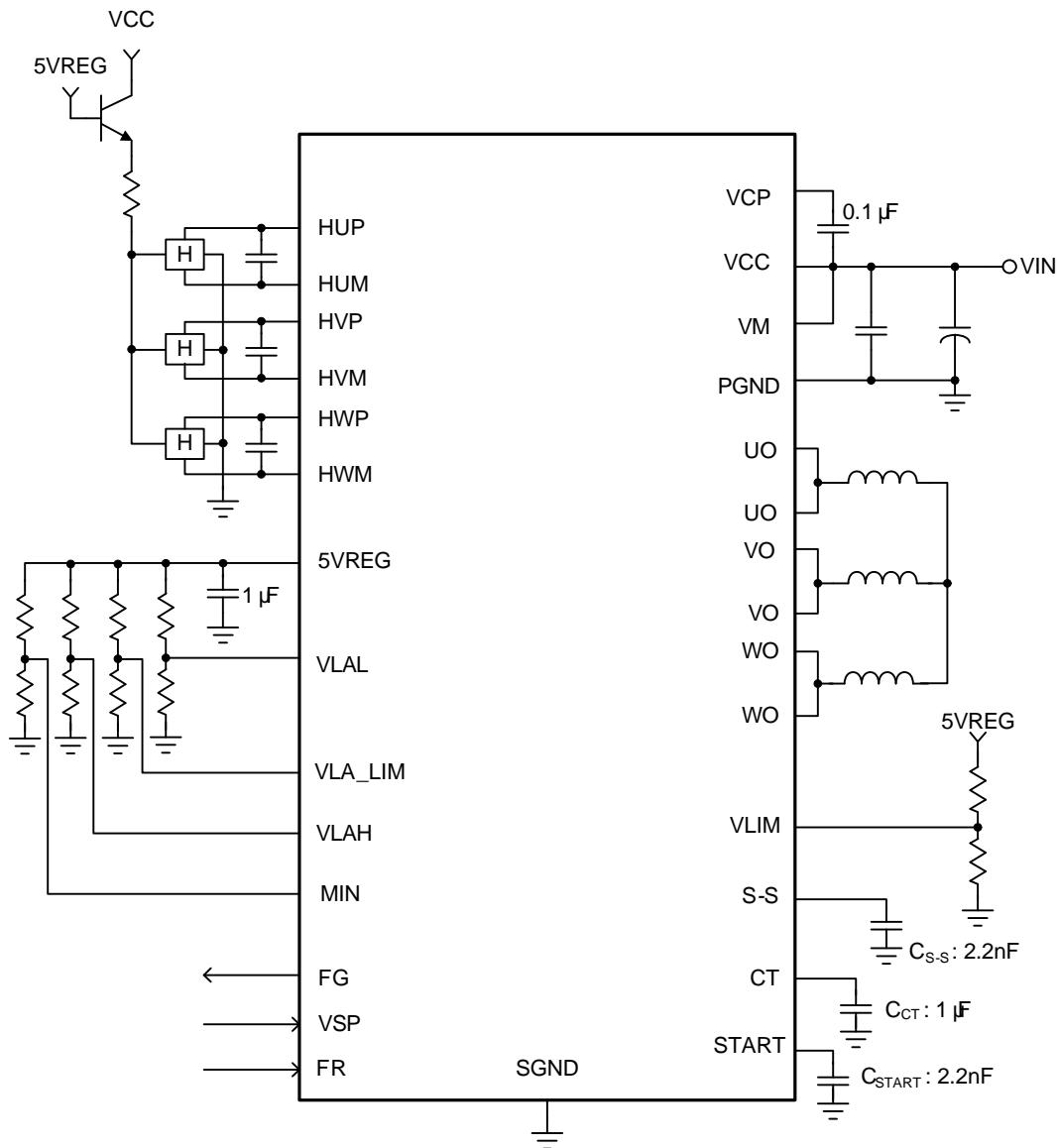
PIN		FUNCTION
NO.	NAME	
1	VLAL	Leading Angle Setting Input Pin. Low bound lead angle (LAL) setting at 0% output duty.
2	VLA_LIM	Leading Angle Setting Input Pin. Maximum lead angle (LAL_LIM) clamp setting.
3	HUP	Hall Input + of U-phase. Connect to hall element positive terminal or the output of hall IC.
4	HUM	Hall Input - of U-phase. Connect to hall element negative terminal.
5	HVP	Hall Input + of V-phase. Connect to hall element positive terminal or the output of hall IC.
6	HVM	Hall Input - of V-phase. Connect to hall element negative terminal or pull up to 5VREG for 1-Hall application.
7	HWP	Hall Input + of W-phase. Connect to hall element positive terminal or the output of hall IC.
8	HWM	Hall Input - of W-phase. Connect to hall element negative terminal or pull up to 5VREG for 1-Hall application.
9	VLAH	Leading Angle Setting Input Pin. High bound lead angle (LAH) setting at 100% output duty.
10	5VREG	5V Regulator Output. This is a 5V constant-voltage output for application circuit biases.
11	FG	Rotation Speed Output.
12	MIN	Minimum Speed Setting. VSP pin will be changed to direct PWM mode when MIN pin connect to 5VREG.
13	FR	Rotation Direction Control. Low Level Input (short to GND): U → V → W (Forward) High Level Input (short to 5VREG): U → W → V (Reverse)
14	VSP	Speed Control Input Pin. Linear voltage or direct PWM input.
15	START	Start-up Time Setting Input Pin. Connect a capacitor to SGND to set the start-up timing.
16	CT	Shutdown Time and Restart Time Setting. Connect a capacitor to SGND to set shutdown time and restart time in lock mode.
17	S-S	Soft-Start Time Setting. Connect a capacitor to SGND to set soft-start time to reduce the large current at power on and lock-restart mode.
18	VLIM	Current Limit Setting Input Pin.
19	WO	Driver Output Pin. Output signal for driving motor phase W. Pin19 and 20 must be short for maximum current rating.
20	WO	Driver Output Pin. Output signal for driving motor phase W. Pin19 and 20 must be short for maximum current rating.
21	VO	Driver Output Pin. Output signal for driving motor phase V. Pin21 and 22 must be short for maximum current rating.
22	VO	Driver Output Pin. Output signal for driving motor phase V. Pin21 and 22 must be short for maximum current rating.
23	UO	Driver Output Pin. Output signal for driving motor phase U. Pin23 and 24 must be short for maximum current rating.
24	UO	Driver Output Pin. Output signal for driving motor phase U. Pin23 and 24 must be short for maximum current rating.
25	PGND	Power Stage GND.
26	VM	Supply Voltage for Output Stage Input Pin.
27	VCC	Supply Voltage Input Pin.
28	VCP	Charge Pump Output. A capacitor must be connected to VCC.
Exposed Pad	SGND	Control Stage GND.

Block Diagram



Typical Application Circuit

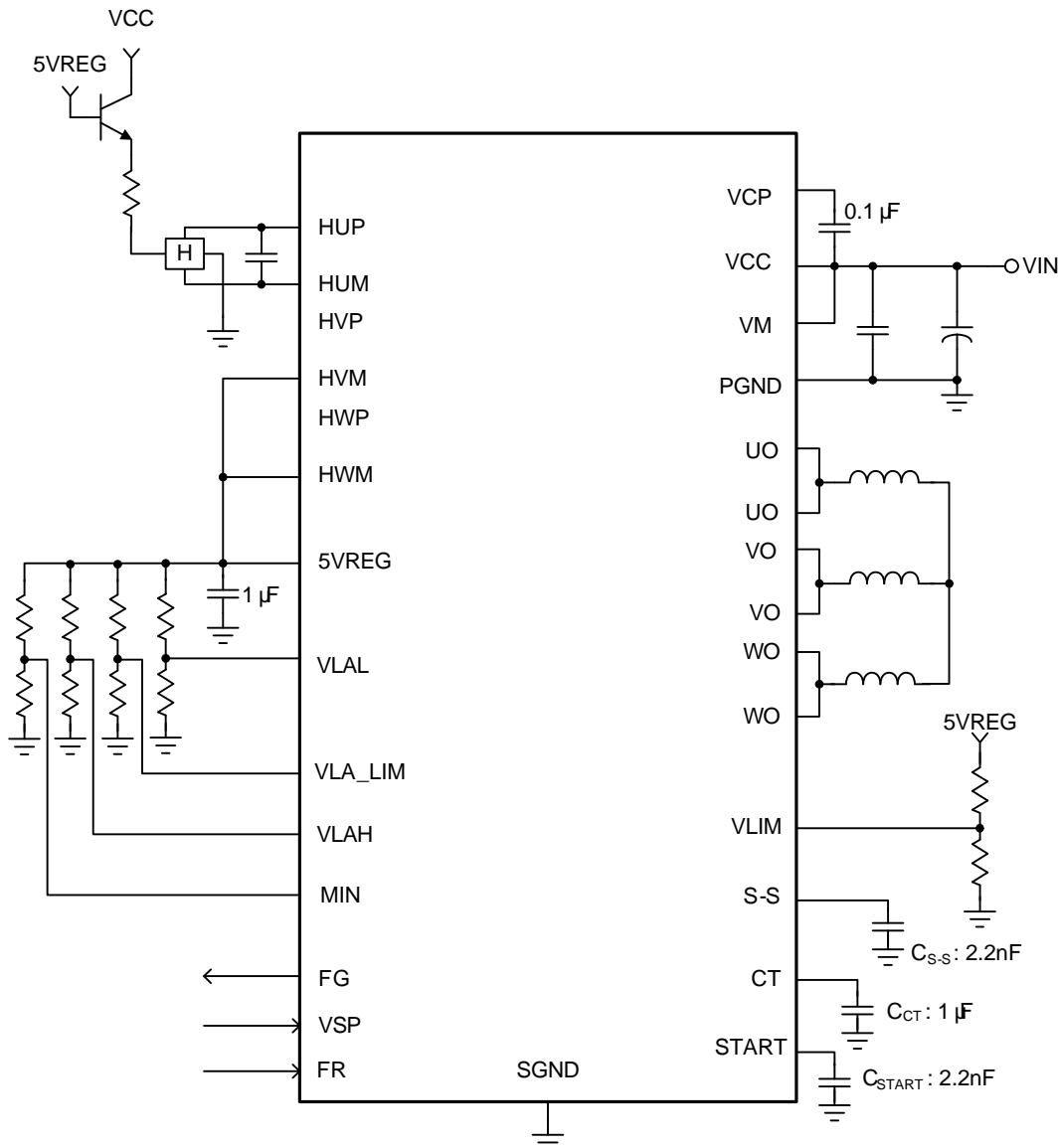
Circuit 1: 3-Hall Input Application



Note: The capacitance of C_{S-S} , C_{START} and C_{CT} can be fine tune for different parameter of motor.

Typical Application Circuit

Circuit 2: 1-Hall Input Application



Note: The capacitance of C_{S-S} , C_{START} and C_{CT} can be fine tune for different parameter of motor.

Function Description

VSP and MIN Output Duty Control

The APX7320 has two input pin VSP and MIN to control output duty of driver for the rotation speed of motor. The input of MIN pin is for the minimum output duty setting, and the VSP is for motor speed control.

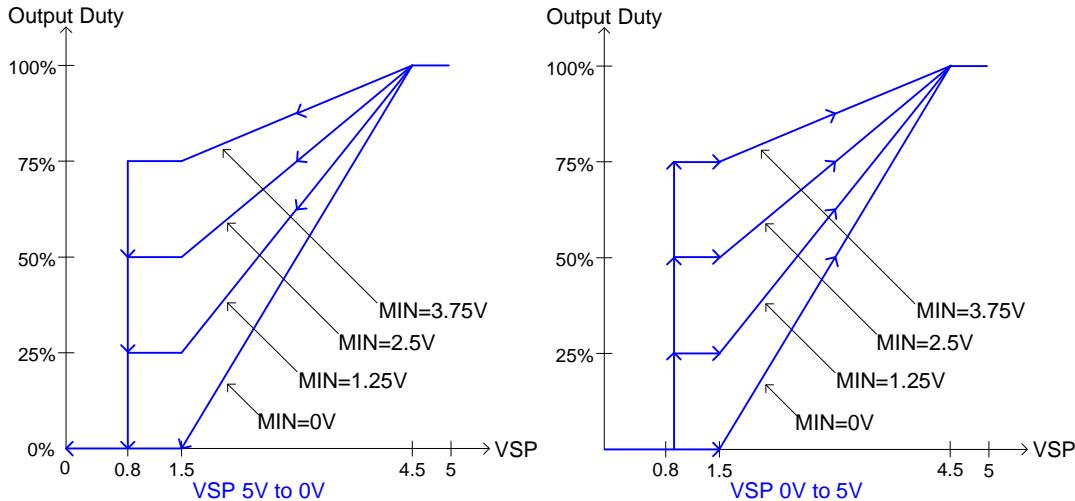


Figure1: Voltage Mode Output Duty Control

VSP Direct PWM Control

The APX7320 also support direct PWM input signal speed control. When the MIN pin pulled up to 5VREG, the VSP will be PWM input pin to control the output duty directly.

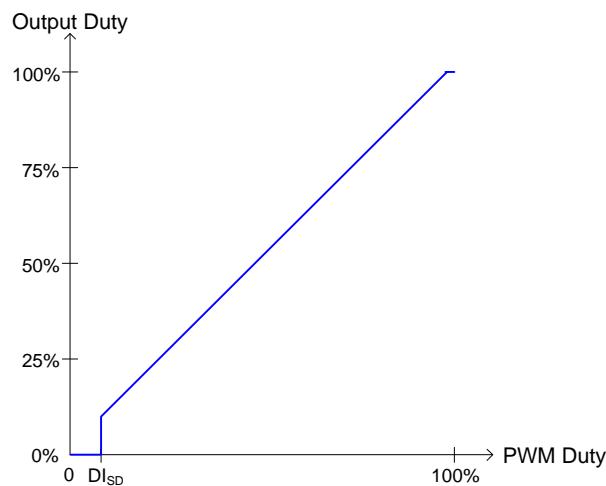


Figure2: Direct PWM Mode Output Duty Control

Function Description

Lead Angle Control

The APX7320 built in automatic lead angle controlled by the duty variation of output. The lead angle can be adjusted between 0°C to 58°C in 32 separate steps according to the input voltages of VLAH, VLAL and VLA_LIM pins, which work with 0V to V_{5VREG} . The lead angle control range is the minimum value LAL (set by VLAL) to the maximum value LAH (set by VLAH) for the output duty 0% to 100%. The VLA_LIM pin input voltage is used to clamp the maximum lead angle of driver operation.

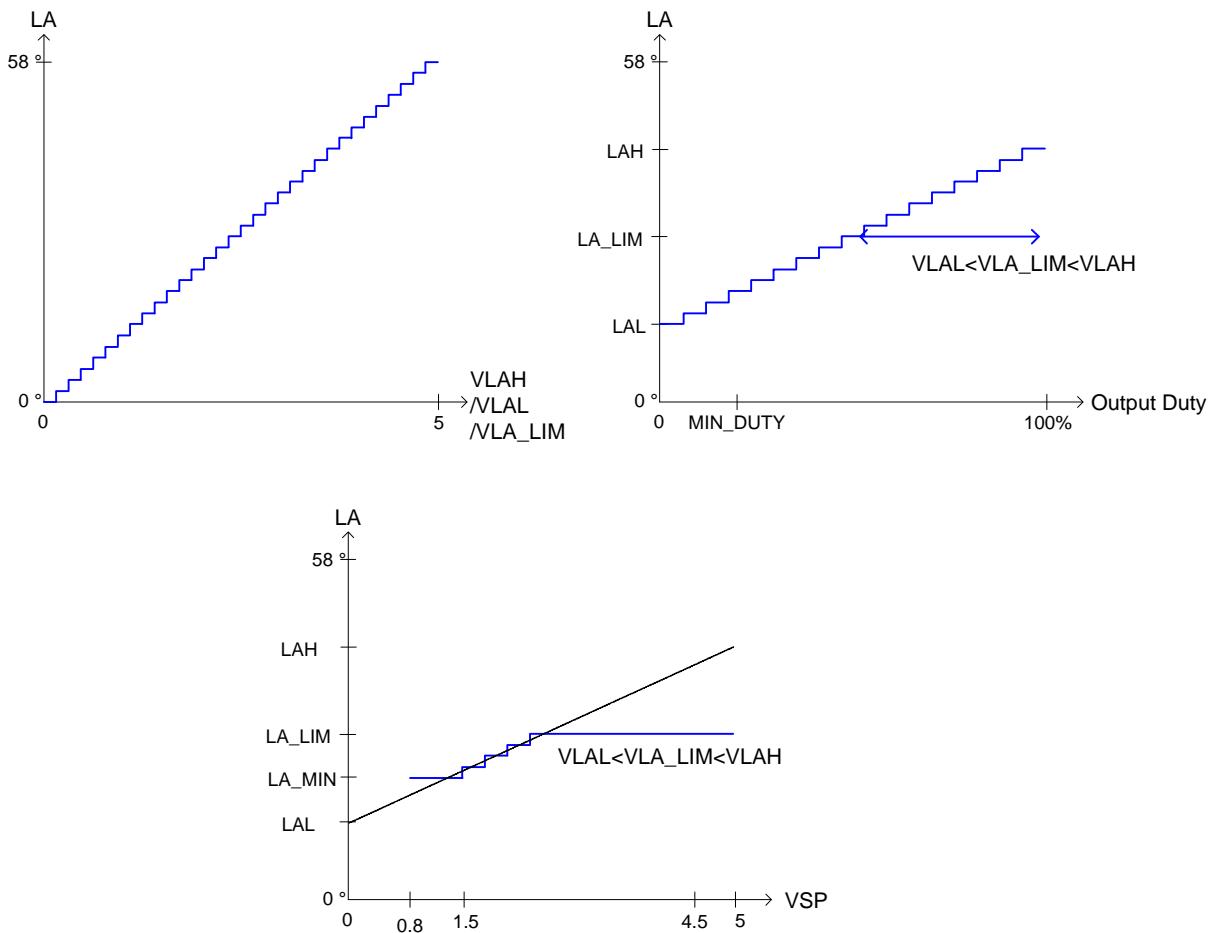


Figure3: Lead Angle Control

Function Description

Hall Element & Hall IC

The APX7320 hall signal input pin offers two types of Hall element and Hall IC application, the circuit design will be more flexible.

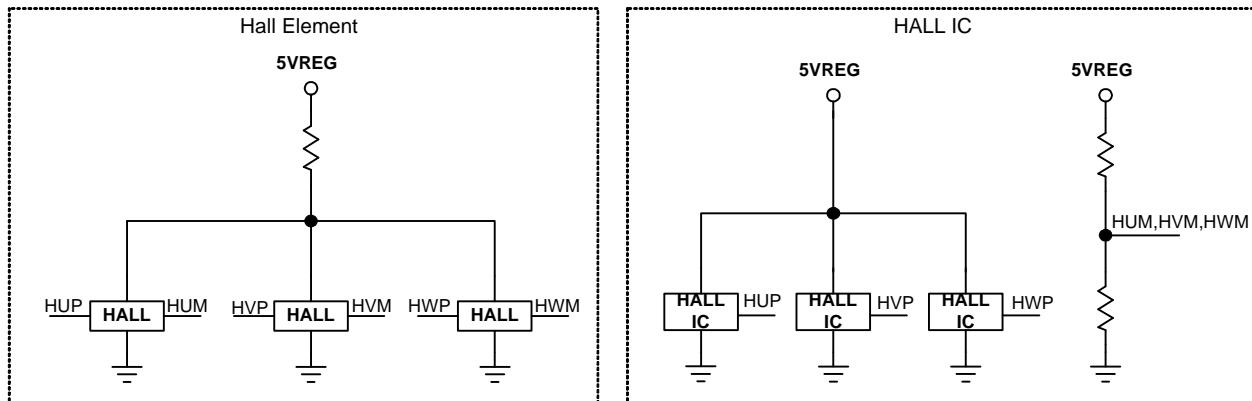


Figure 4: HALL Input Circuits

Function Description

Forward Rotation Timing Chard (FR=GND, VLAH=0V)

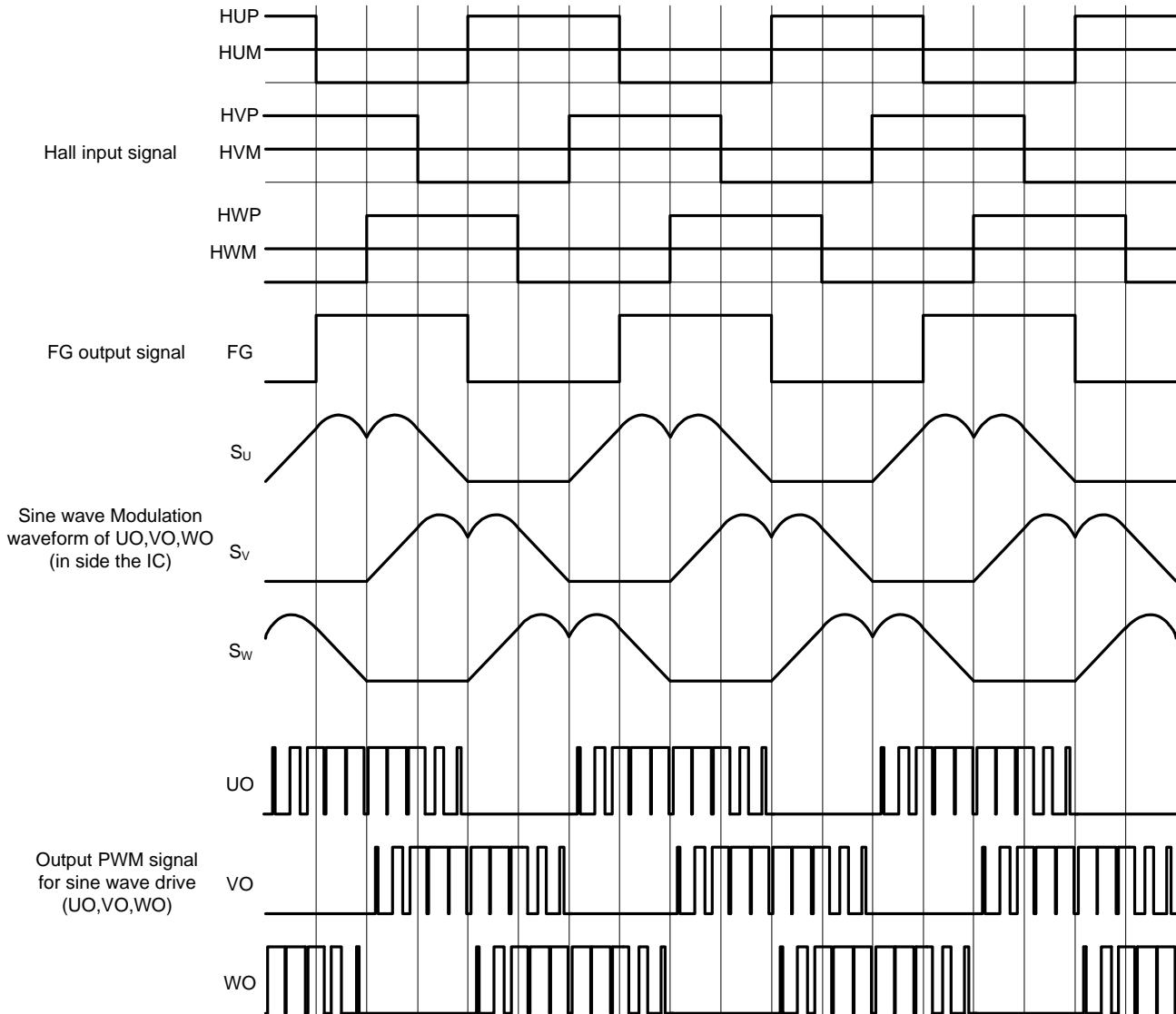


Figure 5: Forward Rotation Input and Output timing chards

Function Description

Reverse Rotation Timing Chard (FR=5VREG, VLAH=0V)

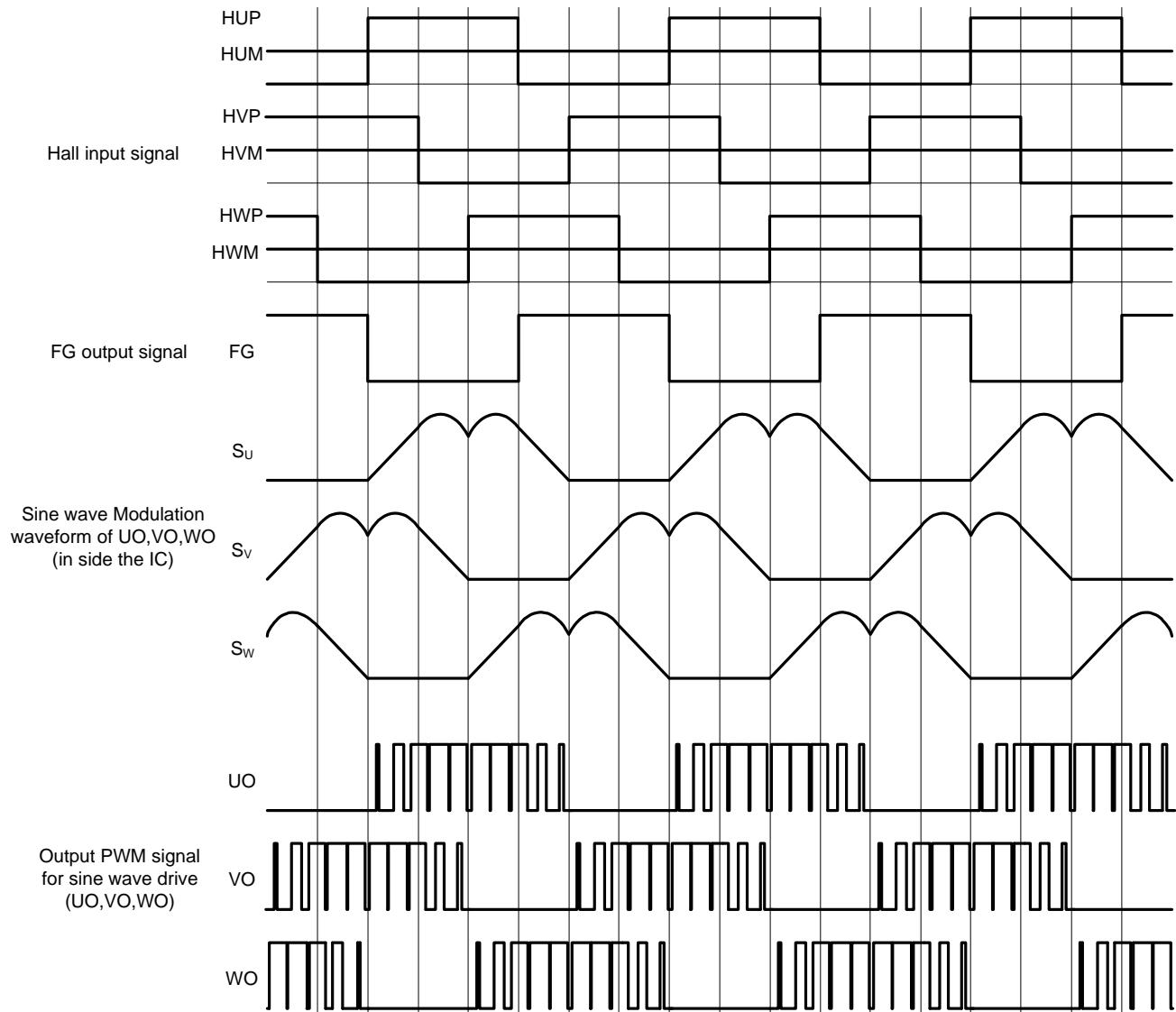


Figure 5: Reverse Rotation Input and Output timing chords

Function Description

Sine Wave Modulation

This is a soft switch PWM output to make the phase current smoother, which can reduce the noise of motor in switch interval. Using PWM duty control to simulate the idea sine wave output current.

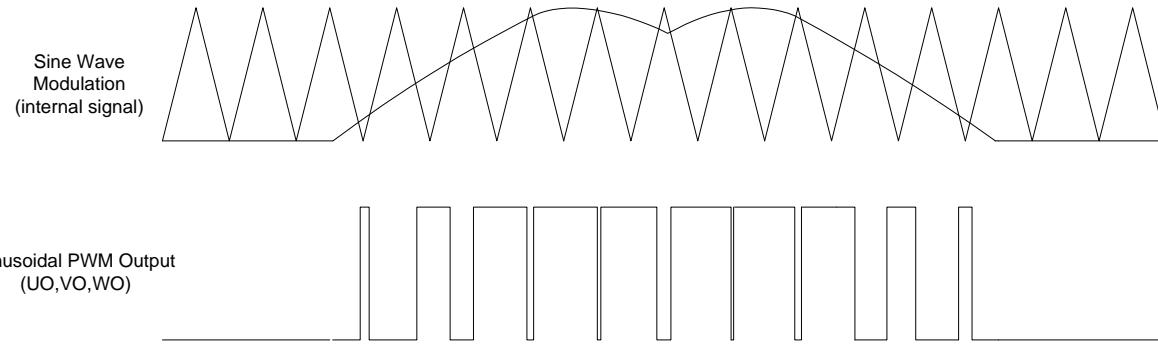


Figure 6: Sine Wave Modulation PWM Output

Lockup Protection and Automatic Restart

The APX7320 provides the lockup protection and automatic restart functions for preventing the coil burnout while the fan motor is locked. When the lock-restart cycle repeated to 20 times, the output will be shut down until pull low VSP pin or re-power on. Connecting the capacitor from CT pin to SGND can determine the shut down time and restart time.

Current Limit and Over Current Protection (OCP)

The APX7320 includes an internal current sense circuits for current limit and over-current protection (OCP). When the total current of three phase over the current limit level, the high side driver will be turned off to stop supplying current to the motor. If the total output current over the OCP current level, the OCP function will be enable to turn-off all of the high side output driver to prevent output short through condition until pull low VSP pin or re-power on.

Thermal Protection

The APX7320 is designed with a thermal protection to protect the IC from the damage of over temperature. When internal junction temperature reaches 165°C, the output devices will be switched off. When the IC's junction temperature cools by 30°C, the thermal sensor will turn the output devices on again resulting in a pulsed output during continuous thermal overload.

Application Information

Input Capacitor

For the noise reduction purpose, all of the capacitors in application circuit should be placed as close as possible to the IC pin.

CT Capacitor

The capacitor that is connected from CT pin to GND determines the shutdown time and restart time.

$$\text{Locked Detection Time} = \frac{C_{CT} \times (V_{CTH} - 0.2V)}{I_{CT1}}$$

$$\text{Restart Time} = \frac{C_{CT} \times (V_{CTH} - V_{CTL})}{I_{CT1}}$$

$$\text{Shutdown Time} = \frac{C_{CT} \times (V_{CTH} - V_{CTL})}{I_{CT2}}$$

For example:

$$V_{CC}=24V, C_{CT}=1\mu F$$

$$V_{CTL}=1V, V_{CTH}=3V, I_{CT1}=2\mu A, I_{CT2}=0.4\mu A$$

$$\text{Locked Detection Time} = 1.4s$$

$$\text{Restart Time} = 1s$$

$$\text{Shutdown Time} = 5s$$

The value of C_{CT} must be considered with soft start up result.

START Capacitor

The START pin capacitor is used to set the force start up timing (T_{START}) of one step (60°C) for sine-wave start up. Adjust START capacitor can set the start up timing for different motor or loading of fan motor.

$$T_{START} = \frac{2 \times (V_{STARTH} - V_{STARTL}) \times C_{START}}{I_{START}} \times 32 \times 32$$

For example:

$$C_{START} = 2.2nF$$

$$V_{STARTL}=0.8V, V_{STARTH}=1.6V, I_{START}=7\mu A$$

The force start up time is 515ms

Application Information

S-S Capacitor

The S-S capacitor is used to set the output duty change rate for soft start. The time (T_{S-S}) is define the time of output duty from 0% to 100%.

$$T_{S-S} = \frac{2 \times (V_{S-SH} - V_{S-SL}) \times C_{S-S}}{I_{S-S}} \times 32 \times 256$$

For example:

$$C_{S-S} = 2.2\text{nF}$$

$$V_{S-SL} = 0.8\text{V}, V_{S-SH} = 1.6\text{V}, I_{S-S} = 7\mu\text{A}$$

The time (TS-S) of duty change from 0% to 100% is 4.12s

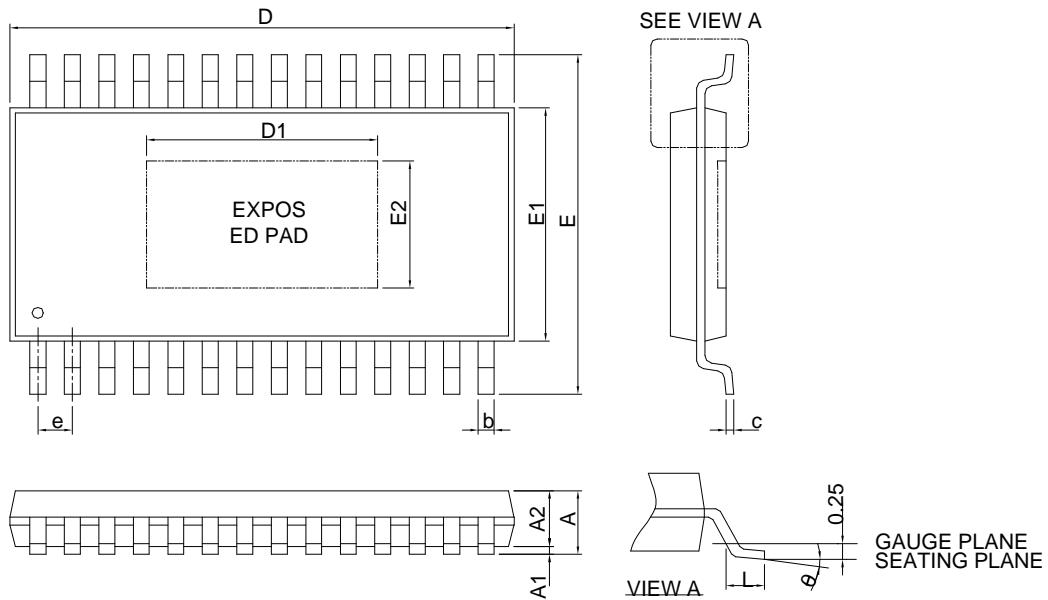
The choices of CT pin and S-S pin capacitors should be considered that fan must start up during restart time at lock mode. When the C_{CT} is determined and the fan can't start up at power-on or lock-restart mode, decrease the C_{S-S} capacitance can let the fan start up successfully but it will reduce the soft start time.

FIL Capacitor

The capacitor connects between HUP and HUM (HVP and HVM, HWP and HWM) pin to filter the noise when phase change to make sure phase change correctly. Its capacitance from 1nF to 10nF is recommended.

Package Information

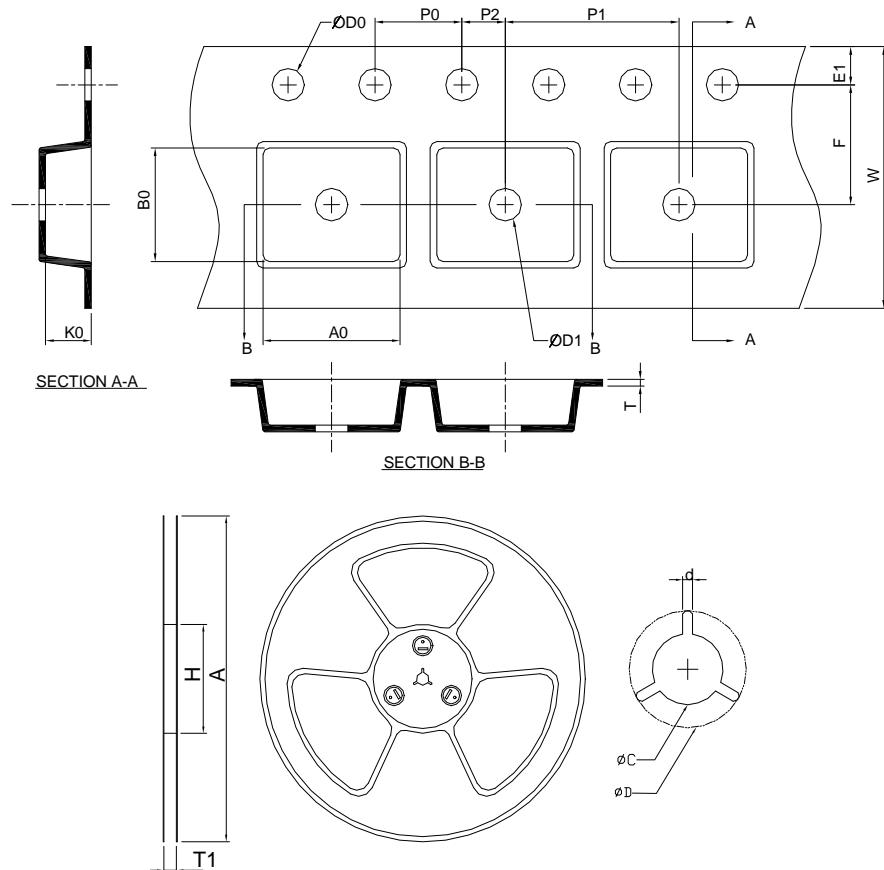
TSSOP-28P



SYMBOL	TSSOP-28P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.20		0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.031	0.041
b	0.19	0.30	0.007	0.012
c	0.09	0.20	0.004	0.008
D	9.60	9.80	0.378	0.386
D1	4.50	6.00	0.177	0.236
E	6.20	6.60	0.244	0.260
E1	4.30	4.50	0.169	0.177
E2	2.50	3.50	0.098	0.138
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.018	0.030
θ	0°	8°	0°	8°

- Note : 1. Followed from JEDEC MO-153 AET.
 2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
 3. Dimension "E1" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TSSOP-28P	330.0 ±0.00	50 MIN.	16.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	16.0 ±0.30	1.75 ±0.10	7.50 ±0.10
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.00 ±0.10	12.00 ±0.10	2.00 ±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.9 ±0.20	10.20 ±0.20	1.50 ±0.20

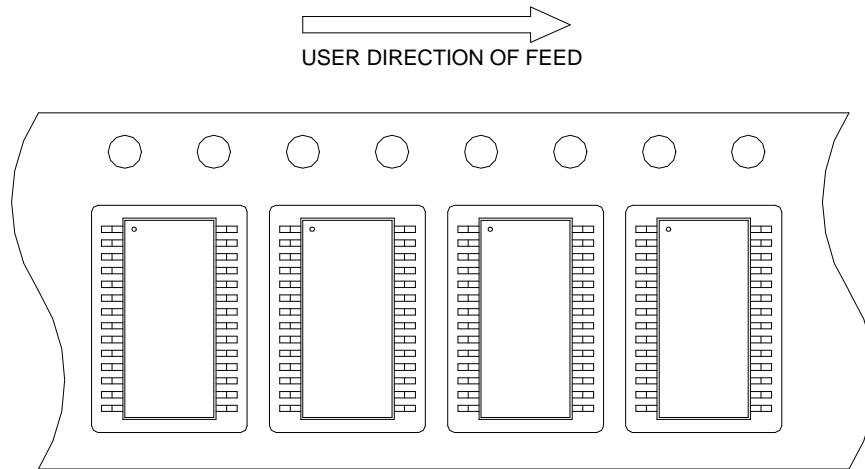
(mm)

Devices Per Unit

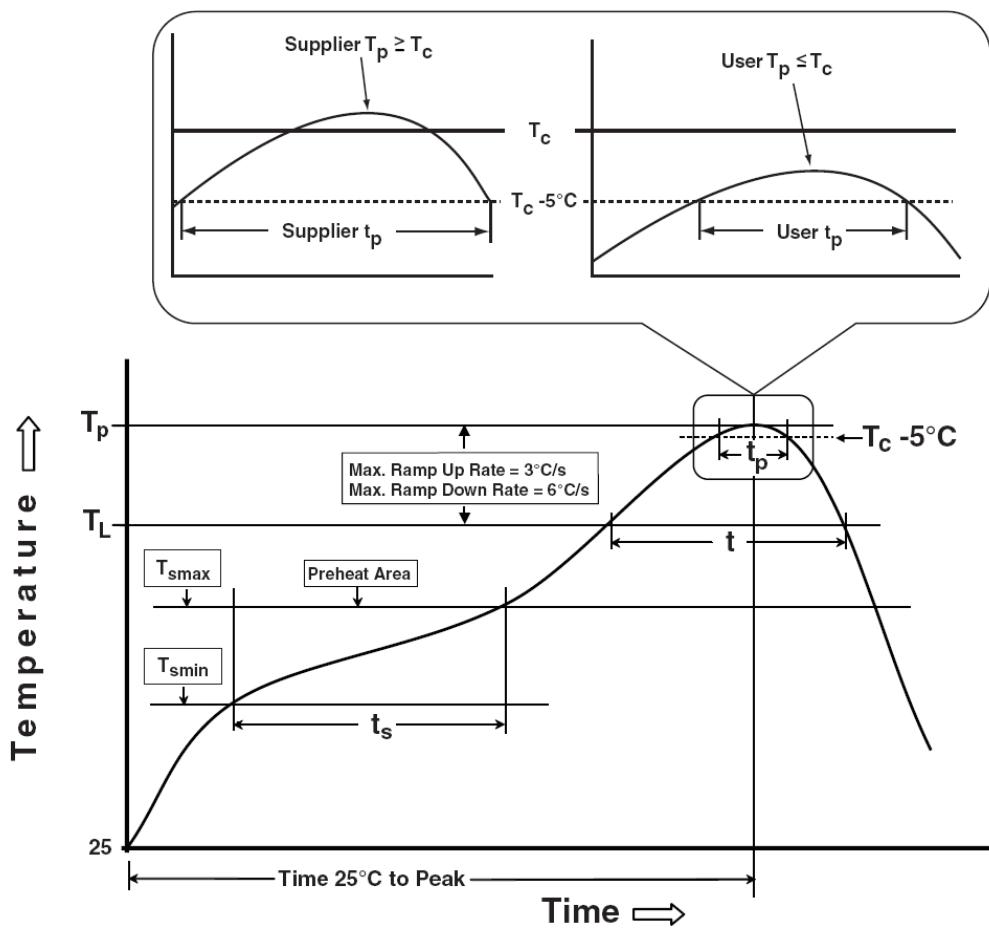
Package Type	Unit	Quantity
TSSOP-28P	Tape & Reel	2000

Taping Direction Information

TSSOP-28P



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_p)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.

* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum.

** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.

Table 1. SnPb Eutectic Process – Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ 350-2000	Volume mm ³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ $T_j=125^\circ C$
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
ESD	MIL-STD-883-3015.7	VHBM 2KV, VMM 200V
Latch-Up	JESD 78	10ms, 1 _{tr} 100mA

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