High Side and Low Side Driver

Features

- **Floating Channel designed for Bootstrap Operation to +600V**
- **Built-in Bootstrap Diode and Resistor**
- **Typically 200mA/350mA Sourcing/Sinking Current Driving Capability**
- **Matched Propagation Delay Time: 200ns(max.)**
- **3.3V and 5V Input Logic Compatible**
- **Built-in Short-Through Prevention Circuit with 1μs (min.) Dead Time**
- **Undervoltage Lockout(UVLO) for V_{cc} and V_{BS}**
- **Built-in Common Mode dv/dt Noise Canceling Circuit**

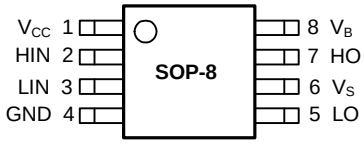
General Description

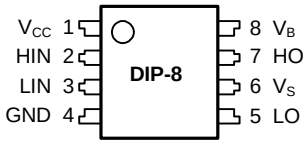
The APX7387 is a high voltage, high speed, power MOSFET and IGBT gate drivers with independent high and low side referenced output channels. The high voltage process and common mode noise canceling technique provide stable operation of high-side driver under high dv/dt noise circumstances. The IC built-in UVLO circuits to prevent malfunction when V_{CC} and V_{BS} are lower than the specified threshold voltage. The APX7387 is available in SOP-8 and DIP-8 packages (see Pin Configuration).

Applications

- **Motor Drive**
- **Ballast**
- **Power Audio Amplifier**

Pin Configuration





Ordering and Marking Information

APX7387 □□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code J: DIP-8 K: SOP-8 Operating Ambient Temperature Range I : -40 to 125 °C Handling Code TU : Tube TR : Tape & Reel Assembly Material G: Halogen and Lead Free Device
APX7387 J : APX7387 XXXXX	XXXXX - Date Code
APX7387 K : APX7387 XXXXX	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight inhomogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Absolute Maximum Ratings (Note 2)

Symbol	Parameter	Ratings	Unit
V_B	High-side Floating Supply Voltage	-0.3 to 625	V
V_S	Hugh-side Floating Supply Offset Voltage	V_B-20 to V_B+0.3	V
V_{HO}	High-side Floating Output Voltage	V_S-0.3 to V_B+0.3	V
V_{CC}	Low-side and Logic-fixed Supply Voltage	-0.3 to 20	V
V_{LO}	Low-side Output Voltage	-0.3 to V_{CC}+0.3	V
V_{IN}	Logic Input Voltage (all of HIN and LIN Pin)	-0.3 to 20	V
dV_S/dt	Offset Voltage Slew Rate	50	V/ns
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 to 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note 2: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
$R_{TH,JA}$	Thermal Resistance-Junction to Ambient (Note 3) SOP-8 DIP-8	 156.25 125	°C/W
P_D	Power Dissipation, T_A=25℃ SOP-8 DIP-8	 0.8 1	W

Note 3: Mounted on a board (76x115x1.6t mm, Glass epoxy).

Recommended Operating Conditions (Note 4)

Symbol	Parameter	Range	Unit
V_B	High-side Floating Supply Voltage	V_S+10 to V_S+15	V
V_S	Hugh-side Floating Supply Offset Voltage	11-V_{CC} to 600	V
V_{CC}	Supply Voltage	10 to 15	V
V_{HO}	High-side Output Voltage	V_S to V_B	V
V_{LO}	Low-side Output Voltage	0 to V_{CC}	V
V_{IN}	Logic Input Voltage (HIN and LIN Pin)	0 to V_{CC}	V
T_A	Ambient Temperature	-40 to 125	°C

Note 4: Refer to the typical application circuit

Electrical Characteristics

V_{CC}, V_{BS} = 15V, T_A = 25°C, unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to GND. The V_O and I_O parameters are referenced to GND and V_S and are applicable to the respective outputs LO and HO.

Symbol	Parameter	Test Conditions	APX7387			Unit
			Min	Typ	Max	
LOW SIDE POWER SUPPLY						
I_{QCC}	V_{CC} Quiescent Supply Current	V_{LIN}= 0V or 5V	-	150	300	μA
V_{CCUV+}	V_{CC} Supply Under-Voltage Positive-going Threshold	V_{BS}=15V, V_{DD} Rising	8	8.9	9.8	V
V_{CCUV-}	V_{CC} Supply Under-Voltage Negative-going Threshold	V_{BS}=15V, V_{DD} Falling	7.4	8.2	9	V
V_{DDHYS}	V_{CC} Supply Under-Voltage Lockout Hysteresis	V_{BS}=15V	-	0.7	-	V
BOOTSTRAPPED POWER SUPPLY						
I_{QBS}	V_{BS} Quiescent Supply Current	V_{HIN}= 0V or 5V	-	150	300	μA
I_{BS}	Bootstrap Current	V_B=0V	-30	-20	-10	mA
V_{BSUV+}	V_{BS} Supply Under-Voltage Positive-going Threshold	V_{DD}=15V, V_{BS} Rising	8	8.9	9.8	V
V_{BSUV-}	V_{BS} Supply Under-Voltage Negative-going Threshold	V_{DD}=15V, V_{BS} Falling	7.4	8.2	9	V
V_{BSHYS}	V_{BS} Supply Under-Voltage Lockout Hysteresis	V_{DD}=15V	-	0.7	-	V
I_{LK}	Offset Supply Leakage Current	V_B=V_S=600V	-	-	50	μA
GATE DRIVER OUTPUT						
V_{OH}	Output High-level Voltage, V_{BIAS}-V_O	I_O=20mA	-	-	1	V
V_{OL}	Output Low-level Voltage, V_O	I_O=20mA	-	-	0.6	V
I_{O+}	Output High Short-circuit Pulsed Current (note5)	V_O=0V, V_{IN}=5V with PW<10μs	120	200	-	mA
I_{O-}	Output Low Short-circuit Pulsed Current (note5)	V_O=15V, V_{IN}=0V with PW<10μs	250	350	-	mA
INPUT LOGIC						
V_{IH}	Logic “1” Input Voltage		2.5	-	-	V
V_{IL}	Logic “0” Input Voltage		-	-	1	V
I_{IN+}	Logic “1” Input Current	V_{IN}=5V	-	25	50	μA
I_{IN-}	Logic “0” Input Current	V_{IN}=0V	-	-	2	μA
R_{IN}	Input Pull-down Resistance		100	200	300	KΩ

Note 5: The parameters are guaranteed by design.

Dynamic Electrical Characteristics

T_A = 25°C, V_{BIAS}(V_{CC}, V_{BS})=15V, V_S=GND, C_{load}=1000pF unless otherwise specified.

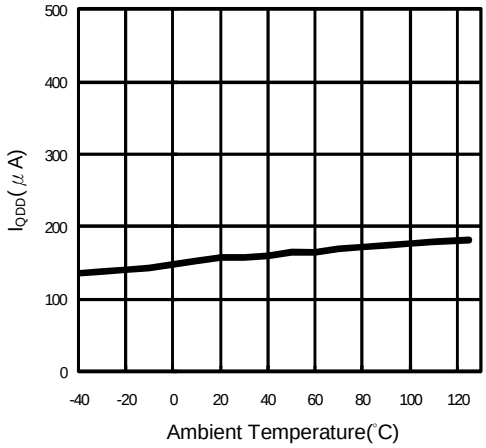
Symbol	Parameter	Test Conditions	APX7387			Unit
			Min	Typ	Max	
t_{ON}	Turn-on Propagation Delay Time	V_S= 0V	-	300	600	ns
t_{OFF}	Turn-off Propagation Delay Time	V_S= 0V	-	300	600	ns
t_R	Turn-on Rise Time		-	100	170	ns
t_F	Turn-off Fall Time		-	80	150	ns
MT1	Turn-on Delay Matching $\|t_{ON(H)}-t_{ON(L)}\|$		-	-	200	ns
MT2	Turn-off Delay Matching $\|t_{OFF(H)}-t_{OFF(L)}\|$		-	-	100	ns
DT	Dead Time		1	-	-	μs

Pin Descriptions

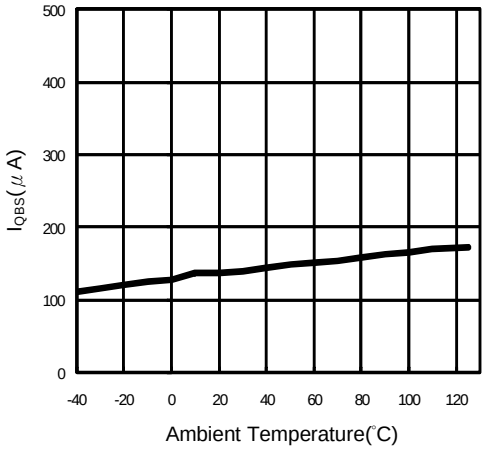
PIN		FUNCTION
NO.	NAME	
1	V_{CC}	Logic and all low-side gate drivers power supply voltage.
2	HIN	Logic input for high-side gate driver.
3	LIN	Logic input for low-side gate driver.
4	GND	Ground of the IC.
5	LO	Low-side gate driver output.
6	V_S	High-side driver floating supply offset voltage.
7	HO	High-side gate driver output.
8	V_B	High-side driver floating supply voltage.

Typical Operating Characteristics

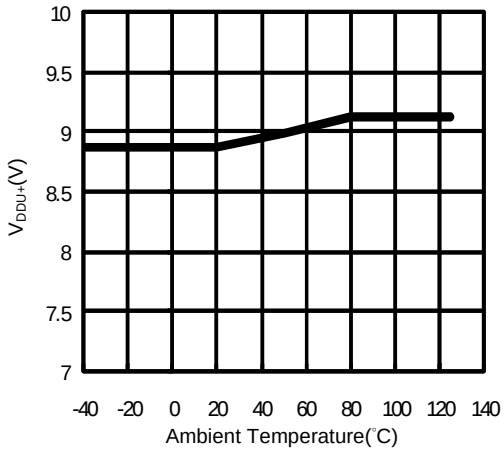
I_{QDD} vs. Ambient Temperature



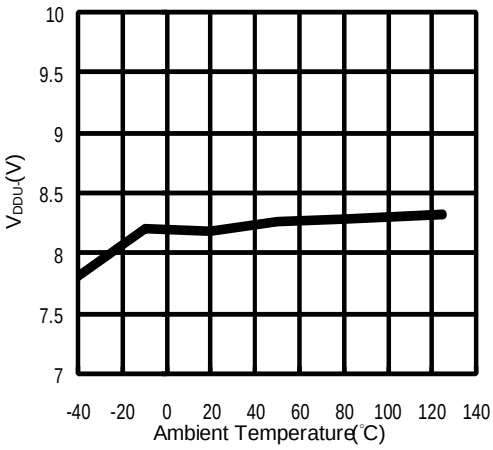
I_{QBS} vs. Ambient Temperature



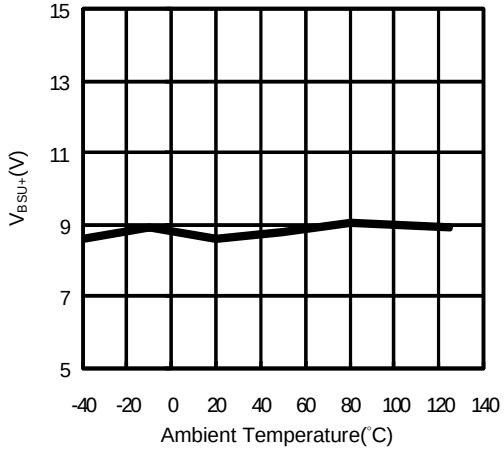
V_{DDU+} vs. Ambient Temperature



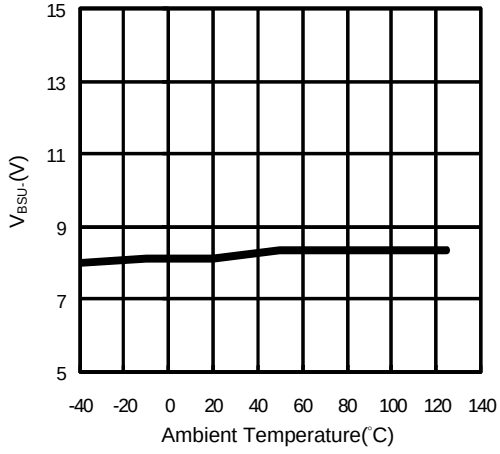
V_{DDU-} vs. Ambient Temperature



V_{BSU+} vs. Ambient Temperature

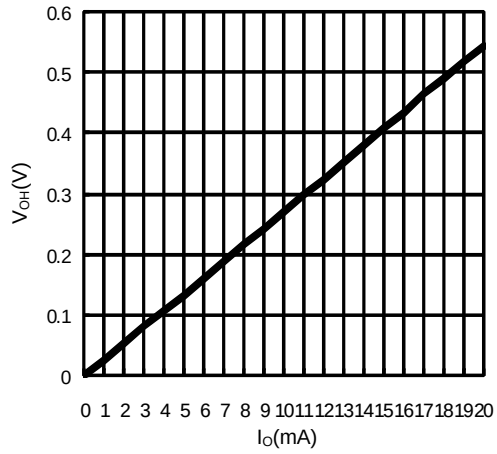


V_{BSU-} vs. Ambient Temperature

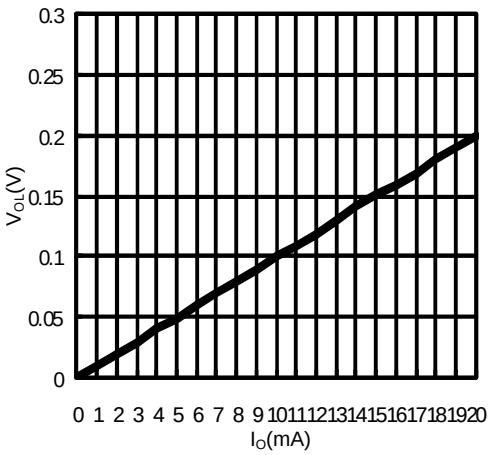


Typical Operating Characteristics

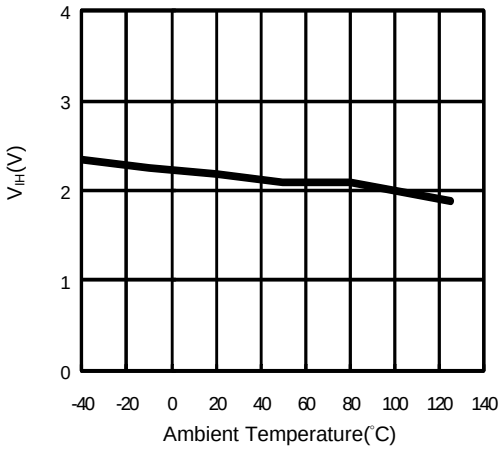
V_{OH} vs. I_O



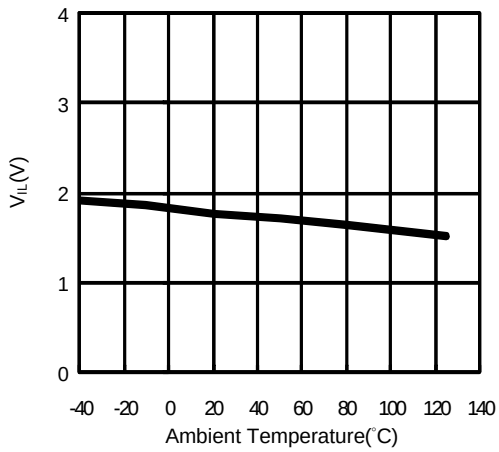
V_{OL} vs. I_O



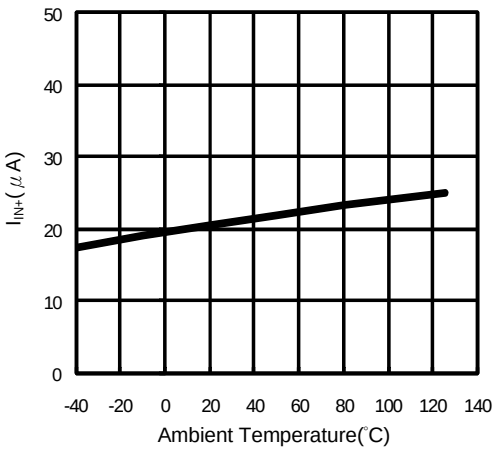
V_{IH} vs. Ambient Temperature



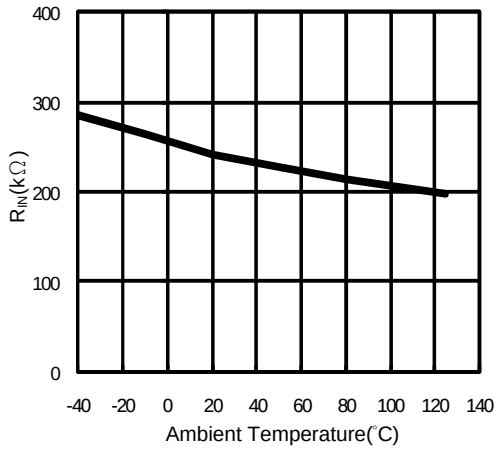
V_{IL} vs. Ambient Temperature



I_{IN+} vs. Ambient Temperature

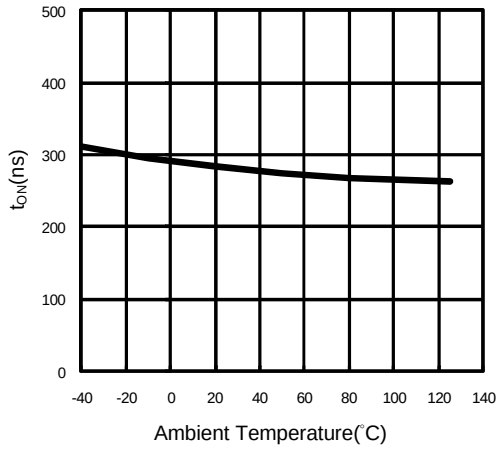


R_{IN} vs. Ambient Temperature

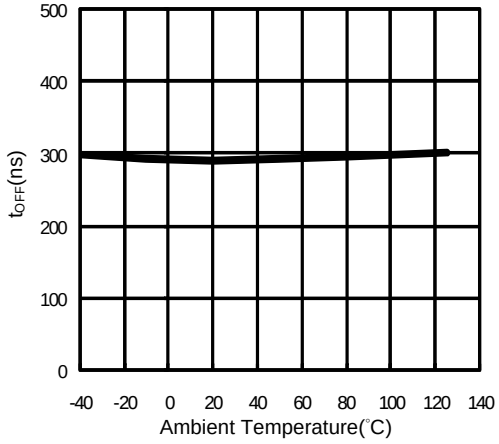


Typical Operating Characteristics

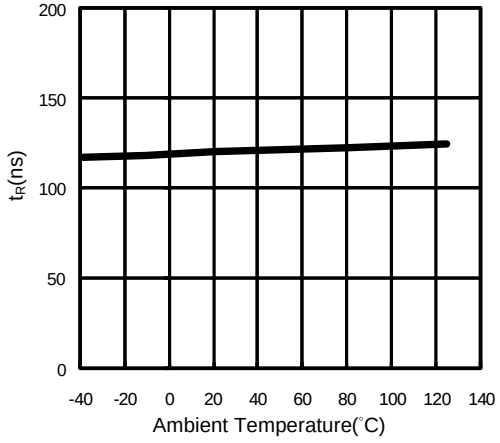
t_{ON} vs. Ambient Temperature



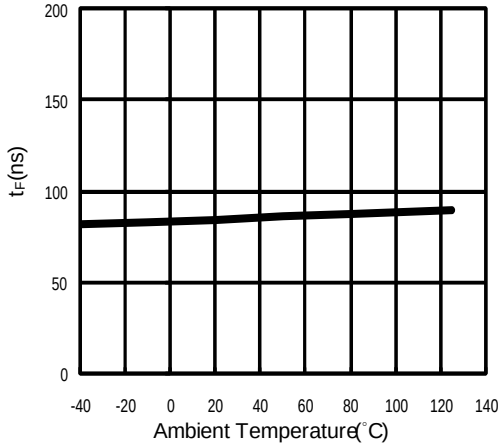
t_{OFF} vs. Ambient Temperature



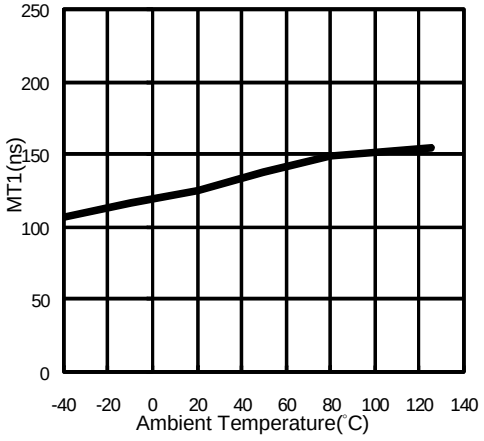
t_R vs. Ambient Temperature



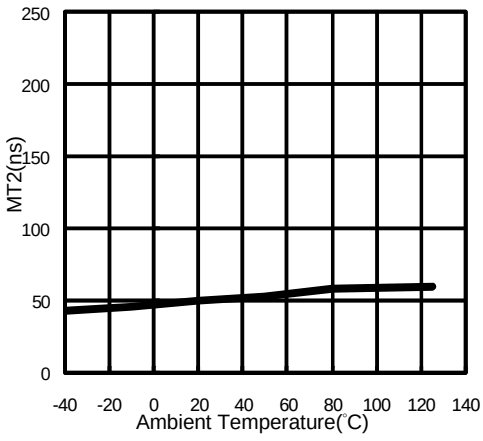
t_F vs. Ambient Temperature



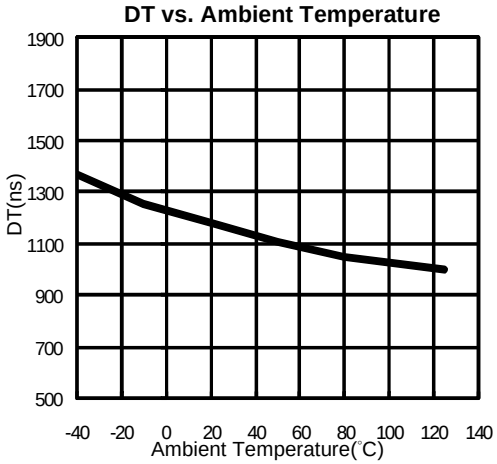
MT1 vs. Ambient Temperature



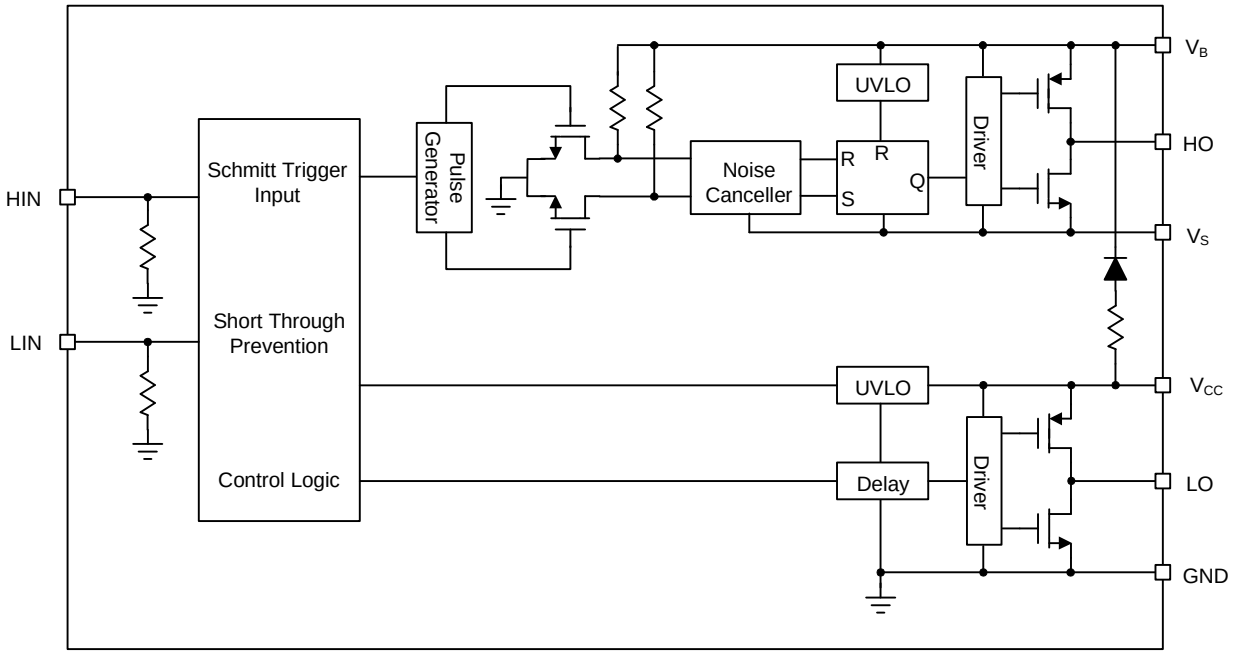
MT2 vs. Ambient Temperature



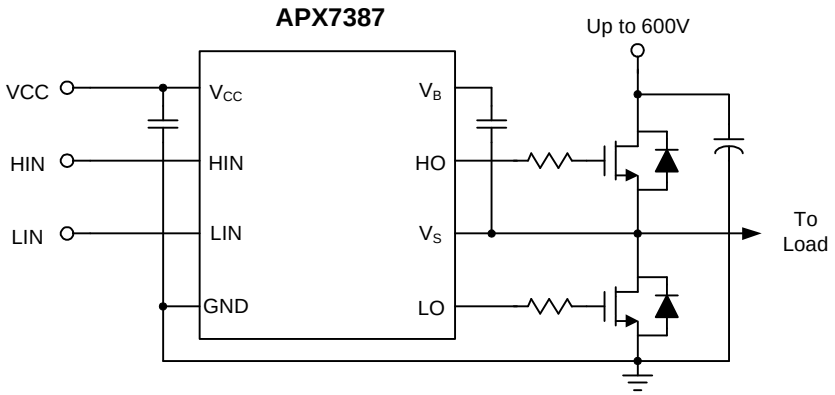
Typical Operating Characteristics



Block Diagram



Typical Application Circuit



Function Description

Under Voltage Lockout(UVLO)

The APX7387 has under-voltage lockout protection circuitry that monitors the supply voltage (V_{CC}) and bootstrap capacitor voltage (V_{BS}) independently. When V_{CC} and V_{BS} are lower than the specified threshold voltage the IC will enable the UVLO function. The UVLO hysteresis prevents chattering during power supply transitions.

Short-Through Prevention

The APX7387 has short-through prevention circuitry monitoring the high-side and low-side control inputs. It can be designed to prevent output when the high and low side control inputs turning on at same time (see Figure1,2)

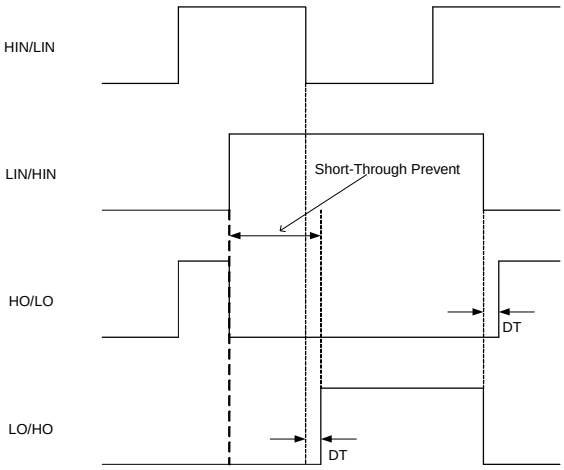


Figure 1. Short-Through Prevention Waveform 1

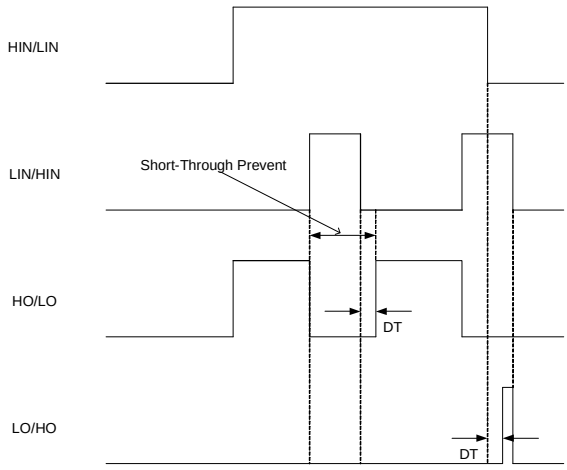


Figure 2. Short-Through Prevention Waveform 2

Switching Time Definition

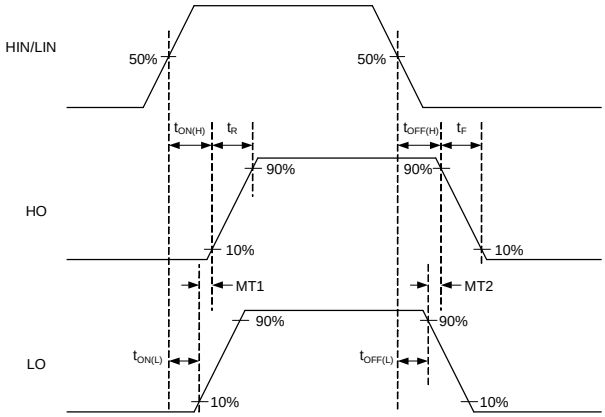
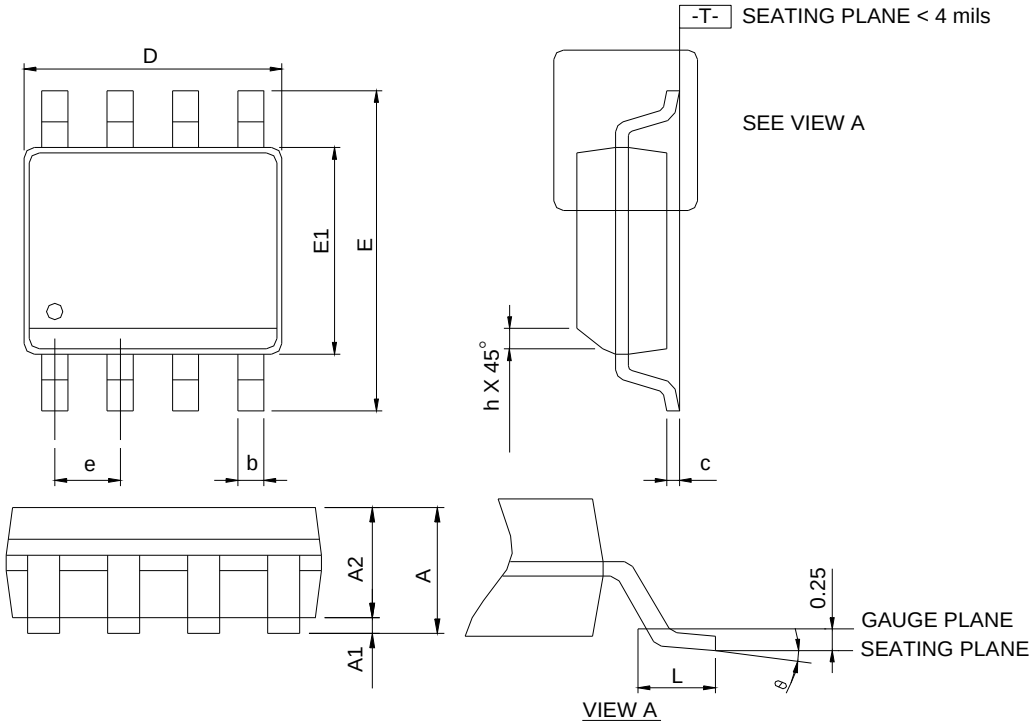


Figure 3. Switching Time Definition

Package Information

SOP-8

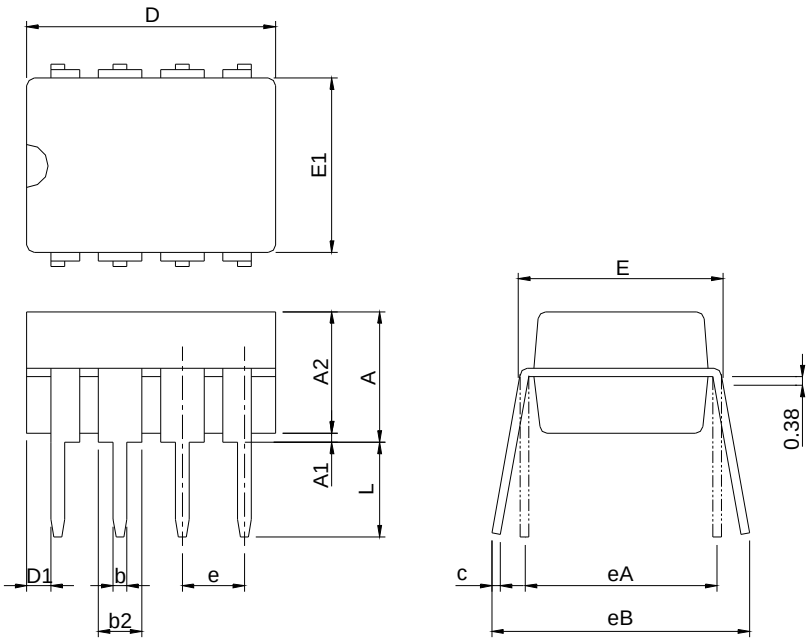


SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MS-012 AA.
2. Dimension “D” does not include mold flash, protrusions or gate burrs.
Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension “E” does not include inter-lead flash or protrusions.
Inter-lead flash and protrusions shall not exceed 10 mil per side.

Package Information

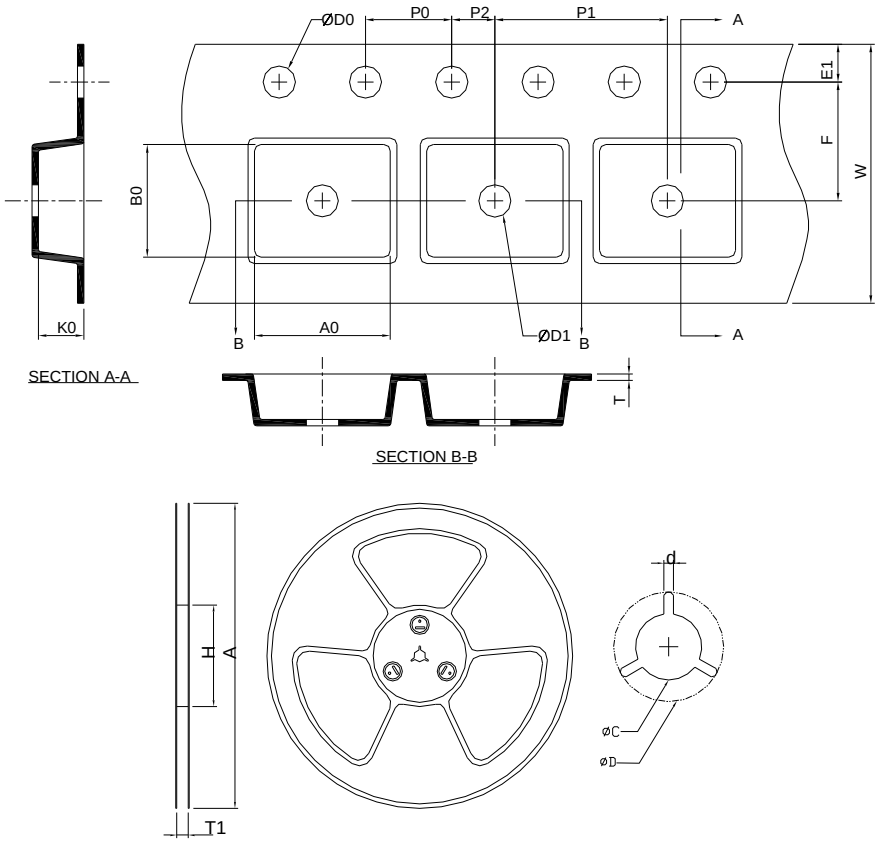
DIP-8



SYMBOL	DIP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		5.33		0.210
A1	0.38		0.015	
A2	2.92	4.95	0.115	0.195
b	0.36	0.56	0.014	0.022
b2	1.14	1.78	0.045	0.070
c	0.20	0.35	0.008	0.014
D	9.01	10.16	0.355	0.400
D1	0.13		0.005	
E	7.62	8.26	0.300	0.325
E1	6.10	7.11	0.240	0.280
e	2.54 BSC		0.100 BSC	
eA	7.62 BSC		0.300 BSC	
eB		10.92		0.430
L	2.92	3.81	0.115	0.150

Note : 1. Followed from JEDEC MS-001 BA
2. Dimension D, D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 10 mil.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOP-8	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20

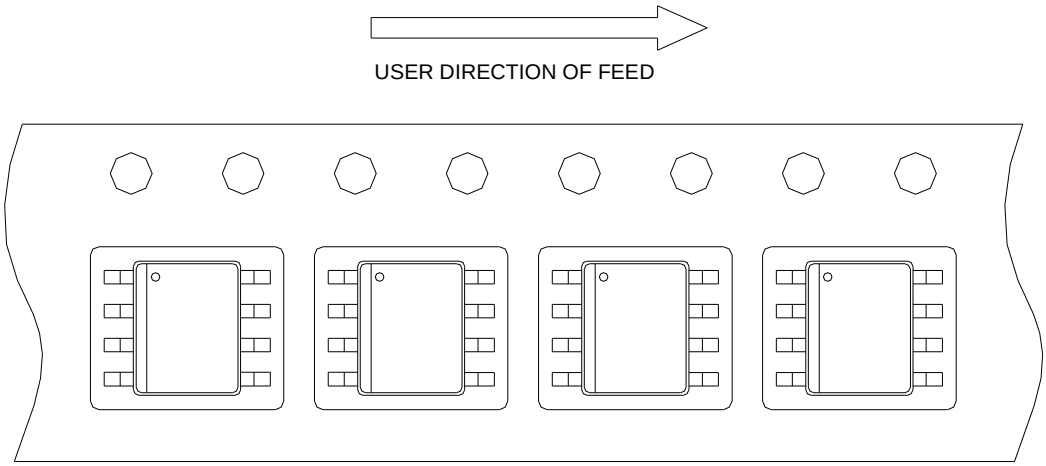
(mm)

Devices Per Unit

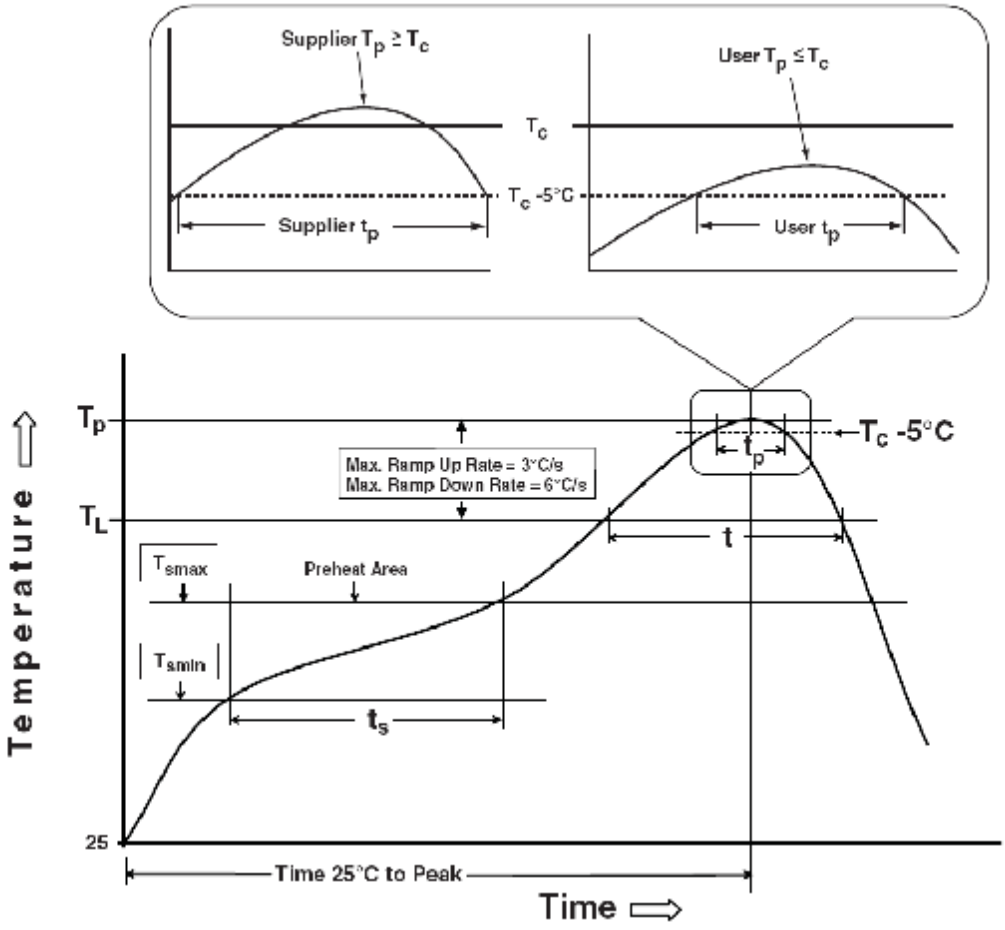
Package Type	Unit	Quantity
SOP-8	Tape & Reel	2500

Taping Direction Information

SOP-8



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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