DATA SHEET

AR1000/AR1010 FM Radio

Single Chip Stereo FM Radio Receiver

Preliminary Datasheet

VERSION 0.80 06-AUG-2007

Airoha Technology Corp.

Revision History

Version	Change Summary	Date	Author
0.10	Created	22-Sept-06	KH Chen
0.11	Spec Update	25-Oct-06	KH Chen
0.20	Spec Revised	07-Dec-06	KH Chen
0.30	Errata and Update (internal release only)	19-Jan-07	KH Chen
0.40	Update (internal release only)	06-Mar-07	KH Chen
0.50	Update	15-Mar-07	KH Chen
0.51	Update	22-Mar-07	KH Chen
0.52	AR1000E only for approval sheet draft	23-Apr-07	KH Chen
0.60	AR1000/AR1010 version	11-May-07	KH Chen
0.80	Update for AR1000 F	06-AUG-07	Purple Liu

Changing List (from 0.10 to 0.11):

- Page 10, Sec 6.1, DATA In, BUSEN to CLOCK P-edge Hold time unit added.
- Page 13, Sec 7.3, Audio output L/R imbalance and stereo separation spec updated.

Changing List (from 0.11 to 0.20):

- Page 5, Chap 1, Package thickness updated.
- Page 6, Chap 3, pin out updated (pin2⇔pin4) & (pin19⇔pin20).
- Page 7, Chap 4, pin out updated (pin2⇔pin4) & (pin19⇔pin20).
- Page 12, Chap 7, Register Table added.
- Page 17, Chap 9, Package thickness updated & Foot Print information added.

Changing List (from 0.20 to 0.30):

- Page 7, Chap 4, Pin6 (VIOEN), pin description updated.
- Page 10, Sec 6.1, 3-wire interface Write/Read procedure graph updated.
- Page 13, Sec 7.2, Register Table, R1(D6,D5) & R2(D8~D0) description updated.
- Page 15, Sec 8.1, Supply voltage spec updated

Changing List (from 0.30 to 0.40):

- Page 10, Sec 5.4, BUSEN High/Low setting for 2-wire/3-wire mode control changed.

Changing List (from 0.40 to 0.50):

- Page 6, Chap 1, Package information updated (from RevD to RevE).
- Page 7~8, Chap 3, Pin Assignment updated. (RevE added)
- Page 9~10, Chap 4, Pin Description updated. (RevE added)
- Page 12, Sec 5.4, Bus mode selection updated. (for RevD & RevE)
- Page 15, Chap 7, Register Map updated.
- Page 18, Sec 8.2, DC spec updated.
- Page 19, Sec 8.3, AC spec updated.
- Page 22, Sec 9.2, SAW type package dimension added. (for RevE)

Changing List (from 0.50 to 0.51):

- Page 8, Sec 3.2, RevE Pin Assignment updated.
- Page 10, Sec 4.2, RevE Pin Description updated.

Changing List (from 0.50 to 0.51):

- Page 6, Chap 1, RevD package info deleted.
- Page 7, Chap 3, RevD pin assignment deleted.
- Page 8, Chap 4, RevD pin description deleted.
- Page 10, Sec 5.4, RevD 2/3-wire control info deleted.
- Register table deleted.

Changing List (from 0.51 to 0.60):

- Introduce AR1010 code into this data sheet. AR1010 is the same and pin to pin compatible to AR1000 in all FM Radio functions except AR1000 supports RDS/RBDS function, while AR1010 not.

Changing List (from 0.60 to 0.80):

- Electrical characteristics update

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1 Features

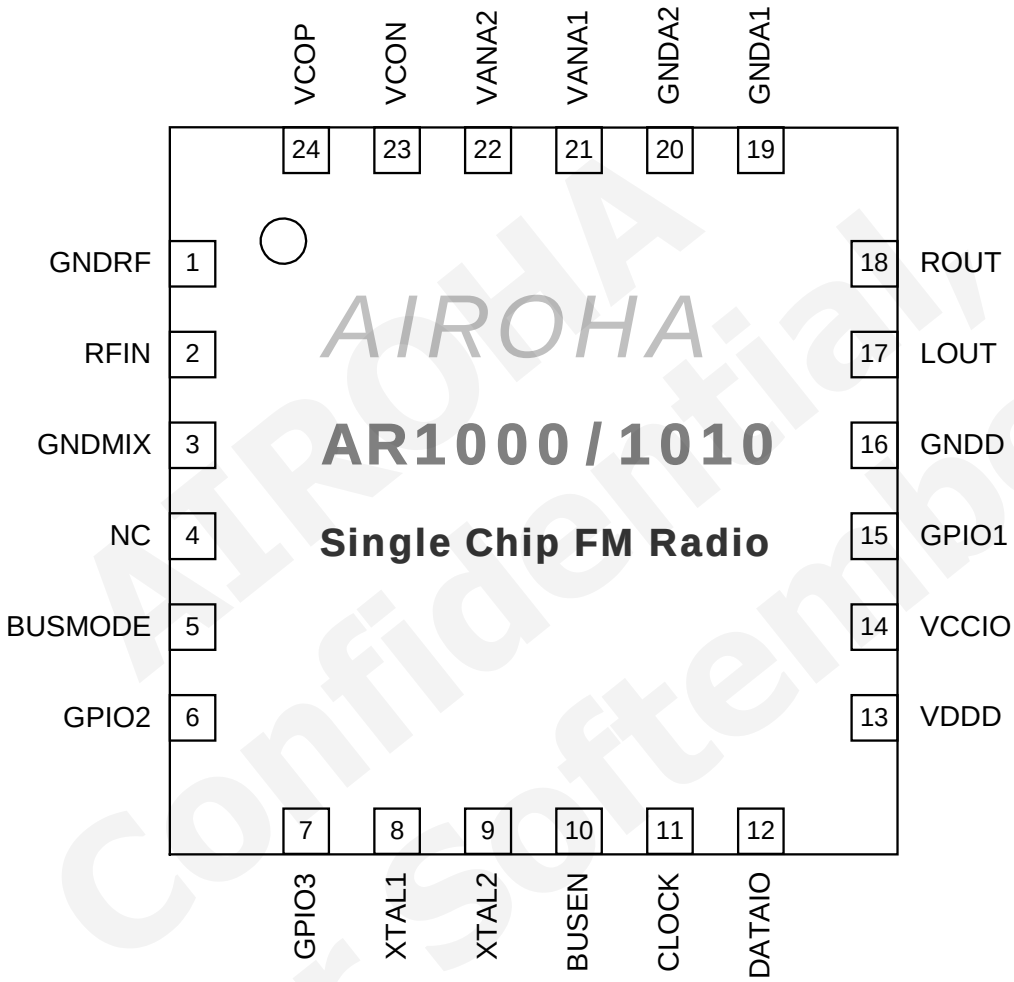
- Worldwide FM band support: 76~108MHz
- Highest integration level with minimized external BOM cost
- Frequency synthesizer with integrated VCO and Automatic Frequency Control (AFC)
- Integrated XO with external reference clock input or external 32.768KHz crystal
- Automatic Gain Control (AGC) on LNA/VGA amplifiers
- Signal strength measurement
- Programmable de-emphasis time constant (50/75us)
- Adaptive noise suppression
- Analog output with volume control and Line-level outputs
- Serial control interface for 2-wire and 3-wire modes
- Support both RDS & RBDS (AR1000 only)
- Embedded Seek tuning function
- Integrated LDO regulators support 2.7 to 5.5 V supply voltage
- QFN 4x4x0.6mm 24-pin package

2 Description

AR1000/AR1010 is a highly integrated single chip stereo FM radio receiver for all kinds of applications. AR1000/AR1010 supports worldwide FM bands from 76 to 108MHz. It integrates LNA, Mixer, Oscillator and LDO regulator to minimize the external BOM cost. The built-in FM signal processing unit with noise reduction mechanism provides optimum sound quality. A simple 2-wire/3-wire interface allows easy control from the host. For AR1000, a Radio Data System (RDS) and Radio Broadcast Data System (RBDS) demodulator and decoder are also supported.

AR1000 and AR1010 are pin-to-pin compatible and are the same in all FM radio receiver functions, specs and packages except the RDS/RBDS function. AR1000 supports RDS/RBDS receiver function, while AR1010 do not.

3 Pin Assignment

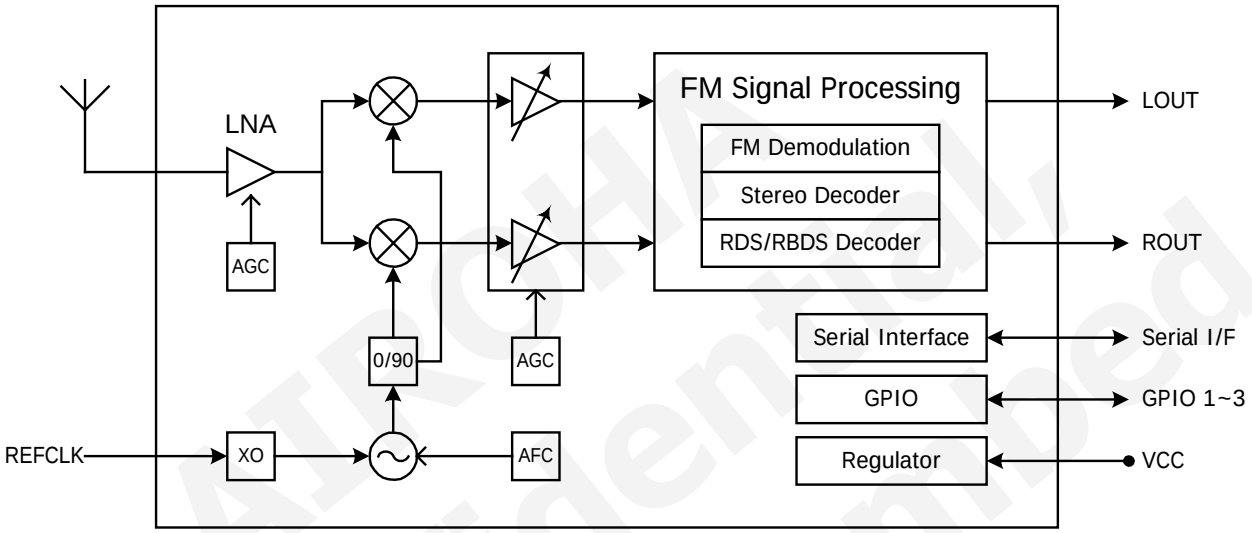


4 Pin Name Description

PIN	SIGANL	TYPE	DESCRIPTION
1	GNDRF	GND	RF Ground
2	RFIN	Input, Analog	RF Input
3	GNDMIX	GND	Mixer Ground
4	NC		Not Connected
5	BUSMODE	Input, Digital Control	2-wire/3-wire Bus Mode Selection
6	GPIO2	Input/Output, Digital	General I/O Port 2
7	GPIO3	Input/Output, Digital	General I/O Port 3
8	XTAL1	Analog	XTAL Input
9	XTAL2	Analog	XTAL Oscillator Input
10	BUSEN	Input, Digital Control	Serial Interface
11	CLOCK	Input, Digital Control	Serial Interface
12	DATAIO	Input/Output, Digital	Serial Interface
13	VDDD	VCC Supply	Supply Voltage for Digital Circuits
14	VCCIO	VCC Supply	Supply Voltage for I/O Ports
15	GPIO1	Input/Output, Digital	General I/O Port 1
16	GNDD	GND	Digital Ground
17	LOUT	Output, Analog	Left Audio Output
18	ROUT	Output, Analog	Right Audio Output
19	GNDA1	GND	Analog Ground
20	GNDA2	GND	Analog Ground
21	VANA1	VCC Supply	Supply Voltage for Analog Circuits
22	VANA2	VCC Supply	Supply Voltage for Analog Circuits
23	VCON	Input, Analog	VCO Tank Input
24	VCOP	Input, Analog	VCO Tank Input

5 Block Diagram and Description

5.1 General Description



AR1000/AR1010 is a single chip FM radio receiver IC, which supports full Europe/US/Japan bands. AR1000/AR1010 integrates on-chip LNA, Mixer, VGA, XO, FM signal processing unit, serial digital I/O interfaces and regulator. The highest integration level minimizes external BOM cost and provides optimum sound quality. A RDS/RBDS decoder is also included in AR1000 to provide broadcasted data.

5.2 Radio Receiver

The Radio Receiver part comprises a LNA, a Low-IF mixer and a VGA. The front-end gain of the LNA could be adjusted automatically and thus optimize the received signal-to-noise ratio. The RF signal is then converted to Low-IF band and amplified by the VGA, which is also automatically adjusted. After then the received signal is fed into the FM signal processing unit.

An internal reference oscillator is integrated, so only an external 32.768KHz crystal or a 32.768KHz REFCLK signal is required.

5.3 FM signal processing Unit

The main function of the FM signal processing unit includes FM Demodulation, Stereo Decoding and RDS/RBDS Decoding. The received FM signal at VGA output is first demodulated into stereo multiplexed signals (Left+Right and Left–Right) and then decoded into Left and Right signals individually by the stereo decoder. Two time constants (50 or 75μs) of de-emphasis are provided and programmable through the serial interface.

The decoded stereo signals are output to the LOUT and ROUT pins. The output volume could be adjusted or mute through the serial interface. The stereo output could be blocked and only mono signal is output under weak signals.

In AR1000, a RDS/RBDS decoder is also implemented for RDS/RBDS decoding, synchronization, error detection and error correction.

5.4 Serial I/O interface

Serial 2-wire and 3-wire interfaces are provided to read and write the control registers.

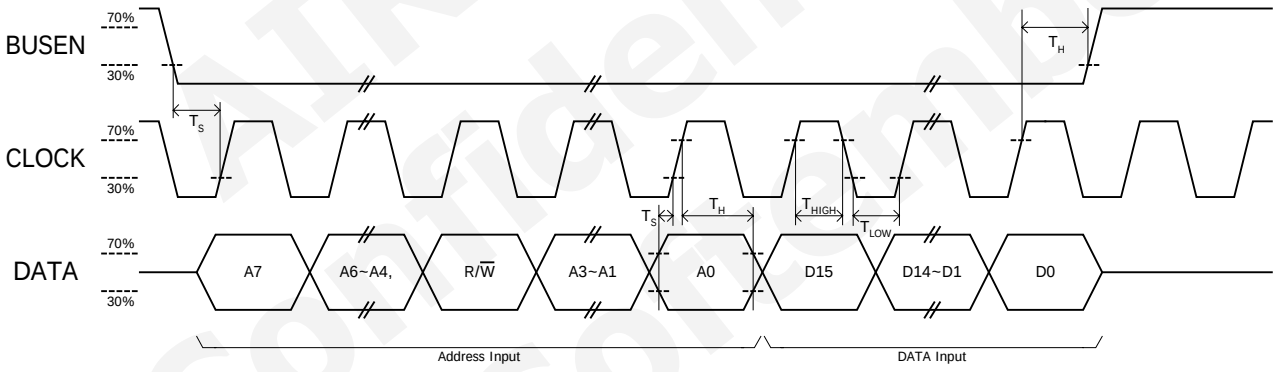
The 2-wire/3-wire bus is selected with BUSMODE pin. 3-wire mode is selected if BUSMODE is HIGH, and 2-wire mode is selected if BUSMODE is LOW.

6 Serial Interface

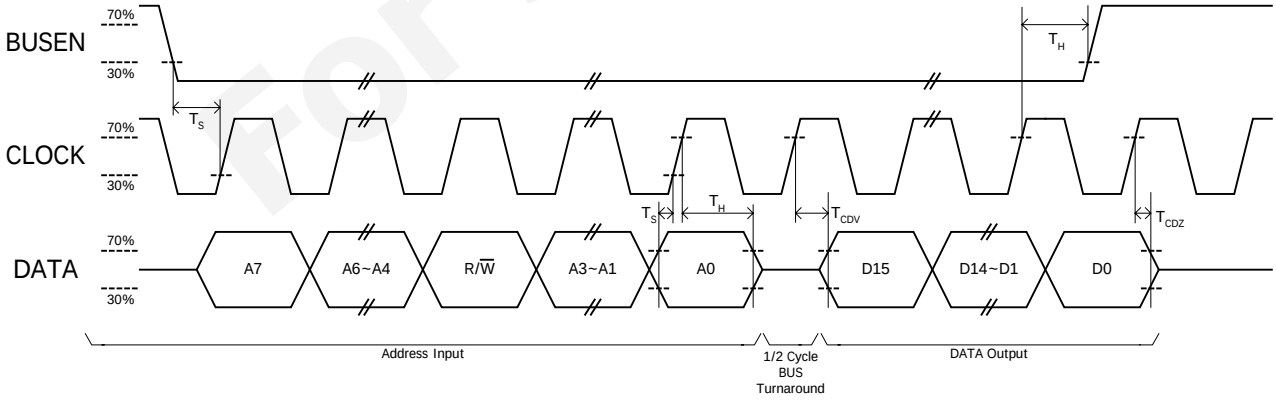
6.1 3-Wire Interface

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
	CLOCK Frequency	0		2.5	MHz
T_S	DATA In, BUSEN to CLOCK P-edge Setup time	20			ns
T_H	DATA In, BUSEN to CLOCK P-edge Hold time	10			ns
T_{HIGH}	CLOCK HIGH duration	25			ns
T_{LOW}	CLOCK LOW duration	25			ns
T_{DV}	CLOCK P-edge to DATA OUT Valid time	2		25	ns
T_{DZ}	CLOCK P-edge to DATA OUT High-Z time	2		25	ns

3-Wire Interface Write Procedure



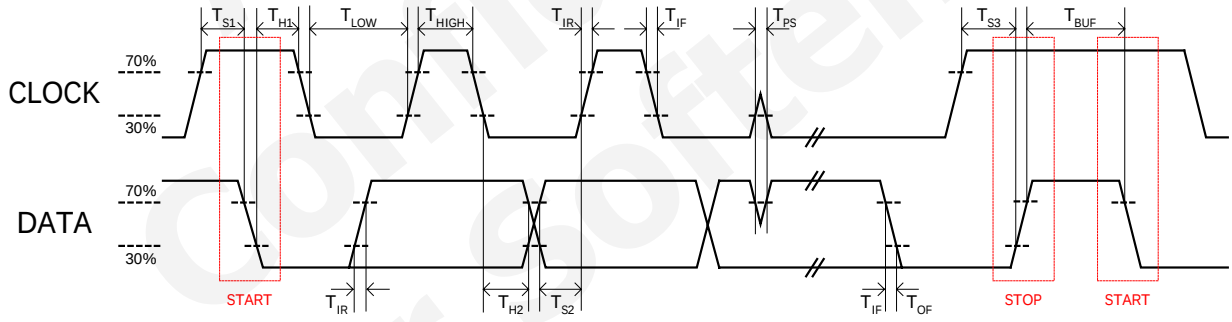
3-Wire Interface Read Procedure



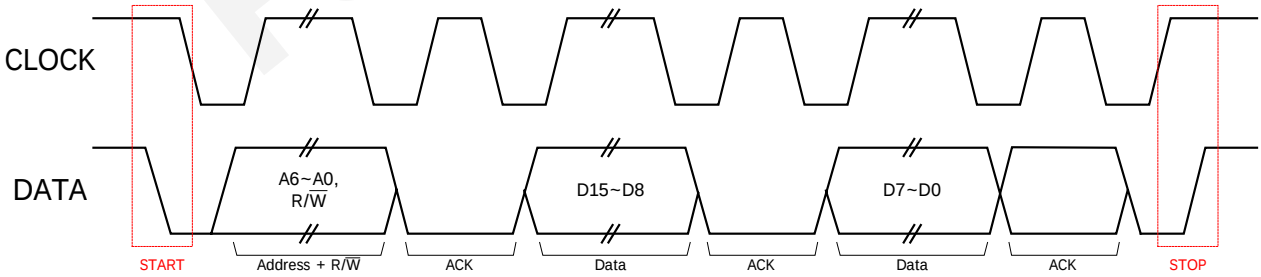
6.2 2-Wire Interface

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
	CLOCK Frequency	0		400	KHz
T_{S1}	CLOCK Input to DATA N-edge Setup time (START)	600			ns
T_{H1}	CLOCK Input to DATA N-edge Hold time (START)	600			ns
T_{S2}	DATA Input to CLOCK P-edge Setup time	100			ns
T_{H2}	DATA Input to CLOCK N-edge Hold time	0		900	ns
T_{S3}	CLOCK Input to DATA P-edge Setup time (STOP)	600			ns
T_{BUF}	STOP to START time	1300			ns
T_{OF}	DATA Output Fall time	20		250	ns
T_{IR}	DATA Input & CLOCK Rise time	20		300	ns
T_{IF}	DATA Input & CLOCK Fall time	20		300	ns
T_{HIGH}	CLOCK HIGH duration	600			ns
T_{LOW}	CLOCK LOW duration	1300			ns
T_{PS}	Input Filter Pulse Suppression			50	ns

2-Wire Interface Read and Write Timing Parameters



2-Wire Interface Read and Write Procedure



7 Electrical Characteristics

7.1 Absolute Maximum Ratings

AR1000/AR1010 could be damaged by any stress in excess of the absolute maximum ratings listed below.

ITEM	MIN.	MAX.
Power supply voltage (VDDD, VANA)	– 0.3V	5.5V
IO port supply voltage (VCCIO)	HOST_IO_VCC – 0.3V	HOST_IO_VCC + 0.3V
Pin voltage	– 0.3V	HOST_IO_VCC + 0.3V
Maximum power dissipation	-	1W
Operating temperature	– 40°C	+85°C
Storage temperature	– 65°C	+150°C
LNA input level	-	+10 dBm

7.2 DC Electrical Specifications

Recommended operating ambient temperature range T_A = -20 to 85°C

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Analog Supply Voltage	VANA		2.7		5.5	V
Digital Supply Voltage	VDDD		2.7		5.5	V
Interface Supply Voltage	VCCIO		1.5		3.6	V
Analog Supply Current	I_A	ENABLE=1		8.5		mA
Analog Power Down Current	I_{PDA}	ENABLE=0		1	10	µA
Digital Supply Current / without RDS	I_D	ENABLE=1, rds_en=0		4.5		mA
Digital Supply Current / with RDS **(AR1000 only)**	I_{D+RDS}	ENABLE=1, rds_en=1		5		mA
Digital Power Down Current	I_{PDD}	ENABLE=0		1	10	µA
Interface Supply Current	I_{IO}	ENABLE=1		470		µA
Interface Power Down Current	I_{PDIO}	ENABLE=0		5	10	µA
Digital Input Voltage – High Level	V_{IH}		0.7*VCCIO		VCCIO+0.3	V
Digital Input Voltage – Low Level	V_{IL}		- 0.3		0.3*VCCIO	V
Digital Input Current – High Level	I_{IH}	V_{IN}=VCCIO=3.6V	-10		10	µA
Digital Input Current – Low Level	I_{IL}	V_{IN}=0V, VCCIO=3.6V	-10		10	µA
Interface Output Voltage – High Level	V_{OH}	I_{OUT} = 500µA	0.8*VCCIO			V
Interface Output Voltage – Low Level	V_{OL}	I_{OUT} = - 500µA			0.2*VCCIO	V

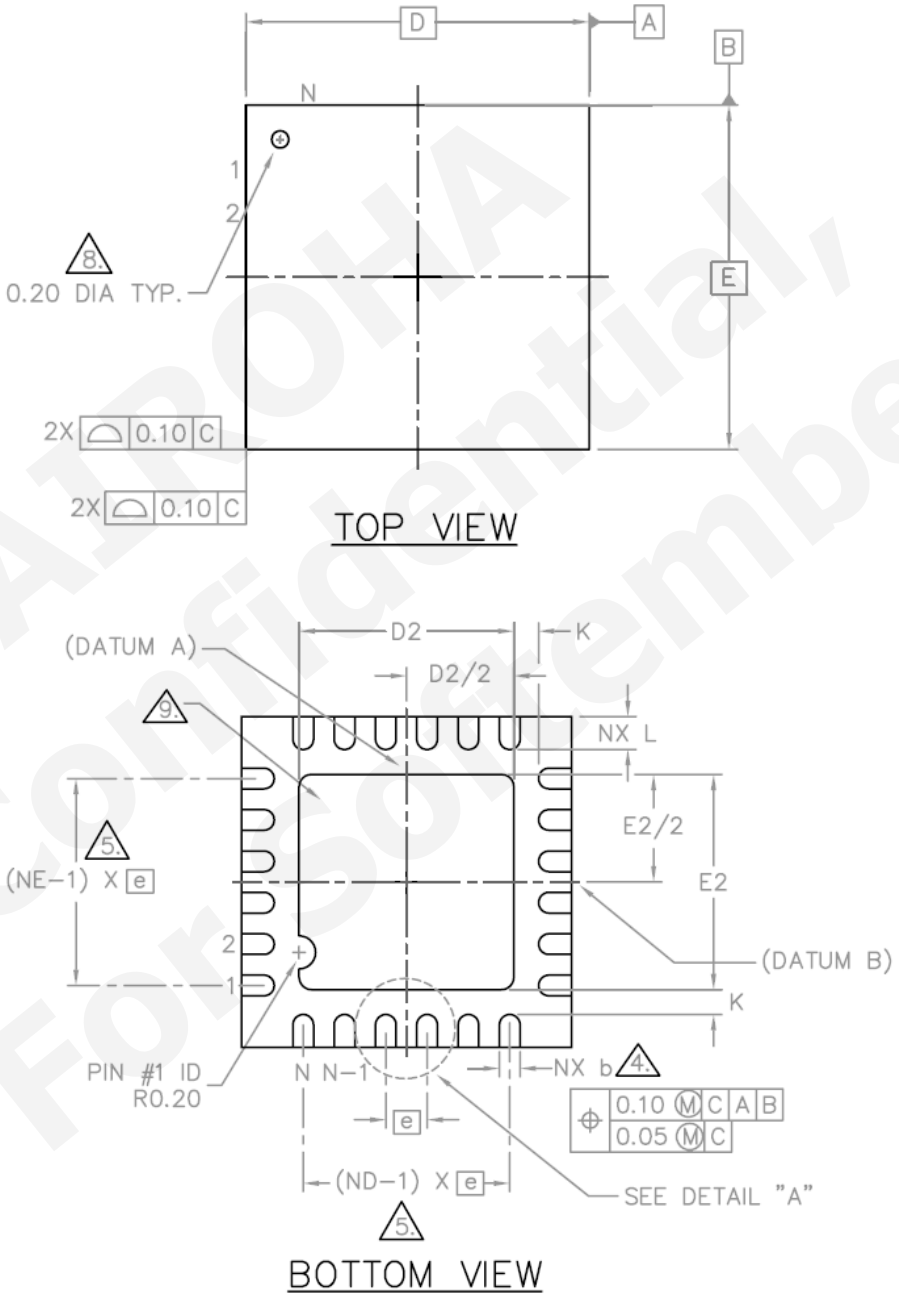
7.3 AC Electrical Specification

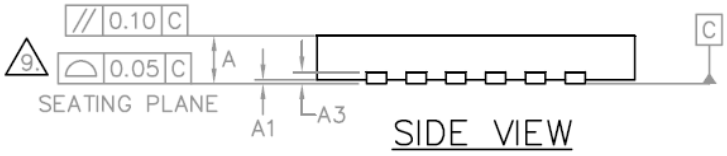
Typical values are tested under VANA,VDDD,VCCIO=3.3V, Ta=25°C unless otherwise specified

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Frequency		76		108	MHz
Sensitivity	(S+N)/N = 26dB		2		µVemf
RDS Sensitivity (AR1000 only)	Δf=2KHz, RDS BLER <5%		14		µVemf
LNA Input Resistance			550		Ohm
LNA Input Capacitance			3.4		pF
IIP3			93		dBµV
AM Suppression	m=0.3		60		dB
Adjacent Channel Selectivity	Low-side, -200KHz		35		dB
	Low-side, +200KHz		55		dB
Alternate Channel Selectivity	Low-side, -400KHz		35		dB
	Low-side, +400KHz		60		dB
Spurious Response Rejection	In-band	35			dB
REFCLK Frequency			32.768		KHz
REFCLK Frequency Tolerance	25 °C	-20		+20	ppm
	-20 °C ~ +85 °C	-150		+150	ppm
Audio Output Voltage			100		mV_{RMS}
Audio Output L/R Imbalance				0.2	dB
Audio Stereo Seperation		30			dB
Audio S/N			60		dB
Audio THD			0.2		%
De-emphasis Time Constant			75		µs
			50		µs
Audio Common-mode Voltage			0.9		V
Audio Output Load Resistance	Single-end	10			KOhm
Audio Output Load Capacitance	Single-end			10	pF

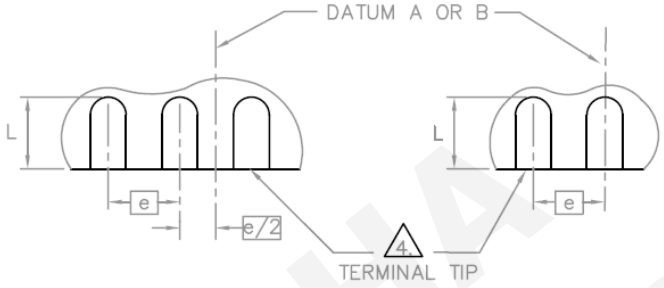
8 Package Dimension

Package: SAW type QFN 4x4x0.6mm, 0.5 pitch, 24pin





SIDE VIEW



EVEN TERMINAL/SIDE ODD TERMINAL/SIDE

DETAIL "A"

SYMBOL	0.50mm LEAD PITCH			NOTE
	MIN.	NOM.	MAX.	
[e]		0.50 BSC.		
N		24		3
ND		6		4
NE		6		4
L	0.35	0.40	0.45	4
b	0.18	0.25	0.30	4
D2	2.50	2.60	2.70	
E2	2.50	2.60	2.70	

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.50	0.55	0.60	
A1	0.00	0.02	0.05	
A3		0.15 REF.		
θ	0	——	12	2
K		0.20 MIN.		
D		4.0 BSC		
E		4.0 BSC		

NOTES :

1. DIMENSIONING AND TOLERANCING CONFORME TO ASME Y14.5M – 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS, θ IS IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
6. MAX. PACKAGE WARPAGE IS 0.05 mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LASER MARKED.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. THIS DRAWING CONFORMES TO JEDEC REGISTERED OUTLINE MO-248