Smart Handheld Device SoC

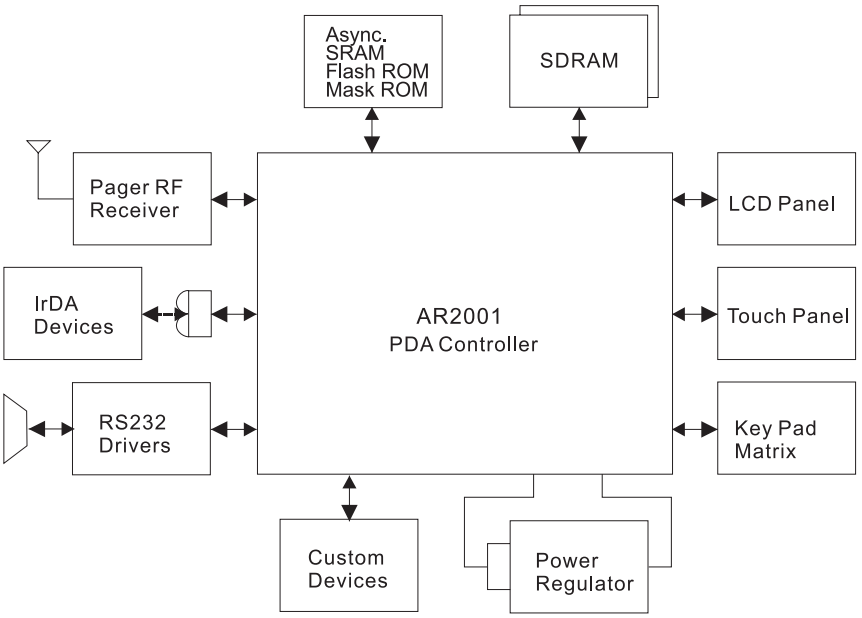
AR2001

ARCHITECTURAL OVERVIEW

The AR2001 IA/SHD SoC is a single chip integrated processor with peripherals suitable for portable and/or embedded control and computation application. The AR2001 IA/SHD SoC functions and capabilities include

- 32-bit processor with separate instruction and data cache
- Support for 32- and 16-bit SDRAM device interface
- Support for 2 SDRAM banks
- 6 device decoder with programmable base, offset, and access wait state select
- 1 dedicated and 6 shared general purpose I/O ports
- Interrupt controller with 8 external interrupt inputs with flexible request to CPU IRQ mapping
- 316-bit programmable timers
- Real time clock with alarm, stop-watch timer, and watch dog timer
- 2 UART channels (both support IrDA)
- Serial peripheral interface: one master device and one slave device
- POCSAG pager decoder with 6 address decoders
- LCD controller with frame buffer
- ADC with touch-screen controller
- Crystal oscillator and clock generator PLL
- Sophisticated power management modes

The following figure shows the block diagram of a typical platform based on AR2001 PDA controller. The 32-bit host interface supports synchronous DRAM and asynchronous SRAM as main memory. Boot ROM decoding is also provided. The LCD controller drives single-panel STN LCD with embedded display memory. In addition, the touch-screen controller directly interfaces with the touch-screen without any additional components. Asynchronous communications interface (UART) supports communications with external computing devices. Both UART channels have IrDA capability to drive the slow infrared (SIr) interface. Likewise, one synchronous serial peripheral interface (SPI) master interface and one slave interface provide convenient communications to other devices in the system. Moreover, the pager decoder provides wireless communication through support of the POCSAG standard with 6 address decoders. Thus, only a single AR2001 with minimum additional components is required to build a powerful computing and communications platform.



AR2001 System Block Diagram

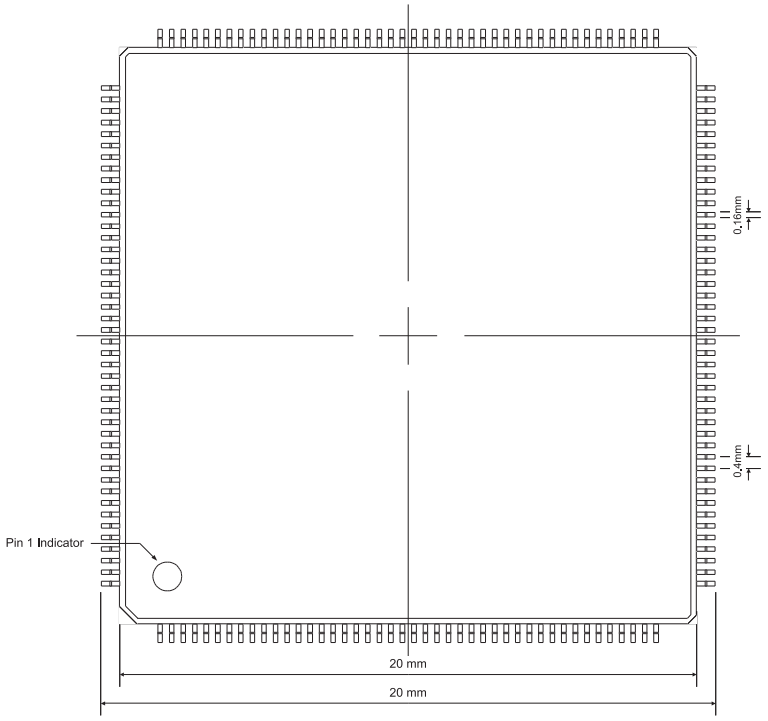
Absolute Maximum Ratings[1]

Symbol	Parameter	Min.	Max.	Units	Conditions
T_{OP}	Operating Temperature	0	80	°C	
T_{STG}	Storage Temperature	-40	125	°C	
V_{DD33}	I/O Supply Voltage	-0.3	4.3	V	
V_{DD25}	Core Supply Voltage	-0.3	3.25	V	
V_{IN}	Input Voltage	-0.3	V_{DD} +0.3	V	

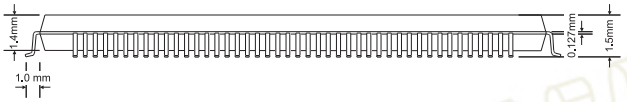
DC Characteristics[1]

(TOP = 0 °C to 70 °C, VDD = 3.3 V ± 0.3V, VSS = 0V)

Symbol	Parameter	Min.	Max.	Units	Conditions
V_{IL}	Input LOW Voltage	-0.3	0.8	V	
V_{IH}	Input HIGH Voltage	2.0	VDD+0.3	V	
V_{OL}	Output LOW Voltage	-	0.4	V	
V_{OH}	Output HIGH Voltage	2.4	-	V	
I_{CC}	Power Supply Current CLK = 50 MHz CLK = 100 MHz	 - -	 170 300	mW	Excuting benchmark programe; without power management
I_{LI}	Input Leakage Current	0	-	µA	
I_{LO}	Output Leakage Current	0	-	µA	
C_{IN}	Input Capacitance	3	8	pF	
C_{OUT}	Output Capacitance	3	8	pF	



LQFP 176 Pin Package Dimensions (top view)



LQFP 176 Pin Package Dimensions (side view)