PRELIMINARY
April 2006

AR2317 Single Chip MAC/Baseband/Radio and Processor for 2.4 GHz Wireless LANs

General Description

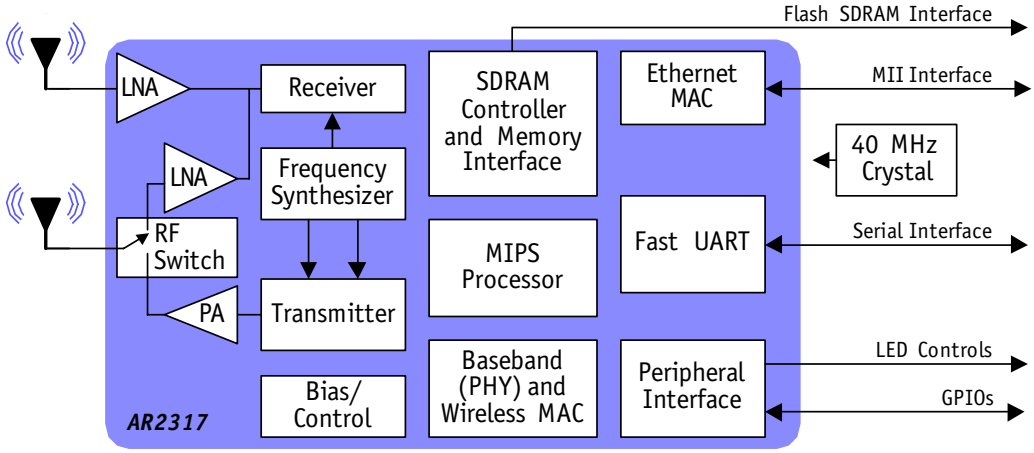
The Atheros AR2317 is an all-CMOS, fully-integrated, single-chip 802.11b/g WLAN solution. It integrates the PA, LNA, 2.4GHz radio, baseband PHY, MAC, and a MIPS 4000 CPU into a single chip for wireless access point and router applications. Other major modules include 802.3 Ethernet MAC and MII interface, SDRAM controller, external memory interface for Flash, ROM, or RAM, a UART, GPIOs as well as LED controls.

The AR2317 implements an 802.11 MAC/BB processor supporting all IEEE 802.11g data rates (1 to 54 Mbps) and all IEEE 802.11b complementary key coding (CCK) data rates (1 to 11 Mbps). Additional features include forward error correction coding at rates for 1/2, 2/3, and 3/4, signal detection, automatic gain control, frequency offset estimation, symbol timing, channel estimation, error recovery, enhanced security, and quality of service (QoS). The AR2317 performs receive and transmit filtering for IEEE 802.3 and 802.11 networks.

Features

- Integrated high-output PA
- Integrated LNA/optional external LNA support
- Integrated 1.8 V voltage regulator; NO need for a 1.8 V supply
- Switched Rx antenna diversity
- Integrated Rx/Tx antenna switch
- Integrated power detector
- 25 MHz output for Ethernet switch
- Integrated MIPS 4000 processor
- 180 MHz processor frequency
- IEEE 802.11b/g Access Point, Ad Hoc, and station functions supported
- OFDM and CCK modulation schemes supported
- Data rates of 1, 2, 5.5, 6, 9, 11, 12, 18, 24, 36, 48, 54 Mbps
- IEEE 802.3 Ethernet MAC supporting 10/100 Mbps, full and half duplex, and MII interface to external Ethernet PHY
- UART for console support
- IEEE 1149.1 standard test access port and boundary scan architecture supported
- EJTAG based debugging of the processor core supported
- Standard 0.18 µm CMOS technology
- 12 mm x 12 mm 260 BGA package

System Block Diagram



1. Pin Descriptions

This section contains both a package pinout (see Table 1-1 through Table 1-3) and tabular listings of the signal descriptions.

The following nomenclature is used for signal names:

- NC indicates no connection should be made to this pin.
- _L at the end of the signal name indicates active low signal.
- P at the end of the signal name indicates the positive side of a differential signal.
- N at the end of the signal name indicates the negative side of a differential signal.

The following nomenclature is used for signal types:

- IA indicates an analog input signal.
- I indicates a digital input signal.
- IH indicates input signals with weak internal pull-up, to prevent signals from floating when left open.
- IL indicates input signals with weak internal pull-down, to prevent signals from floating when left open.
- I/O indicates a digital bidirectional signal.
- OA indicates an analog output signal.
- O indicates a digital output signal.
- P indicates a power or ground signal.

Table 1-1. **AR2317 Pin Assignments (1–11)**

	1	2	3	4	5	6	7	8	9	10	11
A	GND	GND	VDD18_ BYPASS	SD_DATA_14	SD_DATA_15	GPIO_2	GPIO_7	GPIO_5	GPIO_3	NC	AVDD33
B	GND	GND	GND	SD_DATA_1	SD_DATA_13	SD_DATA_0	PROC_REF_CLK	GPIO_4	GPIO_1	GPIO_0	AVDD33
C	VDD33	GND	NA	NA	NA	NA	NA	NA	NA	NA	NA
D	SD_DATA_12	SD_DATA_2	NA	NA	NA	NA	NA	NA	NA	NA	NA
E	SD_DATA_11	SD_DATA_3	NA	NA	NA	NA	NA	NA	NA	NA	NA
F	SD_DATA_5	SD_DATA_4	NA	NA	NA	NA	NA	NA	NA	NA	NA
G	SD_DATA_6	SD_DATA_10	NA	NA	NA	NA	GND	GND	GND	GND	GND
H	SD_DATA_7	SD_DATA_9	NA	NA	NA	NA	GND	GND	GND	GND	GND
J	VDD33	SD_DATA_8	NA	NA	NA	NA	GND	GND	GND	GND	GND
K	VDD33	VDD33	NA	NA	NA	NA	GND	GND	GND	GND	GND
L	VDD33	VDD33	NA	NA	NA	NA	GND	GND	GND	GND	GND
M	VDD18_ BYPASS	VDD18_ BYPASS	NA	NA	NA	NA	GND	GND	GND	GND	GND
N	VDD18_ BYPASS	VDD18_ BYPASS	NA	NA	NA	NA	GND	GND	GND	GND	GND
P	SD_DQM_0	DLDO_PWD	NA	NA	NA	NA	GND	GND	GND	GND	GND
R	DLDO_SEL1	SD_WE_L	NA	NA	NA	NA	GND	GND	GND	GND	GND
T	DLDO_SEL0	SD_DQM_1	NA	NA	NA	NA	GND	GND	GND	GND	GND
U	SD_CAS_L	SD_CLK_FB	NA	NA	NA	NA	NA	NA	NA	NA	NA
V	SD_CKE	SD_CLK	NA	NA	NA	NA	NA	NA	NA	NA	NA
W	SD_RAS_L	SD_ADDR_12	NA	NA	NA	NA	NA	NA	NA	NA	NA
Y	VDD18_ BYPASS	GND	NA	NA	NA	NA	NA	NA	NA	NA	NA
AA	GND	GND	GND	SD_ADDR_11	SD_ADDR_9	SD_ADDR_8	SD_ADDR_7	SD_ADDR_6	SD_ADDR_5	SD_ADDR_4	CLK_25
AB	GND	GND	VDD33	SD_CS_L	SD_BANK_1	SD_BANK_0	SD_ADDR_10	SD_ADDR_0	SD_ADDR_1	SD_ADDR_2	SD_ADDR_3

Table 1-2. **AR2317 Pin Assignments (12–22)**

	12	13	14	15	16	17	18	19	20	21	22
A	RFANT1P	RFANT1P	RFANT1N	RFANT1N	PABIAS	AVDD33	RFANT2N	RFANT2P	AVDD33	GND	GND
B	PABIAS	PABIAS	PABIAS	PABIAS	PABIAS	AVDD33	GND	ALDO_PWD	GND	GND	GND
C	NA	NA	NA	NA	NA	NA	NA	NA	NA	ATBN	NC
D	NA	NA	NA	NA	NA	NA	NA	NA	NA	ALDO_SEL1	ALDO_SEL0
E	NA	NA	NA	NA	NA	NA	NA	NA	NA	AVDD33	RXVDD_ BYPASS
F	NA	NA	NA	NA	NA	NA	NA	NA	NA	AVDD33	AVDD_BYPASS
G	GND	GND	GND	GND	GND	NA	NA	NA	NA	AVDD33	AVDD33
H	GND	GND	GND	GND	GND	NA	NA	NA	NA	RES	RES
J	GND	GND	GND	GND	GND	NA	NA	NA	NA	RES	BIASREF
K	GND	GND	GND	GND	GND	NA	NA	NA	NA	RES	XTALI
L	GND	GND	GND	GND	GND	NA	NA	NA	NA	AVDD33	XTALO
M	GND	GND	GND	GND	GND	NA	NA	NA	NA	UART_SOUT	UART_SIN
N	GND	GND	GND	GND	GND	NA	NA	NA	NA	TCLK	TMS
P	GND	GND	GND	GND	GND	NA	NA	NA	NA	TDO	TDI
R	GND	GND	GND	GND	GND	NA	NA	NA	NA	TRST_L	GPIO_6
T	GND	GND	GND	GND	GND	NA	NA	NA	NA	EJTAG_SEL	COLD_RST_L
U	NA	NA	NA	NA	NA	NA	NA	NA	NA	SPI_CK	VDD33
V	NA	NA	NA	NA	NA	NA	NA	NA	NA	SPI_CS_L	SPI_MOSI
W	NA	NA	NA	NA	NA	NA	NA	NA	NA	ETH_TXD_0	SPI_MISO
Y	NA	NA	NA	NA	NA	NA	NA	NA	NA	GND	ETH_TXD_1
AA	ETH_COL	ETH_MDC	ETH_MDIO	ETH_TXC	ETH_CRS	ETH_RXD_2	ETH_TXEN	ETH_TXD_2	GND	GND	GND
AB	ETH_RXERR	ETH_RESET_L	ETH_RXC	ETH_RXDV	ETH_RXD_0	ETH_RXD_1	ETH_RXD_3	ETH_TXD_3	VDD18_ BYPASS	GND	GND

Table 1-3 provides the signal-to-pin relationship information for the AR2317.

Table 1-3. **Signal-to-Pin Relationships**

Signal Name	Pin	Direction	Description
Radio Control			
RFANT1N	A14, A15	O	Antenna 1 interface. RF transmitter output and alternate receiver input.
RFANT1P	A12, A13	O	
RFANT2N	A18	O	Antenna 2 interface. RF receiver input.
RFANT2P	A19	O	
BIASREF	J22	IA	Connects a 6.19 KΩ ±1% resistor to ground
ATBN	C21	O	Enable for optional external LNA
General			
GPIO_0	B10	I/O	General purpose GPIO pins
GPIO_1	B9	I/O	
GPIO_2	A6	I/O	
GPIO_3	A9	I/O	
GPIO_4	B8	I/O	
GPIO_5	A8	I/O	
GPIO_6	R22	I/O	
GPIO_7	A7	I/O	
COLD_RST_L	T22	I	Reset entire chip
XTALI	K22	I	40 MHz crystal
XTALO	L22	O	40 MHz crystal
PABIAS	A16, B12, B13, B14, B15, B16	IA	Connect to AVDD33
PROC_REF_CLK	B7		Reserved, must be open
Ethernet			
CLK_25	AA11	O	25 MHz clock for external Ethernet hardware
ETH_COL	AA12	I	Collision Detect
ETH_CRS	AA16	I	Carrier Sense
ETH_MDIO	AA14	I/O	PHY chip control bus data
ETH_MDC	AA13	O	PHY chip control bus clock
ETH_RESET_L	AB13	O	PHY Reset
ETH_RXC	AB14	I	Receive Clock (2.5 MHz @ 10 Mb; 25 MHz @ 100 Mb)
ETH_RXD_0	AB16	I	Receive Data
ETH_RXD_1	AB17	I	
ETH_RXD_2	AA17	I	
ETH_RXD_3	AB18	I	
ETH_RXDV	AB15	I	Receive Data Valid
ETH_RXERR	AB12	I	Receive Error
ETH_TXC	AA15	I	Transmit Clock (2.5 MHz @ 10 Mb; 25 MHz @ 100 Mb)
ETH_TXD_0	W21	O	Transmit Data
ETH_TXD_1	Y22	O	
ETH_TXD_2	AA19	O	
ETH_TXD_3	AB19	O	
ETH_TXEN	AA18	O	Transmit Enable
SDRAM Interface			
SD_DATA_15	A5	I/O	Read/write data [15]
SD_DATA_14	A4	I/O	Read/write data [14]
SD_DATA_13	B5	I/O	Read/write data [13]
SD_DATA_12	D1	I/O	Read/write data [12]
SD_DATA_11	E1	I/O	Read/write data [11]
SD_DATA_10	G2	I/O	Read/write data [10]
SD_DATA_9	H2	I/O	Read/write data [9]
SD_DATA_8	J2	I/O	Read/write data [8]
SD_DATA_7	H1	I/O	Read/write data [7]

Table 1-3. **Signal-to-Pin Relationships (continued)**

Signal Name	Pin	Direction	Description
SD_DATA_6	G1	I/O	Read/write data [6]
SD_DATA_5	F1	I/O	Read/write data [5]
SD_DATA_4	F2	I/O	Read/write data [4]
SD_DATA_3	E2	I/O	Read/write data [3]
SD_DATA_2	D2	I/O	Read/write data [2]
SD_DATA_1	B4	I/O	Read/write data [1]
SD_DATA_0	B6	I/O	Read/write data [0]
SD_CLK	V2	O	SDRAM clock
SD_CKE	V1	O	SDRAM clock enable
SD_CLK_FB	U2	I	SDRAM clock feedback
SD_CAS_L	U1	O	Column address select
SD_RAS_L	W1	O	Row address select
SD_CS_L	AB4	O	Chip select for DRAM
SD_BANK_1	AB5	O	Bank address [1]
SD_BANK_0	AB6	O	Bank address [0]
SD_DQM_1	T2	O	Data mask for byte 1
SD_DQM_0	P1	O	Data mask for byte 0
SD_WE_L	R2	O	Write enable
SD_ADDR_12	W2	O	Row/column address within bank
SD_ADDR_11	AA4	O	
SD_ADDR_10	AB7	O	
SD_ADDR_9	AA5	O	
SD_ADDR_8	AA6	O	
SD_ADDR_7	AA7	O	
SD_ADDR_6	AA8	O	
SD_ADDR_5	AA9	O	
SD_ADDR_4	AA10	O	
SD_ADDR_3	AB11	O	
SD_ADDR_2	AB10	O	
SD_ADDR_1	AB9	O	
SD_ADDR_0	AB8	O	
UART Control			
UART_SOUT	M21	O	Serial output data
UART_SIN	M22	I	Serial input data
SPI Interface			
SPI_CK	U21	O	SPI Serial Flash Clock
SPI_CS_L	V21	O	SPI Serial Flash Chip Select
SPI_MISO	W22	I	SPI Serial Flash Data: Master In, Slave out
SPI_MOSI	V22	O	SPI Serial Flash Data: Master Out, Slave In
JTAG Interface			
EJTAG_SEL	T21	I	When asserted, JTAG pins are routed to EJATAG TAP controller. When deasserted, JTAG pins are routed to TAP controller.
TCLK	N21	I	JTAG test clock
TDI	P22	I	JTAG data input
TDO	P21	O	JTAG data output
TMS	N22	I	JTAG test mode
TRST_L	R21	I	JTAG test reset
LDO Control			
ALDO_SEL0	D22	I	Control signals for internal regulators. Connect to GND. These signals have internal pull-up to 3.3 V.
ALDO_SEL1	D21	I	
ALDO_PWD	B19	I	
DLDO_SEL0	T1	I	Control signals for internal regulators. Connect to GND. These signals have internal pull-up to 3.3 V.
DLDO_SEL1	R1	I	
DLDO_PWD	P2	I	

Table 1-4. **Signal-to-Pin Relationships**

Signal Name	Pin	Description
Power		
AVDD_BYPASS	F22	Analog 1.8 V voltage regulator output, to connect to 2.2 µF bypass capacitor
AVDD33	A11, A17, A20, B11, B17, E21, G21, G22, L21	Analog 3.3V supply
RXVDD_BYPASS	E22	Analog 1.8 V voltage regulator output, to connect to 2.2 µF bypass capacitor
VDD18_BYPASS	A3, M1, M2, N1, N2, Y1, AB20	Digital 1.8 V voltage regulator output, to connect to 2.2 µF bypass capacitor
VDD33	C1, J1, K1, K2, L1, L2, U22, AB3	Digital 3.3 V
GND	A1, A2, A21, A22, B1, B2, B3, B18, B20, B21, B22, C2, G7, G8, G9, G10, G11, G12, G13, G14, G15, G16, H7, H8, H9, H10, H11, H12, H13, H14, H15, H16, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, K7, K8, K9, K10, K11, K12, K13, K14, K15, K16, L7, L8, L9, L10, L11, L12, L13, L14, L15, L16, M7, M8, M9, M10, M11, M12, M13, M14, M15, M16, N7, N8, N9, N10, N11, N12, N13, N14, N15, N16, P7, P8, P9, P10, P11, P12, P13, P14, P15, P16, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, T7, T8, T9, T10, T11, T12, T13, T14, T15, T16, Y2, AA1, AA2, AA3, AA20, AA21, AA22, AB1, AB2, AB21, AB22	Digital ground
No Connection		
NC	A10, C22	No connect
RES	H21, H22, J21, K21	Reserved, high impedance. Can be left open or connect to any power level.
NA	C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D20, E3, E4, E5, E6, E7, E8, E9, E10, E11, E12, E13, E14, E15, E16, E17, E18, E19, E20, F3, F4, F5, F6, F7, F8, F9, F10, F11, F12, F13, F14, F15, F16, F17, F18, F19, F20, G3, G4, G5, G6, G17, G18, G19, G20, H3, H4, H5, H6, H17, H18, H19, H20, J3, J4, J5, J6, J17, J18, J19, J20, K3, K4, K5, K6, K17, K18, K19, K20, L3, L4, L5, L6, L17, L18, L19, L20, M3, M4, M5, M6, M17, M18, M19, M20, N3, N4, N5, N6, N17, N18, N19, N20, P3, P4, P5, P6, P17, P18, P19, P20, R3, R4, R5, R6, R17, R18, R19, R20, T3, T4, T5, T6, T17, T18, T19, T20, U3, U4, U5, U6, U7, U8, U9, U10, U11, U12, U13, U14, U15, U16, U17, U18, U19, U20, V3, V4, V5, V6, V7, V8, V9, V10, V11, V12, V13, V14, V15, V16, V17, V18, V19, V20, Y3, Y4, Y5, Y6, Y7, Y8, Y9, Y10, Y11, Y12, Y13, Y14, Y15, Y16, Y17, Y18, Y19, Y20	Not Applicable

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1 summarizes the absolute maximum ratings and Table 2-2 lists the recommended operating conditions for the AR2317. Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

Table 2-1. **Absolute Maximum Ratings**

Symbol	Parameter	Max. Rating	Unit
V_{DD33}	I/O Supply Voltage (3.3 V)	–0.3 to 4.6	V
T_{store}	Storage Temperature	–65 to 150	°C
ESD	Electrostatic Discharge Tolerance	2000	V

2.1.1 Recommended Operating Conditions

Table 2-2. **Recommended Operating Conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD33}	I/O Supply Voltage	± 10%	3.0	3.3	3.6	V
T_{case}	Case Temperature		0	45	105	°C
T_J	Junction Temperature		0	50	115	°C
θ_{JA}	Junction to Ambient Temperature				33	°C/W

2.2 General DC Electrical Characteristics

Table 2-3 lists the general DC electrical characteristics. The following conditions apply to all DC characteristics unless otherwise specified:

V_{dd} = 3.3 V, T_{amb} = 25 °C

Table 2-3. **General DC Electrical Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage	$V_{out} = V_{OH\ (min)}$	2.0	—	V_{dd} + 0.3	V
V_{IL}	Low Level Input Voltage	$V_{out} = V_{OL\ (min)}$	–0.3	—	0.8	V
I_{IL}	Input Leakage Current	Without Pull-up or Pull-down	—	± 5	—	µA
		With Pull-up or Pull-down	—	± 65	—	µA
V_{OH}	High Level Output Voltage	No Load (I_o = 0)	V_{dd} –0.3	—	—	V
		I_o = 12 mA	V_{dd} –0.8	—	—	V
V_{OL}	Low Level Output Voltage	No Load (I_o = 0)	—	—	0.20	V
		I_o = 12 mA	—	—	0.27	V
I_O	Output Current	V_o = 0 to V_{dd}	—	—	6[1]	mA
C_{IN}	Input Capacitance	—	—	6	—	pF

[1]Note these exceptions: the pins SD_ADDR[12:0] are 2 mA, SD_DATA[15:0] are 2mA, and TDO is 8 mA.

2.2.1 Radio Receiver Characteristics

Table 2-4 summarizes the receiver characteristics for the AR2317.

Table 2-4. **Receiver Characteristics for Antenna 2 (Primary Receiver)**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{rx}	Receive input frequency range	5 MHz center frequency	2.312	—	2.484	GHz
NF	Receive chain noise figure	—	—	6	—	dB
S_{rf}	Sensitivity	See Note [1]				dBm
	CCK, 1 Mbps		—	–96	—	
	CCK, 11 Mbps		—	–88	—	
	OFDM, 6 Mbps		—	–91	—	
	OFDM, 54 Mbps		—	–74	—	
IP1dB	Input 1 dB compression (min. gain)	—	—	–10	—	dBm
IIP3	Input third intercept point (min. gain)	—	—	–1	—	dBm
Z_{RFin_input}	Recommended LNA differential drive impedance	See Note [2]	—	TBD	—	—
ER_{phase}	I,Q phase error		—	1	—	degree
ERamp	I,Q amplitude error		—	0.9	—	dB
R_{adj}	Adjacent channel rejection	10 to 20 MHz [3]				dB
	CCK		35	—	—	
	OFDM, 6 Mbps		16	40	—	
	OFDM, 54 Mbps		–1	20	—	
TRpowup	Time for power up (from synth on)	—	—	1	—	µs

[1]Performance is based on the Atheros reference design.
[2]Refer to the *Hardware Design Guide* for information.
[3]Measured with AR2317.

2.2.2 Radio Transmitter Characteristics

Table 2-5 summarizes the transmitter characteristics for the AR2317.

Table 2-5. **Transmitter Characteristics for Antenna 1**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{tx}	Transmit output frequency range	5 MHz center frequency	2.312	—	2.484	GHz
P_{out}[1]	EVM and mask compliant CCK output power	1–11 Mbps	—	20[2]	—	dBm
	EVM and mask compliant OFDM output power	6–24 Mbps	—	20[2]	—	
		36 Mbps	—	19[2]	—	
		48 Mbps	—	17.5[2]	—	
		54 Mbps	—	15.5[2]	—	
SP_{gain}	PA gain step		—	0.5	—	dB
A_{pl}	Accuracy of power leveling loop	See Note [3]	—	±1	—	dB
Z_{RFout_load}	Recommended PA differential load impedance	See Note [4]	—	TBD	—	—
OP1dB	Output P1dB (max. gain)	2.442 GHz	—	20	—	dBm
	Output third order intercept point (max. gain)	2.442 GHz	—	30	—	dBm
SS	Sideband suppression		—	TBD	—	dBc
RS	Synthesizer reference spur:	—	—	TBD		dBc
Tx_{mask}	Transmit spectral mask	—				dBr
	CCK					
	At 11 MHz offset		–30	–40	—	
	At 22 MHz offset		–50	–54	—	
	OFDM					
	At 11 MHz offset		–20	–23	—	
	At 20 MHz offset		–28	–36	—	
	At 30 MHz offset		–40	–55	—	
TTpowup	Time for power up (from synth on)	—	—	1.5	—	µs

[1]Performance is based on the Atheros Reference Design.
[2]Output power variation ±1 dB.
[3]Manufacturing calibration required.
[4]Refer to the design guide for information.

2.2.3 Synthesizer Characteristics

Table 2-6 summarizes the synthesizer characteristics for the AR2317.

Table 2-6. **Synthesizer Composite Characteristics for 2.4 GHz Operation**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pn	Phase noise (at Tx_Out)					dBc/Hz
	At 30 KHz offset		—	–104	—	
	At 100 KHz offset		—	–103	—	
	At 500 KHz offset		—	–115	—	
	At 1 MHz offset		—	–120	—	
F_c	Center channel frequency	Center frequency at 5 MHz spacing See Note [1]	2.312	—	2.484	GHz
F_{ref}	Reference oscillator frequency	± 20 ppm	—	40	—	MHz
F_{step}	Frequency step size (at RF)	See Note	—	1	—	MHz
TS_{powup}	Time for power up (from sleep)	—	—	0.2	—	ms

[1]Frequency is measured at the Tx output.

2.3 Power Consumption

These conditions apply to the following typical characteristics unless otherwise specified:

V_{DD33} = 3.3 V,
T_{amb} = 25 °C

The following table depicts the typical power drain of the on-chip power supply domain as a function of the AR2317's operating mode.

Operating Mode	Unit
3.3 V Supply	280 mA (Rx) 480 mA (Tx)

3. Register Descriptions

This section describes internal registers for the various blocks of the AR2317.

3.1 Reset/Configuration Control Registers

Table 3-1 summarizes the AR2317 Reset/ Configuration registers. These registers use internal base address 0x1100_0000.

Table 3-1. **Reset/Configuration Control Register Summary**

Offset	Name	Description	Page
0x0000	RST_COLD_CTL	Cold reset control	page 16
0x0004	RST_WARM_CTL	Warm reset control	page 16
0x0008	RST_AHB_ARB_CTL	AHB master arbitration control	page 17
0x000C	RST_BYTESWAP_CTL	Byteswap control	page 17
0x0010	RST_NMI_CTL	CPU non-maskable interrupt control	page 18
0x0014	RST_SREV	Silicon revision	page 18
0x0020	RST_MISR	Miscellaneous interrupt status	page 19
0x0024	RST_MIMR	Miscellaneous interrupt mask	page 19
0x0028	RST_GISR	Global interrupt status	page 20
0x0030	RST_GTIME	General timer	page 20
0x0034	RST_GTIME_RELOAD	General timer reload value	page 20
0x0038	RST_WDOG	Watchdog timer	page 21
0x003C	RST_WDOG_CTL	Watchdog timer control	page 21
0x0040	RST_MEMCTL	SDR-DRAM memory controller parameters	page 21
0x0044	RST_CPUPERF_CTL	CPU performance counter control	page 22
0x0048	RST_CPUPERF_0	CPU performance counter 0	page 22
0x004C	RST_CPUPERF_1	CPU performance counter 1	page 23
0x0050	RST_AHBERR0	AHB error status register 0	page 23
0x0054	RST_AHBERR1	AHB error status register 1	page 23
0x0058	RST_AHBERR2	AHB error status register 2	page 24
0x005C	RST_AHBERR3	AHB error status register 3	page 24
0x0060	RST_AHBERR4	AHB error status register 4	page 24
0x0064	RST_PLLC_CTL	CPU/AHB/APB PLL (PLLc) control	page 25
0x006C	RST_CPUCLK_CTL	CPU final clock MUX/divider control	page 26
0x0070	RST_AMBACLK_CTL	AHB/APB final clock MUX/divider control	page 26
0x0088	RST_GPIOIN0	GPIO input, set 0	page 26
0x0090	RST_GPIOOUT0	GPIO output, set 0	page 27
0x0098	RST_GPIODIR0	GPIO direction, set 0	page 27
0x00A0	RST_GPIOINTR	GPIO interrupt control	page 27
0x00A8	RST_SCRATCH0	Scratch register 0	page 28
0x00AC	RST_SCRATCH1	Scratch register 1	page 28
0x00B0	RST_OBS_CTL	Observation control	page 28
0x00B4	RST_MISCCLK_CTL	General clock control	page 29
0x00B8	RST_CIMR	Client interrupt mask	page 29

3.1.1 Cold Reset Control (RST_COLD_CTL)

Offset: 0x0000
Internal Address: 0x1100_0000
Access: Write-only (reads always return 0)
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
0		AHB cold reset. Automatically asserted for 128 clocks on exit from chip reset. Thereafter, writes to this bit perform the following: ■ 0 = No effect ■ 1 = Issue a cold reset to the AHB arbitration and MUXing logic and all connected blocks. Auto-clears after 128 clocks.
1		APB cold reset. Automatically asserted for 128 clocks on exit from chip reset. Thereafter, writes to this bit perform the following: ■ 0 = No effect ■ 1 = Issue a cold reset to the APB arbitration and MUXing logic and all connected blocks. Auto-clears after 128 clocks.
2		CPU cold reset. Automatically asserted for 128 clocks on exit from chip reset. Thereafter, writes to this bit perform the following: ■ 0 = No effect ■ 1 = Issue a cold reset to the MIPS CPU (asserts the CPU's SI_ColdReset and SI_Reset inputs). Auto-clears after 128 clocks.
3		CPU warm reset. Automatically asserted for 128 clocks on exit from chip reset. Thereafter, writes to this bit perform the following: ■ 0 = No effect ■ 1 = Issue a warm reset to the MIPS CPU (asserts the CPU's SI_Reset input). Auto-clears after 128 clocks.
31:4		Reserved

3.1.2 Warm Reset Control (RST_WARM_CTL)

Offset: 0x0004
Internal address: 0x1100_0004
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
0		WMAC warm reset. Resets to 0x1.
1		WBB warm reset. Resets to 0x1.
3:2	RES	Reserved
4		Memory controller warm reset. Resets to 0x0.
6:5	RES	Reserved
7		SPI interface warm reset. Resets to 0x0.
8		UART interface warm reset. Resets to 0x0.
9	RES	Reserved. Resets to 0x0
10		Ethernet interface warm reset. Resets to 0x1.
11		Ethernet MAC warm reset. Resets to 0x1.
31:12	RES	Reserved

3.1.3 AHB Master Arbitration Control (RST_AHB_ARB_CTL)

Offset: 0x0008
Internal address: 0x1100_0008
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected
Notes: Bits [4:0] in this register control whether the associated interface can arbitrate for access to the AHB bus as master. This register does not affect operation of these interfaces as AHB targets. For each bit:

- 0 = Requests for AHB master access from the interface are ignored
- 1 = Requests for AHB master access from the interface process normally.

Bit	Bit Name	Description
0		CPU AHB master arbitration control. Resets to 0x1.
1		WMAC AHB master arbitration control. Resets to 0x0.
2	RES	Reserved
3	res	Reserved
4	res	Reserved
5		Ethernet AHB master arbitration control. Resets to 0x0.
31:6	RES	Reserved

3.1.4 Byteswap Control (RST_BYTESWAP_CTL)

Offset: 0x000C
Internal address: 0x1100_000C
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
0		EC-to-AHB bridge Endianness control. This signal affects how the EC-to-AHB bridge logic handles sub-word-sized reads and writes when acting as AHB master. Resets to 0x0. ■ 0 = EC-to-AHB interface operates in little Endian mode ■ 1 = EC-to-AHB interface operates in big Endian mode
1		WMAC AHB master byteswap control. Resets to CPU_BIG_ENDIAN_RST. See bit [10] of this register. ■ 0 = WMAC AHB master interface does not byteswap data words ■ 1 = WMAC AHB master interface byteswaps data words for both writes and reads
3:2	RES	Reserved
4		Memory controller Endianness control. Resets to 0x0. ■ 0 = The memory controller operates in little Endian mode ■ 1 = The memory controller operates in big Endian mode
5	RES	Reserved
6		Ethernet controller byteswap control. Resets to CPU_BIG_ENDIAN_RST. See bit [10] of this register. ■ 0 = Ethernet controller master interface does not byteswap data words ■ 1 = Ethernet controller byteswaps data words for both writes and reads
8:7	RES	Reserved

Bit	Bit Name	Description
9		CPU write buffer merge mode. Resets to 0x0. ■ 0 = No merge ■ 1 = Full merge
10		CPU Endian control. Resets to 0x1. The reset value of this bit (currently 1), defines the value of the CPU_BIG_ENDIAN_RST parameter referenced as the reset value for various other register fields in the chip. ■ 0 = CPU operates in little Endian mode (CPU's SI_ENDIAN input negated) ■ 1 = CPU operates in big Endian mode (CPU's SI_ENDIAN input asserted)
14:11	RES	Reserved
15		CPU SPI access byteswap control. This bit controls whether the CPU swaps reads and writes to the two AHB SPI regions (AHB addresses 0x0800_0000-0x0FFF_FFFF and 0x1FC0_0000-0x1FFF_FFFF). Resets to CPU_BIG_ENDIAN_RST. See bit [10] of this register. ■ 0 = CPU does not swap SPI read/write data ■ 1 = CPU does swap SPI read/write data
16		CPU DRAM access byteswap control. This bit controls whether the CPU swaps reads and writes to the AHB DRAM region (AHB addresses 0x0000_0000-0x07ff_ffff). Resets to 0x0. ■ 0 = CPU does not swap DRAM read/write data ■ 1 = CPU does swap DRAM read/write data
17	RES	Reserved
18		CPU MMR access byteswap control. This bit controls whether the CPU swaps reads and writes to the AHB MMR regions (AHB addresses 0x1000_0000-0x17FF_FFFF). Resets to 0x0. ■ 0 = CPU does not swap MMR read/write data ■ 1 = CPU does swap MMR read/write data
31:19	RES	Reserved

3.1.5 CPU Non-Maskable Interrupt (NMI) Control (RST_NMI_CTL)

Offset: 0x0010
Internal address: 0x1100_0010
Access: Write-only; reads always return 0x0
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
0		NMI control to CPU. Resets to 0x0. Write of: ■ 0 = No effect ■ 1 = Issues an NMI to the CPU (generates a pulse on the CPU's SI_NMI input)
31:1	RES	Reserved

3.1.6 Silicon Revision (RST_SREV)

Offset: 0x0014
Internal address: 0x1100_0014
Access: Read-only
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
3:0		AR2317 revision level
7:4		AR2317 version level ■ 0x8 = AR2317 1.0 ■ (others) = Reserved
31:8	RES	Reserved

3.1.7 Miscellaneous Interrupt Status (RST_MISR)

Offset: 0x0020
Internal Address: 0x1100_0020
Access: Read/Write-one-to-clear
Cold reset: (See field descriptions)
Warm reset: Unaffected
Notes: Only bits [7:5] are cleared by a write to this register. To clear the other bits, software must clear the interrupt at the associated interface.

Bit	Bit Name	Description
0		UART interrupt pending. Resets to 0x0.
1		Never asserted in the AR2317. Resets to 0x0.
2		SPI interrupt pending. Resets to 0x0.
3		AHB error interrupt pending. Resets to 0x0.
4		APB error interrupt pending. Resets to 0x0
5		General timer interrupt pending. Resets to 0x0.
6		GPIO interrupt pending. Resets to 0x0.
7		Watchdog timer interrupt pending. Resets to 0x0.
8		Never asserted. Resets to 0x0.
31:9	RES	Reserved

3.1.8 Miscellaneous Interrupt Mask (RST_MIMR)

Offset: 0x0024
Internal Address: 0x1100_0024
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
0		UART interrupt mask. Resets to 0x0.
1	RES	Reserved. Resets to 0x0.
2		SPI interrupt mask. Resets to 0x0.
3		AHB error interrupt mask. Resets to 0x0.
4		APB error interrupt mask. Resets to 0x0.
5		General timer interrupt mask. Resets to 0x0.
6		GPIO interrupt mask. Resets to 0x0.
7		Watchdog timer interrupt mask. Resets to 0x0.
8	RES	Reserved. Resets to 0x0.
31:9	RES	Reserved.

3.1.9 Global Interrupt Status (RST_GISR)

Offset: 0x0028
Internal address: 0x1100_0028
Access: Read-only
Cold reset: (See field descriptions)
Warm reset: Unaffected
Notes: This register cannot be written and does not support read-and-clear access. The only way to clear a bit is to clear the underlying interrupt causing the GISR bit to assert.

Bit	Bit Name	Description
0		Miscellaneous interrupt pending. Indicates that the bitwise logical AND of RST_MISR and RST_MIMR is non-zero. Software must read the RST_MISR to determine which miscellaneous interrupts are pending. Connected to bit [0] of the CPU's SI_Int input.
1		WMAC interrupt pending. Indicates that the WMAC is signaling an interrupt. Software must read the WMAC's interrupt-related registers to determine what WMAC interrupts are pending. Connected to bit [1] of the CPU's SI_Int input.
2	RES	Reserved
3	res	Reserved
4		WMAC poll interrupt pending. Indicates that the WMAC has just received a Poll frame and CPU intervention is required to generate a response frame. Software must read the Poll-related WMAC registers to determine how to proceed. Connected to bit [4] of the CPU's SI_Int input.
5		CPU timer interrupt pending. Indicates that the CPU is asserting its SI_TimerInt output because the CPU's cop0 Count register has reached the value stored in the CPU's cop0 Compare register. Software must rewrite the cop0 Compare register to clear this interrupt (see the MIPS32 documentation for more details). Connected to bit [5] of the CPU's SI_Int input.
6		Ethernet interrupt pending. Indicates that the Ethernet interface is signaling an interrupt. Software must read the Ethernet interface's interrupt-related registers to determine which Ethernet interrupts are pending. Connected to bit [2] of the CPU's SI-Int input.
31:6	RES	Reserved

3.1.10 General Timer (RST_GTIME)

Offset: 0x0030
Internal address: 0x1100_0030
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Notes: This register decrements every cycle. When its value reaches zero:

- A general timer interrupt is signaled (see bit [5] of the RST_MISR)
- The register is reloaded with the value of the general timer reload register (RST_GTIME_RELOAD)

Bit	Bit Name	Description
31:0		Current value of general timer. Resets to 0x0.

3.1.11 General Timer Reload Value (RST_GTIME_RELOAD)

Offset: 0x0034
Internal address: 0x1100_0034
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
31:0		Value to be loaded into the general timer register when it reaches zero. Resets to 0x0.

3.1.12 Watchdog Timer (RST_WDOG)

Offset: 0x0038
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected
Notes: This register decrements every cycle. When its value reaches zero, a watchdog interrupt is signaled (see bit [7] of RST_MISR)

Bit	Bit Name	Description
31:0		Current value of watchdog timer. Resets to 0x0.

3.1.13 Watchdog Timer Control (RST_WDOG_CTL)

Offset: 0x003C
Internal address: 0x1100_003C
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
1:0	RES	Reserved
2		Enable AHB error signalling upon watchdog expiration. Resets to 0x0. ■ 0 = Do not signal an AHB error (see bit [2] of the RST_AHBERR0 register) when the watchdog timer expires ■ 1 = Signal an AHB error (see bit [2] of the RST_AHBERR0 register) when the watchdog timer expires.
31:3	RES	Reserved

3.1.14 SDR-DRAM Memory Controller Parameters (RST_MEMCTL)

Offset: 0x0040
Internal address: 0x1100_0040
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
0		Memory controller remap control. Resets to 0x0.
1		Memory controller power down control. Resets to 0x0.
2		Memory controller clear self-refresh/power-down control. Resets to 0x0.
3		SDRAM capture clock select. Resets to 0. ■ 0 = Use delayed hclk (i.e., hclk after being delayed by the coarse and fine delay lines) ■ 1 = Use the SD_CLK_FB pin input from off-chip
31:4	RES	Reserved

3.1.15 CPU Performance Counter Control (RST_CPUPERF_CTL)

Offset: 0x0044
Internal address: 0x1100_0044
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
3:0		Performance counter 0 event select. This field determines the event counted by performance counter 0. Resets to 0x0.
7:4		Performance counter 1 event select. This field determines the event counted by performance counter 1. Uses the same encodings as specified in bits [3:0] of this register for performance counter 0. Resets to 0x3.
8		Performance counter pause. Resets to 0x0. ■ 0 = Both performance counters run normally ■ 1 = Both performance counters hold their values
31:9	RES	Reserved

Value	Event
0	Clock cycles
1	Write buffer pushes without merge
2	Write buffer pushes with merge
3	Instruction completions
4	Instruction cache misses
5	Instruction cache hits
6	Data cache misses
7	Data cache hits
8–15	Reserved

3.1.16 CPU Performance Counter 0 (RST_CPUPERF_0)

Offset: 0x0048
Internal address: 0x1100_0048
Access: Read-and-clear/no write access
Cold reset: (See field descriptions)
Warm reset: Unaffected
Notes: When either CPU performance counter reaches its maximum value, both counters are shifted right by one bit (i.e., divided by 2).

Bit	Bit Name	Description
31:0		Current value of performance counter 0. Read-and-clear access. Resets to 0x0.

3.1.17 CPU Performance Counter 1 (RST_CPUPERF_1)

Offset: 0x004C
Internal address: 0x1100_004C
Access: Read-and-clear/no write access
Cold reset: (See field descriptions)
Warm reset: Unaffected
Notes: When either CPU performance counter reaches its maximum value, both counters shift right by one bit (i.e., divide by two).

Bit	Bit Name	Description
31:0		Current value of performance counter 1. Read-and-clear access. Resets to 0x0.

3.1.18 AHB Error Status Register 0 (RST_AHBERR0)

Offset: 0x0050
Internal address: 0x1100_0050
Access: Special (See field descriptions)
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
0		AHB error indication. Resets to 0x0. Read: ■ 0 = No AHB error has been detected ■ 1 = An AHB error has been detected; other AHB error registers provide more details. Write: ■ 0 = No effect ■ 1 = Clears all bits in this register
1		AHB error overflow indication. Resets to 0x0. Read: ■ 0 = If bit [0] is set, then an AHB error has been detected. However, no additional AHB errors have occurred since detecting and capturing the original error. ■ 1 = An AHB error has been detected, and one or more additional AHB errors were detected before software processed the first error. Writes have no effect.
2		AHB error due to watchdog timer expiration indication. Resets to 0x0. Read: ■ 0 = If bit [0] is set, then an AHB error has been detected and this error was caused by an explicit ERROR response code being observed on the AHB hresp signal. ■ 1 = An AHB error is detected, but the error was implied by watchdog timer expiration rather than by an explicit AHB hresp ERROR response. Probably the AHB bus is hung, as no response is observed on the AHB bus and the watchdog timer eventually expires. Writes have no effect.
31:3	RES	Reserved

3.1.19 AHB Error Status Register 1 (RST_AHBERR1)

Internal address: 0x1100_0054
Access: Read-only
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
31:0	haddr	AHB address for which the error occurred

3.1.20 AHB Error Status Register 2 (RST_AHBERR2)

Offset: 0x0058
Internal address: 0x1100_0058
Access: Read-only
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
31:0	hwdata	AHB write data present when the error occurred

3.1.21 AHB Error Status Register 3 (RST_AHBERR3)

Offset: 0x005C
Internal address: 0x1100_005C
Access: Read-only
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
31:0	hrdata	AHB read data present when the error occurred

3.1.22 AHB Error Status Register 4 (RST_AHBERR4)

Offset: 0x0060
Internal address: 0x1100_0060
Access: Read-only
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
3:0	HMASTER	AHB bus master when the error occurred ■ 0 = Default bus master ■ 1 = WMAC ■ 2 = Ethernet ■ 4:3 = Reserved ■ 5 = CPU ■ 6 = Reserved ■ 7–15 = Undefined
4	HWRITE	AHB write indication when the error occurred ■ 0 = Transaction was a read ■ 1 = Transaction was a write
6:5	HSIZE	AHB transaction size when the error occurred ■ 0 = Byte ■ 1 = Halfword ■ 2 = Word ■ 3 = Reserved
8:7	HTRANS	AHB transaction type when the error occurred ■ 0 = Idle ■ 1 = Reserved ■ 2 = Non-sequential address ■ 3 = Sequential address
11:9	HBURST	AHB burst type when the error occurred ■ 0 = Single beat ■ 1 = Incrementing, unspecified length ■ 2 = WRAP4 ■ 3 = INCR4
31:12	RES	Reserved

3.1.23 CPU/AHB/APB PLL (PLLc) Control (RST_PLLC_CTL)

Offset: 0x0064
Internal address: 0x1100_0064
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
1:0		Reference divider value. Resets to 0. ■ 0 = Sets the value of the PLL 'refdiv' parameter to 1 ■ 1 = Sets the value of the PLL 'refdiv' parameter to 2 ■ 2 = Sets the value of the PLL 'refdiv' parameter to 4 ■ 3 = Sets the value of the PLL 'refdiv' parameter to 5
3:2		Feedback divider value. Because this field specifies the divider value on the feedback path of the PLL, it effectively controls the frequency multiplication performed on the output of the divided-down reference clock. Resets to 25. ■ 0–3 = Reserved ■ 4–31 = Sets the value of the PLL div parameter to the specified value
7		Additional feedback divide-by-2 enable. Resets to 0. ■ 0 = Sets the value of the PLL divby2 parameter to 0 (i.e., enables an additional divide-by-2 in the feedback path) ■ 1 = Sets the value of the PLL divby2 parameter to 1 (i.e., enables an additional divide-by-4 in the feedback path)
13:8	RES	Reserved
16:14		CPU clock final divider select. Resets to 3. ■ 0 = CPU clock output frequency equal to the PLL output frequency divided by 2 ■ 1 = CPU clock output frequency equal to the PLL output frequency divided by 3 (with an unequal duty cycle) ■ 2 = CPU clock output frequency equal to the PLL output frequency divided by 4 ■ 3 = CPU clock output frequency equal to the PLL output frequency divided by 6 ■ 4 = CPU clock output frequency equal to the PLL output frequency divided by 3, with a 50% duty cycle ■ 7:5 = Reserved
18:17	RES	Reserved
19		Power-down enable. Resets to 0. ■ 0 = PLLc operates normally ■ 1 = PLLc is powered down and must not be used as a clock source
22:20		Memory clock final divider select. Resets to 3. ■ 0 = Memory clock output frequency equal to the PLL output frequency divided by 2 ■ 1= Memory clock output frequency equal to the PLL output frequency divided by 3 (with an unequal duty cycle) ■ 2 = Memory clock output frequency equal to the PLL output frequency divided by 4 ■ 3 = Memory clock output frequency equal to the PLL output frequency divided by 6 ■ 4 = Memory clock output frequency equal to the PLL output frequency divided by 3, with a 50% duty cycle ■ 7:5 = Reserved
31:23	RES	Reserved

3.1.24 CPU Final Clock MUX/Divider Control (RST_CPUCLK_CTL)

Offset: 0x006C
Internal address: 0x1100_006C
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected
Notes: The register output drives the proc_clk signal. This signal clocks the MIPS CPU.

Bit	Bit Name	Description
1:0		Input clock select. Resets to 3. ■ 0 = Use PLLc's memory clock as input ■ 1 = Use PLLc's memory clock as input ■ 2 = Use PLLc's CPU clock as input ■ 3 = Use the raw ref_clk as input
3:2		CPU clock divider select. Resets to 0. ■ 0 = CPU clock frequency is equal to the input clock frequency ■ 1 = CPU clock frequency is equal to the input clock frequency divided by 2 ■ 2 = CPU clock frequency is equal to the input clock frequency divided by 4 ■ 3 = CPU clock frequency is equal to the input clock frequency divided by 6
31:4	RES	Reserved

3.1.25 AHB/APB Final Clock MUX/Divider Control (RST_AMBACLK_CTL)

Offset: 0x0070
Internal address: 0x1100_0070
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected
Notes: The output of this register drives the hclk, pclk, and dram_clk signals, which clock the AHB and APB busses, the SDRAM, and all related logic.

Bit	Bit Name	Description
1:0		Input clock select. Resets to 3. ■ 0 = Use PLLc's memory clock as input ■ 1 = Use PLLc's memory clock as input ■ 2 = Use PLLc's CPU clock as input ■ 3 = Use the raw ref_clk as input
3:2		AHB/APB clock divider select. Resets to 0. ■ 0 = AHB/APB clock frequency equal to the input clock frequency ■ 1 = AHB/APB clock frequency equal to the input clock frequency divided by 2 ■ 2 = AHB/APB clock frequency equal to the input clock frequency divided by 4 ■ 3 = AHB/APB clock frequency equal to the input clock frequency divided by 6
31:4	RES	Reserved

3.1.26 GPIO Input, Set 0 (RST_GPIOIN0)

Offset: 0x0088
Internal Address: 0x1100_0088
Access: Read-only
Cold reset: Unaffected
Warm reset: Unaffected

Bit	Bit Name	Description
22:0		Current value of the gpio_in[22:0] signals
31:23	RES	Reserved

3.1.27 GPIO Output, Set 0 (RST_GPIOOUT0)

Offset: 0x0090
Internal Address: 0x1100_0090
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
22:0		Value to drive on the gpio_out[22:0] signals. Resets to 0x0.
31:23	RES	Reserved

3.1.28 GPIO Direction, Set 0 (RST_GPIODIR0)

Offset: 0x0098
Internal Address: 0x1100_0098
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
0		Direction for GPIO[0]. Resets to 0x0. ■ 0 = GPIO[0] is an input ■ 1 = GPIO[0] is an output
1		Direction for GPIO[1]. Resets to 0x0. ■ 0 = GPIO[1] is an input ■ 1 = GPIO[1] is an output
...	...	...
22		Direction for GPIO[22]. Resets to 0x0. ■ 0 = GPIO[22] is an input ■ 1 = GPIO[22] is an output
31:23	RES	Reserved

3.1.29 GPIO Interrupt Control (RST_GPIOINTR)

Offset: 0x00A0
Internal address: 0x1100_00A0
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
5:0		GPIO input select 0. This field selects the first GPIO pin to test for GPIO interrupt assertion. Values of 0–22 are valid. Resets to 0.
7:6		GPIO test select 0. This field determines how the pin selected by bits [5:0] of this register is tested to determine if a GPIO interrupt is signaled. Resets to 0. ■ 0 = Pin never generates a GPIO interrupt ■ 1 = GPIO interrupt generated when pin is low ■ 2 = GPIO interrupt generated when pin is high ■ 3 = GPIO interrupt generated when pin changes state (high-to-low or low-to-high)
13:8		GPIO input select 1. This field selects the second GPIO pin to test for GPIO interrupt assertion. Values from 0-22 are valid. Resets to 0.
15:14		GPIO test select 1. This field determines how the pin selected by bits [13:8] of this register is tested to determine if a GPIO interrupt is signaled. Resets to 0. ■ 0 = Pin never generates a GPIO interrupt ■ 1 = GPIO interrupt generated when pin is low ■ 2 = GPIO interrupt generated when pin is high ■ 3 = GPIO interrupt generated when pin changes state (high-to-low or low-to-high)
31:16	RES	Reserved

3.1.30 Scratch Register 0 (RST_SCRATCH0)

Offset: 0x00A8
Internal address: 0x1100_00A8
Access: Read/Write
Cold reset: Unaffected
Warm reset: Unaffected
Notes: For software use

Bit	Bit Name	Description
31:0		Scratch register value. Unaffected by any reset.

3.1.31 Scratch Register 1 (RST_SCRATCH1)

Offset: 0x00AC
Internal address: 0x1100_00AC
Access: Read/Write
Cold reset: Unaffected
Warm reset: Unaffected
Notes: For software use

Bit	Bit Name	Description
31:0		Scratch register value. Unaffected by any reset.

3.1.32 Observation Control (RST_OBS_CTL)

Offset: 0x00B0
Internal address: 0x1100_00B0
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
12:0	RES	Reserved
14:13		Rx_Clear/CPU clock/GPIO[3] control. Resets to 0. ■ 0 = GPIO[3] used as GPIO ■ 1 = Reserved ■ 2 = GPIO[3] used to output CPU clock ■ 3 = Reserved
15		LED[0]/GPIO[1] control. Resets to 0. ■ 0 = GPIO[1] used as a GPIO ■ 1 = GPIO[1] used to output LED[0]. This bit has priority over bit 8.
16		LED[1]/GPIO[2] control. Resets to 0. ■ 0 = GPIO[2] used as a GPIO ■ 1 = GPIO[2] used to output LED[1]. This bit has priority over bit 8.
17	RES	■ Reserved
18		BTActive/GPIO[7] control. Resets to 0. ■ 0 = GPIO[7] used as a GPIO ■ 1 = Reserved
31:19	RES	Reserved

3.1.33 General Clock Control (RST_MISCCLK_CTL)

Offset: 0x00B4
Internal address: 0x1100_00B4
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
0		pllbypass. Resets to 1. ■ 0 = pllbypass disabled ■ 1 = pllbypass enabled
1		proc_clk_sel. Resets to 0. ■ 0 = ref_clk is the source of ref_clk referred to in the description of RST_CPUCLK_CTL ■ 1 = Reserved
31:2	RES	Reserved

3.1.34 Client Interrupt Mask (RST_CIMR)

Offset: 0x00B8
Internal address: 0x1100_00B8
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected
Notes: Unlike other interrupt mask registers, all bits in this register reset to 1 rather than to 0.

Bit	Bit Name	Description
0		Miscellaneous interrupt pending mask. Resets to 1.
1		WMAC interrupt pending mask. Resets to 1.
2		Ethernet interrupt pending mask. Resets to 1.
3	RES	Reserved
4		WMAC poll interrupt pending mask. Resets to 1.
5		CPU timer interrupt pending mask. Resets to 1.
31:6	RES	Reserved

3.1.35 PLL Programming Notes

The AR2317 system logic contains one PLL (PLLc), which generates the CPU clock, the AHB/APB clock, and the SDRAM clock. The PLL takes as input the 40 MHz reference clock (ref_clk), which proceeds through three conceptual stages.

After the PLL, an additional divider stage takes the vcoout output from the PLL and divides it for use in the rest of the system. PLLc vcoout output is fed into two dividers to yield two outputs, memory clock and CPU clock. See Figure 3-1.

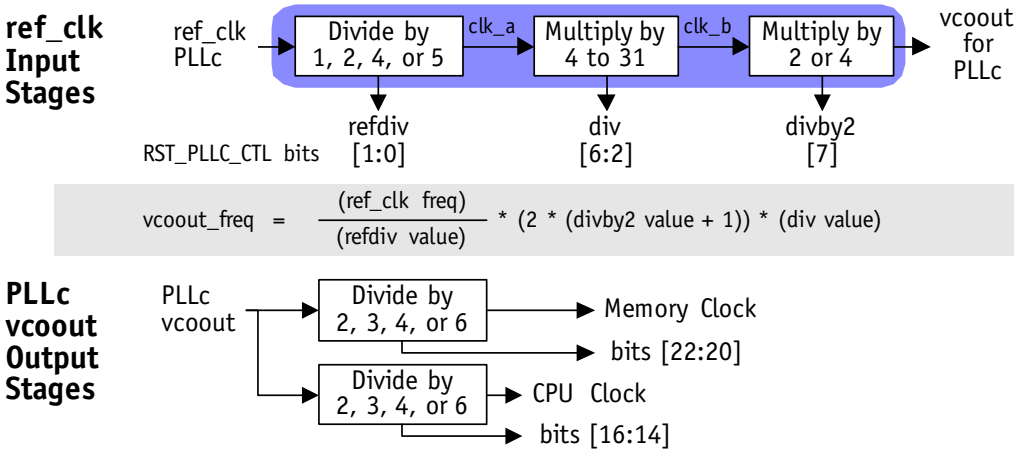


Figure 3-1. **Ref_clk and PLLc vcoout Stages**

From the PLL, the CPU clock and memory clock outputs feed into an additional set of clock MUXes/dividers to generate the on-chip clocks. For all clocks, each final MUX/divide module is identical. See Figure 3-2.

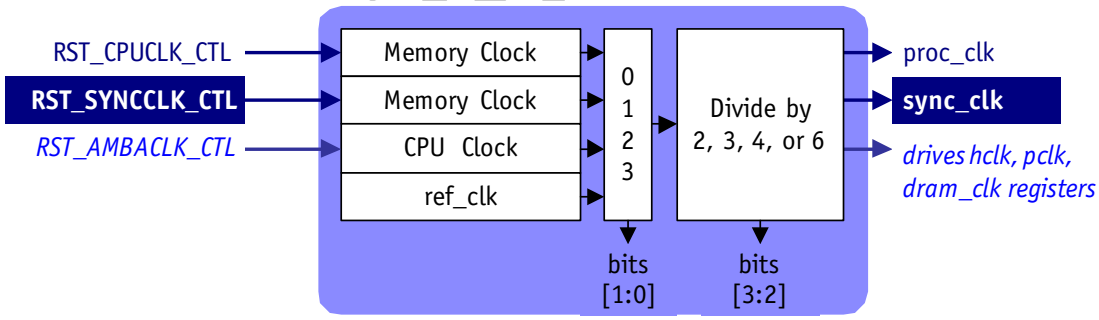


Figure 3-2. **Final Clock Divider**

3.2 SDR-DRAM Controller Registers

Table 3-2 summarizes the SDR-DRAM registers for the AR2317. These registers use the internal base address: 0x1030_0000.

Table 3-2. **SDR-DRAM Register Summary**

Offset	Name	Description	Page
0x0000	MEMCTL_SCONR	SDR-DRAM configuration register	page 31
0x0004	MEMCTL_STMG0R	SDR-DRAM timing register 0	page 32
0x0008	MEMCTL_STMG1R	SDR-DRAM timing register 1	page 32
0x000C	MEMCTL_SCTLR	SDR-DRAM control register	page 33
0x0010	MEMCTL_SREFR	SDR-DRAM refresh interval register	page 33

3.2.1 SDR-DRAM Configuration Register (MEMCTL_SCONR)

Offset: 0x0000
Internal address: 0x1030_0000
Access: Read/Write
Warm reset: Unaffected

Bit	Bit Name	Description
2:0	RES	Reserved
4:3	S_BANK_ADDR _WIDTH	Specifies the number of bank address bits. ■ 0–3 = Correspond to 1–4 bits (thus select 2–16 banks)
8:5	S_ROW_ADDR _WIDTH	Specifies the number of address bits for the row address: ■ 10–15 = Correspond to 11–16 bits ■ 0–10= Reserved
12:9	S_COL_ADDR _WIDTH	Specifies the number of address bits for the column address: ■ 15 = Reserved ■ 7–14= Correspond to 8–15 bits ■ 0–6 = Reserved
14:13	S_DATA_WIDTH	Specifies SDRAM data width in bits for DDR_SDRAM: ■ 00 = 8 bits ■ 01 = 16 bits ■ 10 = 32 bits ■ 11 = 64 Bits For all other SDRAMs, ■ 00 = 16 bits ■ 01 = 32 bits ■ 10 = 64 bits ■ 11 = 128 bits
31:15	RES	Reserved

3.2.2 SSDR-DRAM Timing Register 0 (MEMCTL_STMG0R)

Offset: 0x0004
Internal address: 0x1030_0004
Access: Read/Write
Warm reset: Unaffected

Bit	Bit Name	Description
26, 1:0	CAS_LATENCY	Delay in clock cycles between read command and availability of first data. ■ 0 = 1 clock ■ 1 = 2 clocks ■ 2 = 3 clocks ■ 3 = 4 clocks ■ 7:4 = Reserved
5:2	T_RAS_MIN	Minimum delay between active and precharge commands. Values of 0–15 correspond to T_RAS_MIN of 1-16 clocks.
8:7	T_RCD	Minimum delay between active and read/write commands. Values 0–7 correspond to T_RCD values of 1–8 clocks.
11:9	T_RP	Precharge period. Values of 0–7 correspond to T_RP of 1–8 clocks.
13:12	T_WR	For writes, delay from last data in to next precharge command. Values 0–3 correspond to T_WR of 1–4 clocks.
17:14	T_RCAR	Auto-refresh period. Minimum time between two auto-refresh commands. Values 0–15 correspond to T_RCAR of 1-16 clocks.
21:18	T_XSR	Exits self-refresh to active or auto-refresh command time. Minimum time controller should wait after taking SDRAM out of self-refresh mode before issuing any active or auto-refresh commands. Values of 1–512 correspond to T_XSR of 1–512 clocks.
25:22	T_RC	Specifies the active-to-active command period. Values of 0–15 correspond to the T_RC of 1–16 clocks.
31:27	T_XSR / EXTENDED_T_XSR	Exits self-refresh to active or auto-refresh command time. Minimum time controller should wait after taking SDRAM out of self-refresh mode before issuing any active or auto-refresh commands. Values of 1–512 correspond to T_XSR of 1–512 clocks.

3.2.3 SDR-DRAM Timing Register 1 (MEMCTL_STMG1R)

Offset: 0x0008
Internal address: 0x1030_0008
Access: Read/Write
Warm reset: Unaffected

Bit	Bit Name	Description
15:0	T_INIT	Specifies the number of clock cycles to hold SDRAM inputs stable after power up, before issuing any commands.
19:16	NUM_INIT_REF	Specifies the number of auto-refreshes during initialization. Values of 0–15 correspond to 1–16 auto-refreshes.
31:20	RES	Reserved

3.2.4 SDR-DRAM Control Register (MEMCTL_SCTLR)

Access: Read/Write
Warm reset: Unaffected

Offset: 0x000C
Internal address: 0x1030_000C

Bit	Bit Name	Description
0	INITIALIZE	Forces the memory controller to initialize the SDRAM. The memory controller resets this bit to 0 once the initialization sequence completes.
1	SELF_REFRESH / DEEP_POWER_MODE	Forces the memory controller to put the SDRAM in self-refresh mode. Bit can clear after writing to this bit or with the CLEAR_SR_DP pin, generated by external power management unit.
2	POWER_DOWN _MODE	Forces the memory controller to put the SDRAM in power-down mode.
3	PRECHARGE _ALGORITHM	Determines when a row is precharged: ■ 1 = Delayed precharge; the row stays open after read/write operations ■ 0 = Immediate precharge; the row precharges after read/write operation
4	FULL_REFRESH _BEFORE_SR	Controls the number of refreshes done by the memory controller before the SDRAM is put into self-refresh mode: ■ 1 = Refresh all rows before entering self-refresh mode ■ 0 = Refresh only one row before entering self-refresh mode
5	FULL_REFRESH _AFTER_SR	Controls the number of refreshes done by the memory controller after the SDRAM is taken out of self-refresh mode: ■ 1 = Refresh all rows before entering self-refresh mode ■ 0 = Refresh only one row before entering self-refresh mode
8:6	READ_PIPE	Indicates the number of registers inserted in the read data path for the SDRAM to correctly latch data. Values of 0–7 indicate 0–7 registers.
9	SET_MODE_REG	If set to 1, forces controller to update the SDRAM mode register. The controller clears this bit once it has finished updating the mode register.
10	RES	Reserved
11	SELF_REFRESH _STATUS	Read only. If set to 1, indicates the SDRAM is in self-refresh mode. If self_refresh/deep_power_mode bit (SCTLR bit 1) is set, it may take time before SDRAM enters self-refresh mode, depending on whether all or one row refreshes before entering as defined by the bit FULL_REFRESH_BEFORE_SR. Ensure this bit is set before gating clock in self-refresh mode.
16:12	NUM_OPEN_BANKS	Specifies the number of SDRAM internal banks to be open at any time. Values of 0–15 correspond to 0–15 banks open.
17	S_RD_READY_MODE	SDRAM read-data-ready mode. If set to 1, indicates the SDRAM read data is sampled after S_RD_READY goes active.
18	EXN_MODE_REG _UPDATE	Commands the controller to update the Mobile-SDRAM extended-mode register. Once the update is done, the controller automatically clears the bit.
31:19	RES	Reserved

3.2.5 SDR-DRAM Refresh Interval Register (MEMCTL_SREFR)

Offset: 0x0010
Internal address: 0x1030_0010
Access: Read/Write
Warm reset: Unaffected

Bit	Bit Name	Description
15:0	T_REF	Specifies the number of clock cycles between consecutive refresh cycles.
31:16	RES	Reserved

3.3 UART Registers

Table 3-3 summarizes the UART registers for the AR2317. These registers use the internal base address 0x1110_0000.

Table 3-3. **UART Register Summary**

Offset	Name	Description	Page
0x0000	UART_RBR	Receive buffer	page 34
	UART_THR	Transmit holding	page 34
	UART_DLL	Divisor latch low	page 34
0x0004	UART_IER	Interrupt enable	page 34
	UART_DLH	Divisor latch high	page 34
0x0008	UART_IIR	Interrupt identity	page 35
	UART_FCR	FIFO control	page 35
0x000C	UART_LCR	Line control	page 35
0x0010	UART_MCR	Modem control	page 36
0x0014	UART_LSR	Line status	page 36
0x0018	UART_MSR	Modem status	page 37
0x001C	UART_SCR	Scratch	page 37

3.3.1 Receive Buffer Register (UART_RBR); Transmit Holding Register (UART_THR); Divisor Latch Low Register (UART_DLL)

Offset: 0x0000
Internal address: 0x1110_0000
Access: (Varies)
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
7:0	Address	Specifies address of receive buffer 0. This must be word aligned.
31:8	RES	Reserved

3.3.2 Interrupt Enable Register (UART_IER); Divisor Latch High (UART_DLH)

Offset: 0x0004
Internal address: 0x1110_0004
Access: (Varies)
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
7:0		The UART_DLH register with DLL forms a 16-bit, read/write, Divisor Latch register that contains the UART baud rate divisor. It is accessed by first setting DLAB bit [7] in the "Line Control Register (UART_LCR)". The output baud rate is: baud = (clock frequency)/(16 * divisor) UART_IER is a read/write register containing bits that enable generation of interrupts: ■ Enable Received Data Available (ERBFI) ■ Enable Transmitter Holding Register Empty (ETBEI) ■ Enable Receive Line Status (ELSI) ■ Enable Modem Status (EDSSI)
31:8	RES	Reserved

3.3.3 Interrupt Identity Register (UART_IIR); FIFO Control Register (UART_FCR)

Offset: 0x0008
Internal address: 0x1110_0008
Access: (Varies)
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
7:0		This is a read-only register that identifies the source of an interrupt. Table 3-4 summarizes details of interrupt operation
31:8	RES	Reserved

Table 3-4. **UART Interrupt Control Functions**

Identification Register			Interrupt Set and Reset Function			
Bit 2	Bit 1	Bit 0	Priority	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	1	—	None	None	—
1	1	0	Highest	Receiver line status	Overrun/parity/ framing errors or break interrupt	Reading line status register
1	0	0	Second	Received data available	Receiver data available or read data FIFO trigger level reached	Reading receiver buffer register or the FIFO drops below the trigger level
0	1	0	Third	Transmitter holding register empty	Transmitter holding register empty	Reading IIR register (if source of interrupt) or writing into THR
0	0	0	Fourth	MODEM status	Clear to send, data set ready, ring indicator, or data center detect	Reading MODEM status register

3.3.4 Line Control Register (UART_LCR)

Offset: 0x000C
Internal address: 0x1110_000C
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
1–0	CLS	Controls the number of bits per character in each transmitted or received serial character.
2	STOP	Controls the number of stop bits in each transmitted or received serial character.
3	PEN	Parity Enable. When set, parity is enabled.
4	EPS	Even Parity Select. If parity is enabled, this bit selects between even and odd parity. If set to a logic 1, an even number of logic 1s is transmitted or checked. If set to a logic 0, an odd number of logic 1s is transmitted or checked.
5	Stick Parity	Not Used.
6	Break	Setting this bit sends a break signal by holding the sout line low (when not in Loopback Mode, as determined by "Modem Control Register (UART_MCR)" bit 4, until the Break bit clears. In Loopback Mode, the break condition is internally looped back to the receiver.
7	DLAB	Divisor Latch Access. Setting this bit enables reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup to access other registers.
31:8	RES	Reserved

3.3.5 Modem Control Register (UART_MCR)

Offset: 0x0010
Internal address: 0x1110_0010
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
0	DTR	Drives UART output DTR_L
1	RTS	Drives UART output RTS_L
2	OUT 1	Drives UART output U0_OUT1_L
3	OUT 2	Drives UART output U0_OUT2_L
4	LOOPBACK	When set, data on the sout line is held HIGH, while serial data output loops back to the S-in line, internally. In this mode all interrupts are fully functional.
7–5	RES	Must be filled with 0
31:8	RES	Reserved

3.3.6 Line Status Register (UART_LSR)

Offset: 0x0014
Internal address: 0x1110_0014
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
0	DR	Data Ready. When set, this bit indicates the receiver contains at least one character in the RBR. This bit is cleared when the RBR is read.
1	OE	Overrun Bit. When set, this bit indicates an overrun error has occurred because a new data character was received before the previous data was read. The OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten.
2	PE	Parity Error. This bit is set whenever there is a parity error in the receiver if the parity enable (PEN) bit in the "Line Control Register (UART_LCR)" is set.
3	FE	Framing Error. This bit is set whenever there is a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. The OE, PE and FE bits are reset when a read of this register is performed.
4	BI	Break Interrupt. This bit is set whenever the serial input (SIN) is held in a logic 0 state for longer than the sum of *start time* + *data bits* + *parity* + *stop bit*s. A break condition on `sin` causes one and only one character, consisting of all zeros, to be received by the UART. Reading the Line Status register clears the BI bit.
5	THRE	Transmitter Holding Register Empty. When set, this bit indicates the UART can accept a new character for transmission. This bit is set whenever data is transferred from the THR to the transmitter shift register and no new data has been written to the THR. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled.
6	TEMT	Transmitter Empty. This bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty.
7	FERR	FIFO Receiver Error. This bit is only active when FIFOs are enabled. It is set when there is at least one parity error, framing error, or break indication in the FIFO. This bit clears when the LSR is read, the character with the error is at the top of the receiver FIFO, and there are no subsequent errors in the FIFO. (Not supported.)
31:8	RES	Reserved

3.3.7 Modem Status Register (UART_MSR)

Offset: 0x0018
Internal address: 0x1110_0018
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Bit	Bit Name	Description
0	DCTS	Records whether the modem control line CTS_L has changed since the last time the CPU read the register
1	DDSR	Records whether the modem control line DSR_L has changed since the last time the CPU read the register
2	TERI	Indicates RI_L has changed since the last time the CPU read the register
3	DDCD	Records whether the modem control line DCD_L has changed since the last time the CPU read the register
4	CTS	Contains information on the current state of the modem control lines. CTS is the compliment of CTS_L
5	DSR	Contains information on the current state of the modem control lines. CTS is the compliment of DSR_L
6	RI	Contains information on the current state of the modem control lines. CTS is the compliment of RI_L
7	DCD	Contains information on the current state of the modem control lines. CTS is the compliment of DCD_L
31:8	RES	Reserved

3.3.8 Scratch Register (UART_SCR)

Offset: 0x001C
Internal address: 0x1110_001C
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: Unaffected

Notes: This register is an 8-bit read/write register for programmers to use as a temporary storage space.

Bit	Bit Name	Description
7:0	RES	Unused
31:8	RES	Reserved

3.4 SPI Flash Interface Registers

Table 3-5 summarizes the SPI flash interface registers for the AR2317. These registers use Internal base address 0x1130_0000.

Table 3-5. **SPI Flash Interface Register Summary**

Offset	Name	Description	Page
0x0000	SPI_CS	SPI control/status	page 38
0x0004	SPI_AO	SPI address/opcode	page 39
0x0008	SPI_D	SPI data	page 39

3.4.1 SPI Control/Status (SPI_CS)

Offset: 0x0000
Internal address: 0x1130_0000
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)

Bit	Bit Name	Description
3:0		Tx byte count. Determines the number of bytes transmitted from the AR2317 to the SPI device. Values of 1–8 are valid, other values are illegal. Resets to an undefined value.
7:4		Rx byte count. Determines the number of bytes received from the SPI device into the AR2317. Values of 0–8 are valid, other values are illegal. Resets to an undefined value.
8		SPI transaction start. Only writes to this field are meaningful; reads always return 0. Resets to 0x0. Writes: ■ 0 = No effect ■ 1 = Starts SPI transaction defined by the Tx byte count, Rx byte count, SPI_AO, and SPI_D registers.
15:9	RES	Reserved
16		Transaction busy indication. Read-only; writes to this bit are ignored. Resets to 0x0. ■ 0 = No SPI transaction is ongoing. Software may start a new SPI transaction by writing to the SPI transaction start bit within this register. ■ 1 = An SPI transaction presently is underway. Software must not try to start a new SPI transaction. Software may not alter the value of any field of the SPI_CS, SPI_AO, or SPI_D registers.
18:17		Automatically-determined SPI address size. Read-only; writes to this bit are ignored. Resets to an undefined value, but then updates after the autosizing process completes. ■ 0 = SPI address size is 16 bits ■ 1 = SPI address size is 24 bits ■ 2 = Reserved ■ 3 = Automatic SPI address size determination failed. Typical because: – The SPI device is missing – The SPI device is unprogrammed – The SPI device is programmed with an incorrect SPI_MAGIC value
20:19		SPI autosize override. Resets to 0x0. ■ 0 = Use automatically-determined SPI address size (see bits [18:17]) ■ 1 = Force SPI address size to 16 bits ■ 2 = Force SPI address size to 24 bits ■ 3 = Reserved
23:21	RES	Reserved
25:24		SPI clock frequency select. Resets to 0x11. ■ 0 = SPI clock frequency is proc_clk/8 ■ 1 = SPI clock frequency is proc_clk/16 ■ 2 = SPI clock frequency is proc_clk/32 ■ 3 = SPI clock frequency is proc_clk/64
31:26	RES	Reserved

3.4.2 SPI Address/Opcode (SPI_A0)

Offset: 0x0004
Internal address:
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)

Bit	Bit Name	Description
7:0		SPI opcode. Usually this field specifies the 8-bit opcode (instruction) to transmit to the SPI device as the first part of an SPI transaction.
31:8		Address. Usually this field specifies the 24-bit address to transmit to the SPI device.

3.4.3 SPI Data (SPI_D)

Offset: 0x0008
Internal address: 0x1130_0008
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Same as cold reset)

Bit	Bit Name	Description
31:0		SPI data. This register usually specifies a series of up to four data bytes to transmit to or receive from the SPI device. Resets to an undefined value.

3.4.4 SPI Register Notes

An SPI transaction has three phases: an opcode transmit phase (always a single byte), followed by an optional address 0-3 byte transmit phase and optional 0-4 byte data transmit or receive phase. Thus an SPI transaction is a 1- to 8-byte transmit phase from the AR2317 to the SPI device followed by a 0- to 8-byte receive phase from the SPI device into the AR2317.

The SPI_CS register transmit byte count field controls the size (in bytes) of the transmit phase. Each transmitted byte's source is fixed.

Table 3-6. **SPI_CS Transmitted Byte Source**

Byte	Source
0	SPI_AO[7:0] (SPI opcode field)
1	SPI_AO[31:24] (high byte of the SPI address field)
2	SPI_AO[23:16] (middle byte of the SPI address field)
3	SPI_AO[15:8] (low byte of the SPI address field)
4	SPI_D[7:0] (low byte of the SPI data register)
5	SPI_D[15:8] (next byte of the SPI data register)
6	SPI_D[23:16] (next byte of the SPI data register)
7	SPI_D[31:24] (high byte of the SPI data register)

The SPI_CS register receive byte count field controls the size (in bytes) of the receive phase. Each received byte's source is fixed.

Table 3-7. **SPI_CS Received Byte Source**

Byte	Source
0	SPI_D[7:0] (low byte of the SPI data register)
1	SPI_D[15:8] (next byte of the SPI data register)
2	SPI_D[23:16] (the byte of the SPI data register)
3	SPI_D[31:24] (high byte of the SPI data register)
4	SPI_AO[7:0] (SPI opcode field)
5	SPI_AO[15:8] (low byte of the SPI address field)
6	SPI_AO[23:16] (middle byte of the SPI address field)
7	SPI_AO[31:24] (high byte of the SPI address field)

1. Write appropriate values to the SPI_AO and SPI_D registers.
2. Write appropriate values into the transmit byte count and received byte count fields of the SPI_CS register.
3. Write a 1 to the SPI transaction SPI_CS register start bit (can combine with step 2).
4. To poll: poll the transaction busy indication bit in the SPI_CS register until set, indicating the SPI transaction is complete.
5. If a receive phase is included, retrieve the received data by reading the appropriate bytes from the SPI_D and SPI_AO registers.

4. Package Dimensions

The AR2317 is packaged in a JEDEC M0-207 compliant 260 package. The body size is 12 mm by 12 mm. The BGA package drawings and dimensions are provided in Figure 4-1, and Table 4-1.

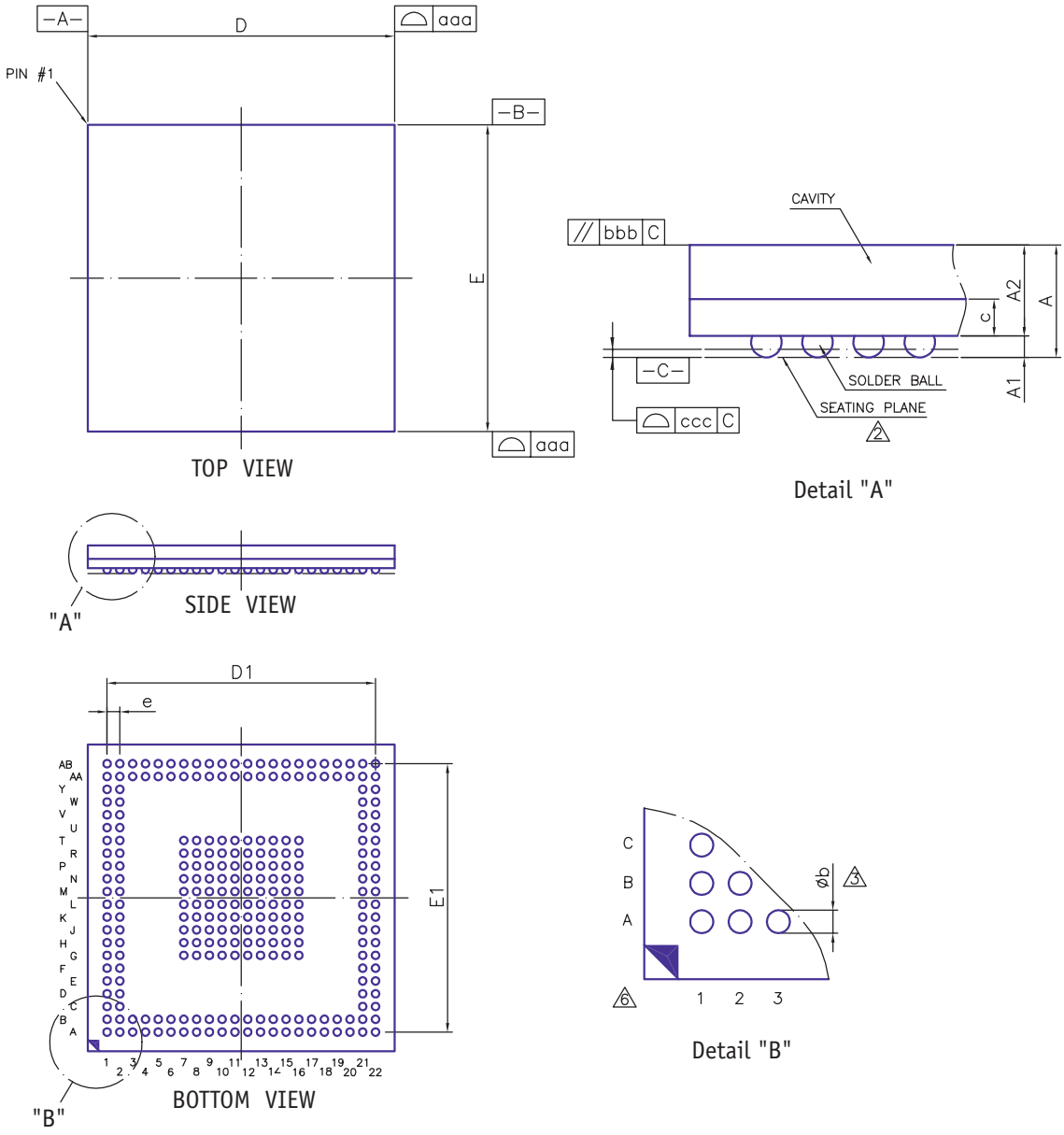


Figure 4-1. **BGA Package Views**

Table 4-1. **BGA Package Dimensions**

Dimension Label	Min	Nom	Max	Unit	Min	Nom	Max	Unit
A	—	—	1.20	mm	—	—	0.047	inches
A1	0.16	0.21	0.26	mm	0.006	0.008	0.010	inches
A2	0.84	0.89	0.94	mm	0.033	0.035	0.037	inches
c	0.32	0.36	0.40	mm	0.013	0.014	0.016	inches
D	11.90	12.00	12.10	mm	0.469	0.472	0.476	inches
E	11.90	12.00	12.10	mm	0.469	0.472	0.476	inches
D1	—	10.50	—	mm	—	0.413	—	inches
E1	—	10.50	—	mm	—	0.413	—	inches
e	—	0.50	—	mm	—	0.020	—	inches
b	0.25	0.30	0.35	mm	0.010	0.012	0.014	inches
aaa		0.15		mm		0.006		inches
bbb		0.20		mm		0.008		inches
ccc		0.08		mm		0.003		inches
ddd		0.15		mm		0.006		inches
eee		0.05		mm		0.002		inches
MD/ME		22/22		mm		22/22		inches

Notes:
1. The controlling dimension is mm.
2. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
3. Dimension b is measured at the maximum solder ball diameter, parallel to datum plane C.
4. There shall be a minimum clearance of 0.25 mm between the edge of the solder ball and the body edge.
5. Reference document: JEDEC MO-207
6. The pattern of pin 1 fiducial is for reference only.
7. Special characteristics for C class: bbb, ccc.

5. Ordering Information

The order number AR2317-AC1A specifies a BGA, lead-free, standard temperature range version of the AR2317.

The order number AR2317-AC0A specifies a current version of the AR2317.

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Document Number: 981-00030-001 MKG-0257 Rev. 1

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