PRELIMINARY
April 2008

AR6002 ROCm™ Single-Chip MAC/BB/Radio for 2.4/5 GHz Embedded WLAN Applications

General Description

The Atheros AR6002 is the 2nd generation of the WLAN ROCm family. Building on the advanced performance and features of the AR6001 family, the compact size and low power consumption of this single chip design make it an ideal vehicle for adding WLAN to hand-held and other battery-powered consumer electronic devices. Both IEEE 802.11g (2.4 GHz) and 802.11a (5 GHz) standards are supported by the AR6002 family. The AR6002 supports both SDIO 1.1 and GSPI host interfaces.

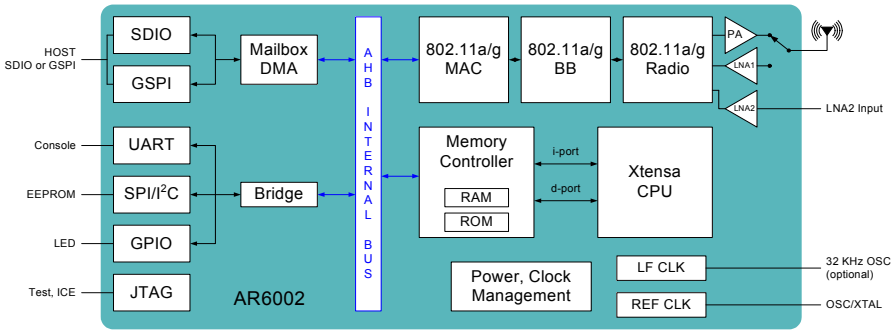
The AR6002 family includes a highly integrated, front-end module ((Power Amplifier, Low-Noise Amplifier and RF switch), enabling low-cost designs with minimal external components. The RF performance, data throughput, and power consumption further improve upon the performance of the AR6001 family. Advanced architecture and protocol techniques save power during sleep, stand-by and active states.

Fast antenna diversity is also supported, allowing optimal antenna selection on a per-packet basis. The AR6002 family supports 2, 3 and 4 wire Bluetooth coexistence protocols with advanced algorithms for predicting channel usage by the co-located Bluetooth transceiver.

The AR6002 family provides multiple peripheral interfaces including UART, SPI, I^2C and 18 GPIO pins. All internal clocks are generated from a single external crystal/oscillator. A variety of reference clocks are supported which include 19.2, 24, 26, 38.4, 40 and 52 MHz. AR6002 chips are available in Wafer Level Chip Scale Packages (WLCSP) or Ball Grid Arrays (BGA) packaging .

AR6002 Features

- All-CMOS IEEE 802.11a/b/g or 802.11b/g single-chip client
- Integrated PA, LNA and RF switch minimizing external component count
- Data rates of 1–54 Mbps for 802.11g, 6-54 Mbps for 802.11a
- Advanced power management to minimize standby, sleep and active power
- Host interface support for SDIO and GSPI
- Security support for WPS, WPA2, WPA, WAPI and protected management frames
- Support for 2.4 and 5 GHz operation in all available bands in all regulatory domains
- Full 802.11e QoS support including WMM and U-APSD
- Standard 2, 3 and 4 wire Bluetooth coexistence handshake support
- IEEE 1149.1, JTAG, test access port and boundary scan
- 18 fully-programmable GPIO pins
- 16550-compliant UART
- SPI or I^2C for EEPROM support
- Internally generated low-frequency oscillator for low-power sleep
- Available in 7 x 7 mm BGA package with 0.5 mm pitch or WLCSP package with 0.4 mm pitch



AR6002 System Block Diagram

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1. Functional Description

1.1 Overview

The AR6002 is a single chip 802.11 (a, b, g) device based on the cutting edge technology. The AR6002 has large internal RAM which precludes the need for external memory. It contains a dual-band radio, a MAC, a CPU, power management functions, and other functions. Its internal logic and boot code are designed to detect the presence of an external host and to automatically begin communicating with that host. The supported Host interfaces are SDIO and GSPI (Generic SPI). See the AR6002 block diagram on page 1.

The XTENSA CPU communicates directly with the RAM and ROM modules within the device without any caching. Boot code in the ROM first detects the presence of an external host. It then begins communicating with this host. The host then downloads additional code into the RAM which the XTENSA CPU can later execute.

The AR6002 supports a total of 18 GPIOs. Some of these GPIOs are shared with the UART interface as well as the SI block. The SI block supports both I^2C as well as SPI interfaces and can be used to communicate with external serial devices such as EEPROMs or programmable oscillators.

1.2 XTENSA CPU

At the heart of the chip is the XTENSA CPU. This CPU has four interfaces:

- The Code RAM/ROM interface (iBus), going to the Virtual Memory Controller (VMC).
- The Data RAM Interface (dBus), going to the VMC
- The AHB interface which has been translated from the CPU's internal XTENSA Local Memory Interface (XLMI) bus. This is used mainly for register accesses.
- JTAG interface for debugging

1.3 Virtual Memory Controller (VMC)

The VMC contains 80 kBytes of ROM and 184 kBytes of RAM. It has three interfaces:

- iBus,
- dBus, and
- AHB interface.

Any one of these interfaces can request access to the ROM or RAM modules within the VMC. The VMC contains arbiters to serve these three interfaces on a first-come-first-serve basis.

1.4 AHB and APB Blocks

The AHB block acts as an arbiter. It has AHB interfaces from three Masters:

- MAC,
- MBOX (from the Host), and
- CPU.

See below for more on the MBOX and MAC. Depending upon the address, the AHB data request can go into one of the two slaves: APB block or the VMC. Data requests to the VMC are generally high-speed memory requests, while requests to the APB block are primarily meant for register access.

The APB block acts as a decoder. It is meant only for access to programmable registers within the AR6002's main blocks. Depending upon the address, the APB request can go to one of the eight places listed below:

- RF Interface (APB serial block)
- VMC
- SI/SPI
- MBOX
- GPIO
- UART
- Real Time Clock (RTC), or
- MAC/BB

The AR6002 RF module has a long-shift interface which allows the CPU to directly control its registers via APB access. Hence the APB block converts 32-bit APB reads and writes by the CPU into serial transfers to the RF module.

1.5 Master SI/SPI Control

The AR6002 has a master serial interface (SI) that can operate in two, three, or four-wire bus configurations to control EEPROMs or other I2C/SPI devices. Multiple I2C devices with different device addresses are supported by sharing the two-wire bus. Multiple SPI devices are supported by sharing the clock and data signals and using separate software-controlled GPIO pins as chip selects.

An SI transaction consists of two phases: a data transmit phase of 0-8 bytes followed by a data receive phase of 0-8 bytes. The flexible SI programming interface allows software to support various address and command configurations in I2C/SPI devices. In addition, software may operate the SI in either polling or interrupt mode.

1.6 GPIO

The AR6002 has 17 GPIO pins with direct software access. Many are multiplexed with other functions such as UART, SI, and Bluetooth coexistence (see Section 6 for details).

Each GPIO supports the following configurations via software programming:

- Input available for sampling by a software register
- Input triggering an edge or level CPU interrupt
- Input triggering a level chip wakeup interrupt
- Open-drain or push-pull output driver
- Output source from a software register or the Sigma Delta Pulse-width Modulation (PWM) DAC In addition, different sets of GPIO pins have internal pull-up/down options that are software configurable.

The AR6002 has one Sigma Delta PWM DAC shared by all of the GPIO pins. It allows the GPIO pins to drive intermediate output voltage levels for functions such as LED dimming. The DAC has a period of 256 samples with a configurable number of clock cycles per sample. By programming a register, software can control the duty cycle of the Sigma Delta PWM DAC, approximating an intermediate voltage level.

1.7 LEDs

The AR6002 can drive LEDs using GPIO pins. An external NPN transistor can provide higher power drive. Note that the LED connects to the battery voltage. For multiple LED groups, multiple GPIOs can be assigned. The GPIO Sigma Delta PWM DAC can provide a continuous dimmer function.

1.8 MBOX

The MBOX is a service module to handle one of two possible external hosts: SDIO or GSPI. The AR6002 can handle only one of these hosts at any given time. The type of host the AR6002 uses depends upon the polarity of some package pins upon system power-up. The MBOX has two interfaces: an APB interface for access to the MBOX registers and an AHB interface which is used by the external host to access the VMC memory or other registers within the AR6002.

1.9 UART

The AR6002 includes a high-speed Universal Asynchronous Receiver/Transmitter (UART) interface that is fully compatible with the 16550 UART industry standard. Unlike standard RS232 modules, AR6002's UART interface supports the transfer of multiple bytes of data between the CPU and the UART. This reduces the bandwidth requirements on AR6002's CPU when it communicates with the UART. The UART supports:

- Polling and interrupt modes
- Full duplex buffer system with 16-byte Tx/Rx FIFOs
- 5-, 6-, 7-, or 8-bit characters
- 1-, 1 1/2-, or 2-stop bit generation
- Odd, even, or no parity.

- Data rates of:
  - 57600 bps
  - 38400 bps
  - 28800 bps
  - 19200 bps
  - 9600 bps
  - 4800 bps
  - 2400 bps

1.10 Reset Control

The AR6002 CHIP_PWD_L or the SYS_RST_L pins can be used to completely reset the entire chip. After these signals have been de-asserted, The AR6002 waits for the host power enable signal to be asserted by the external host processor. Until this signal is asserted, the MAC, BB, and SOC blocks are powered off and all modules except the host interface are held in reset.

Once the HOST_PWR_EN signal has been asserted, then the AR6002 turns on its crystal and later on its PLL. After all clocks are stable and running, the resets to all blocks are

automatically de-asserted. The only resets that stay asserted are given below:

- Warm and cold resets to the MAC
- Warm reset to the radio (The cold reset gets automatically de-asserted)

The above resets are deasserted by software. All AR6002 reset control logic resides in the RTC block to ensure stable reset generation.

1.10.1 CPU Reset

The CPU Reset is a bit different from the other resets mentioned above. There are four scenarios where the CPU Reset can be asserted:

1. It can be driven form the SYS_RST_L pin, de-assertion of HOST_PWR_EN, or from a write to an internal register.
2. The CPU Reset is also dependent upon the boot strap signal EJTAG_SEL which is latched from the GPIO_17 pin upon system initialization. The EJTAG_SEL signal is set when there is an In-Circuit Emulator (ICE) connected to the chip's JTAG port. In this situation, it is desirable to hold the CPU in reset even after the SYS_RST_L pin has been de-asserted and the rest of the chip is running. In this situation, the CPU Reset is asserted until GPIO_13 has been set (presumably by the ICE).
3. It is also possible to hold the CPU in reset until the host clears an internal register. This depends upon the boot-strap signal CPU_INIT_RST which is latched upon system initialization from the GPIO_16 pin. If CPU_INIT_RST is set, then the CPU will be held in reset until the host clears an internal AR6002 register.
4. The CPU can also be reset from the write that set bit-6 of the RTC_RESET register.

1.11 Reset Sequence

After a COLD_RESET event, the AR6002 will enter the SDIO_OFF state and await an enable event from the host. The AR6002 CPU will not execute any instructions until after the host enables the AR6002. The typical AR6002 COLD_RESET sequence is shown below:

1. The host system de-asserts CHIP_PWD_L, if asserted (use of CHIP_PWD_L is optional, but must be de-asserted to use the AR6002).
2. SYS_RST_L is de-asserted. The AR6002 latches the input level on GPIO-4 and GPIO-5 to determine the host interface type. (Use of SYS_RST_L is optional but must be de-asserted if asserted.) See the Host Interface chapter for a table listing interface type options.
3. For SDIO and GSPI interface modes, the AR6002 enters the HOST_OFF state. The host then reads interface registers to determine the type of function that the AR6002 supports.
4. When the host is ready to use the WLAN, it enables the AR6002 by writing to the function enable bit which sets the HOST_PWR_EN signal.
5. The AR6002 enters the WAKEUP state then the SOC_ON state and enables the XTENSA CPU to begin the boot process. Software configures the AR6002 functions and interfaces. When the AR6002 is ready to receive commands from the host, it will set the function ready bit.
6. The host reads the ready bit and can now send function commands to the AR6002.
7. The CPU may continue to be held in reset under some circumstances until its reset is cleared by an external pin or when the host clears a register. See section 1.10 above.
8. The MAC cold reset and the MAC/BB warm reset will continue to stay asserted until their respective reset registers are cleared.

1.12 Power Management

The AR6002 provides integrated power management and control functions and extremely low power operation for maximum battery life across all operational states by:

- Gating clocks for logic when not needed
- Shutting down unneeded high speed clock sources
- Reducing voltage levels to specific blocks in some states
- Reducing Tx and Rx active duty cycles
- Lowering CPU frequency when computational load is reduced

1.12.1 Hardware Power States

AR6002 hardware has six top level hardware power states managed by the RTC block. Table 1-1 describes the input from the MAC, CPU, SDIO/MBOX, interrupt logic, and timers that effect the power states.

Figure 1-1 depicts the state transition diagram.

Table 1-1. **Power Management States**

State	Description
OFF	CHIP_PWD_L pin assertion immediately brings the chip to this state
	Sleep clock is disabled
	No state is preserved
HOST_OFF	WLAN is turned off
	Only the host interface is power on - the rest of the chip is power gated (off)
	The host instructs the AR6002 to transition to WAKEUP by writing a register in the host interface domain
	Embedded CPU and WLAN do not retain state (separate entry) - This state can be bypassed by asserting CLK_REQ during de-assertion CHIP_PWD_L
NON_ASSOCIATED_SLEEP	Only the sleep clock is operating.
	The high speed crystal or oscillator is disabled.
	CPU, MAC, BB can be voltage scaled
	Any wakeup events (host, LF-Timer, GPIO-interrupt) will force a transition from this state to the WAKEUP state
	All internal states are maintained
ASSOCIATED_SLEEP	Only the sleep clock is operating
	The high speed crystal or oscillator is disabled
	CPU, MAC, BB can be voltage scaled
	Any wakeup events (MAC, host, LF-Timer, GPIO-interrupt) will force a transition from this state to the WAKEUP state
	All internal states are maintained
WAKEUP	The system transitions from sleep states to ON
	The high frequency clock is gated off as the crystal or oscillator is brought up and the PLL is enabled
	WAKEUP duration is programmable (default 3.8ms)
ON	The high speed clock is operational and sent to each block enabled by the clock control register
	Lower level clock gating is implemented at the block level, including the CPU, which can be gated off using the WAITI instruction while the system is on. No CPU, host and WLAN activities will transition to sleep states.

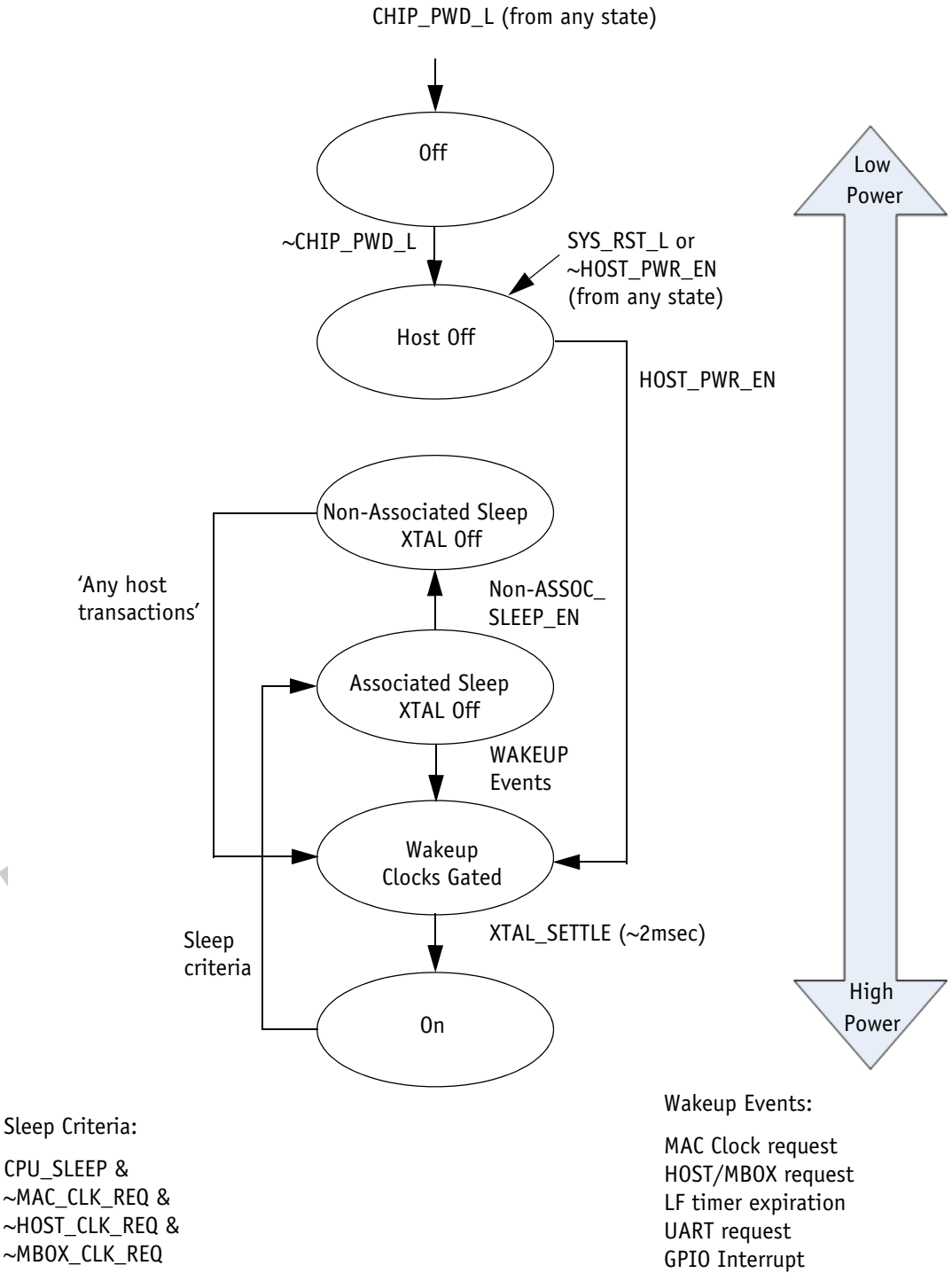

Figure 1-1. **AR6002 State Transitions**

1.12.2 Sleep State Management

Sleep state minimizes power consumption while saving system states. In deep sleep state, all high speed clocks are gated off and the external crystal is powered off. Light sleep is similar to deep sleep, but the XTAL remains running for faster WAKEUP. For the AR6002 to enter sleep state, the MAC, SDIO/MBOX, and CPU systems must be in sleep state.

When the embedded XTENSA CPU executes the WAITI command, the SDIO/MBOX is idle and the MAC system is in sleep state, the AR6002 enters the system Sleep state. In sleep state, the system gates all clock trees based on REF_CLK with only the sleep clock logic operating. The system remains in sleep state until a WAKEUP event causes the system to enter WAKEUP state, wait for the high frequency clock source to stabilize, and finally ungate all enabled clock trees. The CPU exits the WAITI state only when an interrupt arrives, which may result from the system WAKEUP event.

1.13 System Clocking (RTC Block)

The AR6002 has an RTC block which controls the clocks and power going to other internal modules. Its inputs consist of sleep requests from these modules and its outputs consists of clock enable and power signals which are used to gate the clocks going to these modules. The RTC block also manages resets going to other modules with the device. The AR6002's clocking is grouped into two types: high-speed and low-speed.

1.13.1 High Speed Clocking

The crystal drives the primary clock source for the internal PLL within the AR6002. REF_CLK is the primary clock source for the analog and digital systems. It is a high-frequency clock sourced from either an external crystal or oscillator source. It is the input to the RF synthesizer for generating required frequencies for proper 802.11 operation. An on-chip PLL creates the appropriate clock frequency for digital logic. When the AR6002 is in SLEEP state, REF_CLK is not needed. To minimize power consumption, the REF_CLK generator shuts down during deep sleep. If an external crystal is being used, the AR6002 disables the on-chip oscillator driver. If REF_CLK is coming from an external oscillator source, the AR6002 de-asserts its CLK_REQ signal and the external clock source may shut down REF_CLK.

The PLL output is programmable but it will usually run at one of only two frequencies: 320 MHz (during 802.11a mode) or 352 MHz (during 802.11 b/g mode). This base clock is divided into several clocks for the MAC and BB modules. There are clocks running at 160 MHz, 80 MHz, and 40 MHz going to the MAC and BB modules for 802.11a mode. (In 802.11g mode, these are running at 176 MHz, 88 MHz, and 44 MHz.)

The SOC clock comes from a clock divider module which divides the base clock by a programmable value. By default, this value is 8. Hence in 802.11a mode (320 MHz base clock), the default SOC frequency is 40 MHz and in 802.11b/g mode (352 MHz base clock), the SOC frequency is 44 MHz.

When the AR6002 exits SLEEP state, it enters WAKEUP state and asserts CLK_REQ or enables its internal crystal oscillator depending on the clock configuration. The AR6002 remains in WAKEUP state for a programmable duration that must cover clock settling time. CLK_REQ remains asserted in WAKEUP and ON states.

1.13.2 Low-Speed Clocking

The AR6002 has eliminated the need for a second crystal thereby reducing system cost. Instead, there is now a ring oscillator which produces a clock that is nominally running at 2 MHz, but this can depending on process and temperature.

The AR6002 has an internal calibration module which produces a 32.768 KHz output with minimal variation. For this, it uses the high-speed crystal input as the golden clock. Typically, this crystal input is only available when the system is in the normal operating state and is shut down during network sleep.

Hence the calibration module can adjust for process and temperature variations only when the system is in the normal operating state. During network sleep, this module cannot adjust for variations in the ring-oscillator output.

In case the output from the calibration module is not accurate enough, the AR6002 does have the capability to use an external low-speed clock source. This external clock source can be used as the sleep clock instead of the calibration module output. GPIO_8 in the AR6002 can be used as the external clock source pin.

However, the external clock source need not run at 32 KHz. It can be running at any similar low frequency. The TSF and other low frequency timers need to be programmed to match this frequency.

In addition to providing the low-frequency sleep clock for the AR6002, the 2 MHz ring oscillator also runs the state machines and counters inside the AR6002's Power Control Module (PCM). The PCM controls all power and isolation control signals for the entire chip.

1.13.3 Interface Clock

In addition to the clocking mentioned above, there is another clock source for the AR6002. This clock is referred to as the host clock (either SDIO or GSPI). This clock is completely independent from those mentioned above and is driven by the external host to communicate with the AR6002

This clock drives the interface logic as well as a few registers which can be accessed by the host. This allows this host to probe some AR6002 information, including SDIO Common I/O Area (CIA), when the AR6002 is in SLEEP state.

1.13.4 Antenna Switching

For designs that use external front-end components, the AR6002 provides the ability to control those components and the internal LNA with the antenna switch table. The switch table (see Table 1-2) contains 10 entries, each 5 bits wide, and is indexed by:

- The antenna selected by the MAC
- The state of the transceiver (idle, receive, or transmit)
- Controls for Rx attenuation

When fast-receive antenna diversity is enabled, the baseband will temporarily override the antenna selected by the MAC once a packet has been detected.

NOTE: Refer to *AR6002 ART Reference Guide* for more details on switching.

Table 1-2. **Switch Table**

Chip State	Ant Select	Rx Atten	Register Name
Idle	—	—	BB_ANTENNA_CONTROL
Bluetooth Active	1	—	BB_ANTENNA_CONTROL
Tx	1	—	BB_SWITCH_TABLE1
Rx	1	No	
Rx	1	Yes	
Rx	1	Yes	
Tx	2	—	BB_SWITCH_TABLE2
Rx	2	No	
Rx	2	Yes	
Rx	2	Yes	

Each 5-bit register controls the following AR6002 outputs (listed in the order of the most significant bit to the least significant bit):

- ANTE
- ANTD
- ANTC
- ANTB
- ANTA

The least significant bit of the register is ANTA. ANTE, ANTD, ANTC, ANTB, and ANTA are general purpose outputs that can be used to control antenna selection and external LNA, for example. For applications where the AR6002 shares an antenna with another wireless chip, ANTD is reserved for controlling the shared antenna switch.

In normal operation, the polarity of the antenna switch settings align with the progammable switch table in the baseband. For low power states, the polarity of the switch settings are shown in Table 1-3.

Table 1-3. **Switch Polarity for Low Power States**

Chip	Switch Pin	Chip PWD	Host Off	Network Sleep
AR6002G/X (BGA Package)	ANTE	Low	Low	Low
	ANTD	High	BT_CLK_EN*	BT_CLK_EN*
	ANTC	Low	Low	Low
	ANTB	Low	Low	Low
	ANTA	Low	Low	Low
AR6002GZ/XZ (CSP Package)	ANTE	Low	Low	Low
	ANTD	High	High	High
	ANTC	Low	Low	Low
	ANTB	Low	Low	Low
	ANTA	Low	Low	Low

* The polarity of ANTD is the same as BT_CLK_EN.

1.14 MAC/BB/RF Block

The MAC has an APB interface for register accesses as well as an AHB interface which is used by the MAC to access memory within the VMC.

1.14.1 MAC Block

The AR6002 Wireless MAC consists of five major blocks:

- single host interface unit (HIU),
- five queue control units (QCU),
- five DCF control units (DCU),
- single protocol control unit (PCU), and
- single DMA receive unit (DRU).

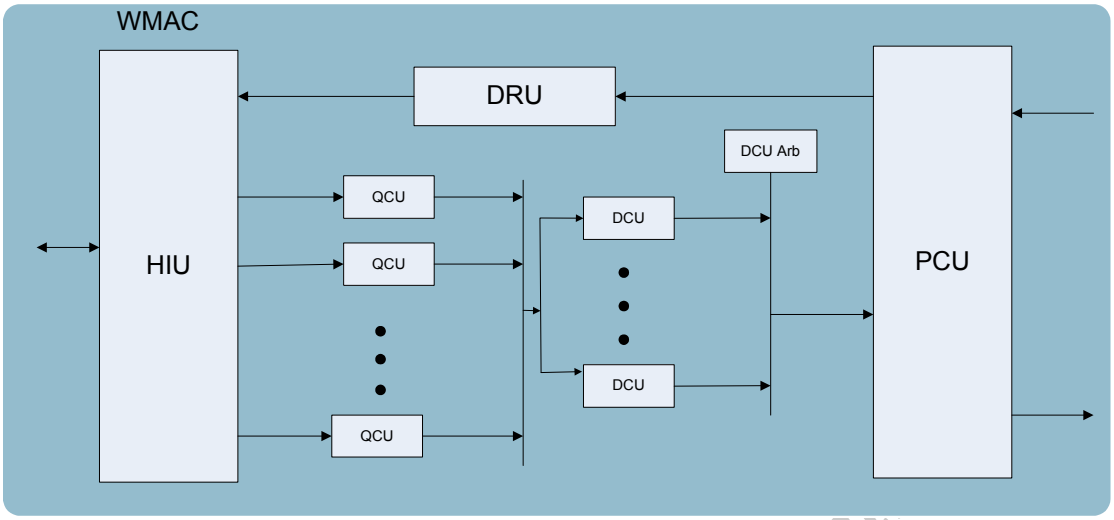

Figure 1-2. **AR6002 WMAC Interface**

The host interface unit connects the MAC to the outside world via a fixed, standardized interface. For AR6002, the HIU is a bridge to the on-chip AHB/APB busses.

Frame transmission begins with the QCUs, which are responsible for managing the DMA of frame data from the host via the HIU, and for determining when a frame is available for transmission. Each QCU feeds into (targets) exactly one DCU. Ready frames are passed from a QCU to its targeted DCU.

The DCU manages the VDCF channel access procedure on behalf of all QCUs associated with it. Once the DCU gains access to the channel, it passes the frame to the PCU, which manages the final details of sending the frame to the baseband logic. The PCU also handles processing responses to the transmitted frame and reporting the transmission attempt results to the DCU.

Frame reception begins in the PCU, which receives the incoming frame bit stream from the baseband logic. The PCU passes the frame data to the DRU, which manages receive descriptors and transfers the incoming frame data and status to the host via the HIU.

The AR6002 MAC implements five QCUs/DCUs, which support 802.11e method of channel access. Though not required by the hardware, usually, QCU 4 is mapped to DCU4 and QCU3 to DCU3 and so on and the intent is for the five DCUs to be used as follows:

- The highest-priority DCU is DCU 4. Typically, this DCU is the one associated with beacons.
- The next highest priority DCU is DCU 3. Typically, this DCU is the one associated with beacon-gated frames (i.e., "CAB" traffic).
- The next highest priority DCU is DCU 2. Typically, this DCU would be designated to use the HCF channel access mechanism, and all frames that are to be transmitted according to the HCF protocol would flow through this DCU.
- The remaining two DCUs (DCU1 and DCU0) typically are used for normal EDCF channel access, with DCU1 having higher priority over DCU0. Software is responsible for mapping the eight priority levels called for in the 802.11e specification on to the two physical EDCF DCUs.

1.15 Clock Distribution, JTAG, and Testing

The AR6002 has clock distribution circuitry which balances all the clocks going to the BB and MAC. The fundamental clock (160/176 MHz) is provided by the RF module which gets

divided. The BB needs this fundamental clock together with several divided versions of it. The MAC requires a divided 40/44 MHz clock. In addition AR6002 has a built in JTAG boundary scan of its pins. It also has features which allow for testing of the MBIST modules, the RF Analog-to-Digital converter (ADC), the RF Digital-to-Analog converter (DAC), as well as the internal clock synthesizer.

1.16 CPU Subsystem

The following Figure 1-3 shows the AR6002's CPU Subsystem:

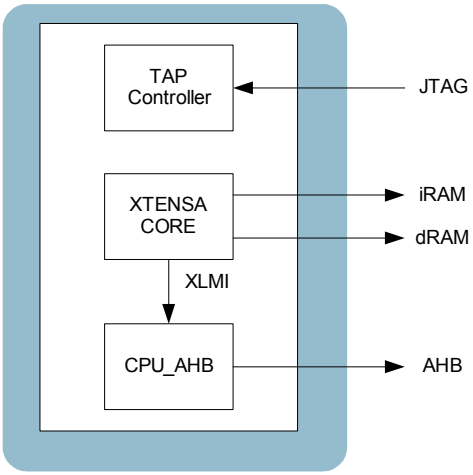

Figure 1-3. **CPU Subsystem**

The heart of the CPU subsystem consists of the XTENSA core. This is a 32-bit RISC core with a 5-stage pipeline and with 16-bit and 24-bit instruction encoding. The AR6002 does not utilize the Tensilica Instruction Extension (TIE) feature.

The core accesses local memory space through iRAM interface for instructions and dRAM interface or data. The core can also access memory through its Xtensa Local memory Interface (XLMI) bus. This bus is used primarily to access registers within the MAC, BB, and other AR6002 functions.

The module "CPU_AHB" converts this XLMI bus into a standard AHB bus. This module can buffer up to 4 write requests. When the XTENSA core makes a read request, all buffered write requests are first completed in order to maintain data integrity.

The CPU subsystem also has a TAP controller which allows for debugging using an external JTAG interface.

1.17 CPU Power Consumption

The XTENSA core power consumption can be controlled by the following means:

- RTC power state control:

The core frequency is controlled by the Real Time Control (RTC) module in AR6002. The XTENSA core is designed to run at a maximum frequency of 60 MHz. In deep sleep mode, the voltage supply to the SOC block, which includes the CPU, can be scaled down to save leakage power. Refer to "System Clocking (RTC Block)" on page 10 for detailed descriptions.

- CPU Idle Instruction:

Software can put the CPU into Idle sleep state by issuing a WAITI instruction. This will gate off all clocks within the CPU core.

- Logic level clock gating:

The core has been configured with several clock gating elements which scale down clocks to circuitry that is not changing.

1.18 Memory

The AR6002 supports the following virtual and physical memory mapping. See Figure 1-4 for details.

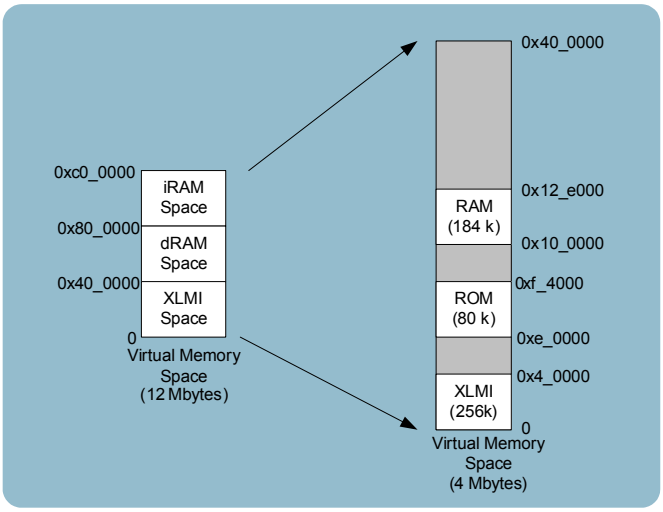

Figure 1-4. **Virtual and Physical Memory Mapping**

1.19 Interrupts

The AR6002 core supports a total of 18 interrupts. The first one (Int. 0) is a software interrupt at level-1 and the second one (Int. 1) is a timer interrupt at level-2. The others are hardware interrupts for various configurations.

2. Host Interfaces

The AR6002 can work in various modes of IO host configuration, including SDIO and Generic SPI (GSPI).

Table 2-1 shows pin settings for mode configuration, sampled during reset.

Table 2-1. **Pin Settings for Mode Configuration**

GPIO5	GPIO4	Configuration
0	0	GSPI Mode
1	X	SDIO Mode
0	1	Reserved

2.1 SDIO and GSPI Interfaces

The AR6002 interface is compliant with SDIO v1.1 and supports the SDIO common information area (CIA) registers for identifying and initializing the AR6002. These registers include the card common control register (CCCR) and function basic register (FBR) as well as CIS tuple space for CIS0 and CIS1. All other interface communication occurs in SDIO function 1 address space. Figure 2-1 shows the generic SDIO address map.

Figure 2-1 shows the generic SDIO address map.

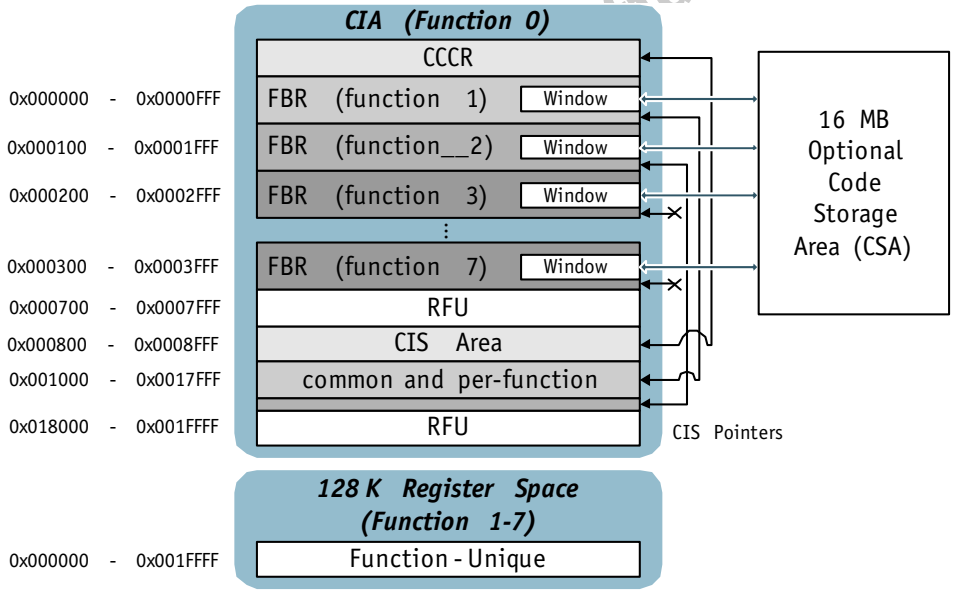

Figure 2-1. **SDIO Address Map**

2.2 Host Interface Address Map

The host sees the same address map interface regardless of the physical interface used, thus allowing the software layer above the physical interface to be identical across physical interface types. The lower 2 KB of address space must map all interface registers. The SDIO and GSPI interface can use mailbox aliases above 2 KB as these aliases provide larger window interfaces for increased performance. An extra 6 KB of address mapping has been added to mailbox 0 for future usage.

Figure 2-2 shows the host interface address map.

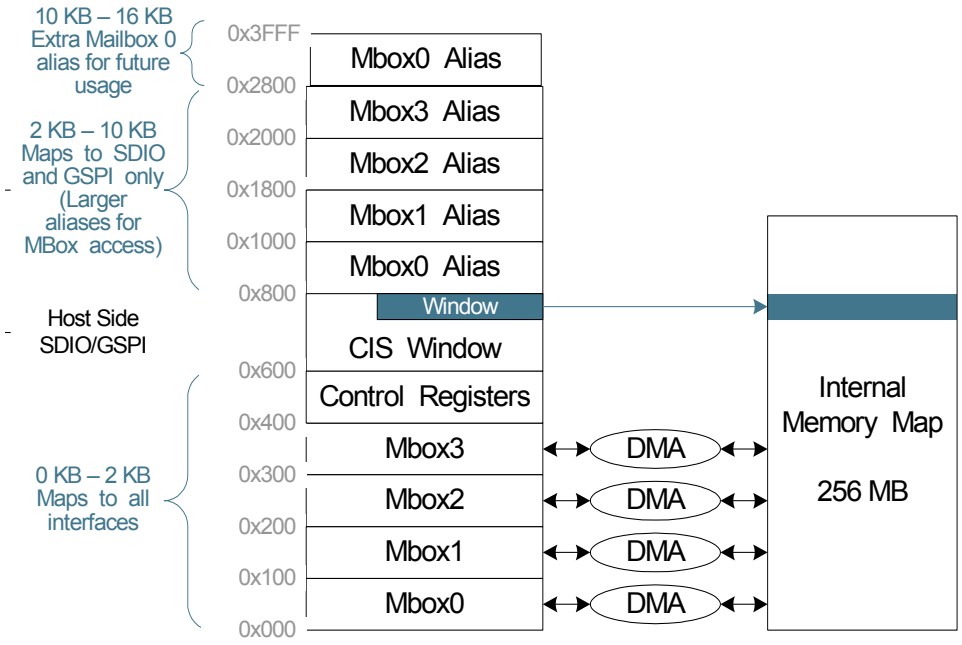

Figure 2-2. **Host Interface Address Map**

2.3 Mailboxes

The AR6002 supports four full duplex mailboxes to move messages between the AR6002 and the external host. Messages include packets, control messages, or any software-defined communication. AR6002 hardware uses End of Message (EOM) markers to denote the end of a message that spans one or more memory descriptors on the AR6002 side.

The flow control of the four mailboxes must be managed by software. To assist software flow control, hardware provides eight counters as a credit mechanism. The counters may count messages, memory buffers, packets, or any unit that software defines. The host and AR6002 CPUs can read and write these counters using ordinary writes or atomic operations. Counter resource use is optional.

2.3.2 Error Conditions

If the host driver and AR6002 software lose flow control synchronization for any reason, mailbox errors conditions could arise.

- Tx Mailbox Overflow

  If no DMA descriptors are available on the AR6002 Tx side, but the host still sends a message, the Tx Mailbox stalls the host physical interface. If the host interface remains stalled with the Tx FIFO full for a timeout period FIFO_TIMEOUT, a timeout error occurs. An interrupt is sent to the AR6002 CPU and the Host CPU. If the host status overflow bit is set, any mailbox Tx bytes that arrive from the host when the mailbox is full, are discarded. When the host clears overflow interrupt, mailbox FIFOs return to normal operation. Software must then either resynchronize flow control state or reset the AR6002 to recover.

- Rx Mailbox Underflow

  If the host DMA engine reads a mailbox that does not contain any data, the host physical interface stalls. If this condition persists for more than a timeout period, the host and the AR6002 are sent an underflow error interrupt. As long as the host status underflow bit is set, any mailbox reads that arrive when the mailbox is empty, return garbage data. When the host clears underflow interrupt, mailbox FIFOs return to normal operation. Software must then either resynchronize flow control state or reset the AR6002 to recover.

2.4 Interrupts

This section summarizes how interrupts flow between the AR6002 CPU and Host CPU. All interrupts can be masked by control registers.

2.4.1 AR6002 to Host

- The AR6002 CPU writes to the interrupt register
- Data ready

  Rx FIFO is not empty (clears on Rx FIFO empty)
- Error interrupts, underflow or overflow
- Wake up interrupt

  Set when the AR6002 exits sleep
- Flow control

  Any COUNT goes from 0 to 1 (cleared when COUNT goes 1 to 0)
- Option

  All AR6002 internal interrupts can be mapped to the host in case the host wants to take complete control of the AR6002 MAC and resources

2.4.2 Host to AR6002

- Host writes to INT_WLAN
- Error Interrupts (underflow or overflow)
- TX_CNT goes from 1 to 0 (out of descriptors)

3. Radio

The AR6002 transceiver consists of four major functional blocks (see Figure 3-1):

- Receiver (Rx)
- Transmitter (Tx)
- Frequency synthesizer (SYNTH)
- Associated bias/control (BIAS)

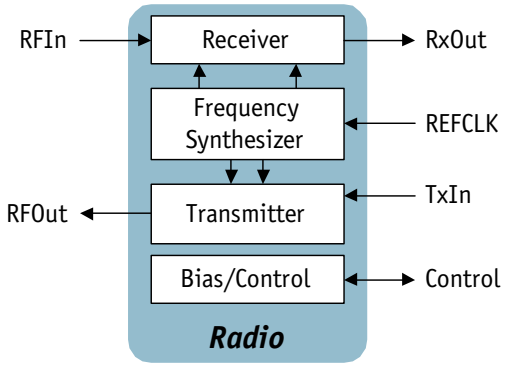

Figure 3-1. **Radio Functional Block Diagram**

3.1 Receiver (Rx) Block

The receiver converts an RF signal (with 20 MHz bandwidth) to baseband I and Q outputs. The receiver is tuned to 2.4 GHz and 5.4 GHz for IEEE 802.11 b/g and 802.11a signals, respectively. Figure 3-2 shows the Radio Tx/Rx block diagram.

For the 5 GHz operation, the receiver is comprised of a low noise amplifier (LNA) followed by a variable gain amplifier (VGA), a radio frequency (RF) mixer, an intermediate frequency (IF) mixer, and a baseband programmable gain filter. For the 5 GHz operation, the receiver is implemented using the sliding IF topology.

For the 2 GHz operation, the receiver is comprised of two separate paths: LNA1 and LNA2. For the LNA1 path, the receiver input is shared with the power amplifier (PA) output, thus eliminating the need for an external transmit/receive (T/R) switch. By eliminating an external T/R switch the overall cost of the final solution is reduced. For the LNA2 path, the T/R switch is needed because LNA2 input is not shared with the PA output. LNA2 path is targeted for applications where the best receiver sensitivity is the primary objective, whereas the LNA1 path is for cost sensitive applications. For the LNA1 path, the receiver is comprised of an LNA, an LNA buffer, a VGA, a direct conversion mixer and a baseband programmable gain filter. For the LNA2 path, the receiver topology includes an LNA, a VGA, a direct conversion mixer and a baseband programmable filter. For the 2 GHz operation, the receiver is implemented using the direct conversion topology.

For both 5G and 2G paths, mixers down convert the signal to baseband in-phase (I) and quadrature-phase (Q) signals. The I and Q signals are low-pass filtered and amplified by the baseband programmable gain filter controlled by digital logic. The baseband I and Q signals are sent to the ADC. The baseband programmable gain filter is shared between the 2G and 5G paths.

The DC offset of the receive chain is reduced using multiple digital to analog converters (DACs) controlled by the MAC/baseband block. Additionally, the receive chain can be digitally powered down to conserve power.

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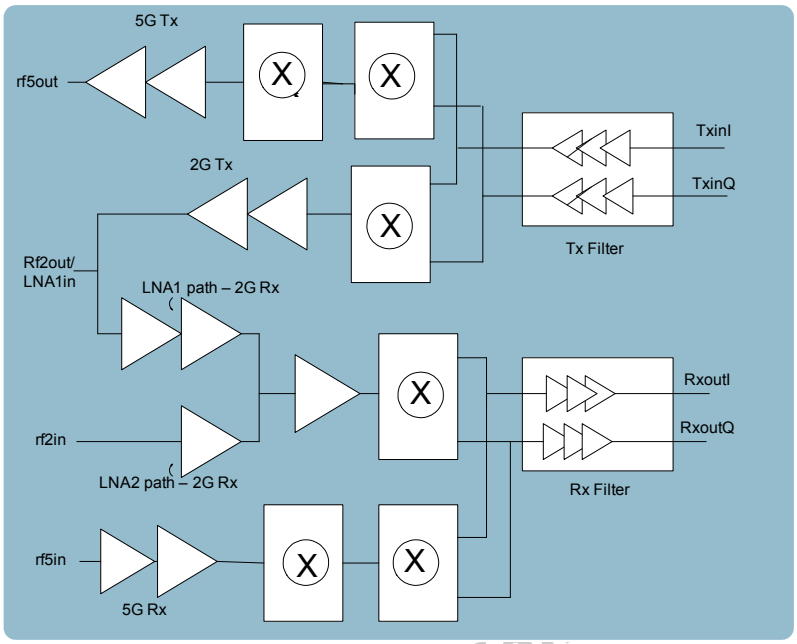

Figure 3-2. **Radio Tx/Rx Block Diagram**

3.2 Transmitter (Tx) Block

The transmitter converts baseband I and Q inputs to bands centered around 2.4 GHz and 5.4 GHz for IEEE 802.11 b/g and 802.11a signals respectively. A block diagram is shown in Figure 3-2.

The outputs of the DAC are low pass filtered through an on-chip reconstruction filter to remove spectral images and out-of-band quantization noise.

For the 5 GHz operation, the transmitter is comprised of the programmable reconstruction filter, an IF mixer, an RF mixer, a preamplifier and a PA. The IF mixer converts baseband signals to an intermediate frequency. The RF mixer converts the IF signal into radio frequency signals, which are driven off_chip through the preamplifier and the PA. For the 5 GHz operation, the transmitter is implemented using the sliding IF topology.

For the 2 GHz operation, the transmitter is comprised of the programmable reconstruction filter, a direct conversion mixer, a preamplifier and a PA. For the 2 GHz operation, the transmitter is implemented using the direct conversion topology.

The transmit chain can be digitally powered down to conserve power. To ensure that FCC limits are observed and output power stays close to the maximum allowed, transmit output power is adjusted by a closed loop digitally programmable control loop at the start of each packet. The closed-loop power control can be based on an on-chip or off-chip power detector.

3.2.1 Synthesizer (SYNTH) Block

The radio supports an on-chip synthesizer to generate local oscillator (LO) frequencies for receiver and transmitter mixers. Figure 3-3 shows the synthesizer topology.

The Synthesizer can use several Xtals such as 19.2, 24, 26, 38.4, 40, and 52 MHz. For AR6002, the default Xtal is 26 MHz.

A reference circuitry generates a signal used as the synthesizer reference input. An on-chip voltage controlled oscillator (VCO) provides the desired LO signal based on a phase/ frequency locked loop. The loop filter components are all integrated on-chip and can be digitally controlled. On power up or

channel reselection, the synthesizer takes about 0.2 msec to settle.

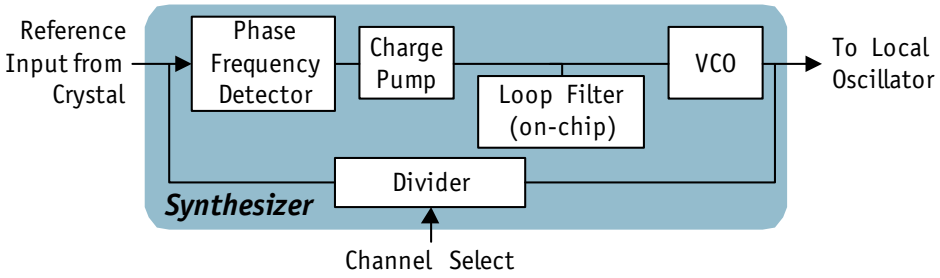

Figure 3-3. **Radio Synthesizer Block Diagram**

3.3 Bias/Control (BIAS) Block

The bias/control block provides reference voltages and currents for all other circuit blocks (see Figure 3-4). An on-chip bandgap reference circuit provides the needed voltage and current references based on an external 6.19 KΩ ± 1% shunted to GND resistor.

3.4 Baseband Block

The AR6002 baseband module (BB) is the physical layer controller for the 802.11a/g air interface. It is responsible for modulating data packets in the transmit direction, and detecting and demodulating data packets in the receive direction. All processing is done at the baseband frequency. See Figure 3-4.

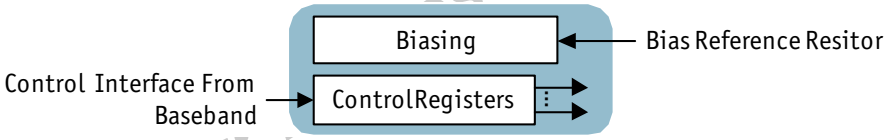

Figure 3-4. **Bias/Control Block Diagram**

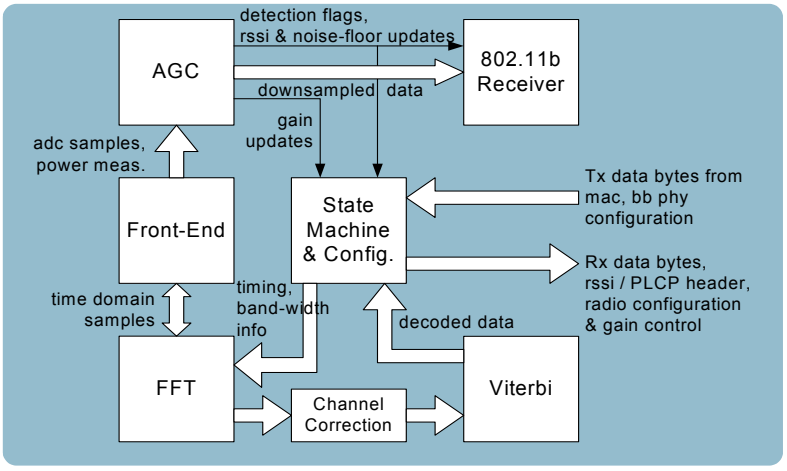

Figure 3-5. **Baseband Module Block Diagram**

There are five major blocks within the baseband module:

- SM
- AGC
- TIM
- FFT
- VIT
- BBB

Described below are the major functions for each block, and how they interact with other blocks in the system.

3.4.1 SM Block

The **SM** block is the main state machine for the baseband PHY. It encapsulates two major interfaces to the MAC and radio modules. The MAC interface is the interface that passes packet data to/from the MAC layer. This is done through a dedicated 8-bit bus interface that is controlled through transmit and receive framing signals. A separate configuration address space for the baseband block is written through the MAC block, as the baseband block is not directly connected to the AHB bus. The baseband to radio interface is a low-latency shift control interface that allows the baseband module to quickly and autonomously adjust radio settings to reflect the current packet sizing and direction flow. This usually takes the form of gain updates, ADC and DAC on/off settings, transmit and receive bias settings, and calibration mode configurations.

For transmitted packets, the SM block also houses the OFDM and CCK encoders/modulators. These encoder/modulator blocks format the packet data from the MAC, and generate symbols which are used for transmission over the air. These symbols are either converted into the frequency domain for OFDM modulation (FFT block), or are directly upsampled to the DAC for CCK modulation (Front-End block). Decisions on rate and output power are directed by the MAC through the use of transmit data headers.

3.4.2 AGC Block

The **AGC** block is responsible for two receive related functions: signal sizing and signal detection. Because the ADC dynamic range does not span all possible input power levels, an automatic gain control feedback loop is designed into the radio and baseband receive data path. This feedback loop recognizes when input signals seen by the ADC are either too small or too large, or even saturated. When this situation happens, the AGC block requests a gain change to the radio through the SM block radio interface.

Because the state of current and previous gain changes usually coincide with the arrival/departure of packets on the air, the AGC block also signals detection status to the SM block, so that it can turn on necessary receiver blocks that would otherwise be idle with no signal to decode. There are two major mechanisms for this: strong signal detection and weak signal detection. Strong signal detection simply looks for large changes in incoming signal strength, and will assume that these "strong signals" are most likely packets to try and decode. Weak signal detection will correlate against known preamble sequences when gain changes are not occurring. A match with a CCK or OFDM short preamble will trigger a detection flag for these types of "weak signals."

3.4.3 TIM Block

The **TIM** block is the time domain baseband front end for the transmitting and receiving of packets. On transmit, it is responsible for filtering and upsampling signals to a bandwidth and sampling rate appropriate to the DAC. If there are any radio impairments that need to be corrected (carrier leak, etc.), they are corrected here. On receive, the TIM block does all data path processing for time domain related signals. Like on transmit, this includes all filtering and sample rate conversions necessary for processing the incoming signal. Power measurements are performed here to aid the AGC block in ADC signal sizing. Correlation to know preamble sequences are also done here for weak signal detection. When a detection flag is set, coarse timing acquisition and frequency correction are done in the TIM block, as these functions are performed on data before translation into frequency domain signals (in the FFT).

3.4.4 FFT and VIT Blocks

The **FFT** block takes a signal sampled in time, and performs a fast fourier transform to get frequency bins of data sampled in frequency bins. These frequency bins are used for OFDM symbol decoding. For receive packets, an estimate of the channel over the air is computed in the FFT block as the long training

sequence is a known sequence in the frequency domain. Before symbols can be decoded, this channel estimate is inverted and applied to the incoming frequency symbols for channel correction. The Viterbi soft-decision decoder is contained within the **VIT** block, and is responsible for descrambling, deinterleaving, and decoding the symbols from the FFT.

For transmitted OFDM symbols, the FFT block is reused and "run in reverse" to compute the inverse fast fourier transform (iFFT). While running in iFFT mode, the FFT block takes in symbols from the SM block, and converts them to time samples that can be upsampled and filtered in the TIM block.

3.4.5 BBB Block

The **BBB** block is the 802.11b receiver used to demodulate and decode CCK packets in the 2.4 GHz range channels. It is a self contained unit that does not need other logic from the OFDM blocks except for some Front-End (TIM) filtering and down conversion. When a potential packet is detected by the AGC block, both the OFDM receiver logic and the BBB block logic are enabled in a voting process. This process reduces potential latency penalties by running both receivers in parallel while the detection state machine (AGC) tries to decide which type of protocol the incoming packet has been modulated with. This is done by comparing the relative preamble correlation power for the two protocol types.

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 4-1 summarizes the absolute maximum ratings and Table 4-2 lists the recommended operating conditions for the AR6002. Absolute maximum ratings are those values beyond which damage to the device can occur.

Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

The AR6002 requires 3 power levels, 1.2V, 1.8V and 3V. The digital core runs off of 1.2V. The analog block requires 1.2V and 1.8V to operate. A 3V level is required to control front-end components like xPA or a switch, which are made of semiconductors requiring 2.8V or higher.

If a 3V supply is available on the board, it can be tied to VDD_ANT. If not, an internal regulator can be used. VCC_FEM accepts voltages from 3.2V to 4.2V and provides an output regulated to 3.0V on LDO_OUT. A lower voltage, down to 3.0V, can be provided, but the output voltage is about 200mV below the input. If LDO is used, VDD_ANT should be tied to LDO_OUT.

NOTE: Maximum rating for signals follows the supply domain of the signals.

Table 4-1. **Absolute Maximum Ratings**

Symbol (Domain)	Parameter	Max Rating	Unit
DVDD12	Digital 1.2V core supply	-0.3 to 1.35	V
AVDD12	Analog 1.2V core supply	-0.3 to 1.35	V
AVDD18	Analog 1.8V I/O supply	-0.3 to 2.5	V
DVDD_SDIO	SDIO I/O supply	-0.3 to 4.0	V
DVDD_GPIO0	GPIO0 I/O supply	-0.3 to 4.0	V
DVDD_GPIO1	GPIO1 I/O supply	-0.3 to 4.0	V
DVDD_BT	BT coexistence I/O supply	-0.3 to 4.0	V
VCC_FEM	Battery voltage LDO input	-0.3 to 4.35	V
VDD_ANT	Antenna control I/O supply	-0.3 to 3.15	V
RF_{in}	Maximum RF input (reference to 50Ω input)	+10	dBm
T_{store}	Storage temperature	–45 to 135	°C
ESD	Electrostatic discharge tolerance	2000 [1]	V

[1]All pins except XTALI (BGA pin A11, CSP bump 85), RF5INN (BGA pin B1, CSP bump 8), and RF5INP (BGA pin B1,CSP bump 9). Maximum rating is 1000V for XTALI and 1500V for RF5INN/RF5INP.

4.2 Recommended Operating Conditions

Table 4-2. **Recommended Operating Conditions**

Symbol (Domain)	Parameter	Min	Typ	Max	Unit
DVDD12	Digital 1.2V core supply	1.14	1.2	1.26	V
AVDD12	Analog 1.2V core supply	1.14	1.2	1.26	V
AVDD18	Analog 1.8V I/O supply	1.71	1.8	1.89	V
DVDD_SDIO	SDIO I/O supply	1.71	1.8	3.46	V
DVDD_GPIO0	GPIO0 I/O supply	1.71	1.8	3.46	V
DVDD_GPIO1	GPIO1 I/O supply	1.71	1.8	3.46	V
DVDD_BT	BT coexistence I/O supply	1.71	1.8	3.46	V
VCC_FEM	Battery voltage LDO input	3.0	3.6	4.2	V
VDD_ANT	Antenna control I/O supply	1.71	3.0	3.46	V
$T_{ambient}$	Ambient temperature	–40	25	85	°C

4.3 DC Electrical Characteristics

Table 4-3 and Table 4-4 list the general DC electrical characteristics over recommended operating conditions (unless otherwise specified).

Table 4-3. **General DC Electrical Characteristics (For 3.3 V I/O Operation)**

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage			0.8 x V_{dd}	-	V_{dd} + 0.3	V
V_{IL}	Low Level Input Voltage			–0.3	-	0.2 x V_{dd}	V
I_{IL}	Input Leakage Current	Without Pull-up or Pull-down	0 V < V_{in} < V_{dd} 0 V < V_{out} < V_{dd}	–10		10	µA
		With Pull-up or Pull-down	0 V < V_{in} < V_{dd} 0 V < V_{out} < V_{dd}	–65		65	µA
V_{OH}	High Level Output Voltage		I_{OH} = –4 mA	V_{dd} – 0.35	-	-	V
			I_{OH} = –12 mA[1]	V_{dd} – 0.35	-	-	V
V_{OL}	Low Level Output Voltage		I_{OL} = 4 mA	-	-	0.40	V
			I_{OL} = 12 mA[1]	-	-	0.40	V
C_{IN}	Input Capacitance[2]		-	-	6	-	pF

[1]For these pins only: SDIO_DATA_0, SDIO_DATA_1, SDIO_DATA_2, SDIO_DATA_3
[2]Parameter not tested; value determined by design simulation

Table 4-4. **General DC Electrical Characteristics (For 1.8 V I/O Operation)**

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage			0.8 x V_{dd}	-	V_{dd} + 0.2	V
V_{IL}	Low Level Input Voltage			–0.3	-	0.2 x V_{dd}	V
I_{IL}	Input Leakage Current	Without Pull-up or Pull-down	0 V < V_{in} < V_{dd} 0 V < V_{out} < V_{dd}	–10	-	10	µA
		With Pull-up or Pull-down	0 V < V_{in} < V_{dd} 0 V < V_{out} < V_{dd}	–35	-	35	µA
V_{OH}	High Level Output Voltage		I_{OH} = –2 mA	V_{dd} – 0.35	-	-	V
			I_{OH} = –6 mA[1]	V_{dd} – 0.35	-	-	V
V_{OL}	Low Level Output Voltage		I_{OL} = 2 mA	-	-	0.3	V
			I_{OL} = 6 mA[1]	-	-	0.3	V
C_{IN}	Input Capacitance[2]		-	-	6	-	pF

[1]For these pins only: SDIO_DATA_0, SDIO_DATA_1, SDIO_DATA_2, SDIO_DATA_3
[2]Parameter not tested; value determined by design simulation

The following three figures show the Power Sequence operation for the AR6002.

I/O Supply = AVDD18, DVDD_SDIO, DVDD_GPIO0, DVDD_GPIO1, DVDD_BT, VCC_FEM, VDD_ANT
1.2V Supply = DVDD12, AVDD12

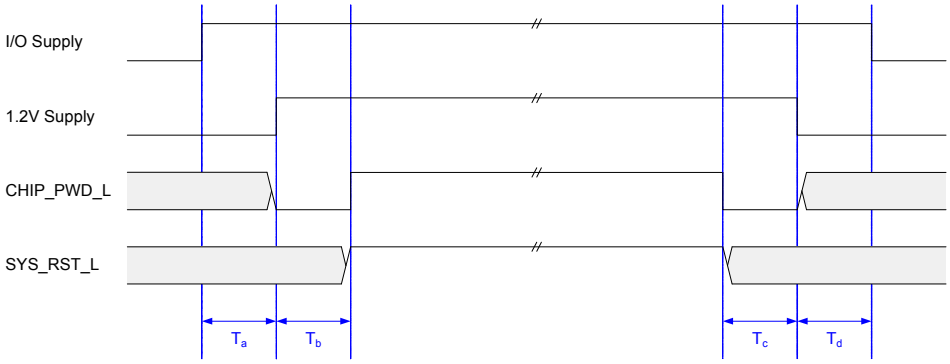

Figure 4-1. **Power Up/Power Down Timing While Asserting CHIP_PWD_L**

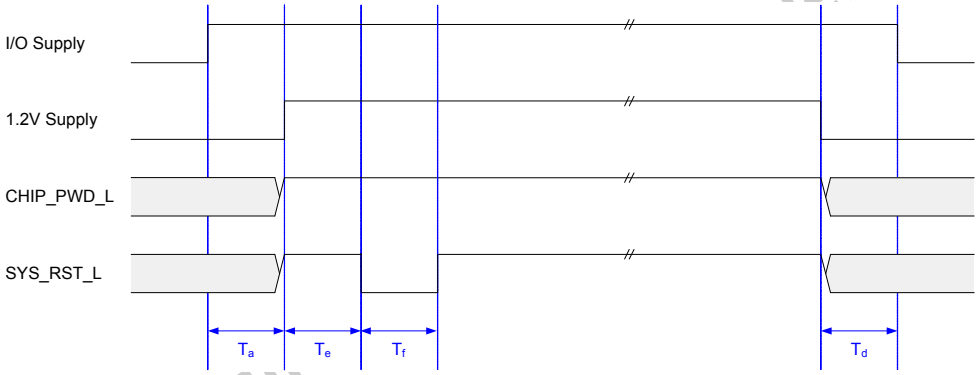

Figure 4-2. **Power Up/Down Timing While Asserting SYS_RST_L**

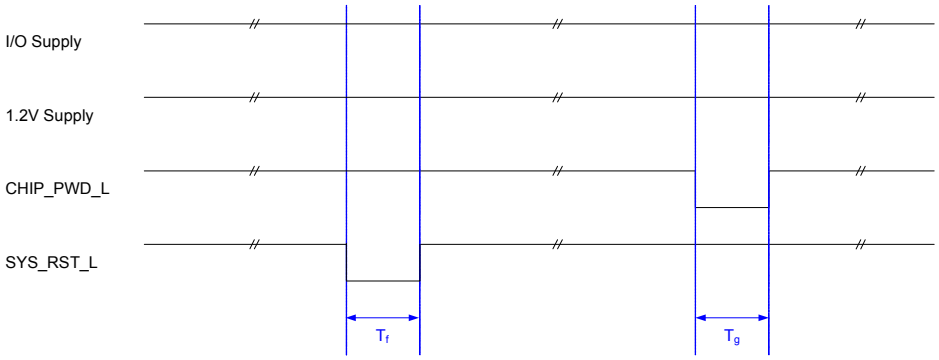

Figure 4-3. **Reset and Power Cycle Timing**

Table 4-5. **Timing Diagram Definitions**

	Description	**Min (**μsec)
T_a	Time between I/O supply valid** and 1.2V supply valid	0
T_b	Time between 1.2V supply valid and CHIP_PWD_L deassertion	5
T_c	Time between CHIP_PWD_L assertion and 1.2V supply invalid	0
T_d	Time between 1.2V supply invalid and I/O supply valid	0
T_e	Time between 1.2V supply invalid and SYS_RST_L deassertion	0
T_f	Length of SYS_RST_L pulse	1
T_g	Length of CHIP_PWD_L pulse	5

** Supply valid represents the voltage level has reached 90% level.

4.4 Radio Receiver Characteristics

Table 4-7 and Table 4-6 and Table 4-8
summarize the AR6002 receiver characteristics.

Table 4-6. **Receiver Characteristics for 2.4 GHz Operation (LNA1 Path - Shared Tx/Rx)**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{rx}	Receive input frequency range	5 MHz channel spacing	2.312	-	2.484	GHz
NF	Receive chain noise figure	See Note [1]	-	5	-	dB
S_{rf}	Sensitivity	See Note [2]				dBm
	1 Mbps		-	-95	-	
	2 Mbps		-	-91	-	
	5.5 Mbps		-	-89	-	
	11 Mbps		-	-86	-	
	6 Mbps		-	-90	-	
	9 Mbps		-	-90	-	
	12 Mbps		-	-89	-	
	18 Mbps		-	-86	-	
	24 Mbps		-	-83	-	
	36 Mbps		-	-79	-	
	48 Mbps		-	-75	-	
	54 Mbps		-	-73	-	
IP1dB	Input 1 dB compression (min. gain)	-	-	+11	-	dBm
IIP3	Input third intercept point (min. gain)	-	-	+19	-	dBm
ER_{phase}	I, Q phase error		-	1	-	degree
ERamp	I, Q amplitude error		-	0.5	-	dB
R_{adj}	Adjacent channel rejection	10 to 20 MHz				dB
	1 Mbps		-	35	-	
	11 Mbps		-	33	-	
	6 Mbps		-	36	-	
	54 Mbps		-	22	-	
TRpowup	Time for power up (from RxOn)	-	-	1.5	-	µs

[1]Does not include the effect of an external RF filter.
[2]Sensitivity performance based on the Atheros reference design, which includes RF filter. No T/R switch, no external LNA. Port shared with the PA.

Table 4-7. **Receiver Characteristics for 2.4 GHz Operation (LNA2 Path - Separate Rx)**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{rx}	Receive input frequency range	5 MHz channel spacing	2.312	-	2.484	GHz
NF	Receive chain noise figure	See Note [1]	-	3.5	-	dB
S_{rf}	Sensitivity	See Note [2]				dBm
	1 Mbps		-	-97	-	
	2 Mbps		-	-93	-	
	5.5 Mbps		-	-91	-	
	11 Mbps		-	-88	-	
	6 Mbps		-	-92	-	
	9 Mbps		-	-92	-	
	12 Mbps		-	-91	-	
	18 Mbps		-	-88	-	
	24 Mbps		-	-85	-	
	36 Mbps		-	-82	-	
	48 Mbps		-	-77	-	
	54 Mbps		-	-75	-	
IP1dB	Input 1 dB compression (min. gain)	-	-	+3	-	dBm
IIP3	Input third intercept point (min. gain)	-	-	+11	-	dBm
ER_{phase}	I,Q phase error		-	1	-	degree
ERamp	I,Q amplitude error		-	0.5	-	dB
R_{adj}	Adjacent channel rejection	10 to 20 MHz				dB
	1 Mbps		-	36	-	
	11 Mbps		-	34	-	
	6 Mbps		-	37	-	
	54 Mbps		-	24	-	
TRpowup	Time for power up (from RxOn)	-	-	1.5	-	µs

[1]Does not include the effect of an external RF filter or Tx/Rx antenna switch.
[2]Sensitivity performance based on the Atheros reference design, which includes RF filter, Tx/Rx antenna switch, no external LNA

Table 4-8. **Receiver Characteristics for 5 GHz Operation**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{rx}	Receive input frequency range	5 MHz center frequency	4.90	-	5.925	GHz
NF	Receive chain noise figure (max. gain)	See Note [1] and [2]	-	5.5		dB
S_{rf}	Sensitivity	See Note [2]				dBm
	6 Mbps		-	-92	-	
	54 Mbps		-	-73	-	
IP1dB	Input 1 dB compression (min. gain)		-	+5	-	dBm
IIP3	Input third intercept point (min. gain)		-	+13	-	dBm
ER_{phase}	I,Q phase error		-	2	-	degree
ERamp	I,Q amplitude error		-	0.5	-	dB
R_{adj}	Adjacent channel rejection	10 to 20 MHz				dB
	6 Mbps		-	22	-	
	54 Mbps		-	5	-	
R_{alt}	Alternate channel rejection	20 to 30 MHz			-	dB
	6 Mbps		-	37		
	54 Mbps		-	20		
TRpowup	Time for power up (from RxOn)	-	-	1.5	-	µs

[1]With an external LNA.

[2]Sensitivity performance is based on the Atheros reference design, which includes RF filter, Tx/Rx antenna switch, and an external LNA.

4.5 Radio Transmitter Characteristics

Table 4-9 and Table 4-10 summarize the transmitter characteristics for AR6002.

Table 4-9. **Transmitter Characteristics for 2.4 GHz operation**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{tx}	Transmit output frequency range	5 MHz center frequency	2.312	-	2.484	GHz
P_{out}	Without xPA: Mask Compliant CCK output power		-	+8	-	dBm
	Without xPA: EVM Compliant OFDM output power for 64 QAM		-	+5	-	dBm
	With xPA: Mask Compliant CCK output power		-	+16	-	dBm
	With xPA: EVM Compliant OFDM output power for 64 QAM		-	+16	-	dBm
SP_{gain}	PA gain step	See Note [1]	-	0.5	-	dB
A_{pl}	Accuracy of power leveling loop	See Notes [2] [3]	-	+1/-1.5	-	dB
OP1dB	Output P1dB (max. gain)	2.442 GHz	-	12	-	dBm
OIP3	Output third order intercept point (max gain)	2.442 GHz	-	19	-	dBm
SS	Sideband suppression		-	-35	-	dBc
TTpowup	Time for power up (from TxOn)	-	-	1.5	-	µs

[1]Guaranteed by design.

[2]Manufacturing calibration required.

[3]Not including tolerance of external power detector and its temperature variation.

Table 4-10. **Transmitter Characteristics for 5 GHz Operation**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{tx}	Transmit output frequency range	20 MHz center frequency	4.9	-	5.925	GHz
P_{out}	EVM Compliant OFDM output power for 64 QAM	See Note [1]	-	-2	-	dBm
SP_{gain}	PA gain step	See Note [2]	-	0.5	-	dB
A_{pl}	Accuracy of power leveling loop	See Note [3]	-	+1/-1.5	-	dB
OP1dB	Output P1dB (max. gain)	5.25 GHz	-	4	-	dBm
OIP3	Output third order intercept point (max gain)	5.25 GHz	-	12	-	dBm
SS	Sideband suppression		-	-32	-	dBc
Tx_{mask}	Transmit spectral mask	See Note [4]				dBr
	At 11 MHz offset		-	-22	-	
	At 20 MHz offset		-	-32	-	
	At 30 MHz offset		-	-52	-	
TTpowup	Time for power up (from TxOn)		-	1.5	-	µs

[1]Measured without a BALUN. Output is single ended.
[2]Guaranteed by design.
[3]Manufacturing calibration required.
[4]Measured at the antenna connector port. Average conducted transmit power levels = 18 dBm at 64 QAM (OFDM). System includes external PA.

4.6 AR6002 Synthesizer Characteristics

Table 4-11 and Table 4-12 summarize the synthesizer characteristics for the AR6002.

Table 4-11. **Synthesizer Composite Characteristics for 2.4 GHz Operation**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pn	Phase noise (at Tx_Out)					dBc/Hz
	At 30 KHz offset		-	–99	-	
	At 100 KHz offset		-	–99	-	
	At 500 KHz offset		-	–108	-	
	At 1 MHz offset		-	–115	-	
F_c	Center channel frequency	Center frequency at 5 MHz spacing [1]	2.312	-	2.484	GHz
F_{ref}	Reference oscillator frequency	± 20 ppm	-	$40/26^2$	-	MHz
F_{step}	Frequency step size (at RF)	See Note	-	1	-	MHz
TS_{powup}	Time for power up (from sleep)	-	-	0.2	-	ms

[1]Frequency is measured at the Tx output.
[2] Other supported frequencies are: 19.2, 24, 26, 38.4, 40, and 52 MHz.

Table 4-12. **Synthesizer Composite Characteristics for 5 GHz Operation**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Pn	Phase noise (at Tx_Out) At 30 KHz offset At 100 KHz offset At 500 KHz offset At 1 MHz offset		 - - - -	 –91 –91 –100 –107	 - - - -	dBc/Hz
F_c	Center channel frequency	Center frequency at 5 MHz spacing [1]	4.90	-	5.925	GHz
F_{ref}	Reference oscillator frequency	± 20 ppm	-	40/26[3]	-	MHz
F_{step}	Frequency step size (at RF)	See Note [2]	-	5	-	MHz
TS_{powup}	Time for power up (from sleep)	-	-	0.2	-	ms

[1]Frequency is measured at the Tx output.
[2]5 MHz channel spacing is for the 5.725 to 5.925 GHz band.
[3] Other supported frequencies are: 19.2, 24, 26, 38.4, 40, and 52 MHz.

4.7 Typical Power Consumption Performance

The following tables illustrate TYPICAL, room temperature power consumption data measured on the Atheros SD21 evaluation board.

Table 4-13. **AR6002 Typical Power Consumption - Low Power States**

Mode		Chip Set	Current Consumption [mA]			Power Consumption [mW]
			@1.2 V	@1.8 V	@3.3 V	
Standby	CHIP_PWD	AR6002G/GZ/X/XZ	0.008	0.000	0.000	**0.010**
	HOST_OFF	AR6002GZ/XZ	0.050	0.007	0.001	**0.076**
		AR6002G	0.050	0.012	0.019	**0.144**
		AR6002X	0.050	0.007	0.019	**0.135**
	SLEEP	AR6002GZ/XZ	0.500	0.007	0.002	**0.619**
		AR6002G	0.500	0.012	0.002	**0.628**
		AR6002X	0.500	0.007	0.002	**0.619**
IEEE PS	DTIM=1	AR6002GZ/XZ	1.750	0.707	0.042	**3.51**
		AR6002G	1.750	0.712	0.042	**3.52**
		AR6002X	1.750	0.707	0.042	**3.51**
	DTIM=3	AR6002GZ/XZ	0.917	0.240	0.015	**1.58**
		AR6002G	0.917	0.245	0.015	**1.59**
		AR6002X	0.917	0.240	0.015	**1.58**
	DTIM=10	AR6002GZ/XZ	0.625	0.077	0.006	**0.91**
		AR6002G	0.625	0.082	0.006	**0.92**
		AR6002X	0.625	0.077	0.006	**0.91**

4.7.1 Measurement Conditions for Low Power State

T_amb = 25 ºC

All I/O pins except CHIP_PWD_L are maintained at their default polarities.

DVDD12 = AVDD12 = 1.2 V

AVDD18 = DVDD_SDIO = 1.8 V

DVDD_GPIO0 = DVDD_GPIO1 = DVDD_BT = DVDD_ANT = VCC_FEM = 3.3 V

CHIP_PWD - all blocks power gated except for "Power, Clock Management"

HOST_OFF - all blocks power gated except for "Power, Clock Management", "SDIO", and "GSPI."

SLEEP - "LF CLK" running; all blocks voltage scaled or power gated except for "Power, Clock Management", "SDIO", "GSPI", and "GPIO"; internal state is maintained.

Table 4-14. **AR6002 Typical Power Consumption - Continuous Receive Using LNA1 Path (Shared Tx/Rx)**

Rate [Mbps]	LNA1 Path (Shared Tx/Rx) [-70 dBm input level]			
	Current Consumption [mA]			Power Consumption [mW]
	@1.2 V	@1.8 V	@3.3 V	
1	63	35	2	**146**
2	64	35	2	**147**
5.5	68	35	2	**152**
11	68	35	2	**152**
6	67	35	2	**150**
9	67	35	2	**150**
12	68	35	2	**152**
18	68	35	2	**152**
24	69	35	2	**153**
36	71	35	2	**155**
48	72	35	2	**156**
54	73	35	2	**158**

4.7.2 Measurement Conditions for Continuous Receive Using LNA1

T_amb = 25 ºC

DVDD12 = AVDD12 = 1.2 V

AVDD18 = 1.8 V

DVDD_SDIO = DVDD_GPIO0 = DVDD_GPIO1 = DVDD_BT = DVDD_ANT = VCC_FEM = 3.3 V

Table 4-15. **AR6002 Typical Power Consumption - Continuous Receive Using LNA2 Path (Separate Rx)**

Rate [Mbps]	LNA2 Path (Separate Rx)			
	Current Consumption [mA]			Power Consumption [mW]
	@1.2 V	@1.8 V	@3.3 V	
1	64	28	2	**134**
2	64	28	2	**134**
5.5	69	28	2	**140**
11	69	28	2	**140**
6	67	28	2	**138**
9	68	28	2	**139**
12	68	28	2	**139**
18	69	28	2	**140**
24	70	28	2	**141**
36	71	28	2	**143**
48	73	28	2	**145**
54	73	28	2	**145**

4.7.3 Measurement Conditions for Continuous Receive Using LNA2

T_amb = 25 ºC

DVDD12 = AVDD12 = 1.2 V

AVDD18 = 1.8 V

DVDD_SDIO = DVDD_GPIO0 = DVDD_GPIO1 = DVDD_BT = DVDD_ANT = VCC_FEM = 3.3 V

Table 4-16. **AR6002 Typical Power Consumption - Continuous Transmit Using xPA**

Rate [Mbps]	Target Output Power [dBm]	AR6002 Current Consumption [mA]			xPA Current Consumption [mA]	Total Power Consumption Including xPA [mW]
		@1.2 V	@1.8 V	@3.3 V	@3.3 V	
1	15	37	51	2	95	**456**
2	15	37	51	2	95	**456**
5.5	15	37	51	2	95	**456**
11	15	37	51	2	95	**456**
6	15	44	65	2	95	**490**
9	15	44	65	2	95	**490**
12	15	44	65	2	95	**490**
18	15	44	65	2	95	**490**
24	15	45	65	2	94	**488**
36	14	45	58	2	89	**459**
48	13	45	55	2	83	**433**
54	11	45	65	2	74	**422**

4.7.4 Measurement Conditions for Continuous Transmit Using xPA

T_amb = 25 ºC

DVDD12 = AVDD12 = 1.2 V

AVDD18 = 1.8 V

DVDD_SDIO = DVDD_GPIO0 = DVDD_GPIO1 = DVDD_BT = DVDD_ANT = VCC_FEM = 3.3 V

Table 4-17. **AR6002 Typical Power Consumption - Continuous Transmit Without xPA**

Rate [Mbps]	Target Output Power [dBm]	Current Consumption [mA]			Power Consumption [mW]
		@1.2 V	@1.8 V	@3.3 V	
1	8	38	108	2	**247**
2	8	38	108	2	**247**
5.5	8	38	108	2	**247**
11	8	38	108	2	**247**
6	8	47	108	2	**258**
9	8	47	108	2	**258**
12	8	47	108	2	**258**
18	8	47	107	2	**256**
24	8	48	107	2	**257**
36	7	48	105	2	**254**
48	6	48	104	2	**252**
54	4	48	102	2	**248**

4.7.5 Measurement Conditions for Continuous Transmit Without xPA

T_amb = 25 ºC

DVDD12 = AVDD12 = 1.2 V

AVDD18 = 1.8 V

DVDD_SDIO = DVDD_GPIO0 = DVDD_GPIO1 = DVDD_BT = DVDD_ANT = VCC_FEM = 3.3 V

5. AC Specifications

5.1 Optional External 32 KHz Input Clock Timing

Figure 5-1 and Table 5-1 show the external 32 KHz input clock timing requirements.

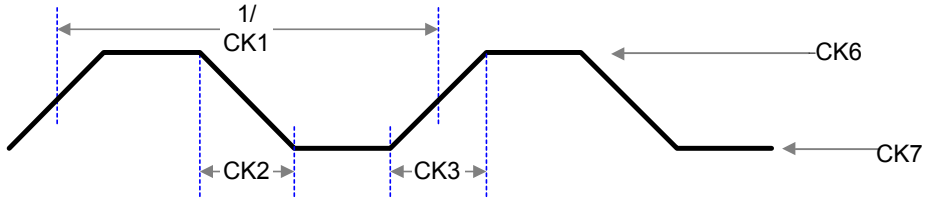

Figure 5-1. **Optional External 32 KHz Input Clock Timing Requirements**

Table 5-1. **Optional External 32 KHz Input Clock Timing**

Symbol	Description	Min	Typ	Max	Unit
CK1	Frequency	-	32.768	-	KHz
CK2	Fall time	-	-	100	ns
CK3	Rise time	-	-	100	ns
CK4	Duty cycle (high-to-low ratio)	15	-	85	%
CK5	Frequency stability	–50	-	50	ppm
CK6	Input high voltage	0.8*VDD_BT	-	VDD_BT+0.2	V
CK7	Input low voltage	-0.3	-	0.2*VDD_BT	V

5.2 External 19.2/24/26/38.4/40/52 MHz Reference Input Clock Timing

Figure 5-2 and Table 5-2 show the external 19.2/24/26/38.4/40/52 MHz reference input clock timing requirements.

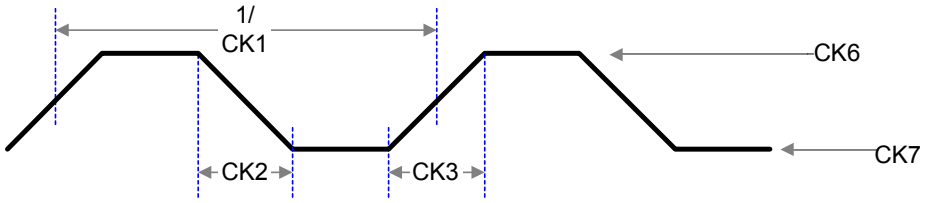

Figure 5-2. **External 19.2/24/26/38.4/40/52 MHz**

Table 5-2. **External 19.2/24/26/38.4/40/52 MHz Reference Input Clock Timing**

Symbol	Description	Min	Typ	Max	Unit
CK2	Fall time	-	-	0.1 * period	ns
CK3	Rise time	-	-	0.1 * period	ns
CK4	Duty cycle (high-to-low ratio)	40	-	60	%
CK5	Frequency stability	-20	-	20	ppm
CK6	Input high voltage	1.14	-	3.46	V
CK7	Input low voltage	-0.1	-	0.3	V

5.3 SDIO/GSPI Interface Timing

Figure 5-3 shows the write timing for a SDIO/ GSPI style transaction.

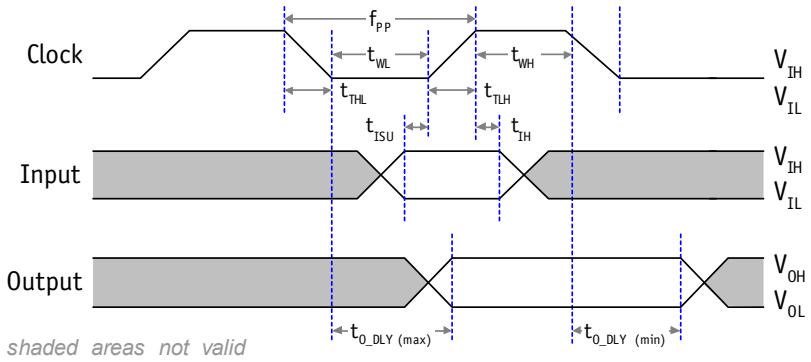

Figure 5-3. **SDIO/GSPI Timing**

Table 5-3 shows the values for timing constraints for SDIO.

Table 5-3. **SDIO Timing Constraints**

Parameter	Description	Min	Max	Unit	Note
f_{PP}	Clock frequency data transfer mode	0	25	MHz	100 pF ≥ C_L (7 cards)
t_{WL}	Clock low time	10	-	ns	100 pF ≥ C_L (7 cards)
t_{WH}	Clock high time	10	-	ns	100 pF ≥ C_L (7 cards)
t_{TLH}	Clock rise time	-	10	ns	100 pF ≥ C_L (10 cards)
t_{THL}	Clock fall time	-	10	ns	100 pF ≥ C_L (7 cards)
t_{ISU}	Input setup time	5	-	ns	25 pF ≥ C_L (1 card)
t_{IH}	Input hold time	5	-	ns	25 pF ≥ C_L (1 card)
$t_{O\_DLY\ (min)}$	Output delay time during data transfer mode	0	14	ns	25 pF ≥ C_L (1 card)
$t_{O\_DLY\ (max)}$	Output delay time during identification mode	0	50	ns	25 pF ≥ C_L (1 card)

Table 5-4 shows the values for timing constraints for GSPI.

Table 5-4. **GSPI Timing Constraints**

Parameter	Description	Min	Max	Unit
f_{PP}	Clock frequency	0	48	MHz
t_{WL}	Clock low time	8.3	-	ns
t_{WH}	Clock high time	8.3	-	ns
t_{TLH}	Clock rise time	-	2	ns
t_{THL}	Clock fall time	-	2	ns
t_{ISU}	Input setup time	5	-	ns
t_{IH}	Input hold time	5	-	ns
t_{O_DLY}	Output delay	0	5	ns

6. Pin Descriptions

This section contains a listing of the signal descriptions (see Table 6-1 for the BGA package pin outs).

The following nomenclature is used for signal names:

NC	No connection should be made to this pin
_L	At the end of the signal name, indicates active low signals
P	At the end of the signal name, indicates the positive side of a differential signal
N	At the end of the signal name indicates the negative side of a differential signal

The following nomenclature is used for signal types described in Table 6-2:

IA	Analog input signal
I	Digital input signal
I, H	Input signals with weak internal pull-up, to prevent signals from floating when left open
I, L	Input signals with weak internal pull-down, to prevent signals from floating when left open
I/O	A digital bidirectional signal
I/O/L	A digital bidirectional signal, with a weak internal pull-down
OA	An analog output signal
O	A digital output signal
P	A power or ground signal

Table 6-1. **BGA Package Pinout**

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	AGND	RF2 OUTN	RF2 OUTP	RF2INP	RF2IN N	PDET	NC	NC	VDD18_ BIAS	VDD12_ XTAL	XTALI	XTALO	BT_CLK _OUT
B	RF5INP	AGND	VDD18_ FE	VDD12_ LNA	VDD12 _BIAS	BIAS REF	NC	NC	VDD12D _SYN	VDD12_ BB	VDD18_ XTAL	BT_CLK _EN	DVDD12
C	RF5INN	VDD12_ FE			AGND	AGND	AGND	AGND	AGND			GPIO17	GPIO16
D	PA5 BIAS	NC										GPIO14	GPIO15
E	RF5 OUT	VDD18_ VCO	AGND		AGND	AGND	AGND	AGND	DVSS			DVDD_ GPIO1	DVDD_ GPIO0
F	VDD12_ TX5	VDD12_ SYNTH	AGND		AGND	AGND	AGND	AGND	DVSS		DVSS	GPIO12	GPIO13
G	XPA BIAS2	XPA BIAS5	AGND		AGND	AGND	AGND	AGND	DVSS		DVSS	GPIO10	GPIIO11
H	VCCFE M	LDO_ OUT	AGND		AGND	AGND	AGND	AGND	DVSS		DVSS	GPIO9	DVDD12
J	ANTA	VDDIO_ ANT	AGND		DVSS	DVSS	DVSS	DVSS	DVSS		DVSS	CLK_ REQ	DVDD12
K	ANTC	ANTB										SYS_ RST_L	CHIP_ PWD_L
L	ANTD	ANTE			DVSS	DVSS	DVSS	DVSS	DVSS			DVDD12	DVDD_ SDIO
M	AGND	GPIO0	GPIO2	DVDD12	GPIO4	GPIO6	GPIO8	TMS	TCK	TDO	SDIO_ DATA3	SDIO_ DATA2	SDIO_ CLK
N	DVDD12	GPIO1	GPIO3	DVDD_ BT	GPIO5	GPIO7	DVDD_ SDIO	DVDD12	TDI	DVDD_ SDIO	SDIO_ CMD	SDIO_ DATA1	SDIO_ DATA0

Table 6-2. **Signal to Pin/Bump Mapping**

Symbol	BGA Pin	CSP Bump	Type	Source or Destination	External PAD Power Supply	Description
Radio						
ANTA	J1	4	O	Antenna	VDD_ANT	Control signal for RF front end components
ANTB	K2	13	O	Antenna	VDD_ANT	Control signal for RF front end components
ANTC	K1	3	O	Antenna	VDD_ANT	Control signal for RF front end components
ANTD	L1	12	O	Antenna	VDD_ANT	Control signal for shared antenna switch
ANTE	L2	2	O	Antenna	VDD_ANT	Control signal for RF front end components
BIASREF	B6	35	IA		-	Reference for internal analog biasing
PDET	A6	55	IA	Power detector	-	External power detector input
RF2INN	A5	37	IA	RF input	-	2.4GHz RF input
RF2INP	A4	29	IA	RF input	-	2.4GHz RF input

Table 6-2. **Signal to Pin/Bump Mapping (continued)**

Symbol	BGA Pin	CSP Bump	Type	Source or Destination	External PAD Power Supply	Description
RF2OUTN	A2	10	OA	RF output	-	2.4GHz RF output
RF2OUTP	A3	20	OA	RF output	-	2.4GHz RF output
RF5OUT	E1	7	OA	RF output	-	5GHz RF output on AR6002X, NC on AR6002G
RF5INN	C1	8	IA	RF input	-	5GHz RF input on AR6002X, NC on AR6002G
RF5INP	B1	9	IA	RF input	-	5GHz RF input on AR6002X, NC on AR6002G
XPABIAS2	G1	5	OA	Analog output	-	Bias voltage for 2GHz external PA
XPABIAS5	G2	6	OA	Digital output	-	Bias voltage for 5GHz external PA on AR6002X, NC on AR6002G
Clock						
CLK_REQ	J12	99	O	-	DVDD_SDIO	Reference clock request signal
XTALI	A11	85	Crystal Input	40 MHz crystal	-	Reference crystal interface signal
XTALO	A12	86	Crystal Output	40 MHz crystal or external clock source	-	Reference crystal interface signal or external reference clock input
Digital Control (BT_ACTIVE, BT_FREQ, BT_PRIORITY, and RX_CLEAR are now mux'd with the GPIO signals)						
SYS_RST_L	K12	98	IH	-	DVDD_SDIO	Full chip reset input
CHIP_PWD_L	K13	89	I	-	DVDD_SDIO	Chip power down input
BT_CLK_EN	B12	96	I		AVDD18	Input enable signal for reference clock output
BT_CLK_OUT	A13	105	O		-	Buffered reference clock output
I^2C (I2C_SCL0 and I2C_SDA0 now mux'd with the GPIO signals)						
UART (RXD0, RXD0, UART_CTS_L and UART_RTS_L now mux'd with the GPIO signals)						
GSPI Master (SPI_CK, SPI_CS0_L, SPI_MISO, and SPI_MOSI now mux'd with the GPIO signals)						
SDIO						
SDIO_CLK	M13	88	I	-	DVDD_SDIO	Also GSPI clock
SDIO_CMD	N11	67	I	-	DVDD_SDIO	Also GSPI MOSI
SDIO_DATA_0	N13	97	I/O	-	DVDD_SDIO	Also GSPI MISO
SDIO_DATA_1	N12	87	I/O	-	DVDD_SDIO	Also GSPI host interrrupt
SDIO_DATA_2	M12	77	I/O	-	DVDD_SDIO	-
SDIO_DATA_3	M11	78	I/O	-	DVDD_SDIO	Also GSPI CS
GSPI Slave: GSPI pins are MUXed with SDIO pins						
GPIO						
GPIO0	M2	22	I/OL	-	DVDD_BT	BT_PRIORITY for Bluetooth coexistence

Table 6-2. **Signal to Pin/Bump Mapping (continued)**

Symbol	BGA Pin	CSP Bump	Type	Source or Destination	External PAD Power Supply	Description
GPIO1	N2	31	I/OL	-	DVDD_BT	WLAN_ACTIVE for Bluetooth coexistence
GPIO2	M3	11	I/OL	-	DVDD_BT	BT_FREQUENCY for Bluetooth coexistence
GPIO3	N3	1	I/OL	-	DVDD_BT	BT_ACTIVE for Bluetooth coexistence
GPIO4	M5	21	I/OL	-	DVDD_SDIO	SDIO/GSPI interface select
GPIO5	N5	30	I/OL	-	DVDD_SDIO	SDIO/GSPI interface select
GPIO6	M6	39	I/OL	-	DVDD_SDIO	-
GPIO7	N6	49	I/OL	-	DVDD_SDIO	TRST for JTAG debug interface
GPIO8	M7	38	I/OL	-	DVDD_BT	Optional external 32kHz clock input
GPIO9	H12	100	I/OL	—	DVDD_GPIO0	I2C SCL or SPI clock
GPIO10	G12	90	I/OL	—	DVDD_GPIO0	I2C SDA or SPI MISO
GPIO11	G13	101	I/OL	—	DVDD_GPIO0	UART RXD or SPI MOSI
GPIO12	F12	91	I/OL	—	DVDD_GPIO0	UART TXD or SPI CS_L
GPIO13	F13	102	I/OL	—	DVDD_GPIO0	Reset input for JTAG interface
GPIO14	D12	94	I/OL	—	DVDD_GPIO1	UART CTS
GPIO15	D13	103	I/OL	—	DVDD_GPIO1	UART RTS
GPIO16	C13	95	I/OL	—	DVDD_GPIO1	-
GPIO17	C12	104	I/OL	—	DVDD_GPIO1	-
Digital Test (EJTAG_SEL and TRST_L are Mux'd with the GPIO Signals)						
TCK	M9	59	IH	—	DVDD_SDIO	JTAG TCK input
TDI	N9	58	IH	—	DVDD_SDIO	JTAG TDI input
TDO	M10	68	OL	—	DVDD_SDIO	JTAG TDO output
TMS	M8	48	IH	—	DVDD_SDIO	JTAG TMS input

Table 6-3. **Pin/Bump Mapping for Power Supplies**

Symbol	BGA Pin	CSP Bump	Type	Voltage	Description
Power					
DVDD12	N1,M4,N8, L12,J13,H13, B13	24, 32, 40, 80, 81, 82, 83	P	Digital 1.2V core supply	
VDD12_SYNTH	F2	25	P	Analog 1.2V core supply	
VDD12_TX5	F1	26	P	Analog 1.2V core supply	
VDD12_FE	C2	27	P	Analog 1.2V core supply	
VDD12_LNA	B4	45	P	Analog 1.2V core supply	
VDD12D_SYN	B9	66	P	Analog 1.2V core supply	

Symbol	BGA Pin	CSP Bump	Type	Voltage	Description
VDD12_XTAL	A10	75	P	Analog 1.2V core supply	
VDD12_BIAS	B5	-	P	Analog 1.2V core supply	
VDD12_BB	B10	64, 76	P	Analog 1.2V core supply	
VDD18_FE	B3	28	P	Analog 1.8V I/O supply	
VDD18_VCO	E2	34	P	Analog 1.8V I/O supply	
VDD18_BIAS	A9	65	P	Analog 1.8V I/O supply	
PA5BIASP	D1	17	P	Analog 1.8V I/O supply	
VDD18_XTAL	B11	84	P	Analog 1.8V I/O supply	
DVDD_SDIO	N7,N10,L13	50, 69, 79	P	SDIO I/O supply	
DVDD_GPIO0	E13	92	P	GPIO0 I/O supply	
DVDD_GPIO1	E12	93	P	GPIO1 I/O supply	
DVDD_BT	N4	23	P	BT coexistence I/O supply	Bluetooth Coexistence I/O Supply
VCC_FEM	H1	33	P	Battery voltage LDO input	Battery Voltage LDO input (output is 3.0 V on LDO_OUT)
VDD_ANT	J2	14	P	Antenna control I/O supply	Antenna bias and control (can be tied to LDO_OUT)
LDO_OUT	H2	15	P	Battery voltage LDO output	LDO output (input is VCC_FEM)
DVSS	J5,L5,J6,L6, J7,L7,J8,L8, J9,L9,E9,F9, G9,H9,F11, G11,H11,J11	41, 51, 60, 70, 71, 72, 73	P	Digital ground	Digital Ground
AGND	E5,F5,G5,H5, E6,F6,G6, H6,E7,F7,G7, H7,E8,F8, G8,H8,E3,F3, G3,H3,J3, M1,C5,C6, C7,C8,C9,B2, A1	42, 43, 44, 52, 53, 54, 61, 62, 63	P	Analog ground	Analog Ground
Reserved Bumps					
NC	A7, A8, B7, B8	46, 47, 56, 57	RES	—	**NOTE:** For AR6002GZ, bumps 6-8 are also No Connect (NC).

7. Package Dimensions

BGA Dimensions

The BGA drawing and measurements are provided in Figure 7-1 and Table 7-1. The AR6002 family is available in:

- 7 x 7 mm, 0.5 mm pitch BGA or
- 0.4 mm pitch WLCSP package information available separately

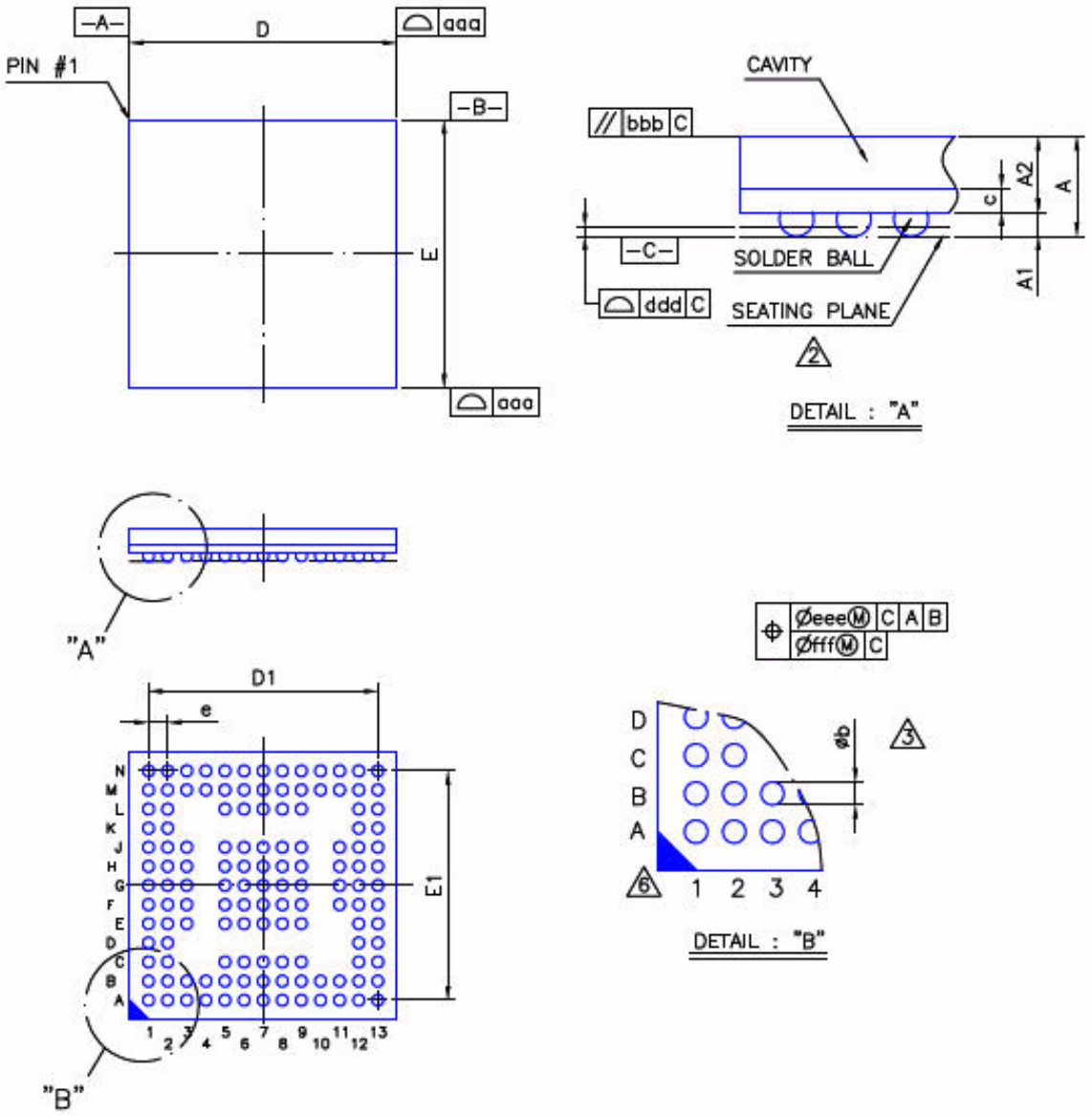

Figure 7-1. **BGA Drawing 7 x 7 mm Package**

Table 7-1. **BGA Dimensions**

Dimension Label	Min.	Nom.	Max.	Unit.	Min.	Nom.	Max.	Unit.
A	---	---	1.00	mm	---	---	0.039	inches
A1	0.16	0.22	0.28	mm	0.006	0.009	0.011	inches
A2	0.61	0.67	0.72	mm	0.024	0.026	0.028	inches
c	0.17	0.21	0.25	mm	0.007	0.008	0.010	inches
D	6.90	7.00	7.10	mm	0.272	0.276	0.280	inches
E	6.90	7.00	7.10	mm	0.272	0.276	0.280	inches
D1	---	6.00	---	mm	---	0.236	---	inches
E1	---	6.00	---	mm	---	0.236	---	inches
e	---	0.50	---	mm	---	0.020	---	inches
b	0.25	0.30	0.35	mm	0.010	0.012	0.014	inches
aaa	0.10			mm	0.004			inches
bbb	0.10			mm	0.004			inches
ddd	0.08			mm	0.003			inches
eee	0.15			mm	0.006			inches
fff	0.05			mm	0.002			inches
MD/ME	13/13			mm	13/13			inches

Notes:
1. Controlling dimension: Millimeters.
2. Minimum clearance of 0.25mm between edge of solder ball and body edge.

8. Ordering Information

The AR6002 may be ordered as follows:

- AR6002G-AC1E (802.11b/g BGA)
- AR6002GZ-BF1E-R (802.11b/g WLCSP)
- AR6002X-AC1E (802.11a/b/g BGA)
- AR6002XZ-BF1E-R (11a/b/g WLCSP)

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