AR6003 Single Chip 802.11n MAC/BB/Radio for Embedded Applications

General Description

The Atheros AR6003 is a single chip, small form factor IEEE 802.11 a/b/g/n MAC/baseband/radio optimized for low-power mobile applications. It is the 3rd generation WLAN design in the ROCm® family, employing the world's lowest power consumption WLAN architecture in the smallest possible form factor. The AR6003 is a single stream 1x1 802.11n implementation providing improved link robustness, extended range, increased throughput and better performance for an unparalleled user experience. The AR6003 is part of the Align™ product family.

The AR6003 family implements sophisticated design techniques to deliver a solution which will greatly extend the battery life of mobile and embedded systems. It leverages its near-zero power in idle and stand-by modes to enable users to leave WLAN "always-on" without impacting battery life.

The AR6003 family implements Atheros' proprietary Internal Efficient Power Amplifier™ (EPA) technology in CMOS with advanced linearization algorithms and an internal LNA, thereby reducing the BOM costs in the system design. It provides the option for an additional external PA for larger output power if needed.

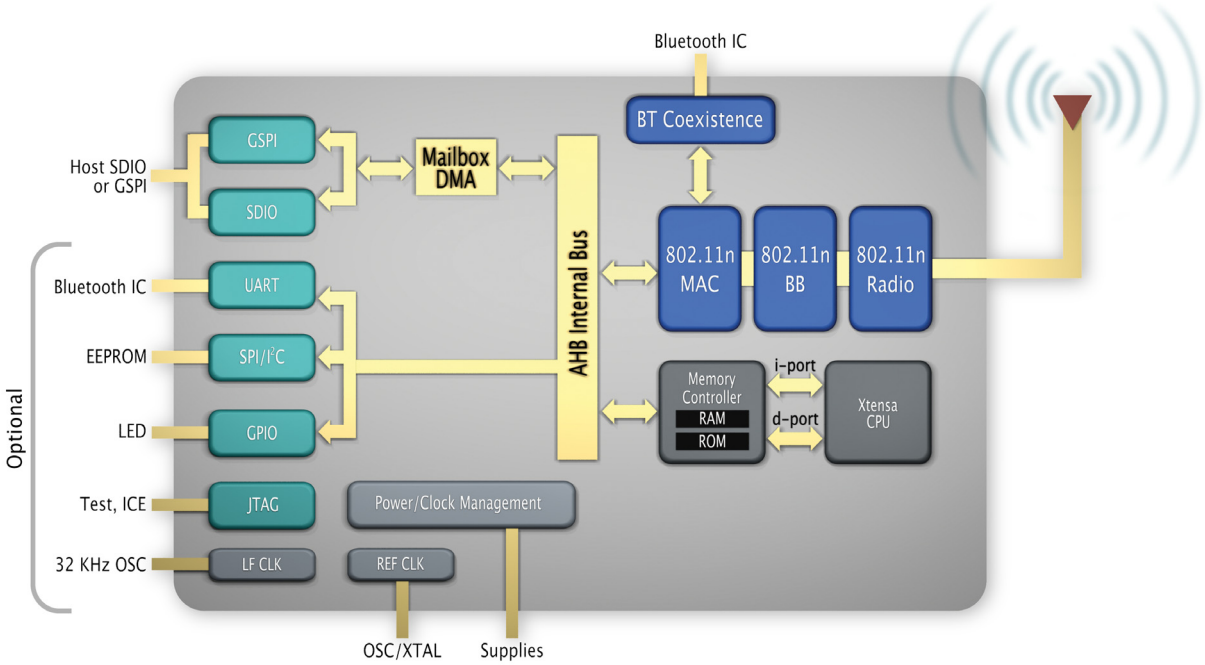
The AR6003 has additional LDOs to provide noise isolation for digital and analog supplies.

The AR6003 family supports 2-, 3-, and 4-wire Bluetooth coexistence protocols with advanced algorithms for predicting channel usage by a co-located Bluetooth transceiver.

The AR6003 family provides multiple peripheral interfaces including UART, SPI, I^2C, etc., via 26 GPIO pins. The only external clock source needed for AR6003-based designs is a high-speed crystal or oscillator. A variety of reference clocks are supported which include 19.2, 24, 26, 38.4, 40 and 52 MHz. AR6003 chips are available in Wafer Level Chip Scale Packages (WLCSP) or Ball Grid Arrays (BGA) packaging.

AR6003 Features

- All-CMOS IEEE 802.11a/b/g/n or 802.11b/g/n single-chip client
- Single stream 802.11n provides highest throughput and superior RF performance for handhelds.
- Advanced 1x1 802.11n features:
  - 40MHz channels at 5GHz
  - Full/Half Guard Interval
  - Frame Aggregation
  - Space Time Block Coding (STBC)
  - Low Density Parity Check (LDPC) Encoding
- Integrated high-output Atheros Efficient Power Amplifier™ and LNA for lowest BOM.
- Supports popular interfaces used in embedded designs: SDIO v2.0 (50MHz, 4-bit and 1-bit) and GSPI.
- Lowest power consumption in the industry with near zero in idle/standby modes, extending battery life.
- Integrated on-chip processor to minimize the loading on host processor.
- Supports 2/3/4-wire enhanced PTA scheme for use with any BT solution for optimal coexistence implementation.
- Supports several reference clocks from 19.2MHz to 52MHz.



AR6003 System Block Diagram

Table of Contents

1. Functional Description

1.1 Overview

The AR6003 is a single chip 802.11 a/b/g/n device based on cutting edge technology, optimized for low power embedded applications. The typical data path consists of the host interface, mailbox DMA, AHB, memory controller, MAC, BB, and radio. The CPU drives the control path via register and memory accesses. External interfaces include SDIO or GSPI, reference clock, and front-end components as well as optional connections such as UART, SPI/I2C, GPIO, JTAG, 32 kHz source. See the AR6003 block diagram.

1.2 XTENSA CPU

At the heart of the chip is the XTENSA CPU. This CPU has four interfaces:

- The Code RAM/ROM interface (iBus), going to the Memory Controller (MC).
- The Data RAM Interface (dBus), going to the MC
- The AHB interface, used mainly for register accesses.
- JTAG interface for debugging

1.3 Memory Controller (MC)

The MC contains 256 kBytes of ROM and 256 kBytes of RAM. It has three interfaces:

- iBus,
- dBus, and
- AHB interface.

Any one of these interfaces can request access to the ROM or RAM modules within the MC. The MC contains arbiters to serve these three interfaces on a first-come-first-serve basis.

1.4 AHB and APB Blocks

The AHB block acts as an arbiter. It has AHB interfaces from three Masters:

- MAC,
- MBOX (from the Host), and
- CPU.

See below for more on the MBOX and MAC. Depending upon the address, the AHB data request can go into one of the two slaves: APB block or the MC. Data requests to the MC are generally high-speed memory requests, while requests to the APB block are primarily meant for register access.

The APB block acts as a decoder. It is meant only for access to programmable registers within the AR6003's main blocks. Depending on the address, the APB request can go to one of the places listed below:

- Radio
- MC
- SI/SPI
- MBOX
- GPIO
- UART
- Real Time Clock (RTC), or
- MAC/BB

1.5 Master SI/SPI Control

The AR6003 has a master serial interface (SI) that can operate in two, three, or four-wire bus configurations to control EEPROMs or other I2C/SPI devices. Multiple I2C devices with different device addresses are supported by sharing the two-wire bus. Multiple SPI devices are supported by sharing the clock and data signals and using separate software-controlled GPIO pins as chip selects.

An SI transaction consists of two phases: a data transmit phase of 0-8 bytes followed by a data receive phase of 0-8 bytes. The flexible SI programming interface allows software to support various address and command configurations in I2C/SPI devices. In addition, software may operate the SI in either polling or interrupt mode.

1.6 GPIO

The AR6003 has 26 GPIO pins with direct software access. Many are multiplexed with other functions such as the host interface, UART, SI, Bluetooth coexistence, etc. (see Chapter 6 for details). Each GPIO supports the following configurations via software programming:

- Internal pull-up/down options
- Input available for sampling by a software register
- Input triggering an edge or level CPU interrupt

- Input triggering a level chip wakeup interrupt
- Open-drain or push-pull output driver
- Output source from a software register or the Sigma Delta Pulse-width Modulation (PWM) DAC

The AR6003 has one Sigma Delta PWM DAC that is shared by all of the GPIO pins. It allows the GPIO pins to approximate intermediate output voltage levels. The DAC has a period of 256 samples with a software controllable duty cycle. In applications where the AR6003 is driving LEDs using GPIO pins, the Sigma Delta PWM DAC can provide a continuous dimmer function.

1.7 MBOX

The MBOX is a service module to handle one of two possible external hosts: SDIO or GSPI. The AR6003 can handle only one of these hosts at any given time. The type of host the AR6003 uses depends upon the polarity of some package pins upon system power-up. The MBOX has two interfaces: an APB interface for access to the MBOX registers and an AHB interface which is used by the external host to access the MC memory or other registers within the AR6003.

1.8 HCI UART Over SDIO

The AR6003 has a high-speed UART which is intended to connect to an external Bluetooth chip though its HCI interface. This UART can directly transfer data between the Bluetooth device and the host.

1.9 Debug UART

The AR6003 includes a high-speed Universal Asynchronous Receiver/Transmitter (UART) interface that is fully compatible with the 16550 UART industry standard. This UART is a general purpose UART although it is primarily used for debug.

1.10 Reset Control

The AR6003 CHIP_PWD_L pin can be used to completely reset the entire chip. After this signal has been de-asserted, the AR6003 waits for host communication. Until then, the MAC, BB, and SOC blocks are powered off and all modules except the host interface are held in reset.

Once the host has initiated communication, the AR6003 turns on its crystal and later on its PLL. After all clocks are stable and running, the resets to all blocks are automatically de-asserted.

1.11 Reset Sequence

After a COLD_RESET event (e.g., the host toggles CHIP_PWD_L) the AR6003 will enter the HOST_OFF state and await communication from the host. From that point, the typical AR6003 COLD_RESET sequence is shown below:

1. When the host is ready to use the AR6003, it initiates communication via SDIO or GSPI.
2. The AR6003 enters the WAKEUP state then the ON state and enables the XTENSA CPU to begin executing ROM code. Software configures the AR6003 functions and interfaces. When the AR6003 is ready to receive commands from the host, it will set an internal function ready bit.
3. The host reads the ready bit and can now send function commands to the AR6003.
4. The CPU may continue to be held in reset under some circumstances until its reset is cleared by an external pin or when the host clears a register.
5. The MAC cold reset and the MAC/BB warm reset will continue to stay asserted until their respective reset registers are cleared by software.

1.12 Power Management Unit

The AR6003 has an integrated Power Management Unit (PMU) which generates all the power supplies required by its internal circuitry from external 3.3V and 1.8V supplies.

The main components of the PMU are as follows:

- A linear regulator (SREG) which converts the host IO supply to a 1.2V supply for some small control blocks which are turned on when CHIP_PWD_L is de-asserted.
- A linear regulator (DREG) which converts the 1.8V input to 1.2V for the bulk of AR6003 core digital circuitry.
- A linear regulator (AREG) which converts the 1.8V input to 1.2V for the AR6003 core analog circuitry.

1.13 Power Transition Diagram

The AR6003 provides integrated power management and control functions and extremely low power operation for maximum battery life across all operational states by:

- Gating clocks for logic when not needed
- Shutting down unneeded high speed clock sources
- Reducing voltage levels to specific blocks in some states

1.13.1 Hardware Power States

AR6003 hardware has five top level hardware power states managed by the RTC block. Table 1-1 describes the input from the MAC, CPU, SDIO/MBOX, interrupt logic, and timers that affect the power states.

1.13.2 Sleep State Management

Sleep state minimizes power consumption while saving system states. In SLEEP state, all high speed clocks are gated off and the external reference clock source is powered off. For the AR6003 to enter SLEEP state, the MAC, MBOX, and CPU systems must not be active.

The system remains in sleep state until a WAKEUP event causes the system to enter WAKEUP state, wait for the reference clock source to stabilize, and then ungate all enabled clock trees. The CPU wakes up only when an interrupt arrives, which may have also generated the system WAKEUP event.

Figure 1-1 depicts the state transition diagram.

Table 1-1. **Power Management States**

State	Description
OFF	CHIP_PWD_L pin assertion immediately brings the chip to this state.
	Sleep clock is disabled.
	No state is preserved.
HOST_OFF	WLAN is turned off.
	Only the host interface is powered on - the rest of the chip is power gated (off).
	The host instructs the AR6003 to transition to WAKEUP by writing a register in the host interface domain.
	Embedded CPU and WLAN do not retain state (separate entry).
	This state can be bypassed by asserting FORCE_HOST_ON_L during CHIP_PWD_L deassertion.
SLEEP	Only the sleep clock is operating.
	The crystal or oscillator is disabled.
	Any wakeup events (MAC, host, LF-Timer, GPIO-interrupt) will force a transition from this state to the WAKEUP state.
	All internal states are maintained.
WAKEUP	The system transitions from sleep states to ON.
	The high frequency clock is gated off as the crystal or oscillator is brought up and the PLL is enabled.
	WAKEUP duration is programmable.
ON	The high speed clock is operational and sent to each block enabled by the clock control register.
	Lower level clock gating is implemented at the block level, including the CPU, which can be gated off using the WAITI instruction while the system is on. No CPU, host and WLAN activities will transition to sleep states.

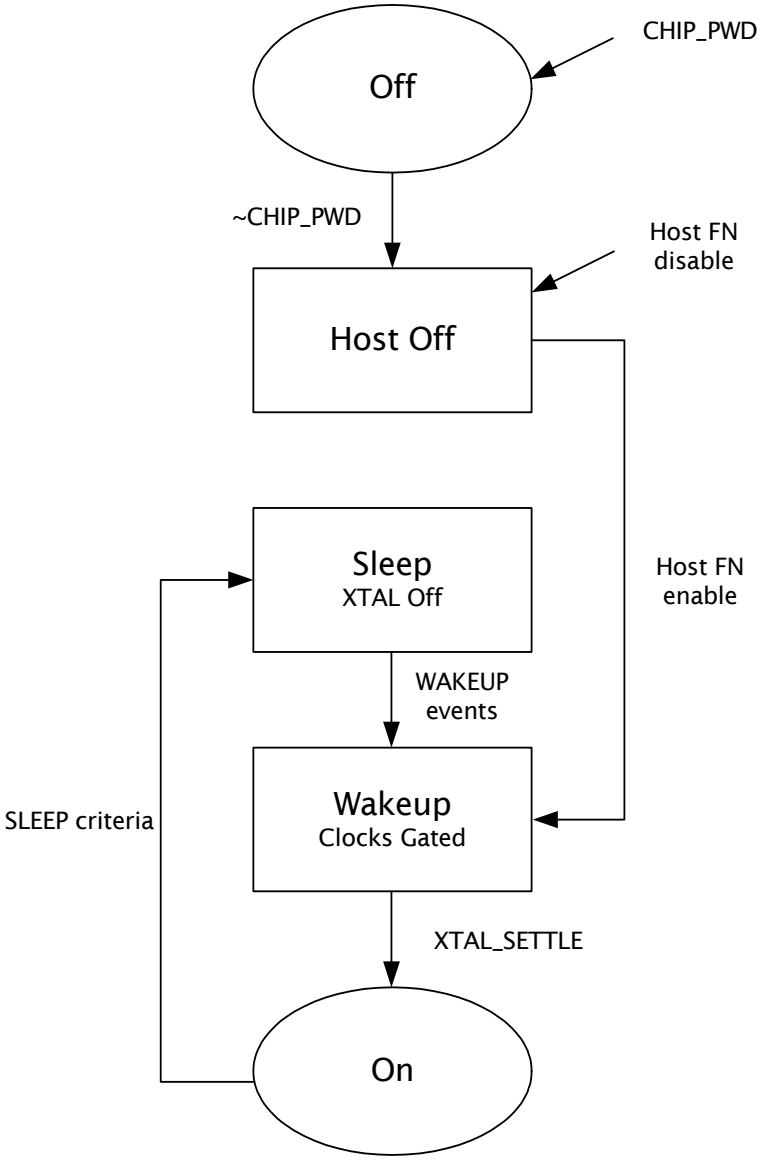


Figure 1-1. **AR6003 Power State**

1.14 System Clocking (RTC Block)

The AR6003 has an RTC block which controls the clocks and power going to other internal modules. Its inputs consist of sleep requests from these modules and its outputs consists of clock enable and power signals which are used to gate the clocks going to these modules. The RTC block also manages resets going to other modules with the device. The AR6003's clocking is grouped into two types: high-speed and low-speed.

1.14.1 High Speed Clocking

The reference clock source drives the PLL and RF synthesizer within the AR6003. It can be either an external crystal or oscillator. To minimize power consumption, the reference clock source is powered off in SLEEP, HOST_OFF, and OFF states. For an external crystal, the AR6003 disables the on-chip oscillator driver. For an external oscillator, the AR6003 de-asserts its CLK_REQ signal to indicate that a reference clock is not needed.

When exiting SLEEP state, the AR6003 waits in WAKEUP state for a programmable duration. During this time, the CLK_REQ signal is asserted to allow for the reference clock source to settle. The CLK_REQ signal remains asserted in ON state.

The AR6003 supports reference clock sharing in all power states. For an external crystal, the on-chip oscillator driver drives a reference clock output whenever an external clock request signal is asserted. For an external oscillator, the external clock request signal is forwarded on the CLK_REQ signal, and the input clock is passed along to the reference clock output.

1.14.2 Low-Speed Clocking

The AR6003 has eliminated the need for an external sleep clock source thereby reducing system cost. Instead, an internal ring oscillator is used to generate a low frequency sleep clock. It is also used to run the state machines and counters related to low power states.

The AR6003 has an internal calibration module which produces a 32.768 KHz output with minimal variation. For this, it uses the reference clock source as the golden clock. As a result, the calibration module adjusts for process and temperature variations in the ring oscillator when the system is in ON state.

The AR6003 also supports using an external low frequency sleep clock source in applications where one is already available.

1.14.3 Interface Clock

The host interface clock represents another clock domain for the AR6003. This clock comes from the SDIO or GSPI host and is completely independent from the other internal clocks. It drives the host interface logic as well as certain registers which can be accessed by the host in HOST_OFF and SLEEP states.

1.15 Front End Control

For applications that use external front-end components, the AR6003 provides the ability to control them with five antenna switch control outputs named as follows:

- ANTA
- ANTB
- ANTC
- ANTD
- ANTE

A programmable switch table indexed by transceiver state offers flexibility for various front-end configurations. The AR6003 supports antenna sharing with another wireless chip in all power states by using ANTE to control the shared antenna switch.

1.16 MAC/BB/RF Block

The AR6003 Wireless MAC consists of five major blocks:

- Host interface unit (HIU) for bridging to the AHB for MC data accesses and APB for register accesses
- Ten queue control units (QCU) for transferring TX data
- Ten DCF control units (DCU) for managing channel access
- Protocol control unit (PCU) for interfacing to baseband
- DMA receive unit (DRU) for transferring RX data

1.17 Baseband Block

The AR6003 baseband module (BB) is the physical layer controller for the 802.11a/b/g/n air interface. It is responsible for modulating data packets in the transmit direction, and detecting and demodulating data packets in the receive direction. It has a direct control interface to the radio to enable hardware to adjust analog gains and modes dynamically.

1.18 Design for Test

The AR6003 has a built in JTAG boundary scan of its pins. It also has features which enable testing of digital blocks via ATPG scan, memories via MBIST, analog components, and the radio.

2. Radio

The AR6003 transceiver consists of five major functional blocks (see Figure 2-1):

- Receiver (Rx)
- Transmitter (Tx)
- Frequency synthesizer (SYNTH)
- Associated bias/control (BIAS)
- Power Management Unit (PMU)

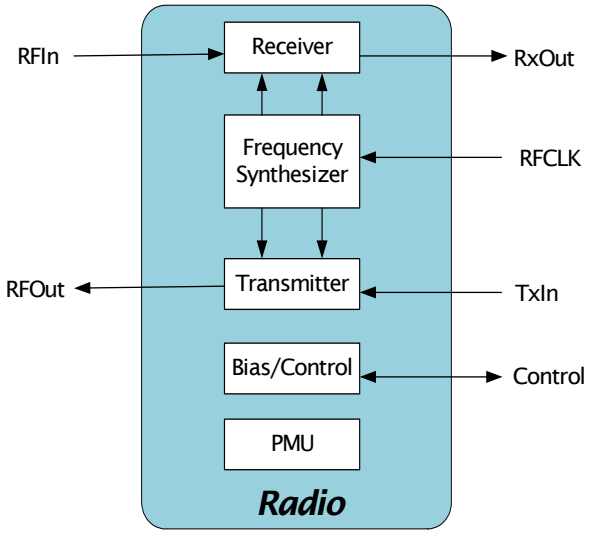


Figure 2-1. **Radio Functional Block Diagram**

2.1 Receiver (Rx) Block

The receiver converts an RF signal (with 40 MHz bandwidth) to baseband I and Q outputs. The receiver is tuned to 2.4 GHz and 5 GHz for IEEE 802.11 b/g/n and 802.11a/n signals, respectively. Figure 2-2 shows the Radio Tx/Rx block diagram.

For 5 GHz operation, the receiver is comprised of a low noise amplifier (LNA) followed by a variable gain amplifier (VGA), a radio frequency (RF) mixer, an intermediate frequency (IF) mixer, and a baseband programmable gain filter. This receiver is implemented using the sliding IF topology.

For 2 GHz operation, the receiver is comprised of an LNA, a direct conversion mixer, and a baseband programmable gain filter. This receiver is implemented using the direct conversion topology.

For both 5 GHz and 2 GHz paths, mixers down convert the signal to baseband in-phase (I) and quadrature-phase (Q) signals. The I and Q signals are low-pass filtered and amplified by the baseband programmable gain filter controlled by digital logic. The baseband I and Q signals are sent to the ADC. The baseband programmable gain filter is shared between the 2 GHz and 5 GHz paths.

The DC offset of the receive chain is reduced using multiple digital to analog converters (DACs) controlled by the MAC/baseband block. Additionally, the receive chain can be digitally powered down to conserve power.

.

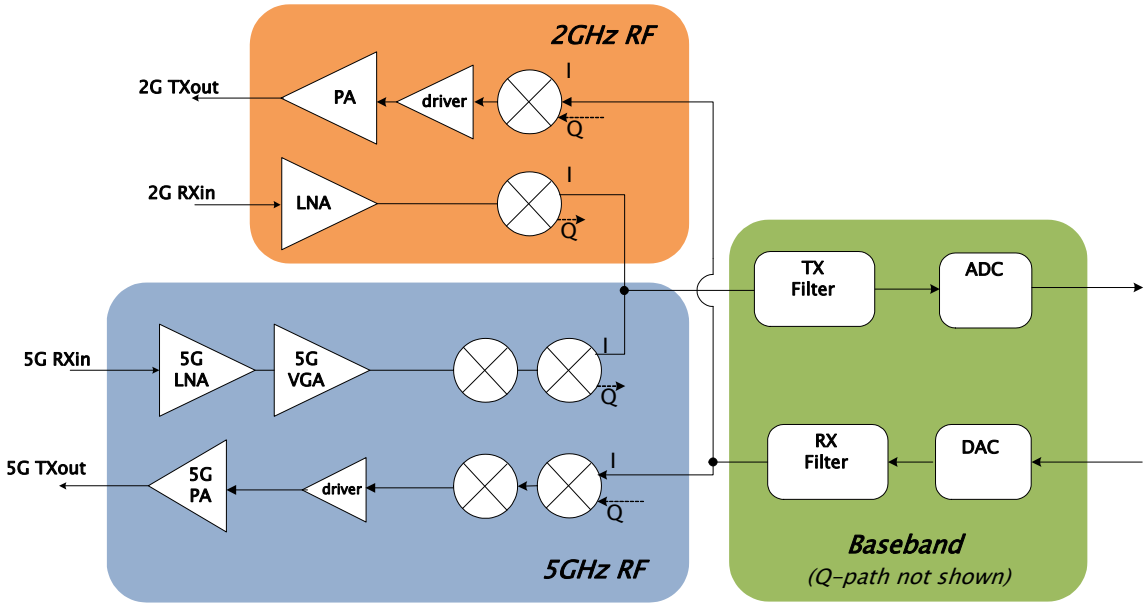


Figure 2-2. **Radio Tx/Rx Block Diagram**

2.2 Transmitter (Tx) Block

The transmitter converts baseband I and Q inputs to bands centered around 2.4 GHz and 5 GHz for IEEE 802.11 b/g/n and 802.11a/n signals respectively. A block diagram is shown in Figure 2-2.

The outputs of the DAC are low pass filtered through an on-chip reconstruction filter to remove spectral images and out-of-band quantization noise.

For 5 GHz operation, the transmitter is comprised of a programmable reconstruction filter, an IF mixer, an RF mixer, a preamplifier and a PA. The IF mixer converts baseband signals to an intermediate frequency. The RF mixer converts the IF signal into radio frequency signals, which are driven off chip through a preamplifier and the PA. This transmitter is implemented using the sliding IF topology.

For 2 GHz operation, the transmitter is comprised of a programmable reconstruction filter, a direct conversion mixer, a preamplifier and a PA. This transmitter is implemented using the direct conversion topology.

The transmit chain can be digitally powered down to conserve power. To ensure that FCC limits are observed and that output power stays close to the maximum allowed, the transmit output power is adjusted by a digitally programmable control loop at the start of each packet. The power control can also compensate for temperature variation.

2.3 Synthesizer (SYNTH) Block

The radio supports an on-chip synthesizer to generate local oscillator (LO) frequencies for the receiver and transmitter mixers. Figure 2-3 shows the synthesizer topology.

The synthesizer can use several crystals such as 19.2, 24, 26, 38.4, 40, and 52 MHz. For AR6003, the default crystal frequency is 26 MHz.

A reference circuitry generates a signal used as the synthesizer reference input. An on-chip voltage controlled oscillator (VCO) provides the desired LO signal based on a phase/ frequency locked loop. The loop filter

components are all integrated on-chip and can be digitally controlled.

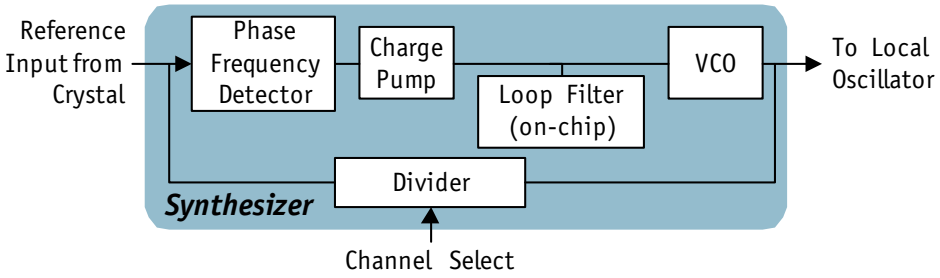


Figure 2-3. **Radio Synthesizer Block Diagram**

2.4 Bias/Control (BIAS) Block

The bias/control block provides reference voltages and currents for all other circuit blocks (see Figure 2-4). An on-chip bandgap reference circuit provides the needed voltage and current references based on an external 6.19 KΩ ± 1% shunted to GND resistor.

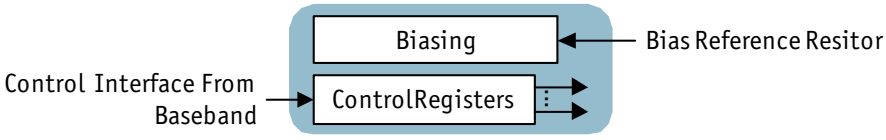


Figure 2-4. **Bias/Control Block Diagram**

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1 summarizes the absolute maximum ratings and Table 3-2 lists the recommended operating conditions for the AR6003. Absolute maximum ratings are those values beyond which damage to the device can occur.

Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

NOTE: Maximum rating for signals follows the supply domain of the signals.

Table 3-1. **Absolute Maximum Ratings**

Symbol (Domain)	Parameter	Max Rating	Unit
VREG	Digital 1.8V supply	-0.3 to 2.5	V
AVDD18	Analog 1.8V supply	-0.3 to 2.5	V
DVDD_SOC1	SOC1 GPIO I/O supply	-0.3 to 4.0	V
VDD18_XTAL	Clock sharing interface I/O supply (same as DVDD_SOC1)	-0.3 to 4.0	V
DVDD_SOC2	SOC2 GPIO I/O supply	-0.3 to 4.0	V
DVDD_SDIO	Host interface I/O supply	-0.3 to 4.0	V
VDD33_ANT	Antenna control I/O supply	-0.3 to 4.0	V
VDD33_PA	EPA supply	-0.3 to 4.0	V
PAREG_BASE	External 3.3V supply	-0.3 to 4.0	V
VBATTERY_42	External 3.3V supply	-0.3 to 4.0	V
RF_{in}	Maximum RF input (reference to 50-ohm input)	+10	dBm
T_{store}	Storage temperature	-45 to 135	°C
ESD	Electrostatic discharge tolerance		V

3.2 Recommended Operating Conditions

Table 3-2. **Recommended Operating Conditions**

Symbol (Domain)	Parameter	Min	Typ	Max	Unit
VREG	Digital 1.8V supply	1.71	1.8	1.89	V
AVDD18	Analog 1.8V supply	1.71	1.8	1.89	V
DVDD_SDIO	Host interface I/O supply	1.71		3.46	V
DVDD_SOC1	SOC1 GPIO I/O supply	1.71		3.46	V
VDD18_XTAL	Clock sharing interface I/O supply (same as DVDD_SOC1)	1.71		3.46	V
DVDD_SOC2	SOC2 GPIO I/O supply	1.71		3.46	V
VBATTERY_42	External 3.3V supply	2.97	3.3	3.63	V
VDD33_ANT	Antenna control I/O supply	1.71		3.46	V
VDD33_PA	EPA supply	2.97	3.3	3.63	V
PAREG_BASE	External 3.3V supply	2.97	3.3	3.63	V
$T_{ambient}$	Ambient temperature	-40		85	°C

3.3 DC Electrical Characteristics

Table 3-3 and Table 3-4 list the general DC electrical characteristics over recommended operating conditions (unless otherwise specified).

Table 3-3. **General DC Electrical Characteristics (For 3.3 V I/O Operation)**

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage						V
V_{IL}	Low Level Input Voltage						V
I_{IL}	Input Leakage Current	Without Pull-up or Pull-down					µA
		With Pull-up or Pull-down					µA
V_{OH}	High Level Output Voltage						V
							V
V_{OL}	Low Level Output Voltage						V
							V
C_{IN}	Input Capacitance[1]						pF

[1]Parameter not tested; value determined by design simulation

Table 3-4. **General DC Electrical Characteristics (For 1.8 V I/O Operation)**

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage						V
V_{IL}	Low Level Input Voltage						V
I_{IL}	Input Leakage Current	Without Pull-up or Pull-down					µA
		With Pull-up or Pull-down					µA
V_{OH}	High Level Output Voltage						V
							V
V_{OL}	Low Level Output Voltage						V
							V
C_{IN}	Input Capacitance[1]						pF

[1]Parameter not tested; value determined by design simulation

The following two figures show the recommended power up/down and reset sequences for the AR6003 using external 3.3V and 1.8V supplies.

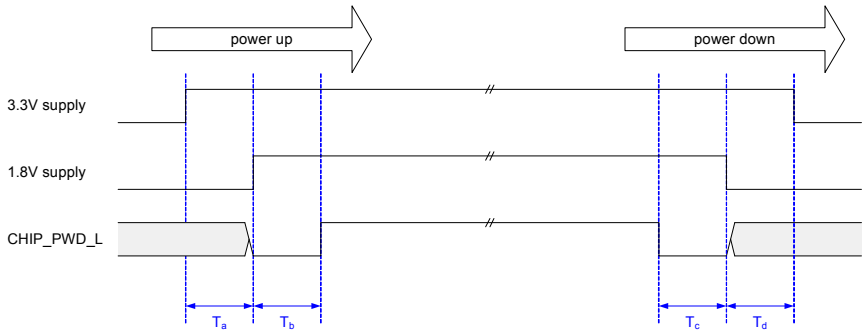


Figure 3-1. **Power Up/Power Down Timing**

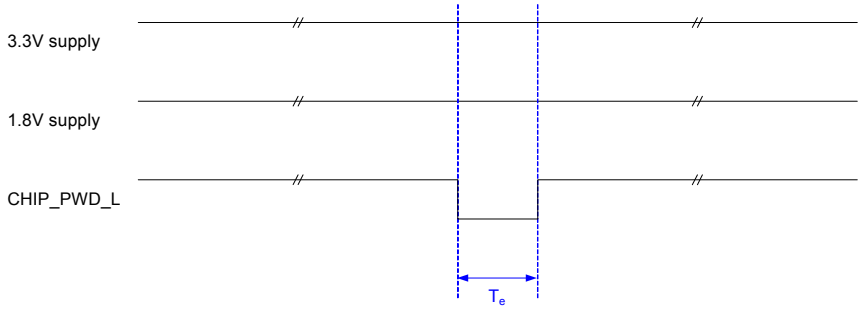


Figure 3-2. **Reset and Power Cycle Timing**

Table 3-5. **Timing Diagram Definitions**

	Description	**Min (**μsec)
T_a	Time between VBATT supply valid and I/O supply valid	
T_b	Time between I/O supply valid and CHIP_PWD_L deassertion	
T_c	Time between CHIP_PWD_L assertion and I/O supply invalid	
T_d	Time between 1.2V supply invalid and VBATT supply invalid	
T_e	Length of CHIP_PWDP_L pulse	

3.4 Radio Receiver Characteristics

Table 3-6, and Table 3-7 summarize the AR6003 receiver characteristics.

Table 3-6. **Receiver Characteristics for 2.4 GHz Operation**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{rx}	Receive input frequency range		2.412		2.484	GHz
NF	Receive chain noise figure (max gain)					dB
S_{rf}	Sensitivity					
	CCK, 1 Mbps	[1]		-97		dBm
	CCK, 2 Mbps			-93		
	CCK, 5.5 Mbps			-91		
	CCK, 11 Mbps			-89		
	OFDM, 6 Mbps			-92		
	OFDM, 9 Mbps			-92		
	OFDM, 12 Mbps			-91		
	OFDM, 18 Mbps			-88		
	OFDM, 24 Mbps			-85		
	OFDM, 36 Mbps			-82		
	OFDM, 48 Mbps			-77		
	OFDM, 54 Mbps			-75		
	HT20, MCS0			-92		
	HT20, MCS1			-90		
	HT20, MCS2			-88		
	HT20, MCS3			-84		
	HT20, MCS4			-81		
	HT20, MCS5			-77		
	HT20, MCS6			-76		
	HT20, MCS7			-74		
IP1dB	Input 1 dB compression (min. gain)					dBm
IIP3	Input third intercept point (min. gain)					dBm
ER_{phase}	I, Q phase error					degree
ER_{amp}	I, Q amplitude error					dB
R_{adj}	Adjacent channel rejection					
	OFDM, 6 Mbps	[1]		37		dB
	OFDM, 54 Mbps			23		
	HT20, MCS0			37		
	HT20, MCS7			20		
TR_{powup}	Time for power up					µs

[1]Performance based on the AR5BSD-00031A not including a cellular coexistence filter.

Table 3-7. **Receiver Characteristics for 5 GHz Operation**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{rx}	Receive input frequency range		4.90		5.925	GHz
NF	Receive chain noise figure (max gain)					dB
S_{rf}	Sensitivity					
	OFDM, 6 Mbps	[1]		-92		dBm
	OFDM, 9 Mbps			-91		
	OFDM, 12 Mbps			-90		
	OFDM, 18 Mbps			-88		
	OFDM, 24 Mbps			-84		
	OFDM, 36 Mbps			-81		
	OFDM, 48 Mbps			-77		
	OFDM, 54 Mbps			-75		
	HT20, MCS0			-92		
	HT20, MCS1			-90		
	HT20, MCS2			-88		
	HT20, MCS3			-84		
	HT20, MCS4			-81		
	HT20, MCS5			-77		
	HT20, MCS6			-76		
	HT20, MCS7			-74		
	HT40, MCS0			-88		
	HT40, MCS1			-87		
	HT40, MCS2			-84		
	HT40, MCS3			-80		
	HT40, MCS4			-78		
	HT40, MCS5			-73		
	HT40, MCS6			-72		
	HT40, MCS7			-70		
IP1dB	Input 1 dB compression (min. gain)					dBm
IIP3	Input third intercept point (min. gain)					dBm
ER_{phase}	I, Q phase error					degree
ER_{amp}	I, Q amplitude error					dB

Table 3-7. **Receiver Characteristics for 5 GHz Operation**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{adj}	Adjacent channel rejection					
	OFDM, 6 Mbps	[1]				dB
	OFDM, 54 Mbps					
	HT20, MCS0					
	HT20, MCS7					
	HT40, MCS0					
	HT40, MCS7					
TR_{powup}	Time for power up					µs

[1]Performance based on the AR5BSD-00032A not including a cellular coexistence filter.

3.5 Radio Transmitter Characteristics

Table 3-8 and Table 3-9 summarize the transmitter characteristics for AR6003.

Table 3-8. **Transmitter Characteristics for 2.4 GHz operation**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{tx}	Transmit output frequency range		2.412		2.484	GHz
P_{out}	Output power	[1]				
	11b mask compliant	1Mbps		17		dBm
	11g mask compliant	6Mbps		18		
	11n HT20 mask compliant	MCS0		17		
	11g EVM compliant	54Mbps		14		
	11n HT20 EVM compliant	MCS7		12		
SP_{gain}	PA gain step					dB
A_{pl}	Accuracy of power leveling loop	[2]		±1.5		dB
OP1dB	Output P1dB (max. gain)					dBm
OIP3	Output third order intercept point (max. gain)					dBm
SS	Sideband suppression					dBc
TT_{powup}	Time for power up					µs

[1]Performance based on the AR5BSD-00031A not including a cellular coexistence filter.
[2]Performance based on the AR5BSD-00031A after calibration.

Table 3-9. **Transmitter Characteristics for 5 GHz Operation**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{tx}	Transmit output frequency range		4.90		5.925	GHz
P_{out}	Output power	[1]				
	11a mask compliant	6Mbps		18		dBm
	11a EVM compliant	54Mbps		15		
	11n HT20 mask compliant	MCS0		17		
SP_{gain}	PA gain step					dB
A_{pl}	Accuracy of power leveling loop	[2]		±1.5		dB
OP1dB	Output P1dB (max. gain)					dBm
OIP3	Output third order intercept point (max. gain)					dBm
SS	Sideband suppression					dBc
TT_{powup}	Time for power up					µs

[1]Performance based on the AR5BSD-00032A which includes Tx/Rx antenna switch and xPA.
[2]Performance based on the AR5BSD-00032A after calibration.

3.6 AR6003 Synthesizer Characteristics

Table 3-10 and Table 3-11 summarize the synthesizer characteristics for the AR6003.

Table 3-10. **Synthesizer Composite Characteristics for 2.4 GHz Operation**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pn	Phase noise (at Tx_Out) At 30 KHz offset At 100 KHz offset At 500 KHz offset At 1 MHz offset					dBc/Hz
F_c	Center channel frequency	Center frequency at 5MHz spacing[1]	2.412		2.484	GHz
F_{ref}	Reference oscillator frequency	±20ppm		26[2]		MHz
F_{step}	Frequency step size (at RF)			1		MHz
TS_{powup}	Time for power up (from sleep)			0.2		ms

[1]Frequency is measured at the Tx output.
[2]Other supported frequencies are: 19.2, 24, 26, 38.4, 40, and 52MHz.

Table 3-11. **Synthesizer Composite Characteristics for 5 GHz Operation**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Pn	Phase noise (at Tx_Out) At 30 KHz offset At 100 KHz offset At 500 KHz offset At 1 MHz offset					dBc/Hz
F_c	Center channel frequency	Center frequency at 5MHz spacing[1]	4.90		5.925	GHz
F_{ref}	Reference oscillator frequency	±20ppm		26[2]		MHz
F_{step}	Frequency step size (at RF)	[3]		5		MHz
TS_{powup}	Time for power up (from sleep)	-		0.2		ms

[1]Frequency is measured at the Tx output.
[2]Other supported frequencies are: 19.2, 24, 26, 38.4, 40, and 52MHz.
[3]5MHz channel spacing is for the 5.725 to 5.925GHz band.

3.7 Typical Power Consumption Performance

Table 3-12. **AR6003 Typical Current Consumption – Low Power States (Individual Voltage Rails)**

Mode		Typical Current Consumption [mA]	
		1.8V[1]	3.3V[2]
Standby	OFF	0.000	0.004
	HOST_OFF	0.039	0.005
	SLEEP	0.222	0.005
IEEE PS[3]	DTIM=1	1.847	0.026
	DTIM=3	0.824	0.005
	DTIM=10	0.466	0.005

[1]VREG, VDD18_XTAL, DVDD_SOC1, DVDD_SDIO, DVDD_SOC2, VDD18_BB_SYNTH, VDD18_RF
[2]PAREG_BASE, VBATTERY_42, VDD33_ANT, VDD33_PA
[3]Calculated assuming Rx time of 2ms + 0.1* DTIM

3.7.1 Measurement Conditions for Low Power States

- T_ambient = 25C
- All I/O pins except CHIP_PWD_L are maintained at their default polarities (I/Os without default internal pulls are pulled low).

.

Table 3-13. **AR6003 Typical Current Consumption [2.4 GHz operation] – Continuous Receive (Individual Voltage Rails)**

Mode/Rate [Mbps]	Typical Current Consumption [mA]	
	1.8V[1]	3.3V[2]
CCK, 1 Mbps	74	3
CCK, 11 Mbps	75	3
OFDM, 6 Mbps	76	3
OFDM, 54 Mbps	78	3
HT20, MCS0	77	3
HT20, MCS7	79	3

[1]VREG, VDD18_BB, VDD18_SYNTH, VDD18_RF
[2]PAREG_BASE, VBATTERY_42, VDD18_XTAL, DVDD_SOC1, DVDD_SDIO, DVDD_SOC2, VDD33_ANT, VDD33_PA

3.7.2 Measurement Conditions for Continuous Receive [2.4 GHz Operation]

- T_ambient = 25C
- Measured using AR5BSD-00031A with AR6003 Atheros Radio Test software running in broadcast throughput receive mode

Table 3-14. **AR6003 Typical Current Consumption [2.4 GHz operation] – Continuous Transmit (Individual Voltage Rails)**

Mode/Rate [Mbps]	Target Output Power [dBm]	Typical Current Consumption [mA]	
		1.8V[1]	3.3V[2]
CCK, 1 Mbps	17	51	149
CCK, 11 Mbps	17	51	147
OFDM, 6 Mbps	18	56	159
OFDM, 54 Mbps	14	57	123
HT20, MCS0	17	56	150
HT20, MCS7	12	56	116

[1]VREG, VDD18_BB, VDD18_SYNTH, VDD18_RF
[2]PAREG_BASE, VBATTERY_42, VDD18_XTAL, DVDD_SOC1, DVDD_SDIO, DVDD_SOC2, VDD33_ANT, VDD33_PA

3.7.3 Measurement Conditions for Continuous Transmit [2.4 GHz Operation]

- T_ambient = 25C
- Measured using AR5BSD-00031A with AR6003 Atheros Radio Test software running in continuous transmit mode.
- Output power is targeted on AR5BSD-00031A not including a cellular coexistence filter.

.

Table 3-15. **AR6003 Typical Current Consumption [5 GHz operation] – Continuous Receive (Individual Voltage Rails)**

Mode/Rate [Mbps]	Typical Current Consumption [mA]	
	1.8V[1]	3.3V[2]
HT20, MCS7	91	12
HT40, MCS7	103	12

[1]VREG, VDD18_BB, VDD18_SYNTH, VDD18_RF
[2]PAREG_BASE, VBATTERY_42, VDD18_XTAL, DVDD_SOC1, DVDD_SDIO, DVDD_SOC2, VDD33_ANT, VDD33_PA

3.7.4 Measurement Conditions for Continuous Receive [5 GHz Operation]

- T_ambient = 25C
- Measured using AR5BSD-00032A with AR6003 Atheros Radio Test software running in broadcast throughput receive mode

Table 3-16. **AR6003 Typical Current Consumption [5 GHz operation] – Continuous Transmit (Individual Voltage Rails)**

Mode/Rate [Mbps]	Target Output Power [dBm]	Typical Current Consumption [mA]	
		1.8V[1]	3.3V[2]

[1]VREG, VDD18_BB, VDD18_SYNTH, VDD18_RF
[2]PAREG_BASE, VBATTERY_42, VDD18_XTAL, DVDD_SOC1, DVDD_SDIO, DVDD_SOC2, VDD33_ANT, VDD33_PA

3.7.5 Measurement Conditions for Continuous Transmit [5 GHz Operation]

- T_ambient = 25C
- Measured using AR5BSD-00032A with AR6003 Atheros Radio Test software running in continuous transmit mode.
- Output power is targeted on AR5BSD-00032A not including a cellular coexistence filter.

4. AC Specifications

4.1 Optional External 32 KHz Input Clock Timing

Figure 4-1 and Table 4-1 show the optional external 32 KHz input clock timing requirements.

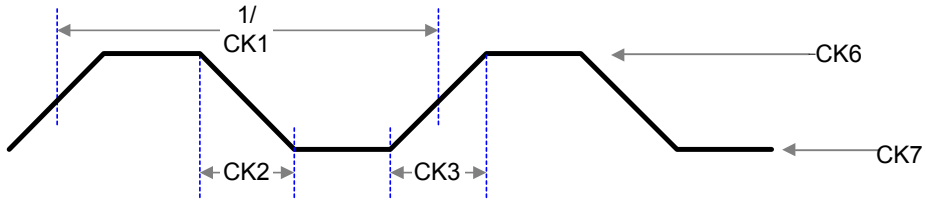


Figure 4-1. **External 32 KHz Input Clock Timing Requirements**

Table 4-1. **External 32 KHz Input Clock Timing**

Symbol	Description	Min	Typ	Max	Unit
CK1	Frequency	-	32.768	-	KHz
CK2	Fall time	1	-	100	ns
CK3	Rise time	1	-	100	ns
CK4	Duty cycle (high-to-low ratio)	15	-	85	%
CK5	Frequency stability	–50	-	50	ppm
CK6	Input high voltage				V
CK7	Input low voltage				V

4.2 External 19.2/24/26/38.4/40/52 MHz Reference Input Clock Timing

Figure 4-2 and Table 4-2 show the external 19.2/24/26/38.4/40/52 MHz reference input clock timing requirements.

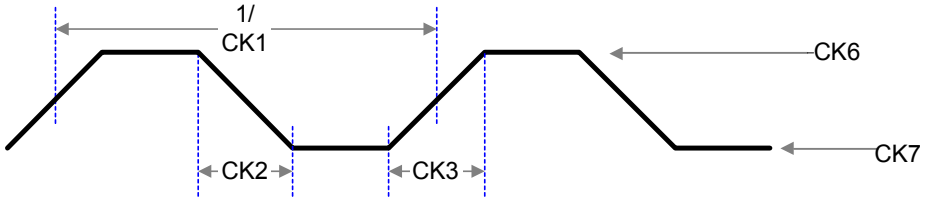


Figure 4-2. **External 19.2/24/26/38.4/40/52 MHz**

Table 4-2. **External 19.2/24/26/38.4/40/52 MHz Reference Input Clock Timing**

Symbol	Description	Min	Typ	Max	Unit
CK2	Fall time	-	-		ns
CK3	Rise time	-	-		ns
CK4	Duty cycle (high-to-low ratio)	40	-	60	%
CK5	Frequency stability	-20	-	20	ppm
CK6	Input high voltage				V
CK7	Input low voltage				V

4.3 SDIO/GSPI Interface Timing

Figure 4-3 shows the SDIO timing. Figure 4-4 shows the write timing for GSPI style transactions.

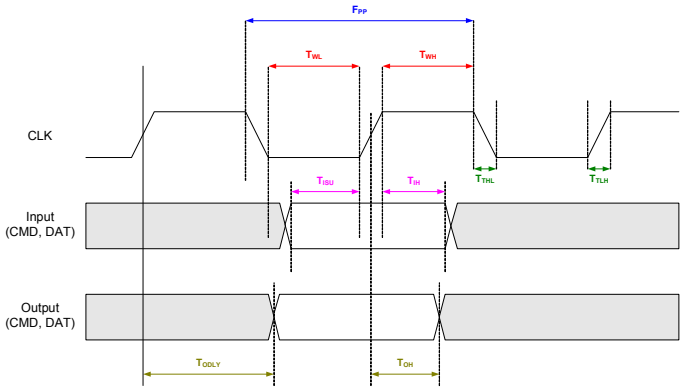


Figure 4-3. **SDIO 2.0 Timing**

.

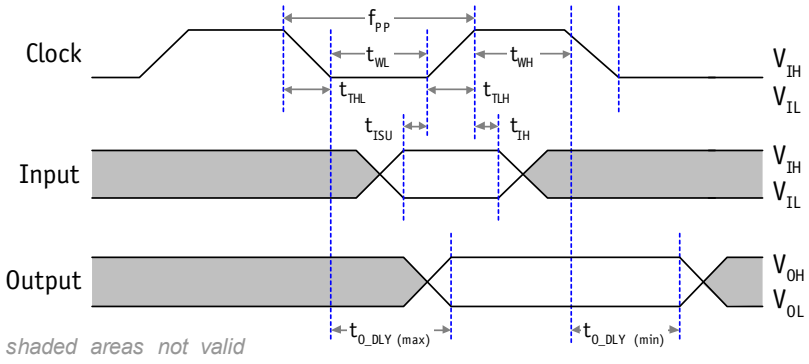


Figure 4-4. **GSPI Timing**

Table 4-3 shows the values for timing constraints for SDIO.

Table 4-3. **SDIO Timing Constraints**

Parameter	Description	Min	Max	Unit	Note
f_{PP}	Clock frequency data transfer mode	0	50	MHz	40 pF ≥ C_L
t_{WL}	Clock low time	7	-	ns	40 pF ≥ C_L
t_{WH}	Clock high time	7	-	ns	40 pF ≥ C_L
t_{TLH}	Clock rise time	-	10	ns	40 pF ≥ C_L
t_{THL}	Clock fall time	-	10	ns	40 pF ≥ C_L
t_{ISU}	Input setup time	6	-	ns	40 pF ≥ C_L
t_{IH}	Input hold time	2	-	ns	40 pF ≥ C_L
t_{OH}	Output hold time	2.5	-	ns	40 pF ≥ C_L
$t_{O\_DLY\ (min)}$	Output delay time during data transfer mode	0	14	ns	40 pF ≥ C_L

Table 4-4 shows the values for timing constraints for GSPI.

Table 4-4. **GSPI Timing Constraints**

Parameter	Description	Min	Max	Unit
f_{PP}	Clock frequency	0	48	MHz
t_{WL}	Clock low time	8.3	-	ns
t_{WH}	Clock high time	8.3	-	ns
t_{TLH}	Clock rise time	-	2	ns
t_{THL}	Clock fall time	-	2	ns
t_{ISU}	Input setup time	5	-	ns
t_{IH}	Input hold time	5	-	ns
t_{O_DLY}	Output delay	0	5	ns

5. Pin Descriptions

This section contains a listing of the signal descriptions (see Table 5-1 for the BGA package pin outs).

The following nomenclature is used for signal names:

NC	No connection should be made to this pin
_L	At the end of the signal name, indicates active low signals
P	At the end of the signal name, indicates the positive side of a differential signal
N	At the end of the signal name indicates the negative side of a differential signal

The following nomenclature is used for signal types described in Table 5-2:

IA	Analog input signal
I	Digital input signal
IO	Digital bidirectional signal
OA	An analog output signal
O	A digital output signal
P	A power or ground signal

Table 5-1 shows the BGA pinout.

Table 5-1. **BGA Package Pinout**

	1	2	3	4	5	6	7	8	9	10	11
A	RF2INP	RF2INN	RF5INP	RF5INN	RF2OUTP	RF2OUTN	RF5OUTP	RF5OUTN	GPIO_19	GPIO_21	GPIO_18
B	NC	VDD18_RF	GND	GND	VDD33_PA	VDD33_PA	GND	GPIO_22	GPIO_20	GPIO_17	GPIO_16
C	VDD12_BB	VDD12_SYNTH								DVDD_SOC2	GPIO_15
D	BIAS_REF	VDD18_SYNTH		GND	GND	GND	GND	DVDD12		GPIO_8	GPIO_7
E	ANTD	VDD18_BB		GND	GND	GND	GND	DVDD12		GPIO_6	GPIO_5
F	ANTC	ANTA		GND	GND	GND	GND	DVDD12		GPIO_14	GPIO_13
G	XPABIAS2	ANTB		GND	GND	GND	GND	GND_SWREG		GPIO_12	GPIO_11
H	XPABIAS5	ANTE		DVDD12	DVDD12	GND	GND_SWREG	GND_SWREG		GPIO_10	GPIO_9
J	XTALI	VDD33_ANT								DVDD_SDIO	SREG_OUT
K	XTALO	VDD18_XTAL	DVDD_SOC1	GPIO_0	GPIO_2	PM_MODE	PM_ENABLE	VBATTERY_42	VBATTERY_42	CHIP_PWD	DREG_OUT
L	GPIO_24	GPIO_25	GPIO_23	GPIO_1	GPIO_3	GPIO_4	PAREG_BASE	PAREG_VDD33_OUT	SWREG_OUT	SWREG_OUT	VREG

Table 5-2 shows the signal and pin descriptions.

Table 5-2. **Signal and Pin Descriptions**

Symbol	Type	External PAD Power Supply	Description
Radio			
ANTA	O	VDD33_ANT	Control signal for RF front end components
ANTB	O	VDD33_ANT	Control signal for RF front end components
ANTC	O	VDD33_ANT	Control signal for RF front end components
ANTD	O	VDD33_ANT	Control signal for RF front end components
ANTE	O	VDD33_ANT	Control signal for shared antenna switch
BIAS_REF	IA		Reference for internal analog biasing
RF2INN	IA		2.4 GHz RF input
RF2INP	IA		2.4 GHz RF input
RF5INN	IA		5 GHz RF input
RF5INP	IA		5 GHz RF input
RF2OUTN	OA		2.4 GHz RF output
RF2OUTP	OA		2.4 GHz RF output
RF5OUTN	OA		5 GHz RF output
RF5OUTP	OA		5 GHz RF output
XPABIAS2	OA		Bias Voltage for 2.4 GHz external PA
XPABIAS5	OA		Bias Voltage for 5GHz external PA
Clock			
GPIO_25	O	VDD18_XTAL	CLK_REQ signal indicating when a reference clock is needed.
GPIO_24	I	VDD18_XTAL	Clock request signal from BT chip
GPIO_23	O	1.2V	Reference clock output to BT chip
GPIO_21	I	DVDD_SOC2	Optional external input sleep clock
XTALI			Reference crystal interface signal
XTALO			Reference crystal interface signal or external reference clock input
Digital/MMU Control			
CHIP_PWD_L	I	DVDD_SDIO	Reset signal to power down the AR6003
PM_ENABLE			No connection should be made to this pin.
PM_MODE			No connection should be made to this pin.
SDIO			
GPIO_9	IO	DVDD_SDIO	SDIO command
GPIO_10	IO	DVDD_SDIO	SDIO data pin bit 3
GPIO_11	IO	DVDD_SDIO	SDIO data pin bit 2
GPIO_12	IO	DVDD_SDIO	SDIO data pin bit 1
GPIO_13	IO	DVDD_SDIO	SDIO data pin bit 0
GPIO_14	I	DVDD_SDIO	SDIO clock
BT Coexistence			
GPIO_0	I	DVDD_SOC1	BT FREQUENCY signal from BT chip
GPIO_1	O	DVDD_SOC1	WLAN ACTIVE signal to BT chip
GPIO_2	I	DVDD_SOC1	BT ACTIVE signal from BT chip
GPIO_3	I	DVDD_SOC1	BT_PRIORITY signal from BT chip
Digital Test			
GPIO_5	I	DVDD_SOC2	JTAG TMS Input

Table 5-2. **Signal and Pin Descriptions (continued)**

Symbol	Type	External PAD Power Supply	Description
GPIO_6	I	DVDD_SOC2	JTAG TCK Input
GPIO_7	I	DVDD_SOC2	JTAG TDI Input
GPIO_8	O	DVDD_SOC2	JTAG TDO Output
HCI UART			
GPIO_15	O	DVDD_SOC2	HCI UART TXD
GPIO_16	O	DVDD_SOC2	HCI UART RTS
GPIO_17	I	DVDD_SOC2	HCI UART RXD
GPIO_18	I	DVDD_SOC2	HCI UART CTS
Miscellaneous			
GPIO_4	I	DVDD_SOC1	Optional software GPIO
GPIO_19	I	DVDD_SOC2	GPIO_19 and GPIO_20 are used to select the host interface (SDIO or GSPI).
GPIO_20	I	DVDD_SOC2	
GPIO_22	O	DVDD_SOC2	Optional Wake On Wireless output
Supplies			
SWREG_OUT			No connection should be made to this pin.
VREG	P	1.8V	Digital 1.8V supply
PAREG_VDD33 _OUT			No connection should be made to this pin.
PAREG_BASE	P	3.3V	External 3.3V supply
VBATTERY_42	P	3.3V	External 3.3V supply
DREG_OUT	P	1.2V	Main 1.2V Output for digital core logic
SREG_OUT	P	1.2V	SREG output
DVDD12	P	1.2V	Digital 1.2V core supply
VDD18_XTAL	P	1.8V - 3.3V	Clock sharing interface I/O supply
DVDD_SOC1	P	1.8V - 3.3V	SOC1 GPIO I/O supply
DVDD_SDIO	P	1.8V - 3.3V	Host interface I/O supply
DVDD_SOC2	P	1.8V - 3.3V	SOC2 GPIO I/O supply
VDD33_ANT	P	3.3V	Antenna control I/O supply
VDD33_PA	P	3.3V	EPA supply
VDD18_BB	P	1.8V	Analog 1.8V supply
VDD18_SYNTH	P	1.8V	Analog 1.8V supply
VDD18_RF	P	1.8V	Analog 1.8V supply
VDD12_SYNTH	P	1.2V	Analog 1.2V supply
VDD12_BB	P	1.2V	Analog 1.2V output
GND	P		Analog/Digital ground

6. Package Dimensions

- 5 x 5 mm, 0.4 mm pitch BGA or
- 0.3 mm pitch WLCSP package information available separately

BGA Dimensions

The BGA drawing and measurements are provided in Figure 6-1 . Also seeTable 6-1 for BGA dimensions.

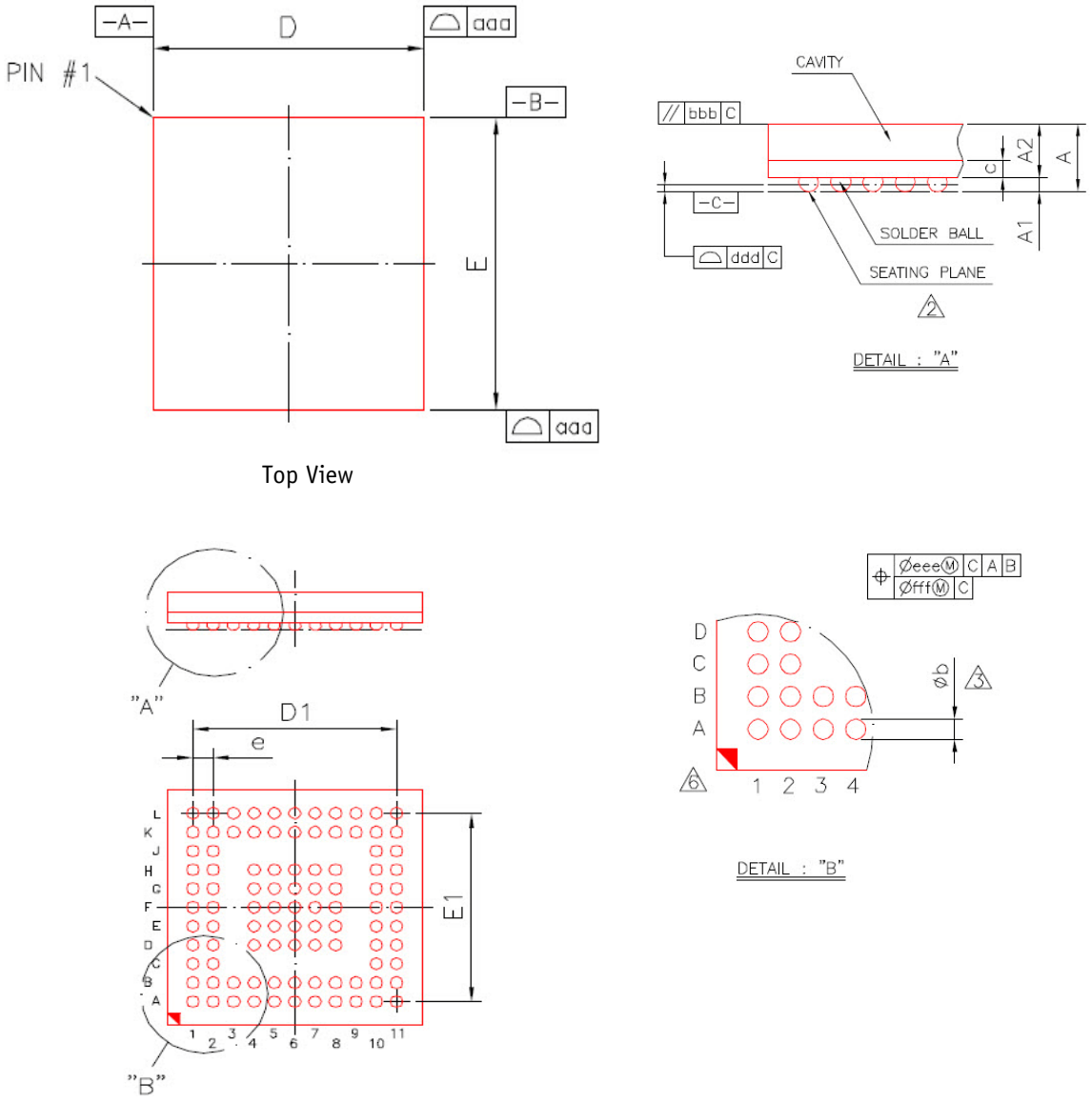


Figure 6-1. **BGA Drawing 5 x 5 mm Package**

Table 6-1. **BGA Dimensions**

Dimension Label	Min.	Nom.	Max.	Unit.	Min.	Nom.	Max.	Unit.
A	---	---	1.0	mm	---	---	0.039	inches
A1	0.13	0.18	0.23	mm	0.005	0.007	0.009	inches
A2	0.61	0.65	0.71	mm	0.024	0.026	0.028	inches
c	0.17	0.21	0.25	mm	0.007	0.008	0.010	inches
D	4.90	5.00	5.10	mm	0.193	0.197	0.201	inches
E	4.90	5.00	5.10	mm	0.193	0.197	0.201	inches
D1	---	4.00	---	mm	---	0.157	---	inches
E1	---	4.00	---	mm	---	0.157	---	inches
e	---	0.40	---	mm	---	0.016	---	inches
b	0.20	0.25	0.30	mm	0.008	0.010	0.012	inches
aaa	0.10			mm	0.004			inches
bbb	0.10			mm	0.004			inches
ddd	0.08			mm	0.003			inches
eee	0.15			mm	0.006			inches
fff	0.05			mm	0.002			inches
MD/ME	11/11			mm	11/11			inches

Notes:
1. Controlling dimension: Millimeters.
2. Minimum clearance of 0.25mm between edge of solder ball and body edge.

7. Ordering Information

The AR6003 may be ordered as follows:

- AR6003G-AC2B (2.4GHz, BGA)
- AR6003G-AC2B-R (2.4GHz, BGA, T&R)
- AR6003G-AF1B-R (2.4GHz, CSP, T&R)
- AR6003X-AC2B (2.4/5GHz, BGA)
- AR6003X-AC2B-R (2.4/5GHz, BGA, T&R)
- AR6003X-AF1B-R (2.4/5GHz, CSP, T&R)

MKG-1269 Rev. 4

Atheros Communications, Incorporated
5480 Great America Parkway
Santa Clara, CA 95054
t: 408/773-5200
f: 408/773-9940
www.atheros.com