National Semiconductor

MICROCIRCUIT DATA SHEET

MNAR629A-X REV 0A0

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GATE ARRAY (CMOS 1.5u)

General Description

The AR629A Terminal Controller (TC) is a bus interface device (terminal) meeting the requirements of the ARINC 629 Digital Autonomous Terminal Access Communication databus specification housing in a 180 CPGA. ARINC 629 is a multiple transmitter, broadcast type, autonomous terminal access, time division multiplex system that supports deterministic data communcation over a common single channel transmission medium. The databus protocol is Carrier Sense/Multiple Access-Clash Avoidance on bus (CS/MA-CA) permitting 100% utilization of the bus bandwidth during overload conditions. Equal terminal access to the bus is provided at all times.

Industry Part Number

AR629A-U9MIO

NS Part Numbers

AR629AU9/883

Prime Die

SCX6B150MIO

Controlling Document

5962-9958101QXC

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8	Functional tests at	+125
8	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

(Absolute Maximum Ratings)

(Note 1)

Vdd, Supply Voltage

MIN	MAX	UNITS
-0.5	+7.0	V

Vi, Vo Input or Output Voltage

MIN	MAX	UNITS
-.05	Vdd + 0.5	V

Ts, Storage Temperature

MIN	MAX	UNITS
-65	+150	C

Power Dissipation

500mW

Lead Temperature
No longer than 10 seconds

MIN	MAX	UNITS
	+300	C

Thermal Resistance, PGA Junction to Ambient
Zero Air Flow

MIN	MAX	UNITS
	+26	C/W

Note 1: Operation in excess of those max and min ratings listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated under (DC Characteristics) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Vdd, Supply Voltage

MIN	MAX	UNITS
4.75	5.25	V

Vi, Input Voltage

MIN	MAX	UNITS
Vss	Vdd	V

Vo, Output Voltage

MIN	MAX	UNITS
Vss	Vdd	V

Ta, Ambient Temperature

MIN	MAX	UNITS
-55	+125	C

Electrical Characteristics

DC PARAMETERS: DYNAMIC TESTS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vdd = Vcc = 5V ±5%, Vss = GND, -55 C<Ta<+125 C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
	Continuity Test	Upper Diode, Lower Diode			Pass			1, 2, 3
SIDD	Known State Idd	Vdd = 5V				6	mA	1, 2, 3
SISS	Known State Iss (Magnitude)	Vdd = 4.75V, Vdd = 5.0V, Vdd = 5.25V				1.5	mA	1, 2, 3
Cin	Input Capacitance	f = 1Mhz	1			20	pF	4
Cout	Output Capacitance	f = 1Mhz	1			20	pF	4
Vih	High level Input Voltage	Vdd = Vdd max, Vdd = Vdd min	2		2.0		V	1, 2, 3
Vil	Low Level Input Voltage	Vdd = Vdd max, Vdd = Vdd min	2			0.8	V	1, 2, 3
Voh	High Level Output Voltage	Vi = Vdd or Vss, Ioh = -20uA			Vdd-0.1		V	1, 2, 3
Vol	Low Level Output Voltage	Vi = Vdd or Vss, Iol = 20uA				0.1	V	1, 2, 3
Ioh	High Level Output Current	Vi = Vdd or Vss, Voh = Vdd -0.8V, Vdd = Vdd min				-4.0	mA	1, 2, 3
Iol	Low Level Output Current	Vi = Vdd or Vss, Vol = 0.4, Vdd = Vdd min			4.0		mA	1, 2, 3
Iil	Input Leakage Current	No Pull Resistor			-10	10	uA	1, 2, 3
Iih	Input Leakage Current	Vi = Vdd or Vss, Vdd = Vdd max			-10	10	uA	1, 2, 3
Ipu	Input Current With Pull-up Resistor	Vi = Vss or Vdd, Vdd = Vdd max			-200	20	uA	1, 2, 3
IOZH	Output leakage Current High, No Pull	Vo = Vdd, Vdd = Vdd max	3			10	uA	1, 2, 3
IOZL	Output leakage Current Low, No Pull	Vo = Vss, Vdd = Vdd max	3		-10		uA	1, 2, 3

Electrical Characteristics

DC PARAMETERS: FUNCTIONAL TESTS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vdd = Vcc = 5V ±5%, Vss = GND, -55 C<Ta<+125 C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
IOPL	Output Leakage Current - Pull-Up	Vo = Vss	3		-200		uA	1, 2, 3
IOPH	Output Leakage Current - Pull-Up	Vo = Vdd, Vdd = Vdd max				20	uA	1, 2, 3
DIDD	Dynamic Supply Current	FC = 32MHz, Vdd = Vdd max				110	mA	1, 2, 3
Vt+	Positive Going Schmitt Trigger Input Threshold	Vdd = Vdd max, Vdd = Vdd min				0.75 Vdd	V	1, 2, 3
Vt-	Negative Going Schmitt Trigger Input Threshold	Vdd = Vdd max, Vdd = Vdd min			1.0		V	1, 2, 3
VH	Schmitt Hysteresis Voltage	Vdd = Vdd max, Vdd = Vdd min			1.0		V	1, 2, 3
	Gross Functional	Vdd = 5.0V, Vdd = 4.75V, Vdd = 5.25V			Pass			7, 8
	Fmax Functional	Vdd = 5.0V, Vdd = 5.25V, Vdd = 4.75V			Pass			7, 8

AC: SUBSYSTEM READ CHARACTERISTICS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vdd = Vcc = 5V ±5%, Vss = GND, -55 C <TA<+125 C, CL = 50pF

TAAS	AD Setup Time to ASO High	Vdd = 4.75V, Vdd = 5.25V			3T-40	3T+25	nS	9, 10, 11
TBDMA	DMA Start To DMA Start	Vdd = 5V ±5%			315T		nS	9, 10, 11
TD3S	Delay from DSO rising edge to Tri-State	Vdd = 4.75V, Vdd = 5.25V			1T-20	1T+40	nS	9, 10, 11
TDAS	Delay from RICK to ASO Low	Vdd = 4.75V, Vdd = 5.25V			1T	1T+40	nS	9, 10, 11
TDBAH	BSAO High Delay from BUSA High					25	nS	9, 10, 11
TDBAK	BUSA Response Time	Vdd = 4.75V, Vdd = 5.25V			0	130T	nS	9, 10, 11
TDBAK1	BUSA Response Time (1 WAT)	Vdd = 5V ±5%			0	126T	nS	9, 10, 11
TDBAKW	BUSA Response Time (WAIT)	Vdd = 5V ±5%			0	122T-TWRWT	nS	9, 10, 11
TDBAL	BSAO Low Delay from BUSR High, BUSA Low					25	nS	9, 10, 11

Electrical Characteristics

AC: SUBSYSTEM READ CHARACTERISTICS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vdd = Vcc = 5V ±5%, Vss = GND, -55 C <TA<+125 C, CL = 50pF

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
TDBABR	Time from BUSA low to BUSR Tri-State	0 Wait				17T+61	nS	9, 10, 11
		1 Wait				21T+61	nS	9, 10, 11
		Max Wait				148T+61	nS	9, 10, 11
TDBRBA	BUSR High to BUSA High Delay				31		nS	9, 10, 11
TDBRQ	Delay from RICK to BUSR Low					80	nS	9, 10, 11
TDBSW	Time BUSA Low Prior to RICK				1T-10	5T+26	nS	9, 10, 11
TDDS	DSO Delay from RICK					80	nS	9, 10, 11
TDDSBR	DSO High to BUSR Tri-State	Vdd = 4.75V, Vdd = 5.25V			1T-20	1T+50	nS	9, 10, 11
TDIO	IOCK high after rising edge of RICK					37	nS	9, 10, 11
TDRDSH	RICK to DSO High	Vdd = 4.75V, Vdd = 5.25V			1T	1T+40	nS	9, 10, 11
TDRW	RWO Delay from RICK					80	nS	9, 10, 11
THASA	AD Hold Time from ASO High	Vdd = 4.75V, Vdd = 5.25V			2T-35	2T+40	nS	9, 10, 11
THAW	Wait Hold after RICK				22		nS	9, 10, 11
THDI	Data in Hold after RICK				30		nS	9, 10, 11
THDS	DSO Hold after WAIT	Vdd = 4.75V, Vdd = 5V ±5%			5T	9T+30	nS	9, 10, 11
THRW	RWO Hold after WAIT	Vdd = 4.75V, Vdd = 5V ±5%			6T	10T+30	nS	9, 10, 11
THWAS	ASO Hold after WAIT	Vdd = 5V ±5%			6T	10T+30	nS	9, 10, 11
TSDI	Data Setup Prior to RICK				30		nS	9, 10, 11
TSWA	WAIT Setup to RICK				22		nS	9, 10, 11
TWAS	ASO Pulse Width	Vdd = 4.75V, Vdd = 5.25V			2T-25	2T+25	nS	9, 10, 11

Electrical Characteristics

AC: SUBSYSTEM READ CHARACTERISTICS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vdd = Vcc = 5V ±5%, Vss = GND, -55 C <TA<+125 C, CL = 50pF

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
TWDS	DSO Pulse Width	Vdd = 4.75V, Vdd = 5.25V			6T-25		nS	9, 10, 11
TWRWT	Read WAIT Pulse Width	Vdd = 4.75V, Vdd = 5V ±5%				122T	nS	9, 10, 11
TWWH	WAIT Pulse Width High				4T+22		nS	9, 10, 11

AC: SUBSYSTEM WRITE CHARACTERISTICS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vdd = Vcc = 5V ±5%, Vss = GND, -55 C <TA<+125 C, CL = 50pF

TDASDS	Delay from ASO HIGH to DSO Low	Vdd = 4.75V, Vdd = 5.25V			4T-25	4T+25	nS	9, 10, 11
TDBAK	BUSA Response Time	TG = 2, Vdd = 5V ±5%			0	130T	nS	9, 10, 11
		TG = 3, Vdd = 5V ±5%			0	162T	nS	9, 10, 11
		TG = 4, Vdd = 5V ±5%			0	194T	nS	9, 10, 11
		TG = 5, Vdd = 5V ±5%			0	226T	nS	9, 10, 11
		TG = 6, Vdd = 5V ±5%			0	258T	nS	9, 10, 11
TDBAK1	BUSA Response Time (1WAT)	TG = 2, Vdd = 5V ±5%			0	126T	nS	9, 10, 11
		TG = 3, Vdd = 5V ±5%			0	158T	nS	9, 10, 11
		TG = 4, Vdd = 5V ±5%			0	190T	nS	9, 10, 11
		TG = 5, Vdd = 5V ±5%			0	222T	nS	9, 10, 11
		TG = 6, Vdd = 5V ±5%			0	254T	nS	9, 10, 11

Electrical Characteristics

AC: SUBSYSTEM WRITE CHARACTERISTICS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vdd = Vcc = 5V ±5%, Vss = GND, -55 C <TA<+125 C, CL = 50pF

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
TDBAKW	BUSA Response Time (WAIT)	TG = 2, Vdd = 5V ±5%			0	122T-TWWWT	nS	9, 10, 11
		TG = 3, Vdd = 5V ±5%			0	154T-TWWWT	nS	9, 10, 11
		TG = 4, Vdd = 5V ±5%			0	186T-TWWWT	nS	9, 10, 11
		TG = 5, Vdd = 5V ±5%			0	218T-TWWWT	nS	9, 10, 11
		TG = 6, Vdd = 5V ±5%			0	250T-TWWWT	nS	9, 10, 11
THDDS	Data Out to DSO Low	Vdd = 4.75V, Vdd = 5.25V			2T-35		nS	9, 10, 11
THDSD	Data Out Hold from DSO	Vdd = 4.75V, Vdd = 5.25V			1T-5	1T+25	nS	9, 10, 11
TRTDMA	Rcv DMA Start to Transmit DMA Start	TG = 2, Vdd = 5V ±5%			275T		nS	9, 10, 11
		TG = 3, Vdd = 5V ±5%			307T		nS	9, 10, 11
		TG = 4, Vdd = 5V ±5%			315T		nS	9, 10, 11
		TG = 5, Vdd = 5V ±5%			315T		nS	9, 10, 11
		TG = 6, Vdd = 5V ±5%			315T		nS	9, 10, 11
TWDS	DSO Pulse Width	Vdd = 4.75V, Vdd = 5.25V	4		4T-25		nS	9, 10, 11
TWWWT	Write WAIT Pulse Width	TG = 2, Vdd = 5V ±5%				122T	nS	9, 10, 11
		TG = 3, Vdd = 5V ±5%				154T	nS	9, 10, 11
		TG = 4, Vdd = 5V ±5%				186T	nS	9, 10, 11
		TG = 5, Vdd = 5V ±5%				218T	nS	9, 10, 11
		TG = 6, Vdd = 5V ±5%				250T	nS	9, 10, 11

Electrical Characteristics

AC: SUBSYSTEM WRITE CHARACTERISTICS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vdd = Vcc = 5V ±5%, Vss = GND, -55 C <TA<+125 C, CL = 50pF

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
TDBABR	Time from BUSA Low to BUSR Tri-State	0 WAIT, Vdd = 5V ±5%				17T+61	nS	9, 10, 11
		1 WAIT, Vdd = 5V ±5%				21T+61	nS	9, 10, 11
		MAX WAIT, Vdd = 4.75V				148T+61	nS	9, 10, 11

AC: INTERNAL REGISTER ACCESS CHARACTERISTICS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vdd = Vcc = 5V ±5%, Vss = GND, -55 C <TA<+125 C, CL = 50pF

TDASDS	Delay from ASO High to DSO falling edge				20		nS	9, 10, 11
TDCSAS	Delay from CS falling edge to ASO falling edge				0		nS	9, 10, 11
TDCSDS	Delay from DSO rising edge to CS rising edge				0		nS	9, 10, 11
TDCSFW	Delay from CS falling edge to WAIT High					26	nS	9, 10, 11
TDCSRW	Delay from CS rising edge to WAIT release					27	nS	9, 10, 11
TDHO	Data valid after rising edge of DSO				0		nS	9, 10, 11
TDSO	Error register Data valid after falling edge of DSO	Vdd = 5V ±5%				2T+25	nS	10, 11
TDSO	LWM/IVR DAta Valid after falling edge of DSO					40	nS	9, 10, 11
THAI	Address hold time after rising edge of ASO				15		nS	9, 10, 11
TSAI	Address setup time prior to rising edge of ASO				30		nS	9, 10, 11
TWAS	Address strobe pulse width				30		nS	9, 10, 11

Electrical Characteristics

AC: INTER. REG./REC. VALID & INTERRUPT VECTOR STROBE TIMING

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vdd = Vcc = 5V ±5%, Vss = GND, -55 C <TA<+125 C, CL = 50pF

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
TDAOA	Delay from AE Low to AO active	Vdd = 4.75V, Vdd = 5.25V	4		0	25	nS	9, 10, 11
TDAOZ	Delay from AE High to AO Tri-State	Vdd = 4.75V, Vdd = 5.25V	4		0	40	nS	9, 10, 11
TLRERF	RERF Pulse Width	Vdd = 5V ±5%			7T		nS	9, 10, 11
TLXERF	XERF Pulse Width	Vdd = 5V ±5%			7T		nS	9, 10, 11

AC: INTERNAL REGISTER/RECEIVE DATA CHARACTERISTICS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vdd = Vcc = 5V ±5%, Vss = GND, -55 C <TA<+125 C, CL = 50pF

TDBRIVS	Delay from BUSQ to leading RIVS Low	Vdd = 5V ±5%	5			90T	nS	9, 10, 11
TDBUSQ	Delay from end of last bit time to BUSQ				6T-40	7T+46	nS	9, 10, 11
TDBUSQ1	Delay from last word of string to BUSQ				5T-40	7T+46	nS	9, 10, 11
TDERR	Delay from BUSQ, to Error Reg. valid (non-NRBA)	Vdd = 4.75V, Vdd 5V ±5%			7T	64T	nS	9, 10, 11
TDERR	Delay from BUSQ, to Error Reg. valid (NRBA)	TG = 2; Vdd = 5V ±5%			160T		nS	9, 10, 11
TDERR	Delay from BUSQ, to Error Reg. valid(NRBA error on next to last date word)	Vdd = 5V ±5%				292T	nS	9, 10, 11
TDFSTAC	Delay from RIVS Low to STAC Low	Vdd = 4.75V, Vdd = 5.25V			5T-30	5T+35	nS	9, 10, 11
TDINT	Delay from BUSQ to IVR valid				68T	75T	nS	9, 10, 11
TDLRIVS	Time from RIVS Low to 12th bit time					5T	nS	9, 10, 11
TDLTRIVS	Delay from leading RIVS to trailing RIVS	Vdd = 5V ±5%	6			31T	nS	9, 10, 11

Electrical Characteristics

AC: INTERNAL REGISTER/RECEIVE DATA CHARACTERISTICS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vdd = Vcc = 5V ±5%, Vss = GND, -55 C <TA<+125 C, CL = 50pF

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
TDLWM	Delay from BUSQ, to LWM valid	Vdd = 5V ±5%			12T	20T	nS	9, 10, 11
TDRSTAC	Delay from RIVS High to Stac High	Vdd = 4.75V, Vdd = 5.25V			2T-30	2T+35	nS	9, 10, 11
TDTRIVS	Delay from end of DMA to trailing RIVS Low				2T	46T	nS	9, 10, 11
THRAL	AO hold after leading RIVS falling edge	Vdd = 5V ±5%			65T		nS	9, 10, 11
THRAT	AO hold after trailing RIVS falling edge	Vdd = 4.75V, Vdd = 5.25V			4T-35		nS	9, 10, 11
TSAR	AO setup prior to RIVS falling edge	Vdd = 4.75V, Vdd = 5.25V			2T-35		nS	9, 10, 11
TSDMA	Delay from end of last bit time to DMA start	Vdd = 4.75V, Vdd = 5V ±5%			13T	20T	nS	9, 10, 11
TWBUSQ	Width of BUSQ High during data sync					38T	nS	9, 10, 11
TWBUSQ1	Width Bus Quiet high during interstring gap					64T	nS	9, 10, 11
TWRIVS	RIVS pulse Low width	Vdd = 4.75V, Vdd = 5.25V			2T-10	2T+35	nS	9, 10, 11
TDAOBUSR	Time from AO valid to DMA start	Vdd = 5V ±5%			30T		nS	9, 10, 11

AC: INTERNAL REGISTER/TRANSMIT DATA CHARACTERISTICS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vdd = Vcc = 5V ±5%, Vss = GND, -55 C <TA<+125 C, CL = 50pF

TAODMA	Time from AO valid to DMA window start	Vdd = 5V ±5%			1T		nS	9, 10, 11
TDBUSQ	Delay from end of last bit time to BUSQ				6T-40	7T+46	nS	9, 10, 11
TDBUSQ1	Delay from last word of string to BUSQ	Vdd = 5V ±5%			5T-40	7T+46	nS	9, 10, 11

Electrical Characteristics

AC: INTERNAL REGISTER/TRANSMIT DATA CHARACTERISTICS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vdd = Vcc = 5V ±5%, Vss = GND, -55 C <TA<+125 C, CL = 50pF

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
TDERR	Delay from BUSQ to Error Reg. Valid (Non NXBA)	Vdd = 4.75V, Vdd = 5V ±5%			15T	124T	nS	9, 10, 11
TDERR	BUSQ to error register valid (NXBA)	Vdd = 5V ±5%			-340T		nS	9, 10, 11
TDFSTAC	Delay from XIVS to STAC Low	Vdd = 4.75V, Vdd = 5.25V			5T-30	5T+35	nS	9, 10, 11
TDINT	Delay from IVR valid to XIVS				14T	20T	nS	9, 10, 11
TDLWM	Delay from BUSQ to LWM valid	Vdd = 5V ±5%				20T	nS	9, 10, 11
TDLXIVS	Delay from 3rd bit to leading XIVS	Vdd = 4.75V, Vdd = 5.25V			3T-35	3T+55	nS	9, 10, 11
TDRSTAC	Delay from XIVS to STAC High	Vdd = 4.75V, Vdd = 5.25V			2T-30	2T+35	nS	9, 10, 11
TDTXIVS	Delay from parity bit to trailing XIVS	Vdd = 4.75V, Vdd = 5V ±5%			48T	96T	nS	9, 10, 11
THXAL	AO hold after leading XIVS falling edge	Vdd = 5V ±5%			65T		nS	9, 10, 11
THXAT	AO hold after trailing edge of XIVS falling	Vdd = 4.75V, Vdd = 5.25V			4T-35		nS	9, 10, 11
TSAX	AO setup prior to falling edge of XIVS	Vdd = 4.75V, Vdd = 5.25V			2T-35		nS	9, 10, 11
TSDMA	Delay from bit 7 to DMA start	Vdd = 4.75V, Vdd = 5.25V			13T-35	13T+60	nS	9, 10, 11
TWBUSQ	Width of BUSQ High during data sync	Vdd = 5V ±5%			30T	38T	nS	9, 10, 11
TWBUSQ1	BUS Quiet High during interstring gap	Vdd = 5V ±5%			55T	64T	nS	9, 10, 11
TWXIVS	XIVS pulse Low width	Vdd = 4.75V, Vdd = 5.25V			2T-10	2T+35	nS	9, 10, 11

Electrical Characteristics

AC: PERSONALITY PROM INTERFACE (XPP/RPP/MPP) CHARACTERISTICS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vdd = Vcc = 5V ±5%, Vss = GND, -55 C <TA<+125 C, CL = 50pF

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
TDCLXCS	Delay from CLRX High to XCS Low	Vdd = 5V ±5%			24T	27T+9	nS	9, 10, 11
TDEXST	Delay from EXST High to STAC Low		7			3T+35	nS	9, 10, 11
TDSTEX	Delay from STAC Low to EXST High		8			5T+35	nS	9, 10, 11
THBEX	EX3-0 output hold after EXT. strobe	Vdd = 4.75V, Vdd = 5.25V			2T-10		nS	9, 10, 11
THRB	BUS1 address hold time after RICK	Single Byte			2T		nS	9, 10, 11
THRB2	BUS2 data input to RICK hold time				60		nS	9, 10, 11
THRCS	Receive PROM chip select hold after RICK				2T		nS	9, 10, 11
THRLS	Load Strap hold time after RICK				2T		nS	9, 10, 11
THRRZ	RZ2-0 address hold time after RICK				2T		nS	9, 10, 11
THRXX	XX address hold time after RICK				2T		nS	9, 10, 11
THRXY	XY address hold time after RICK				2T		nS	9, 10, 11
THRXZ	XZ address hold time after RICK				2T		nS	9, 10, 11
THXCS	Transmit PROM chip select hold after RICK				2T		nS	9, 10, 11
TMHR	Minimum data hold time				60		nS	9, 10, 11
TMSR	Minimum data setup time				30		nS	9, 10, 11
TSBEX	EX3-0 output stable before EXT. strobe	Vdd = 4.75V, Vdd = 5.25V			6T-35		nS	9, 10, 11
TSRB	BUS1 address setup time prior to RICK	Single byte, Double byte, Triple byte			14T-150		nS	9, 10, 11
TSRB2	BUS2 data input to RICK setup time				30		nS	9, 10, 11

Electrical Characteristics

AC: PERSONALITY PROM INTERFACE (XPP/RPP/MPP) CHARACTERISTICS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vdd = Vcc = 5V ±5%, Vss = GND, -55 C <TA<+125 C, CL = 50pF

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
TSRLS	Load Strap setup time prior to RICK	Vdd = 4.75V, Vdd = 5.25V			14T-70		nS	9, 10, 11
TSRRZ	RZ2-0 address setup time prior to RICK	Single byte, Double byte, Triple byte			14T-150		nS	9, 10, 11
TSRXX	XX address setup time prior to RICK	Single byte, Double byte, Triple byte			14T-150		nS	9, 10, 11
TSRXY	XY address setup time prior to RICK	Single byte, Double byte, Triple byte			14T-150		nS	9, 10, 11
TSRXZ	XZ address setup time prior to RICK	Single byte, Double byte, Triple byte			14T-150		nS	9, 10, 11
TWCLRX	CLRX Pulse Width	Vdd = 4.75V, Vdd = 5.25V			2T-10	2T+20	nS	9, 10, 11
TWEXST	Extension Strobe Pulse width	Vdd = 4.75V, Vdd = 5.25V			2T-10		nS	9, 10, 11
TWRCS	Receive PROM chip select setup time	Single byte, Double byte, Triple byte			14T-40		nS	9, 10, 11
TWXCS	Transmit PROM chip select setup time	Single byte, Double byte, Triple byte			14T-40		nS	9, 10, 11

Electrical Characteristics

AC: SERIAL TRANSMIT CHARACTERISTICS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vdd = Vcc = 5V ±5%, Vss = GND, -55 C <TA<+125 C, CL = 50pF

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
T1	Time from TXHB Low to TXO rising edge	Vdd = 4.75V, Vdd = 5.25V			1T-12	2T+24	nS	9, 10, 11
T2	Time from TXHB High to TXO falling edge	Vdd = 4.75V, Vdd = 5.25V			1T-12	1T+24	nS	9, 10, 11
TDGAST	Time from GA rising edge to STAC falling edge	Vdd = 5V ±5%			104T	110T	nS	9, 10, 11
TWGA	GA pulse Width	Vdd = 4.75V, Vdd = 5.25V			3T-14	4T+10	nS	9, 10, 11
TWDB	Data bit pulse width	Vdd = 4.75V, Vdd = 5.25V	9		16T-15		nS	9, 10, 11
TWHDB	1/2 Data bit pulse width	Vdd = 4.75V, Vdd = 5.25V	10, 11		8T-15		nS	9, 10, 11
TWPPSSP	PPSSP pulse width	Vdd = 4.75V, Vdd = 5.25V	10		8T-10	10T+25	nS	9, 10, 11
TWPSSP	PSSP pulse width	Vdd = 4.75V, Vdd = 5.25V	10		8T-15		nS	9, 10, 11

AC: XICK/RICK CHARACTERISTICS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vdd = Vcc = 5V ±5%, Vss = GND, -55 C <TA<+125 C, CL = 50pF

FC	Receive or Transmit input Clock Freq.	Vdd = 5V ±5%			0	32.32	Mhz	9, 10, 11
TC	Clock period	Vdd = 5V ±5%, TS = 1/FC			30.94		nS	9, 10, 11
TDIO	Propagation Delay from RICK to IOCK		4			37	nS	9, 10, 11
TWH	Clock Pulse Width, High	Vdd = 4.75V, Vdd = 5.25V	12		0.33T	0.67T	nS	9, 10, 11
TWL	Clock Pulse Width, Low	Vdd = 4.75V, Vdd = 5.25V	12		0.33T	0.67T	nS	9, 10, 11

AC: SPECIAL TEST

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vdd = Vcc = 5V ±5%, Vss = GND, -55 C <TA<+125 C, CL = 50pF

THDATA	Hold Time of ADDATA Bus after falling edge of DSO	Vdd = 4.75V, Vdd = 5.25V				5	nS	9, 10, 11

(Continued)

Note 1: Tested during initial qual only and after process/design changes; tested at 25 C only.
Note 2: TTL input only.
Note 3: All output leakage current is measured at tri-state.
Note 4: Same as NSC symbol TDAE.
Note 5: Same as NSC symbol TDBUSQRIVS.
Note 6: Same as NSC symbol TDRIVSRIVS.
Note 7: Same as NSC symbol TDES.
Note 8: Same as NSC symbol TDSE.
Note 9: Same as NSC symbol TWTXO.
Note 10: These parameters are measured at 2.0V on the rising and falling edges of a high pulse and extrapolated to 0.8V on the rising and falling edges of a low pulse.
Note 11: Same as NSC symbol TWTXOH and TWTXOL.
Note 12: TWH is measured from 0.75Vdd on the clock rising edge and 0.75Vdd -1.0V on the clock falling edge. TWL is measured from 1V on the clock falling edge and 2V on the clock rising edge. The clock used to measure these parameters has a minimum slew rate of 1.0V/nS.

Burn-in/QCI Electrical End-Point Tests

OP#	Operation description	Sub-Groups
01	Group C end-point electrical parameters	1,2
02	Group D end-point electrical parameters	1,2

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0003455	06/15/99	Rose Malone	Initial MDS Release: MNAR629A-X, Rev. 0A0 (New SMD Dwg. 5962-9958101QXC)