ARK7116

Multiple Standards

Digital Video Decoder

(Primarily & Brief)

Version 1.0

2014.10

Revision Record:

Date	Revision	Modification Description
2014-10	V1.0	Initial Version

1. General Description

ARK7116 is a composite video broadcast signal（CVBS）decoder SoC integrating following function blocks, a 1-channel analog preprocessing circuit, 10-bit A/D converters(ADC), an automatic clamp and gain control(AGC), a clock generation circuit (CGC), digital multi-standard decoder (support PAL, NTSC, and SECAM), brightness, contrast, hue and saturation control circuit etc. ARK7116 converts composite video broadcast signal（CVBS） including weak and distorted signals into standard ITU656 YUV 4:2:2 component video. ITU601 output up to 1024*768.

2. Features

- Composite video signal Input; Multiple standards supported: NTSC M, NTSC N, NTSC 4.43 and NTSC-Japan; PAL (B, D, G, H, I, M, N, etc.), SECAM (D, K, K1, L, B, G)
- Four Analog Inputs: 3xCVBS Inputs, internal analog sources selectors
- One analog processing channel including anti-aliasing filter
- ITU601 output up to 1024*768
- One 10-bit CMOS video Analog-to-Digital Converters (ADCs)
- On-chip clock generator
- Line-locked system clock frequencies
- Digital PLL for horizontal sync processing and clock generation, horizontal and vertical sync detection
- Only One Crystal (27 MHz) required for All Standards
- Adaptive 2-D Comb Filter for Luminance and Chrominance Separation
- Precise Chrominance Demodulation
- PAL delay line for correcting PAL phase errors
- Video Noise Reduction
- Automatic detection of 50 and 60 Hz field frequency, and automatic switching between NTSC, PAL and SECAM standards
- Automatic detection of 3.58MHz and 4.43MHz color subcarrier frequency

- Brightness, contrast, saturation, hue, and sharpness control through I2C
- Standard ITU 656 YCbCr 4 : 2 : 2 format (8-bit) on output bus
- Enhanced ITU 656 output format on output bus, containing: active video; raw CVBS data for INTERCAST applications (27 MHz data rate)
- Cropping enables the user to output any subsection of the video image. The cropping area can be programmed to start and stop at any position on the video frame.
- Single +3.3V Power supply, Build-in LDO for 1.2V core power and external power
- 40-pin QFN package
- Power saving mode by chip enable input
- Programming via I2C bus (slave-address:0XB0 0XB2 0XB4 0XB6 0XB8)

3. Application Field

- TV Box and Security
- Portable TV and car entertainment
- Digital photo frame with analog TV
- Other application need AV to ITU656 or ITU601

4. Block Diagram

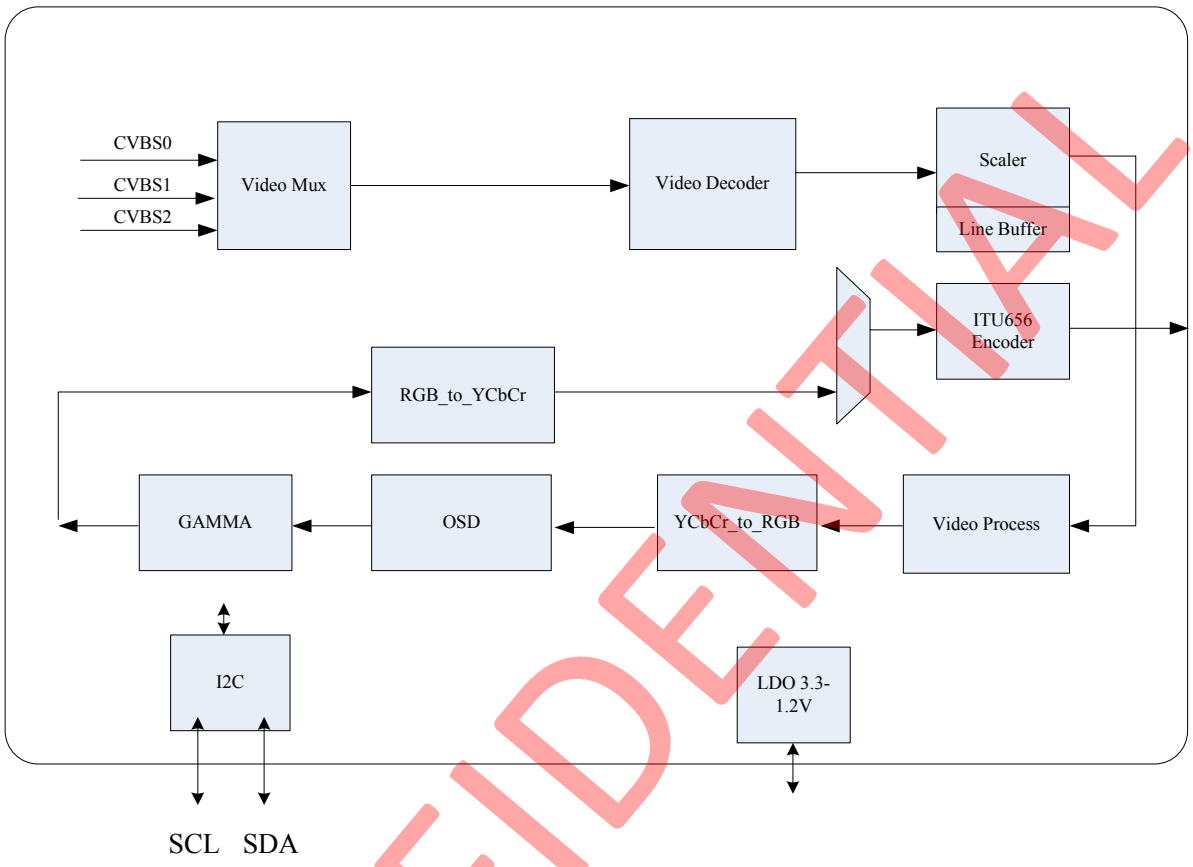


Fig.1 Block Diagram

5. Pin Diagram

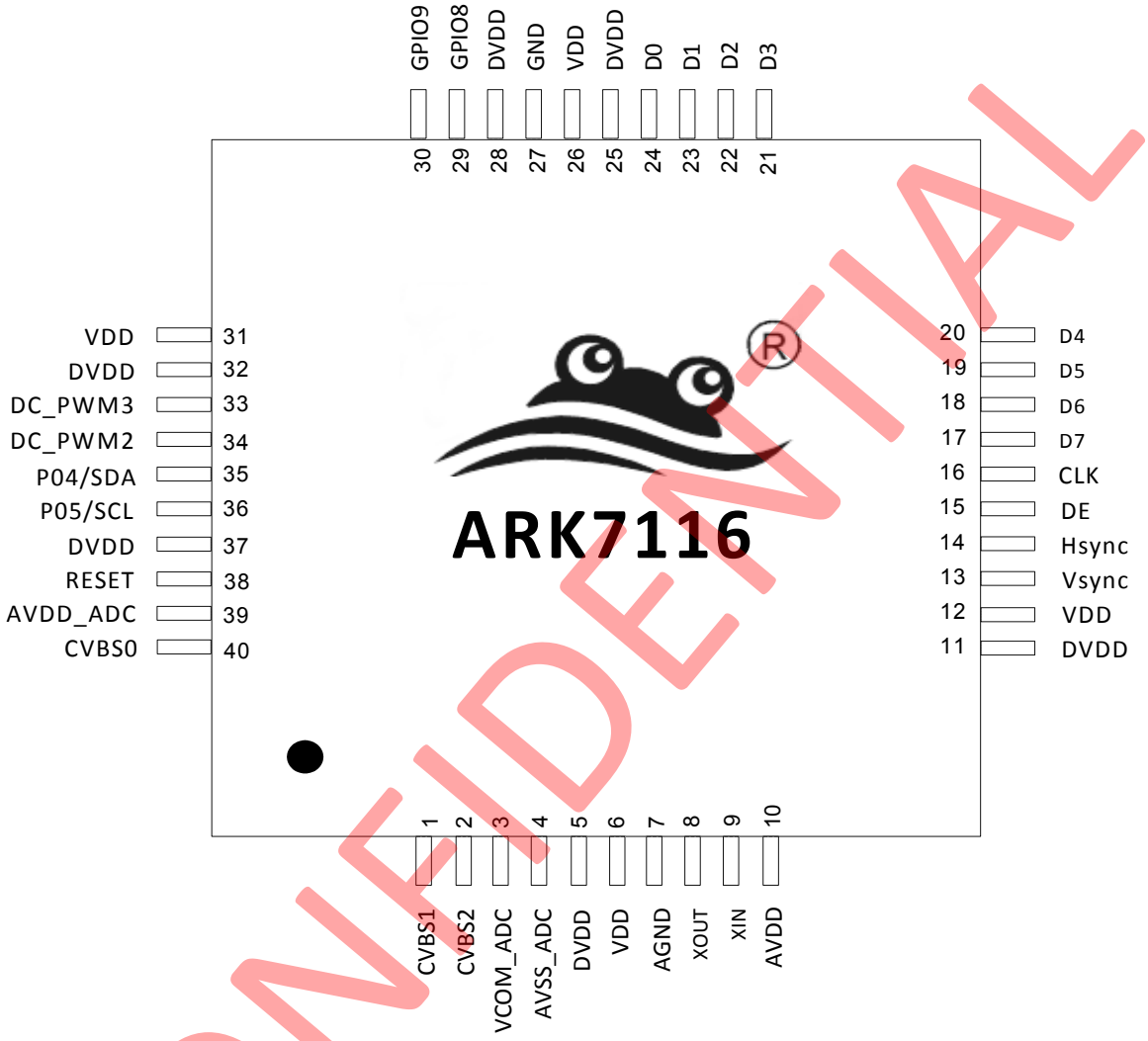


Fig.2 PIN OUT Diagram

6. Pin Definition

40 PAD Definitions

PIN#	PIN NAME	TYPE	PIN DESCRIPTION
1	CVBS1	I	CVBS channel1 in
2	CVBS2	I	CVBS channel2 in
3	VCOM_ADC	I	ADC Common Input, connect to GND by 22nF cap
4	AVSS_ADC	P	Analog ADC ground
5	DVDD	P	LDO 3.3v Input

6	VDD	P	LDO 1.2v output, connect to GND by 2.2uF and 0.1uF cap
7	AGND	P	OSC Ground
8	XOUT	A	Crystal in
9	XIN	A	Crystal out
10	AVDD	P	OSC Supply, 3.3v
11	DVDD	I	IO supply, 3.3v
12	VDD	P	Core supply, 1.2v
13	Vsync	O	Vsync
14	Hsync	O	Hsync
15	DE	O	Data enable
16	CLK	O	Clock
17	D7	O	ITU656/ITU601 Data bit7
18	D6	O	ITU656/ITU601 Data bit6
19	D5	O	ITU656/ITU601 Data bit5
20	D4	O	ITU656/ITU601 Data bit4
21	D3	O	ITU656/ITU601 Data bit3
22	D2	O	ITU656/ITU601 Data bit2
23	D1	O	ITU656/ITU601 Data bit1
24	D0	O	ITU656/ITU601 Data bit0
25	DVDD	P	IO supply, 3.3v
26	VDD	P	Core supply, 1.2v
27	GND	P	Ground
28	DVDD	P	IO supply, 3.3v
29	GPIO8	IO	GPIO8
30	GPIO9	IO	GPIO9
31	VDD	P	Core supply, 1.2v
32	DVDD	P	IO supply, 3.3v
33	DC_PWM3	IO	DC_PWM3
34	DC_PWM2	IO	DC_PWM2
35	SDA	IO	SDA
36	SCL	IO	SCL
37	DVDD	P	IO supply, 3.3v
38	RESET	I	Reset
39	AVDD_ADC	P	ADC supply, 3.3v
40	CVBS0	I	CVBS channel0 in

7. Electrical Characteristics

7.1 DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DVDD	Digital IO supply voltage		3.0	3.3	3.6	V
I_{DVDD}	Digital supply current		--	50	60	mA
AVDD_ADC	Analog ADC supply voltage		3.0	3.3	3.6	V
I_{AVDD}	Total analog supply current	CVBS input	30	40	50	mA

7.2 AC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog part						
Iclamp	Clamping current	VI=1VDC	--	+-16	--	uA
Vi(p_p)	Input voltage (Peak-to-peak value)	For normal video levels 1V(p-p), 3dB termination 18/56 and AC coupling required; Coupling capacitor=22nF	--	2	3.6	V
|Zin|	Input impedance	Clamping current off	200	--	--	KΩ
Ci	Input capacitance		--	--	10	pF
@cs	Channel crosstalk	fi<5MHz	--	--	-50	dB
9-bit analog-to-digital converters						
B	Analog bandwidth	At -3dB	--	7	--	MHz
Φdiff	Differential phase		--	2	--	Deg
Gdiff	Differential gain		--	2	--	%
Fadc	ADC clock frequency		13.5	27	54	MHz
DNL	DC differential linearity Error		--	0.7	--	LSB
INL	DC integral linearity error		--	1	--	LSB
PLL						
FOUT	PLL output range		--	--	480	MHz
FIN	Input reference frequency range		1	--	6	MHz
Fvco	VCO frequency range		--	--	480	MHz

Tjitter	Timing Jitter Peak to Peak		--	88	--	Ps
Tjitter rms	Timing Jitter RMS		--	18	--	Ps
12BIT SAR ADC						
resolution			--	12	--	BIT
Vi(p_p)	input voltage (peak-to-peak value)		--	2	3.3	V
Fadc	Sample clock		--	--	1	MHz
INL	DC integral linearity error		--	--	+-2	LSB
DNL	DC differential linearity error		--	--	+-2	LSB
Digital inputs						
VIL(n)	Low-level input voltage		0		0.4	V
VIH(n)	High-level input voltage		2.4		3.6	V
Digital outputs						
VOL	Low-level output voltage		0		0.4	V
VOH	High-level output voltage		2.4		vcc+0.5	V
Temperature						
TA	Ambient Operation Temperature		0		70	℃
TSTG	Storage Temperature		-40		125	℃
Tj	Junction Temperature				125	℃

7.3 Serial Communication Characters

The ARK7116 supports the 'fast mode' standard I2C-bus protocol (data rate up to 400 KBit/s)

7.3.1 I²C bus format

Write procedure:

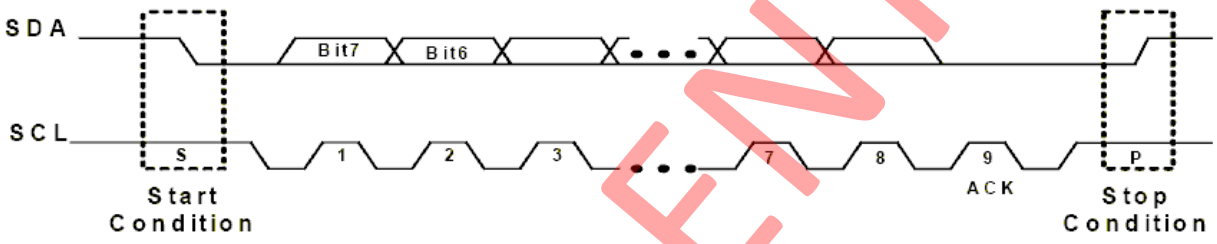
S	SLAVE ADDRESS	ACK-s	SUBADDRESS	ACK-s	DATA	ACK-s	P

Read procedure:

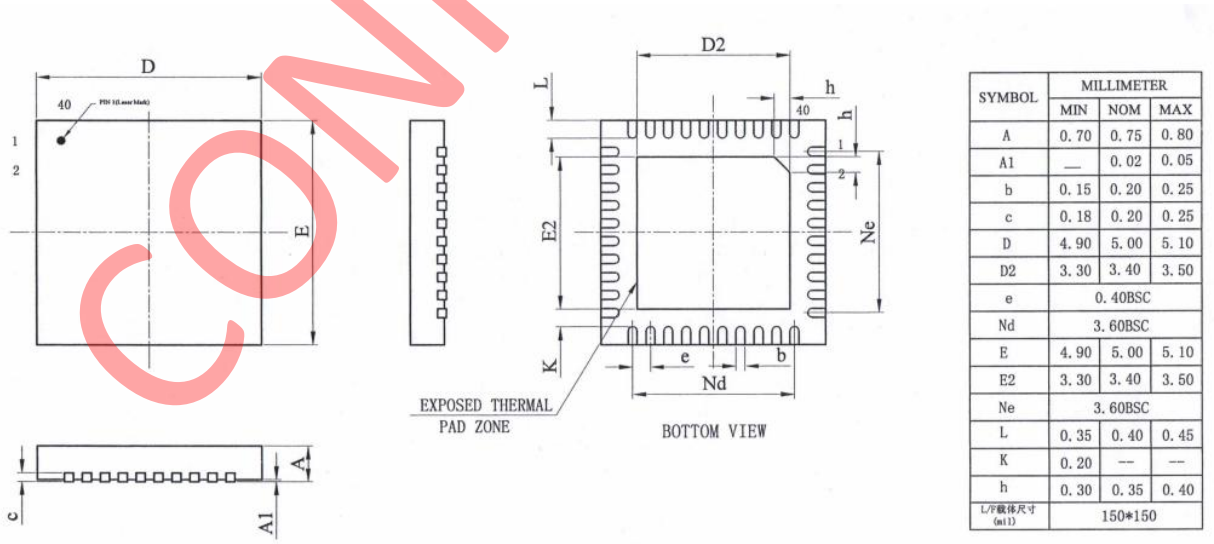
S	SLAVE ADDRESS	ACK-s	SUBADDRESS	Re-S	SLAVE ADDRESS|0X01	ACK-s	DATA	ACK-m	P

7.3.2 Description of I²C-bus format

SYMBOL	FUNCTION
S	START condition
SLAVE ADDRESS	Device address (0XB0 0XB2 0XB4 0XB6 0XB8)
SUBADDRESS	Register address
Re-S	Repeated start
ACK-s	acknowledge generated by the slave
ACK-m	acknowledge generated by the master
SUBADDRESS	sub address byte
DATA	data byte; if more than one byte DATA is transmitted the sub address pointer is automatically incremented
P	Stop condition



8. Package



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.30	3.40	3.50
e	0.40BSC		
Nd	3.60BSC		
E	4.90	5.00	5.10
E2	3.30	3.40	3.50
Ne	3.60BSC		
L	0.35	0.40	0.45
K	0.20	—	—
h	0.30	0.35	0.40
L/F载体尺寸 (mil)	150*150		