DATASHEET

0.11 µm Processor System for ARM926EJ-S™

cw001200_agflxr_2_0

February 2005

Preliminary

LSI LOGIC®

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This document describes LSI Logic Corporation's 0.11 µm Processor System for ARM926EJ-S cw001200_agflxr_2_0 and will remain the official reference source for all revisions/releases of this product until rescinded by an update.

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Preface

The 0.11 µm Processor System for ARM926EJ-S™ (cw001200_agflxr_2_0) is compatible with the RapidWorx® design tools and design methodology and based on 0.11 µm process technology.

Audience

This document is intended for software engineers, hardware engineers, system architects, platform ASIC designers, engineering managers, and marketing managers who are evaluating the Processor System for ARM926EJ-S.

This document assumes that you have some familiarity with microprocessors and related support devices. The people who benefit from this book are:

- Engineers and managers who are evaluating the processor for possible use in a system
- Engineers who are designing the processor into a system

Organization

This document contains the following chapters:

- Chapter 1, **Introduction**, defines the RapidChip® system, introduces its main CoreWare components, and provides an overview of RapidChip Platform ASIC, CoreWare IP, and the Processor System for ARM926EJ-S.
- Chapter 2, **Architectural Description**, describes the Processor System for ARM926EJ-S architecture.
- Chapter 3, **Registers**, describes the Processor System for ARM926EJ-S programming model.

- Chapter 4, **Signal Summary**, describes the signals used by the Processor System for ARM926EJ-S.
- Chapter 5, **Specifications**, describes the specifications required by the Processor System for ARM926EJ-S.

Related Publications

The following LSI Logic publications are related to this document:

- *0.11 µm Processor System for ARM926EJ-S Technical Manual*, DB14-000299-01
- *0.11 µm Processor System for ARM926EJ-S Integration Guide*, DB09-000147-02
- *0.11 µm Processor System for ARM926EJ-S Release Notes*
- *0.11 µm Processor System for ARM926EJ-S Errata*

Conventions Used in This Manual

The word *assert* means to drive a signal true or active. The word *deassert* means to drive a signal false or inactive. Signals that are active LOW end in an “n.”

Hexadecimal numbers are indicated by the prefix “0x”—for example, 0x32CF. Binary numbers are indicated by the prefix “0b”—for example, 0b0011.0010.1100.1111.

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Chapter 1
Introduction

The 0.11 µm Processor System for ARM926EJ-S™ is compatible with the RapidWorx® design tools and design methodology and ready to integrate into the RapidChip® Platform ASIC families.

This chapter contains the following sections:

1.1 RapidChip Technology Overview

RapidChip Platform ASICs, RapidWorx design methodology, and RapidWorx design tools are all based on RapidChip Technology. This section briefly explains these concepts. For more information about RapidChip Technology, go to http://www.rapidchip.com.

1.1.1 RapidChip Platform ASICs

RapidChip Technology allows you to customize the metal layers of a partially manufactured semiconductor wafer that contains multiple copies of a predefined platform ASIC. The silicon layers of a platform ASIC have diffused IP resources that are later connected with user-specific metallization patterns.

Because platform ASICs are available as partially manufactured devices, customers benefit from dramatically reduced lead times for prototypes and production units as well as lower inventory costs. The broad range of resources available in platform ASICs meets the needs of many different systems and applications.

Each platform ASIC incorporates diffused memory blocks, PLLs, and IP blocks from our extensive CoreWare® library. In addition, each platform ASIC has a transistor fabric region and an I/O ring, which are both user-configurable.

1.1.2 CoreWare IP Program

The LSI Logic CoreWare IP library provides the industry's most comprehensive set of IP solutions that work seamlessly in the cell-based ASIC design flow and the RapidWorx Design Kit. Customers can leverage CoreWare IP solutions to significantly reduce the risk and turn-around times associated with complex System on a Chip (SoC) designs. CoreWare IP includes:

- GigaBlaze® and HyperPHY® high-speed, standards-compliant SerDes
- High-performance ARM® and MIPS processors and associated systems and reference designs
- Processor peripherals and AMBA on-chip-bus structures
- DSP cores
- USB cores
- Memory PHYs and controllers
- Ethernet MAC and PHY cores
- PCI Express, XGXS, SPI4.2, and other protocol layer IP

1.1.3 RapidReady™ Certification

CoreWare IP can have RapidReady certification, which means it meets the highest level of compatibility with the RapidWorx design methodology and design tools and is ready to be integrated into RapidChip Platform ASICs. For more information about RapidReady certification refer to http://www.rapidchip.com.

1.1.4 RapidWorx

The RapidWorx design tools and design methodology are used to customize a RapidChip Platform ASIC, creating a unique metallized device, called an *instance*.

RapidWorx design tools help you create design structures for implementing a custom IC design. Based on user inputs, these tools automatically generate clock, memory, test, and I/O structures, relieving the design team of more mundane design tasks. This dramatically reduces the overall manpower resource required to design custom high-performance ICs. Additionally, these structures are “correct by construction” and optimized to ensure ease of implementation during the physical design phase.

RapidWorx design methodology is compatible with best-in-class third-party EDA tools. Rules and constraints guide designers throughout the design process to ensure predictable results and reduced design times when compared to fully optimized ASICs.

1.2 Processor System for ARM926EJ-S Product Description

This section provides an overview of the Processor System for ARM926EJ-S, including its features and benefits, product options, and product deliverables.

1.2.1 Processor System for ARM926EJ-S Overview

The 0.11 µm Processor System for ARM926EJ-S is a general purpose microprocessor typically used in the following applications:

- Portable communications
- Hand-held computing
- Multimedia
- Digital consumer
- Embedded solutions

Product Name	0.11 µm Processor System for ARM926EJ-S
CoreWare IP Number	cw001200_agflxr_2_0
Process Technology	0.11 Micron
IP Type	Firm IP
Library	Gflx™-r

1.2.2 Processor System for ARM926EJ-S Features and Benefits

The Processor System for ARM926EJ-S offers the following features and benefits:

- ARM926EJ-S processor
- Two AHB slave ports for connecting a multiport memory controller or other AHB slave to the ARM926EJ-S 32-bit instruction and data buses
- APB peripheral set: UARTs, GPIO, timers, and I^2C bus controllers.
- Industry standard AMBA 2.0 Bus family
  - Advanced High-Performance Bus (AHB)
  - Advanced Peripheral Bus (APB)
- Supports little endian systems only
- JTAG debug port
- Clocking system supports integer-multiple bus frequencies for AHB and APB buses
- External SRAM, flash, and ROM memory controller
  - 32-bit external data bus
  - 32-bit external address bus
  - Assembles and disassembles 8-bit, 16-bit, and 32-bit AHB requests to external 8-bit, 16-bit, and 32-bit devices
  - Programmable wait state control (1–16) that supports external flash memory
- AHB Arbiter
- Vectored Interrupt Controller (ApVic)
- I-AHB and D-AHB can access external SRAM, flash, and ROM memory controller
- 10/100 Mbit/s Ethernet Controller (ApE110) with AMBA Master DMA interface
- 32-bit AHB Master Expansion Port
- I-AHB and D-AHB can access 32-bit AHB to AHB synchronous Segmentation Bridge for external AHB slaves

1.2.3 Processor System for ARM926EJ-S Options

Configuration options for the Processor System for ARM926EJ-S are as follows:

- Compile-Time Options

  The Processor System for ARM926EJ-S has no compile time options.

- Programmable Options

  Programmable options are customer selectable options. The programmable options are peripheral dependent and are captured by the peripheral register section.

- Strappable Options

  Strap pins are options available at the system boundary. These strappable pins must be held HIGH or LOW to enable or disable the particular feature. The following table lists the options.

Interface	Signal	Strapping
Decoding Logic	BRBOOTSEL	LOW: Processor boots from SRAM, Flash, ROM port HIGH: Processor boots from AHB Slave Expansion Port
ApE110	CLKS	Clock Select pin
ApSramCtlr	CS7WIDTH	Chip Select 7 Data Select Width defines the data path width
ARM926EJ-S	DRSIZE	Data TCM size; set internally by TCM configuration process
ApE110	E110RX_RAM_SIZE	Receive FIFO RAM size
ApE110	E110TX_RAM_SIZE	Transmit FIFO RAM size
ARM926EJ-S	INITRAM	Enables Instruction TCM at reset
ARM926EJ-S	IRSIZE	Instruction TCM size; set internally by TCM configuration process
ARM926EJ-S	VINITHI	LOW: Exception vectors start at 0x00000000 HIGH: Exception vectors start at 0xFFFF0000

1.2.4 Processor System for ARM926EJ-S Deliverables

Typical Firm IP Deliverables:

Deliverable	Yes/No
Encrypted or Behavioral Verilog to support the following simulators: Mentor Graphics Modelsim, Cadence NCVerilog, and Synopsys VCS	Yes
Verilog gate level netlist	Yes
Verilog test wrapper to support automated test insertion flow	Yes
Abstracted Timing (estimated) and LEF models to support chip level RTL analysis	Yes
Timing constraints for synthesis and physical layout	Yes
RapidWorx data files	Yes
Simulation testbench, run control scripts, and test stimuli	Yes
Datasheet	Yes
Technical Manual	Yes
Integration Guide	Yes
Release Notes	Yes
Errata	Yes

1.3 Required Platform ASIC Resources

This Processor System for ARM926EJ-S requires the ARM926EJ-S processor identified below:

Compatible CoreWare IP	Description	Format
cw001124_1_0	ARM926EJ-S processor, rev r0p4	Hard R-Cell

The table below identifies the platform ASIC resources for the Processor System for ARM926EJ-S:

Resource	Description
Memory	Ethernet memories are external to the cw001200; you can choose the memory size using strap pin settings and how to implement the memory (R-Cell, diffused memory in slice, and so on)
R-Cells	Requires the ARM926EJ-S processor core
I/O Buffers	No special I/O requirements, however some signals (SRAM, GPIO, UART, I^2C, and so on) require them
PLLs	No special PLL requirement other than you must generate the CLK, HCLK, PCLK, HOST_CLK, and so on

1.4 Required Cores

The following table identifies the physical requirements of the Processor System for ARM926EJ-S:

Requirement	Description
Type (Firm)	• Encrypted RTL • Test ready netlist
Memory Requirements	• Data TCM—Single Port SRAM, size determined by customer • Instruction TCM—Single Port SRAM, size determined by customer • Ethernet Receive FIFO—Dual Port SRAM, size determined by customer • Ethernet Transmit FIFO—Dual Port SRAM, size determined by customer
Clocks Required	• Six clocks required • Up to three clock enables depending on clock frequencies
Reset Scheme	• Asynchronous with de-assertion synchronous • Three resets required

Chapter 2
Architectural Description

The 0.11 µm Processor System for ARM926EJ-S, part of the CoreWare IP library, easily integrates with the RapidChip Platform ASIC design flow. This fully integrated, general purpose system is built from existing LSI Logic CoreWare IP blocks and delivered as a Fixed IP block. Expansion ports let you add external features and application-specific hardware to the subsystem.

This chapter contains the following sections:

2.1 Processor System for ARM926EJ-S Block Diagram

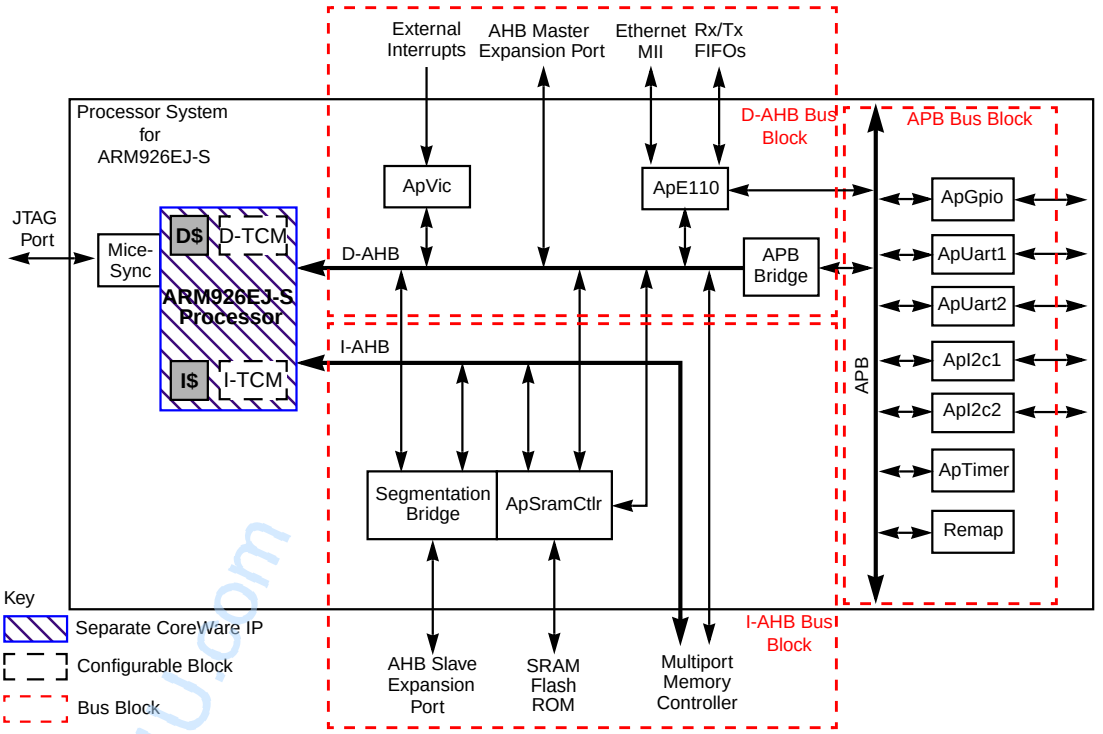
The Processor System for ARM926EJ-S is intended as the primary processor in a larger AMBA system. Other system processors are expected to be Slaves for startup and system control functions.

Because the Processor System for ARM926EJ-S serves as the main communication protocol control processor for a larger AMBA system, the Processor System for ARM926EJ-S includes a 10/100 Ethernet Controller (ApE110). Additional IP blocks, such as USB interfaces and PCI interfaces, can be added to the system using the AHB Slave Expansion Port, the AHB Master Expansion Port, and the Multiport Memory Controller ports.

The processor system includes an ARM926EJ-S microprocessor and commonly required system peripherals, such as timers, UARTs, a vectored interrupt controller, an Ethernet controller, and controllers for SRAM, flash, and ROM memories.

Figure 2.1 shows the Processor System for ARM926EJ-S block diagram.

Figure 2.1 Processor System for ARM926EJ-S Block Diagram



2.2 ARM926EJ-S Processor Block Description

The ARM926EJ-S processor is a separate CoreWare IP component. This block consists of the ARM926EJ-S soft macro, memories to create the data and instruction tightly coupled memories (TCMs), if supported by the Processor System for ARM926EJ-S component, and the processor.

2.3 Instruction AHB Bus Block Description

The instruction AHB bus is based on the AMBA 2.0 AHB standard from ARM Ltd. This ARM926EJ-S AHB Master bus includes the following Slave devices:

- External SRAM Controller (ApSramCtlr)
- AHB-lite port to an external Multiport Memory Controller
- Segmentation Bridge to an expansion AHB-lite bus

The Bus Matrix boots the subsystem from either the External SRAM Controller or Segmentation Bridge which are aliased at both 0x0 and 0xF000.0000. The boot device is controlled by the BTBOOTSEL strap pin. Booting HIGH or LOW is controlled by the VINITHI strap pin.

The AHB-lite port lets you connect to a memory controller, for example the LSI Logic DDR SDRAM controller.

2.4 Data AHB Bus Block Description

The data AHB bus is based on the AMBA 2.0 AHB standard from ARM Ltd. This AHB bus has three masters:

- 10/100 Mbit/s Ethernet Controller (ApE110)
- ARM926EJ-S Processor
- Expansion Master Port

The three masters are controlled by a priority arbiter. The highest priority master is the Ethernet controller (ApE110), the intermediate level master is the ARM926EJ-S, and the lowest priority master is the Expansion Master Port.

The Expansion Master Port is an AHB port to allow an external Master access to peripherals on the data AHB bus. This port lets you add additional IP to the system.

The data AHB bus has the following Slave devices:

- External SRAM Controller (ApSramCtlr)
- AHB-lite port to an external Multiport Memory Controller
- Vectored Interrupt Controller (ApVic and ApVicBridge)
- APB Bridge
- Segmentation Bridge to an expansion AHB-lite bus

The Expansion Master Port, AHB expansion bus port, and the AHB-lite port, for an external Multiport Memory Controller, lets you add additional IP to the system. The AHB-lite port is provided to allow connection to memory controller, such as the LSI Logic DDR SDRAM controller.

The APB bridge allows all data AHB Masters to access peripherals on the APB bus.

2.5 APB Bus Block Description

The APB is a Slave bus based on the AMBA 2.0 APB standard from ARM Ltd. The APB includes the following peripherals:

- Two UART (16550 type) instantiations
- A 32-bit GPIO block
- Two I^2C Bus Controller instantiations
- Timer block (two timers)
- Ethernet Controller Configuration port
- Remap block

2.6 Interrupts

The 32-bit input interrupt channel to the Vectored Interrupt Controller, ApVic, is brought to the top interface of the system as an input. You must connect the peripheral interrupt outputs to the appropriate ApVic interrupt channels. There are no interrupts connected to the ApVic internally.

Interrupts for all the instantiated system peripherals are brought to the top interface of the system as outputs. These include:

- One interrupt for the Ethernet Controller
- One interrupt for each I^2C instantiation
- One interrupt for each UART instantiation
- Six interrupts for the Timer block
- Four interrupts for the GPIO block

Chapter 3
Registers

This chapter summarizes the Processor System for ARM926EJ-S registers.

This chapter contains the following sections:

3.1 Register Summary

This section summarizes the system registers.

3.1.1 External SRAM Registers

Eight Chip Select Control registers control the AHB address chip select decoding. Chip Select 7 has the highest priority, Chip Select 0 the lowest.

The registers are accessed through the AHB from the D-AHB bus.

The peripheral register set consists of the registers summarized in Table 3.1.

Table 3.1 Chip Select Control Register Summary

Register Name	R/W	Function
Chip Select Control Register 0/1/2/3/4/5/6/7	R/W	Controls the chip select decoding of the AHB address

3.1.2 GPIO Registers

The GPIO registers set the external GPIO bits for use as General-Purpose Input/Output. Each GPIO bit can be configured as an

input or output through the Direction register. The GPIO also can generate interrupts to the processor's FIQ/IRQ interrupt system.

Each register set defines a particular behavior for all of the external GPIO pins. There is one bit for each GPIO pin. This definition is the same for all register sets. For example:

- GPIO Data Direction Register 1, bit 7 controls the direction for external GPIO bit 7.
- GPIO Data Direction Register 1, bit 0 controls the direction for external GPIO bit 0.
- GPIO Data Direction Register 2, bit 7 controls the direction for external GPIO bit 15.
- GPIO Data Direction Register 2, bit 0 controls the direction for external GPIO bit 8.

The GPIO register set is summarized in Table 3.2.

Table 3.2 GPIO Register Summary

Register Name	R/W	Function
GPIO Data Direction 1/2/3/4	R/W	Sets the direction of the corresponding GPIO bits
GPIO Data In 1/2/3/4	R	Reads the data value for the corresponding GPIO bit
GPIO Data Out 1/2/3/4	W	Writes the data value for the corresponding GPIO bit
GPIO Edge 1/2/3/4	R/W	Selects whether an edge or level signal on the GPIO generates an interrupt
GPIO Enable Clear 1/2/3/4	R/W	Clears the enables for the GPIO interrupts
GPIO Enable Set 1/2/3/4	R/W	Sets the enables for the GPIO interrupts
GPIO Polarity 1/2/3/4	R/W	Selects whether the GPIO interrupt is active HIGH or LOW (edge bit = level), or, if edge triggered (edge bit = edge), on the falling or rising edge
GPIO Raw Status 1/2/3/4	R/W	Reads the raw (premasked) interrupt status of the GPIO interrupts; on writes, a 1 in a bit position clears the corresponding interrupt bit
GPIO Resync 1/2/3/4	R/W	Selects whether the GPIO inputs are resynchronized to the internal clock when configured as an input
GPIO Status 1/2/3/4	R	Reads the (postmasked) interrupt status of the GPIO interrupts

3.1.3 UART Registers

The registers are accessed through the APB. The Divisor Latch Access Bit (DLAB) is set and cleared by writing to bit 7 of the Line Control Register (LCR).

The UART register set consists of 17 registers, summarized in Table 3.3.

Table 3.3 UART Register Summary

Register Name	R/W	Description
Divisor Latch Low/High (DLL/DLH)	R/W	Stores the divisor for a baud generator in a 16-bit binary format
FIFO Control (FCR)	W	Provides control for both the receive and transmit FIFOs
Interrupt Enable (IER)	R/W	Enables the five types of UART interrupts
Interrupt Identification (IIR)	R	Stores the four levels of prioritized interrupts and indicates the highest priority pending interrupt when read
Line Control (LCR)	R/W	Specifies the format of the asynchronous data communications exchange and set the DLAB
Line Status (LSR)	R	Provides data transfer status information
Modem Control (MCR)	R/W	Provides control functions
Modem Status (MSR)	R/W	Provides modem status information
Receiver Buffer (RBR)	R	Provides temporary storage for receive data
Scratch	R/W	Provides a place where software can store data temporarily
Speedsense Complete (SCR)	R	Determines whether the Speedsense process is complete (1) or not complete (0)
Speedsense Value Low/Med/High (SVL/SVM/SVH)	R	Matches the baudrate of the UART to that of the other modem device; reflects the low, middle, or high byte of the Speedsense value
Start Speedsense (SSR)	W	Triggers the Speedsense function when any value to the register is written
Transmit Holding (THR)	W	Provides temporary storage for transmit data

3.1.4 APB Timer Registers

The Timer register set consists of 13 registers, summarized in Table 3.4, which are accessed through the APB.

Table 3.4 APB Timer Register Summary

Register Name	R/W	Description
Timer 1/2	R/W	Returns the current value of the Timer on reads; updates the Timer at the next rising edge of the Timer 1/2 clock on writes
Timer Control 1/2	R/W	Controls specific Timer functions including freezing, up/down count, interval or periodic mode, and trigger point register selection
Timer Prescaler 1/2	R/W	Contains the value controlling the unit of time that each tick of the Timer represents when combined with the input Timer 1/2 clock
Timer Trigger Control	R/W	Selects between Timer 1 and Timer 2 to compare against the value held in each of the Timer Trigger Point registers
Timer Trigger Point 1/2/3/4/5/6	R/W	Defines when an interrupt is generated

3.1.5 Ethernet Controller Registers

All Ethernet Control registers are accessed over the APB.

The Ethernet Control register summary is shown in Table 3.5.

Table 3.5 Ethernet Controller Register Summary

Register Name	R/W	Description
Carrier Loss Counter	R/W	Contains the number of times the carrier is lost in the middle of a Transmit frame since the last time the counter was read
Collisions Counter: *x* (1–15) or More Back-to-Back	R/W	Contains the number of packets that collided *x* (1–15) or more times before being transmitted
DMAC Configuration	R/W	Configures the AHB-Master DMA controller
DMAC Interrupt Enable	R/W	Enables the interrupts to the processor used to control the DMA
DMAC Interrupt Status	R/W	Provides status of the interrupts to the processor used to control the DMA
Ethernet Back-to-Back IPG	R/W	Programmable Transmit IPG for back-to-back transmissions
Ethernet Interrupt Active	R	Asserts the E110_INT signal
Ethernet Interrupt Diagnostic	R/W	Generates an unconditional interrupt for test purposes; initializes the Transmit and Receive FIFOs for gate-level simulation

Table 3.5 Ethernet Controller Register Summary (Cont.)

Register Name	R/W	Description
Ethernet Interrupt Enable	R/W	Enables individual interrupt types selectively
Ethernet Interrupt Status	R/W	Can be used to poll the interrupt flags; contains interrupt status and is unaffected by interrupt enables
Ethernet IPG Part 1	R/W	Programmable transmit IPG Part 1 for non back-to-back transmissions
Ethernet IPG Part 2	R/W	Programmable transmit IPG Part 2 for non back-to-back transmissions
Ethernet MAC Address (Bytes 1–4)	R/W	Address of the Ethernet device
Ethernet MAC Address (Bytes 5–6)	R/W	Address of the Ethernet device
Ethernet Main Control	R/W	Lets you reset the MAC, determine retransmission delay retries and wait times, and set full- or half-duplex mode
Ethernet MII Control Status	R/W	Status information and control of MIIM functions to the MII PHY
Ethernet MII Read	R	Contains Status Register data read from the addressed MII PHY
Ethernet MII Write	R/W	PHY and register address and write data for MII PHY register accesses
Ethernet Receive Control	R/W	Controls Receive functions such as Virtual LAN protocol, Multicase block, Broadcase block, and Promiscuous Mode
Ethernet RNG Seed	R/W	Seed value to generate random number sequence used in collision backoff timing
Ethernet Transmit Control	R/W	Controls transmit functions such as packet padding, preamble, maximum packet size that can be transmitted, and CRC insertion
Events Dropped Counter	R/W	Contains the number of receive overruns since last read
FCS/Alignment Errors Counter	R/W	Contains the number of packets received since last read
Flow Control	R/W	Enables transmit flow control when PAUSE frames are received; provides false carrier sense in half-duplex mode
Fragment Packets Counter	R/W	Contains the number of packets received that are less than 64 octets in length (excluding framing bits, but including FCS octets) and have either a bad FCS or a nonintegral number of octets (Alignment Error)
Jabber Counter	R/W	Contains the number of packets received that are greater than 1518 octets for non-VLAN packets or if VLAN is disabled or greater than 1522 octets if VLAN is enabled and the packet is a VLAN packet (excluding framing bits, but including FCS octets), and have either a bad FCS or a nonintegral number of octets (Alignment Error)

Table 3.5 Ethernet Controller Register Summary (Cont.)

Register Name	R/W	Description
Late Collisions Counter	R/W	Contains the number of late collisions that occurred since it was last read regardless of whether the Multiple Collisions (COL) interrupt is enabled
Oversize Packets Counter	R/W	Contains the number of packets received that are greater than 1518 octets for non-VLAN packets or if VLAN is disabled or greater than 1522 octets if VLAN is enabled and the packet is a VLAN packet (excluding framing bits, but including FCS octets) and are otherwise well-formed
Peripheral Reset	R	Resets the peripheral
Runt Packets Counter	R/W	Contains the number of packets received that are less than 64 octets in length (excluding framing bits, but including FCS octets) and are otherwise well-formed
Receive Pointers	R	Determines whether data is transferred to and from the Receive FIFO—*for test purposes only*
State	R	Provides current state of match, receive and transmit state machines
Transmit Underruns Counter	R/W	Contains the number of transmit underruns that occurred since it was last read
Transmit and Receive BMD Pointer	R/W	Contains the upper address of the first Transmit/Receive Buffer Memory Descriptors (BMDs) in the lists
Transmit Pointers	R	Determines whether data is transferred to and from the Transmit FIFO—*for test purposes only*
Transmit Poll Timer	R/W	Contains the number of clock cycles the transmit section must wait before polling a BMD with the valid bit cleared
Transmit Threshold	R/W	Controls how much data is required in the Transmit FIFO before the E-100 MAC starts transmitting

3.1.6 ApI2c Registers

The ApI2c interface allows access for up to 64 addressable 16-bit registers aligned on 32-bit boundaries. The registers are used to control I^2C Master and Slave access to the I^2C bus. Reserved registers or fields are read-only and return all zeros when read.

The ApI2c registers are summarized in Table 3.6.

Table 3.6 ApI2c Register Summary

Register Name	R/W	Description
Global Control	R/W	Enables or disables the Master and Slave units independently; enables and disables the IBML time-out timers globally
I^2C Monitor	R/W	Lets the host manually read and control the SCL and SDA I^2C bus signals
IBML $t_{LOW:MEXT}$ Control	R/W	Measures the time the SCL signal is extended LOW by the Master controller during data byte transmission or reception
IBML $t_{LOW:SEXT}$ Control	R/W	Measures the time the SCL signal is extended LOW by the Slave controller during message transmission or reception
IBML $t_{TIMEOUT}$ Control	R/W	Measures the time the SCL signal is detected LOW
Interrupt Enable	R/W	Enables/disables interrupt status reporting for the Master and Slave interrupt sources in the corresponding Interrupt Status Register bit and external interrupt signal
Interrupt Status	R/W	Reports the Master and Slave interrupt source status
Master Address Register 1	R/W	Sent as the first byte in the address phase of an I^2C transaction
Master Address Register 2	R/W	Sent as the second byte in the address phase of an I^2C transaction if ten-bit addressing is enabled
Master Command	R/W	Issues commands to the Master state machine
Master Data	R/W	Writes data into the Master Transmit FIFO, reads get data from the top of the Master Receive FIFO
Master Interrupt Enable	R/W	Enables/disables the individual Master interrupts; bits correspond to the Master Interrupt Status register bits
Master Interrupt Status	R	Records the status results of the last command issued
Master Receive Bytes Transferred	R	Tracks the number of successfully received (acknowledged) data bytes
Master Receive FIFO Status	R	Indicates the number of data bytes currently in the Master Receive FIFO
Master Receive Transfer Length	R/W	Determines the number of bytes transferred during receive transfers
Master Transmit Bytes Transferred	R	Tracks the number of successfully transmitted (acknowledged) data bytes
Master Transmit FIFO Status	R	Indicates the number of data bytes currently in the Master Transmit FIFO
Master Transmit Transfer Length	R/W	Determines the number of data bytes sent during transmit transfers
SCL High Period	R/W	Determines the high period for the SCL clock generated by I^2C Master

Table 3.6 Apl2c Register Summary (Cont.)

Register Name	R/W	Description
SCL Low Period	R/W	Determines the low period for the SCL clock generated by the I^2C Master
SDA Hold Time	R/W	Controls the data hold time whenever the core controls SDA (Master or Slave)
SDA Setup Time	R/W	Controls the data setup time when the Master is driving SCL and SDA
Slave Address 1	R/W	Contains the first I^2C Slave address
Slave Address 2	R/W	Contains the second I^2C Slave address
Slave Address Decode Control	R/W	Enables/disables the two Slave address decoders and the General Call Address decode
Slave Data	R/W	Provides access to Slave read or write data
Slave Interrupt Enable	R/W	Enables/disables the individual Slave interrupts; bits correspond to the Slave Interrupt Status register bits
Slave Interrupt Status	R	Contains status information for Slave operations
Slave Read Dummy Byte	R/W	Provides a data byte for an I^2C Master read transaction if the I^2C Slave state machine has not received a data byte in the Slave Data register before the SCL timer expires
Slave Receive FIFO Status	R	Provides access to the Receive Status FIFO which provides the status word for the data at the top of the Receive FIFO
Slave Receive Control	R/W	Controls the acknowledge cycle response during the data phase of a Slave write transfer
Soft Reset	R/W	Lets the host independently clear the I^2C interface
Spike Filter Length	R/W	Controls the spike filter for SCL and SDA; filter stages determine the maximum size of the spike the filter suppresses
Timer Clock Divider Control	R/W	Divides the APB clock frequency for use by all timers
Wait Timer Control	R/W	Controls the Master/Slave Wait Timer; times the different I^2C transactions and causes the appropriate state machine to take action when time-out occurs

3.1.7 ApVic Registers

The ApVic contains registers, summarized in Table 3.7, that initialize and control interrupts within the system.

Table 3.7 ApVic Register Summary

Register Name	R/W	Description
Edge Select	R/W	Determines whether the interrupts are edge- or level-sensitive
FIQ Current Priority Level (CPR)	R/W	Sets the current priority level for the FIQ interrupts
FIQ Enable Clear	W	Clears the corresponding bit in the FIQ Enable register when writing a 1; writing a 0 has no effect
FIQ Enable Set	R/W	Sets up the mask for each interrupt that generates an interrupt into the nFIQ signal of the processor
FIQ Index	R/W	On reads this register contains the FIQ channel index location with the highest service priority; on writes it loads a hardware jump table
FIQ Interrupt Service Routine (ISR) Vector	R/W	Contains the starting address vector of the ISR for the FIQ interrupt with the highest service priority
FIQ Last Priority Level (LPR)	R	Returns the last priority level for the FIQ interrupts
FIQ Raw Status/Clear	R/W	Contains the premasked interrupts on reads; on writes, it clears active interrupts
FIQ Status	R	Contains postmasked interrupts ORed together to form the FIQ interrupt
IRQ Current Priority Level (CPR)	R/W	Sets the current priority level for the IRQ interrupts
IRQ Enable Clear	W	Clears the corresponding bit in the IRQ Enable register when writing a 1; writing a 0 has no effect
IRQ Enable Set	R/W	Sets up the mask for each interrupt that can generate an interrupt to the processor nIRQ output
IRQ Index	R/W	On Reads this register contains the IRQ channel index location with the highest service priority; on Writes it loads a hardware jump table
IRQ Interrupt Service Routine (ISR) Vector	R/W	Contains the starting address vector of the ISR for the IRQ interrupt with the highest service priority
IRQ Last Priority Level (LPR)	R	Returns the last priority level for the IRQ interrupts
IRQ Raw Status/Clear	R/W	Contains the premasked interrupts when read; on writes, the Clear register clears active interrupts
IRQ Status	R	Contains postmasked interrupts ORed together to form the IRQ interrupt
IRQ/FIQ Soft Interrupt	R/W	Sets a software interrupt

Table 3.7 ApVic Register Summary (Cont.)

Register Name	R/W	Description
Polarity Select	R/W	Determines whether a HIGH or LOW state on each INTERRUPTS[31:0] input causes an interrupt
Priority Table Channel *x*	R/W	Sets channel priorities; there are 32 Priority Table Channel registers, one for each interrupt channel
Resync Select	R/W	Determines whether or not the external interrupts are resynced internally

3.1.8 Remap Register

The remap peripheral located on the APB bus has only one register located at offset 0x0 from the remap base address.

Table 3.8 Chip Select Control Register Summary

Register Name	R/W	Description
Remap Register	R/W	Lets you change the address map after reset when writing to the Remap bit (Remap register bit 0); read this register to determine the address map currently used by the system decoding logic

3.2 System Memory Map

This section summarizes the system boot settings and memory maps.

3.2.1 System Boot Settings

The boot method is selected by using the strap pins BRBOOTSEL, VINITHI, and INITRAM. These three pins determine which device and which address location the ARM926EJ-S processor uses. Possible boot devices are the External SRAM, an external slave connected to the AHB Slave Expansion Port using the Segmentation Bridge, or the Instruction TCM, if the Processor System for ARM926EJ-S supports the use of TCMs. Check the ARM926EJ-S processor datasheet.

The system memory maps and decoding support the boot methods shown in Table 3.9 and Table 3.10.

Table 3.9 System Boot Setting: BRBOOTSEL=0

Address	BRBOOTSEL = 0			
	VINITHI = 0 INITRAM = 0	VINITHI = 1 INITRAM = 0	VINITHI = 0 INITRAM = 1	VINITHI = 1 INITRAM = 1
0x0000.0000–0x0FFF.FFFF	External SRAM	—	Instruction TCM	—
0x1000.0000–0xEFFF.FFFF	—	—	—	—
0xF000.0000–0xFFFF.FFFF	—	External SRAM	—	External SRAM

Table 3.10 System Boot Setting: BRBOOTSEL=1

Address	BRBOOTSEL = 1			
	VINITHI = 0 INITRAM = 0	VINITHI = 1 INITRAM = 0	VINITHI = 0 INITRAM = 1	VINITHI = 1 INITRAM = 1
0x0000.0000–0x0FFF.FFFF	Segmentation Bridge	—	Instruction TCM	—
0x1000.0000–0xEFFF.FFFF	—	—	—	—
0xF000.0000–0xFFFF.FFFF	—	Segmentation Bridge	—	Segmentation Bridge

3.2.2 Memory Map and Addressing

Table 3.11, Table 3.12, Table 3.13, and Table 3.14 show the I-AHB and D-AHB memory maps. Table 3.15 provides an address map for the APB peripherals. Together, these maps specify the memory addresses for every peripheral in the system.

Table 3.11 Address Map for Instruction AHB Bus—TCMs Disabled[1]

Device on Instruction AHB Bus		BRBOOTSEL State				Memory Space
		BRBOOTSEL = 0 (SRAM, Flash, ROM Port)		BRBOOTSEL = 1 (AHB Slave Exp Port)		
		After Reset	After Remap	After Reset	After Remap	
ARM926EJ-S TCMs & External Memory	Instruction TCM (1 Mbyte max)					256 Mbytes
	Data TCM (1 Mbyte max)					
	External SRAM	0x0000.0000–0x0FFF.FFFF				
	Segmentation Bridge (AHB Slave Expansion Port)			0x0000.0000–0x0FFF.FFFF		
	Multiport Memory Controller Port with select pin IHSEL		0x0000.0000–0x0FFF.FFFF		0x0000.0000–0x0FFF.FFFF	
Multiport Memory Controller Port with select pin IHSEL		0x1000.0000–0x7FFF.FFFF				1.75 Gbytes
Segmentation Bridge (AHB Slave Expansion Port)		0x8000.0000–0xDFFF.FFFF				1.5 Gbytes
External SRAM				0xE000.0000–0xEFFF.FFFF		256 Mbytes
Segmentation Bridge (AHB Slave Expansion Port)		0xE000.0000–0xEFFF.FFFF				
External SRAM		0xF000.0000–0xFFFF.FFFF				256 Mbytes
Segmentation Bridge (AHB Slave Expansion Port)				0xF000.0000–0xFFFF.FFFF		

1. TCMs Disabled: INITRAM = 0 at boot and TCMs are not enabled later.

Table 3.12 Address Map for Instruction AHB Bus—TCMs Enabled[1]

Device on Instruction AHB Bus		BRBOOTSEL State				Memory Space
		BRBOOTSEL = 0 (SRAM, Flash, ROM Port)		BRBOOTSEL = 1 (AHB Slave Exp Port)		
		After Reset	After Remap	After Reset	After Remap	
ARM926EJ-S TCMs & External Memory	Instruction TCM (1 Mbyte max)	0x0000.0000–0x001F.FFFF				256 Mbytes
	Data TCM (1 Mbyte max)	0x0020.0000–0x003F.FFFF				
	External SRAM	0x0040.0000–0x0FFF.FFFF				
	Segmentation Bridge (AHB Slave Expansion Port)			0x0040.0000–0x0FFF.FFFF		
	Multiport Memory Controller Port with select pin IHSEL		0x0040.0000–0x0FFF.FFFF		0x0040.0000–0x0FFF.FFFF	
Multiport Memory Controller Port with select pin IHSEL		0x1000.0000–0x7FFF.FFFF				1.75 Gbytes
Segmentation Bridge (AHB Slave Expansion Port)		0x8000.0000–0xDFFF.FFFF				1.5 Gbytes
External SRAM				0xE000.0000–0xEFFF.FFFF		256 Mbytes
Segmentation Bridge (AHB Slave Expansion Port)		0xE000.0000–0xEFFF.FFFF				
External SRAM		0xF000.0000–0xFFFF.FFFF				256 Mbytes
Segmentation Bridge (AHB Slave Expansion Port)				0xF000.0000–0xFFFF.FFFF		

1. TCMs Enabled: INITRAM = 1 at boot or when TCMs are enabled later.

Table 3.13 Address Map for Data AHB Bus—TCMs Disabled[1]

Device on Data AHB Bus		BRBOOTSEL State				Memory Space
		BRBOOTSEL = 0 (SRAM, Flash, ROM Port)		BRBOOTSEL = 1 (AHB Slave Exp Port)		
		After Reset	After Remap	After Reset	After Remap	
ARM926EJ-S TCMs, & External Memory	Instruction TCM (1 Mbyte max)					256 Mbytes
	Data TCM (1 Mbyte max)					
	External SRAM	0x0000.0000–0x0FFF.FFFF				
	Segmentation Bridge (AHB Slave Expansion Port)			0x0000.0000–0x0FFF.FFFF		
	Multiport Memory Controller Port with select pin DHSEL		0x0000.0000–0x0FFF.FFFF		0x0000.0000–0x0FFF.FFFF	
Multiport Memory Controller Port with select pin DHSEL		0x1000.0000–0x7FFF.FFFF				1.75 Gbytes
ApVic		0x8000.0000–0x83FF.FFFF				64 Mbytes
External SRAM configuration registers		0x8400.0000–0x87FF.FFFF				64 Mbytes
Multiport Memory Controller Port configuration registers with select pin DHSELCFG		0x8800.0000–0x8FFF.FFFF				128 Mbytes
APB Bridge (see Table 3.15 for detailed APB address map)		0x9000.0000–0x9FFF.FFFF				256 Mbytes
Segmentation Bridge (AHB Slave Expansion Port)		0xA000.0000–0xDFFF.FFFF				1.0 Gbytes
External SRAM				0xE000.0000–0xEFFF.FFFF		256 Mbytes
Segmentation Bridge (AHB Slave Expansion Port)		0xE000.0000–0xEFFF.FFFF				
External SRAM		0xF000.0000–0xFFFF.FFFF				256 Mbytes
Segmentation Bridge (AHB Slave Expansion Port)				0xF000.0000–0xFFFF.FFFF		

1. TCMs Disabled: INITRAM = 0 at boot and TCMs are not enabled later.

Table 3.14 Address Map for Data AHB Bus—TCMs Enabled[1]

Device on Data AHB Bus		BRBOOTSEL State				Memory Space
		BRBOOTSEL = 0 (SRAM, Flash, ROM Port)		BRBOOTSEL = 1 (AHB Slave Exp Port)		
		After Reset	After Remap	After Reset	After Remap	
ARM926EJ-S TCMs, & External Memory	Instruction TCM (1 Mbyte max)	0x0000.0000–0x001F.FFFF				256 Mbytes
	Data TCM (1 Mbyte max)	0x0020.0000–0x003F.FFFF				
	External SRAM	0x0040.0000–0x0FFF.FFFF				
	Segmentation Bridge (AHB Slave Expansion Port)			0x0040.0000–0x0FFF.FFFF		
	Multiport Memory Controller Port with select pin DHSEL		0x0040.0000–0x0FFF.FFFF		0x0040.0000–0x0FFF.FFFF	
Multiport Memory Controller Port with select pin DHSEL		0x1000.0000–0x7FFF.FFFF				1.75 Gbytes
ApVic		0x8000.0000–0x83FF.FFFF				64 Mbytes
External SRAM configuration registers		0x8400.0000–0x87FF.FFFF				64 Mbytes
Multiport Memory Controller Port configuration registers with select pin DHSELCFG		0x8800.0000–0x8FFF.FFFF				128 Mbytes
APB Bridge (see Table 3.15 for detailed APB address map)		0x9000.0000–0x9FFF.FFFF				256 Mbytes
Segmentation Bridge (AHB Slave Expansion Port)		0xA000.0000–0xDFFF.FFFF				1.0 Gbytes

(Sheet 1 of 2)

Table 3.14 Address Map for Data AHB Bus—TCMs Enabled[1] (Cont.)

Device on Data AHB Bus	BRBOOTSEL State				Memory Space
	BRBOOTSEL = 0 (SRAM, Flash, ROM Port)		BRBOOTSEL = 1 (AHB Slave Exp Port)		
	After Reset	After Remap	After Reset	After Remap	
External SRAM			0xE000.0000–0xEFFF.FFFF		256 Mbytes
Segmentation Bridge (AHB Slave Expansion Port)	0xE000.0000–0xEFFF.FFFF				
External SRAM	0xF000.0000–0xFFFF.FFFF				256 Mbytes
(Sheet 2 of 2)					

1. TCMs Enabled: INITRAM = 1 at boot or when TCMs are enabled later.

Table 3.15 Address Map for APB Bus Peripherals (TCMs Enabled[1] or Disabled[2])

Device on APB Bus	BRBOOTSEL State				Memory Space
	BRBOOTSEL = 0 (SRAM, Flash, ROM Port)		BRBOOTSEL = 1 (AHB Slave Exp Port)		
	After Reset	After Remap	After Reset	After Remap	
GPIO	0x9**0.0000–0x9**0.FFFF[3]				64 Kbytes
Timers	0x9**1.0000–0x9**1.FFFF[3]				64 Kbytes
UART (instance 0)	0x9**2.0000–0x9**2.FFFF[3]				64 Kbytes
UART (instance 1)	0x9**3.0000–0x9**3.FFFF[3]				64 Kbytes
I^2C (instance 0)	0x9**4.0000–0x9**4.FFFF[3]				64 Kbytes
I^2C (instance 1)	0x9**5.0000–0x9**5.FFFF[3]				64 Kbytes
ApE110	0x9**6.0000–0x9**6.FFFF[3]				64 Kbytes
Remap	0x9**7.0000–0x9**7.FFFF[3]				64 Kbytes
Unused	0x9**8.0000–0x9**F.FFFF[3]				~255 Mbytes

1. TCMs Enabled: INITRAM = 1 at boot or when TCMs are enabled later.
2. TCMs Disabled: INITRAM = 0 at boot and TCMs are not enabled later.
3. Indicates that address bits [27:20] are not decoded by any of the system logic, which allows the peripherals to be aliased within this region. The APB peripheral addresses are set up so software can define the peripherals within a 1 Mbyte region. This feature allows you to manage all APB peripherals with a single locked down entry in the ARM926EJ-S Translation Lookaside Buffer (TLB).

The ARM926EJ-S Instruction TCM (I-TCM) and Data TCM (D-TCM) can be placed anywhere in the physical address space. The locations shown in Table 3.12 and Table 3.14 are examples. In these examples, the TCMs are overlaying the External SRAM controller, Segmentation Bridge, and Multiport Memory Controller Ports at address 0x0. Typically, this is done so the exception vectors at location 0x0 can be contained in the I-TCM, improving performance.

You must not overlay the TCMs on peripheral address space, such as the ApVic or APB peripheral spaces. You must also configure the I-TCM and D-TCM size to match the system configuration. The I-TCM and D-TCM sizes are configured after releasing the reset by writing the ARM926EJ-S system control coprocessor (CP15) registers; the SVE initialization code provides some examples.

If the Processor System for ARM926EJ-S supports TCMs, the *0.11 µm Processor System for ARM926EJ-S Integration Guide* contains information about configuring the TCMs.

Chapter 4
Signal Summary

This chapter summarizes the Processor System for ARM926EJ-S external interface signals in these sections:

4.1 System Interfaces

Figure 4.1 is a block diagram showing the Processor System for ARM926EJ-S external signals. The signals are grouped by function and listed alphabetically within each group.

Figure 4.1 System Interfaces

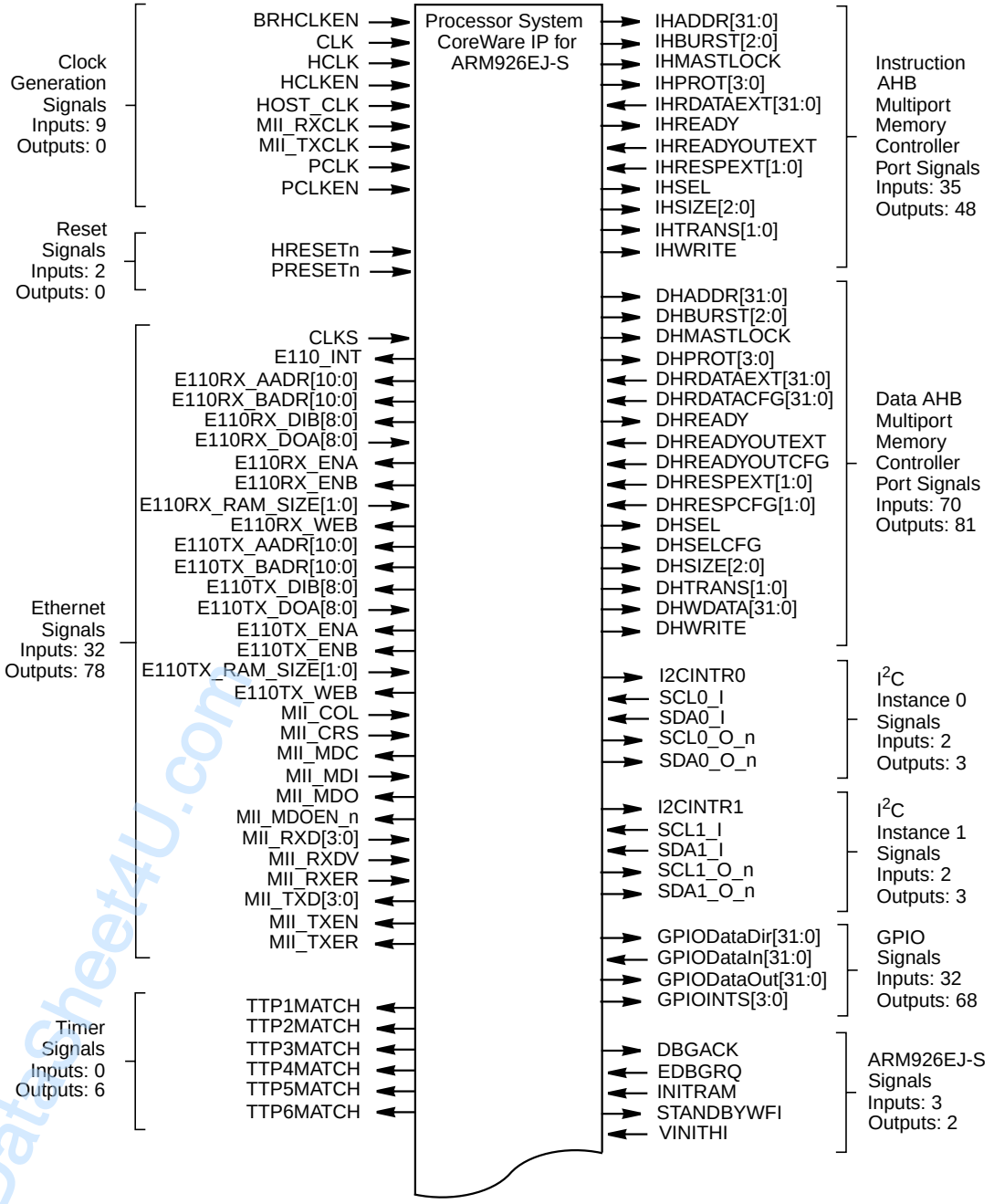
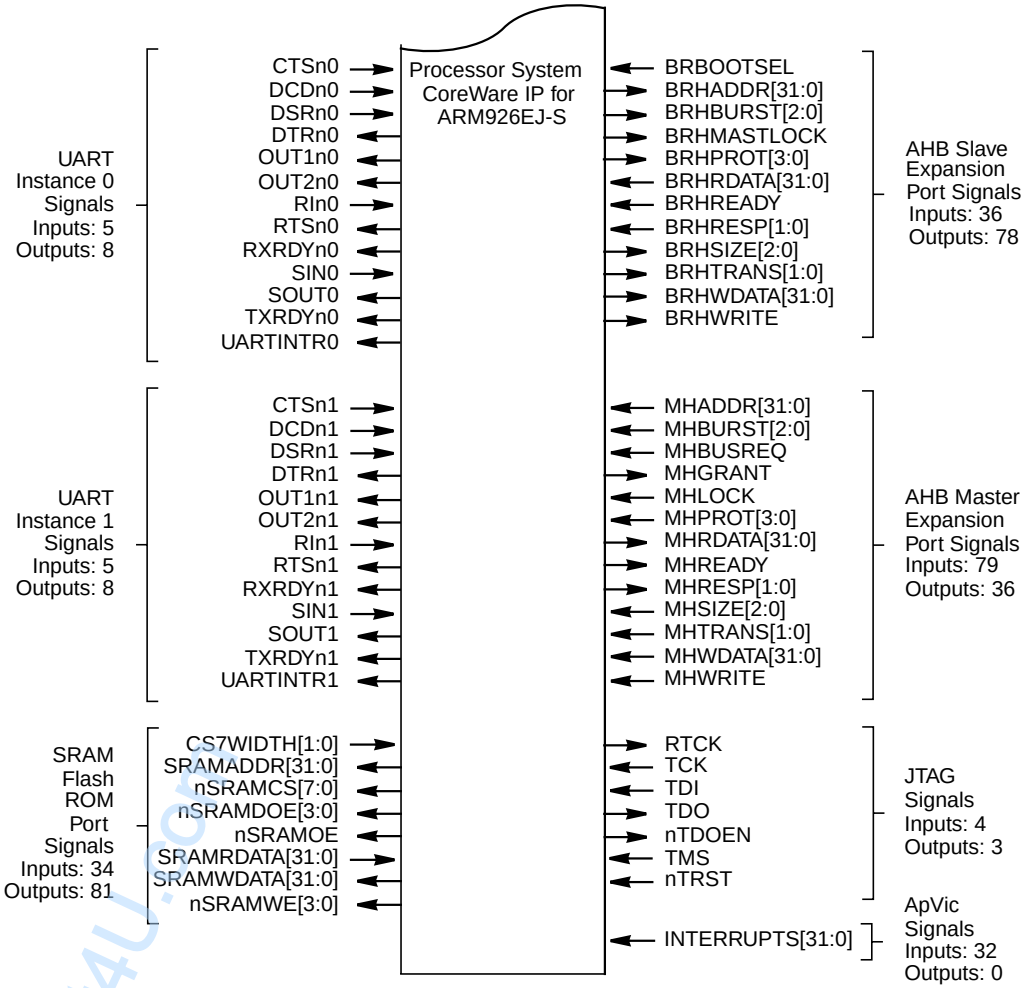


Figure 4.1 System Interfaces (Cont.)



4.2 Interface Signals

Table 4.1 through Table 4.15 briefly describe the Processor System for ARM926EJ-S signals, grouped by function.

- Clock Generation Signals
- Reset Signals
- ARM926EJ-S Signals
- AHB Master Expansion Port Signals
- Ethernet Signals
- ApVic Signals
- ApI2c Signals
- UART Signals
- GPIO Signals
- Timer Signals
- SRAM, Flash, ROM Port Signals
- Instruction AHB Multiport Memory Controller Port Signals
- Data AHB Multiport Memory Controller Port Signals
- AHB Slave Expansion Port Signals
- JTAG Signals

Table 4.1 Clock Generation Signals

Signal Mnemonic	Signal Function	I/O
BRHCLKEN	Segmentation Bridge AHB Clock Enable—Describes the relationship between HCLK and the external AHB-lite bus clock	Input
CLK	Processor Clock	Input
HCLK	System AHB Clock—AHB bus clock for the I-AHB and D-AHB	Input
HCLKEN	System AHB Clock Enable—Describes the relationship between the processor clock and the AHB Clock	Input
HOST_CLK	Host Clock—Derives the MII_MDC clock	Input
MII_RXCLK	Ethernet Receive Nibble or Symbol Clock—Continuous clock providing a timing reference for transferring the MII_RXDV, MII_RXD[3:0], and MII_RXER signals from the PHY to the Ethernet Core	Input

Table 4.1 Clock Generation Signals (Cont.)

Signal Mnemonic	Signal Function	I/O
MII_TXCLK	Ethernet Transmit Nibble or Symbol Clock—Continuous clock providing a timing reference for transferring the MII_TXER signals from the Ethernet Core to the PHY	Input
PCLK	System APB Clock—AMBA peripheral bus (APB) clock	Input
PCLKEN	System APB Clock Enable—Describes the relationship between the AHB Clock and the APB Clock	Input

Table 4.2 Reset Signals

Signal Mnemonic	Signal Function	I/O
HRESETn	AHB Clock System Reset—Carries a chip reset from an external source; asynchronously asserted and synchronously deasserted to AHB Clock	Input
PRESETn	APB Clock System Reset—Carries a chip reset from an external source; asynchronously asserted and synchronously deasserted to APB Clock	Input

Table 4.3 ARM926EJ-S Signals

Signal Mnemonic	Signal Function	I/O
DBGACK	Debug Acknowledge—When HIGH, this signal indicates that the processor is in the debug state	Output
EDBGRQ	External Debug Request—When asserted, it causes the processor to enter the debug state	Input
INITRAM	Tightly-Coupled Memory Enable—When HIGH, the instruction TCM is enabled during reset, when LOW, the TCM is disabled during reset	Input
STANDBYWFI	Stand By–Wait For Interrupt—When HIGH, this signal indicates that the processor is in “wait for interrupt” mode	Output
VINITHI	Exception Vector Location at Reset—Determines the reset location of the exception vectors for the processor	Input

Table 4.4 AHB Master Expansion Port Signals

Signal Mnemonic	Signal Function	I/O
MHADDR[31:0]	AHB Address Bus—32-bit system address bus	Input
MHBURST[2:0]	AHB Burst Type—Indicates whether the transfer is part of a burst and the burst type	Input
MHBUSREQ	AHB Bus Request—When asserted, indicates that the bus Master requires the bus	Input
MHGRANT	AHB Bus Grant—Indicates the expansion Master is currently the highest priority Master	Output
MHLOCK	AHB Locked Transfer—When HIGH, indicates that the Master requires locked access to the bus, and that no other Masters can be granted the bus until it goes LOW	Input
MHPROT[3:0]	AHB Protection Control—Provides information about the bus access level of protection	Input
MHRDATA[31:0]	AHB Read Data Bus—Transfers data from bus Slaves to the bus Master during read operations	Output
MHREADY	AHB Transfer Done—Indicates the existing transfer on the bus is being completed and a new transfer is starting	Output
MHRESP[1:0]	AHB Transfer Response—Provides additional information about the transfer status	Output
MHSIZE[2:0]	AHB Transfer Size—Indicates the size of the transfer	Input
MHTRANS[1:0]	AHB Transfer Response—Provides additional information on the transfer status	Input
MHWDATA[31:0]	AHB Write Data Bus—Transfers data from the Master to the bus Slaves during write operations	Input
MHWRITE	AHB Transfer Direction—Indicates a write transfer when asserted or a read transfer when deasserted	Input

Table 4.5 Ethernet Signals

Signal Mnemonic	Signal Function	I/O
CLKS	Clock Select—Determines the relationship between MII_MDC and the HOST_CLK clock frequencies	Input
E110_INT	Ethernet Interrupt—Interrupt line from the peripheral	Output
E110RX_AADR[10:0]	Receive FIFO Read Address—Read address bus to the Receive FIFO	Output
E110RX_BADR[10:0]	Receive FIFO Write Address—Write address bus to the Receive FIFO	Output

Table 4.5 Ethernet Signals (Cont.)

Signal Mnemonic	Signal Function	I/O
E110RX_DIB[8:0]	Receive Data into FIFO Port B—Carries receive data written into the Receive FIFO by the E-110 MAC	Output
E110RX_DOA[8:0]	Receive Data out of FIFO Port A—Carries receive data read from the Receive FIFO by the ApE110 DMAC	Input
E110RX_ENA	Receive Enable Port A—Output enable to the Receive FIFO RAM read port	Output
E110RX_ENB	Receive Enable Port B—Enable to the Receive FIFO RAM write port	Output
E110RX_RAM_SIZE[1:0]	Receive FIFO RAM Size—Strap these inputs to define the Receive FIFO RAM size	Input
E110RX_WEB	Receive Write Enable Port B—Write enable from the E-110 MAC to strobe data into the Receive FIFO	Output
E110TX_AADR[10:0]	Transmit FIFO Read Address—Read address bus to the Transmit FIFO	Output
E110TX_BADR[10:0]	Transmit FIFO Write Address—Write address bus to the Transmit FIFO	Output
E110TX_DIB[8:0]	Transmit Data into FIFO Port B—Carry transmit data the ApE110 DMAC wrote into the Transmit FIFO	Output
E110TX_DOA[8:0]	Transmit Data out of FIFO Port A—Carry transmit data the E-110 MAC read from the Transmit FIFO	Input
E110TX_ENA	Transmit Enable Port A—Output enable to the Transmit FIFO RAM read port	Output
E110TX_ENB	Transmit Enable Port B—Enable to the Transmit FIFO RAM write port	Output
E110TX_RAM_SIZE[1:0]	Transmit FIFO RAM Size—Strap these inputs to define the Transmit FIFO RAM size	Input
E110TX_WEB	Transmit Write Enable Port B—Write enable from the ApE110 DMAC to strobe data into the Transmit FIFO	Output
MII_COL	Ethernet Collision Detected—When the Ethernet PHY detects a collision, it asserts the MII_COL signal asynchronously with minimum delay from the start of collision on the media	Input
MII_CRS	Ethernet Carrier Sense—When a non-idle medium is detected, the Ethernet PHY asserts the MII_CRS signal asynchronously with minimum delay	Input
MII_MDC	Ethernet Management Data Clock—The Ethernet PHY uses MII_MDC as a timing reference for the transfer of information on the MII_MDI and MII_MDO signal lines	Output
MII_MDI	Ethernet Management Data In—The Ethernet PHY device places the Ethernet control information on MII_MDI, and MII_MDC clocks it synchronously	Input

Table 4.5 Ethernet Signals (Cont.)

Signal Mnemonic	Signal Function	I/O
MII_MDO	Ethernet Management Data Out—Transfers Ethernet control information on the MII_MDO signal to the Ethernet PHY device	Output
MII_MDOEN_n	Ethernet Management Data Output Enable—Provides the 3-state enable for MII_MDO when MII_MDO and MII_MDI are combined into a bidirectional line (MII_MDIO) outside the Ethernet peripheral	Output
MII_RXD[3:0]	Ethernet Receive Nibble Data—Consists of four data signals that the Ethernet PHY drives synchronously to the rising edge of MII_RXCLK	Input
MII_RXDV	Ethernet Receive Data Valid—The Ethernet PHY asserts MII_RXDV to indicate that the Ethernet PHY is presenting recovered and decoded nibbles on the MII_RXD[3:0] signals, and that MII_RXCLK is synchronous to the recovered data	Input
MII_RXER	Ethernet Receive Error—The Ethernet PHY asserts MII_RXER to indicate to the Ethernet core that a media error (for example, a coding error) was detected somewhere in the frame being transferred to the Ethernet PHY	Input
MII_TXD[3:0]	Ethernet Transmit Nibble Data—Consists of four data signals that are synchronous to the rising edge of MII_TXCLK	Output
MII_TXEN	Ethernet Transmit Enable—Indicates that the Ethernet core is presenting MII_TXD[3:0] nibbles on the MII for transmission	Output
MII_TXER	Ethernet Transmit Coding Error—Causes the Ethernet PHY to transmit one or more symbols not part of the frame to indicate there has been a transmitter coding error	Output

Table 4.6 ApVic Signals

Signal Mnemonic	Signal Function	I/O
INTERRUPTS[31:0]	System External Interrupt—External interrupt inputs to the Vectored Interrupt Controller	Input

Table 4.7 ApI2c Signals

Signal Mnemonic	Signal Function	I/O
I2CINTR#	I^2C Interrupt—Indicates an internal interrupt is pending from one of the Master or Slave sources	Output
SCL#_I	I^2C Bus SCL In—SCL input clock signal	Input

Table 4.7 ApI2c Signals (Cont.)

Signal Mnemonic	Signal Function	I/O
SCL#_O_n	I^2C Bus SCL Output—ApI2c output signal drives the I^2C bus SCL clock signal	Output
SDA#_I	I^2C Bus SDA In—SDA serial data input signal	Input
SDA#_O_n	I^2C Bus SDA Output—ApI2c output signal drives the I^2C bus SDA data signal	Output

Table 4.8 UART Signals

Signal Mnemonic	Signal Function	I/O
CTSn#	Clear to Send—Indicates the modem or data set is ready to exchange data	Input
DCDn#	Data Carrier Detect—Indicates the data carrier has been detected by the modem or data set	Input
DSRn#	Data Set Ready—Indicates the modem or data set is ready to establish communications with the UART	Input
DTRn#	Data Terminal Ready—Informs the modem or data set the UART is ready to establish communications	Output
OUT1n#	User Controlled Output—User-designated output	Output
OUT2n#	User Controlled Output—User-designated output	Output
RIn#	Ring Indicator—Indicates a telephone ringing signal has been received by the modem or data set	Input
RTSn#	Request to Send—Informs the modem or data set the UART is ready to exchange data	Output
RXRDYn#	Receiver Ready—Receiver DMA signaling is available	Output
SIN#	Serial Input—Serial data input from the communications link	Input
SOUT#	Serial Output—Composite serial data output to the communications link	Output
TXRDYn#	Transmitter Ready—Transmitter DMA signaling is available	Output
UARTINTR#	UART Interrupt—Goes HIGH when one of the interrupt types has an active HIGH condition	Output

Table 4.9 GPIO Signals

Signal Mnemonic	Signal Function	I/O
GPIODataDir[31:0]	General-Purpose I/O Data Direction—Reflects the contents of the GPIO Data Direction Registers and indicates whether a GPIO bit is an input or output	Output
GPIODataIn[31:0]	GPIO Data In—Inputs to the GPIO peripheral	Input
GPIODataOut[31:0]	GPIO Data Out —Outputs from the GPIO peripheral	Output
GPIOINTS[3:0]	Interrupt Vector—Indicates an interrupt was detected in GPIO (n+1)	Output

Table 4.10 Timer Signals

Signal Mnemonic	Signal Function	I/O
TTP1MATCH	Timer Trigger Point 1 Match—Indicates a match between the Trigger Point 1 value and selected timer value	Output
TTP2MATCH	Timer Trigger Point 2 Match—Indicates a match between the Trigger Point 2 value and selected timer value	Output
TTP3MATCH	Timer Trigger Point 3 Match—Indicates a match between the Trigger Point 3 value and selected timer value	Output
TTP4MATCH	Timer Trigger Point 4 Match—Indicates a match between the Trigger Point 4 value and selected timer value	Output
TTP5MATCH	Timer Trigger Point 5 Match—Indicates a match between the Trigger Point 5 value and selected timer value	Output
TTP6MATCH	Timer Trigger Point 6 Match—Indicates a match between the Trigger Point 6 value and selected timer value	Output

Table 4.11 SRAM, Flash, ROM Port Signals

Signal Mnemonic	Signal Function	I/O
CS7WIDTH[1:0]	Chip Select 7 Data Width Select—Provides the reset value of the Chip Select 7 Control Register Width field	Input
nSRAMCS[7:0]	External SRAM Chip Selects—Controls the chip select signals for the external SRAM	Output
nSRAMDOE[3:0]	SRAM Data Output Enable—Controls the direction of the data for the external SRAM controller	Output
nSRAMOE	External SRAM Output Enable—Enables the SRAM outputs	Output
nSRAMWE[3:0]	External SRAM Write Enables—Indicates valid write operations to the SRAM	Output

Table 4.11 SRAM, Flash, ROM Port Signals (Cont.)

Signal Mnemonic	Signal Function	I/O
SRAMADDR[31:0]	External SRAM Address—External SRAM address bus	Output
SRAMRDATA[31:0]	SRAM Read Data—Carries the data read out from the SRAM	Input
SRAMWDATA[31:0]	SRAM Write Data—Carries the data written to the SRAM	Output

Table 4.12 Instruction AHB Multiport Memory Controller Port Signals

Signal Mnemonic	Signal Function	I/O
IHADDR[31:0]	AHB Address Bus—32-bit system address bus	Output
IHBURST[2:0]	AHB Burst Type—Indicates whether the transfer is part of a burst and the burst type	Output
IHMASTLOCK	AHB Locked Sequence—Indicates the current Master is performing a locked transfer sequence	Output
IHPROT[3:0]	AHB Protection Control—Provides information about protection level of a bus access	Output
IHRDATAEXT[31:0]	AHB Read Data Bus—Transfers data from bus Slaves to the bus Master during read operations	Input
IHREADY	AHB Transfer Done—Indicates the existing transfer on the bus is complete and a new transfer is starting	Output
IHREADYOUTEXT	AHB Transfer Done—Indicates that a transfer has finished on the bus	Input
IHRESPEXT[1:0]	AHB Transfer Response—Provides additional information on the transfer status	Input
IHSEL	AHB Slave Select to Memory—Combinational address bus decode	Output
IHSIZE[2:0]	AHB Transfer Size—Indicates the transfer size	Output
IHTRANS[1:0]	AHB Transfer Type—Current transfer type	Output
IHWRITE	AHB Transfer Direction—Indicates a write transfer when asserted or a read transfer when deasserted	Output

Table 4.13 Data AHB Multiport Memory Controller Port Signals

Signal Mnemonic	Signal Function	I/O
DHADDR[31:0]	AHB Address Bus—32-bit system address bus	Output
DHBURST[2:0]	AHB Burst Type—Indicates whether the transfer is part of a burst and the burst type	Output
DHMASTLOCK	AHB Locked Sequence—Indicates the current Master is performing a locked transfer sequence	Output

Table 4.13 Data AHB Multiport Memory Controller Port Signals (Cont.)

Signal Mnemonic	Signal Function	I/O
DHPROT[3:0]	AHB Protection Control—Provides information about protection level of a bus access	Output
DHRDATACFG[31:0]	AHB Configuration Port Read Data Bus—Transfers data from bus Slaves to the bus Master during read operations	Input
DHRDATAEXT[31:0]	AHB Memory Port Read Data Bus—Transfers data from bus Slaves to the bus Master during read operations	Input
DHREADY	AHB Transfer Done—Indicates the existing transfer on the bus is complete and a new transfer is starting	Output
DHREADYOUTCFG	AHB Configuration Port Transfer Done—Indicates that a configuration port bus transfer is complete	Input
DHREADYOUTEXT	AHB Memory Port Transfer Done—Indicates that a memory port bus transfer is complete	Input
DHRESPCFG[1:0]	AHB Configuration Port Transfer Response—Provides additional information about the configuration port transfer status	Input
DHRESPEXT[1:0]	AHB Memory Port Transfer Response—Provides additional information about the memory port transfer status	Input
DHSEL	AHB Slave Select to Memory—Indicates memory accesses to a DDR SDRAM controller	Output
DHSELCFG	AHB Slave Select to Register Configuration—Indicates register configuration accesses to a DDR SDRAM controller	Output
DHSIZE[2:0]	AHB Transfer Size	Output
DHTRANS[1:0]	AHB Transfer Type—Current transfer type	Output
DHWDATA[31:0]	AHB Write Data Bus—Transfers data from the Master to the bus Slaves during write operations	Output
DHWRITE	AHB Transfer Direction—Indicates a write transfer when asserted or a read transfer when deasserted	Output

Table 4.14 AHB Slave Expansion Port Signals

Signal Mnemonic	Signal Function	I/O
BRBOOTSEL	Bridge Boot Select—Indicates from which port the processor will boot	Input
BRHADDR[31:0]	AHB Address Bus—32-bit system address bus	Output
BRHBURST[2:0]	AHB Burst Type—Indicates whether the transfer is part of a burst and the burst type	Output
BRHMASTLOCK	AHB Master Lock—Indicates whether the Master requires locked access on the external bus	Output

Table 4.14 AHB Slave Expansion Port Signals (Cont.)

Signal Mnemonic	Signal Function	I/O
BRHPROT[3:0]	AHB Protection Control—Provides information about protection level of a bus access	Output
BRHRDATA[31:0]	AHB Read Data Bus—Transfers data from the Slave(s) on the external bus during read operations	Input
BRHREADY	AHB Transfer Done—Indicates whether a transfer has finished on the external bus	Input
BRHRESP[1:0]	AHB Transfer Response—Provides additional information on the transfer status	Input
BRHSIZE[2:0]	AHB Transfer Size	Output
BRHTRANS[1:0]	AHB Transfer Type	Output
BRHWDATA[31:0]	AHB Write Data Bus—Transfers data from the bridge to the Slave(s) on the external bus during write operations	Output
BRHWRITE	AHB Transfer Direction—Indicates a write transfer when asserted or a read transfer when deasserted	Output

Table 4.15 JTAG Signals

Signal Mnemonic	Signal Function	I/O
nTDOEN	JTAG Test Data Output Enable—Enables test data output	Output
nTRST	JTAG Test Reset—Used to reset ARM926EJ-S debug logic including the EmbeddedICE™ logic, TAP controller, and boundary scan cells; does not reset the entire processor system	Input
RTCK	JTAG Returned Test Clock—Returned TCK that can be used by ARM Multi-ICE® debug tools with adaptive clocking to synchronize to the JTAG port	Output
TCK	JTAG Test Clock—Used as a data enable in the synchronizing logic included in the processor system	Input
TDI	JTAG Test Data Input—Test data input signal	Input
TDO	JTAG Test Data Output—Test data output signal	Output
TMS	JTAG Test Mode Select	Input

Chapter 5
Specifications

This chapter summarizes the Processor System for ARM926EJ-S physical specifications.

This chapter contains the following sections:

5.1 Physical Specifications

The physical specifications of the Processor System for ARM926EJ-S are shown below:

Process Technology	0.11 µm (Gflx-r)
Gate Count	164,000[1]
Metal Stack	N/A

1. Excluding the ARM926EJ-S and its TCMs

5.2 Operating Conditions

The core is characterized for:

- Setup times: Worst Case Industrial (wcind)
- Hold times: N/A

Table 5.1 shows the Processor System for ARM926EJ-S timing conditions.

Table 5.1 Processor System for ARM926EJ-S Timing Conditions

AC Timing	Process	VDD (V)	Junction Temperature (^{o}C)
Best Case, Industrial	0.81	1.26	–40
Worst Case, Industrial	1.32	1.08	125

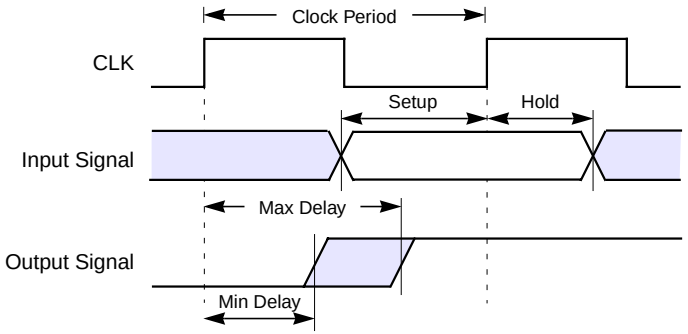
5.3 AC Electrical Specifications

All AC timing values are referenced to an ideal system clock input to the Processor System for ARM926EJ-S.

Input setup time is measured from the time the signal is valid to the rising edge of an ideal clock and includes the sink flip-flop setup time. Input hold time is measured from the rising edge of the ideal clock to the time the signal goes invalid. For input setup times, the driver must drive the signal valid before any receivers need it. For input hold times, the driver must hold the signal valid longer than needed by any receiver. The maximum delay times for outputs are measured from the rising edge of ideal clock, and include CP->Q of the source flip-flop.

Figure 5.1 shows how AC timing is measured.

Figure 5.1 AC Specifications



The maximum frequency for each clock of the Processor System for ARM926EJ-S in each technology is shown in Table 5.2:

Table 5.2 Maximum Clock Frequency

Clock	Maximum frequency (MHz) (cw001200_agflxr_2_0)
CLK	200
HCLK	100
PCLK	50
HOST_CLK	25–33
MII_RXCLK	2.5 or 25
MII_TXCLK	2.5 or 25

Maximum frequency is heavily dependent on the system. The maximum clock frequency estimate assumes input and output delays as a function of the clock period.

The Processor System for ARM926EJ-S is a Firm core that delivers a netlist without placement information. Therefore hold time values are not precise enough to be useful and are not reported in this document.

This design has been rated using static timing analysis for a 50/50 duty cycle. The design is nearly independent of duty cycle because it is fully synchronous other than the lock-up latches for scan.

5.3.1 Input Timing

Table 5.3, Table 5.4, Table 5.6, Table 5.7, Table 5.8, and Table 5.9 show the AC timing values for the Processor System for ARM926EJ-S input pins. The input value is a percentage of the maximum clock frequency for a given technology. Because the IP is delivered as a Firm netlist, the

input times represented are only estimates and are valid for all technologies.

Table 5.3 Input Timing in the CLK Domain

Input Pin	Input Setup cw001200_agflxr_2_0 with cw001124_1_0
EDBGRQ	35%
INITRAM	15%
VINITHI	15%

Table 5.4 Input Timing in the HCLK Domain

Input Pin	Input Setup cw001200_agflxr_2_0 with cw001124_1_0
BRBOOTSEL	40%
BRHCLKEN	20%
BRHRDATA[*]	5%
BRHREADY	20%
BRHRESP[*]	20%
CS7WIDTH[*]	10%
DHRDATACFG[*]	25%
DHRDATAEXT[*]	25%
DHREADYOUTCFG	40%
DHREADYOUTEXT	40%
DHRESPCFG[*]	40%
DHRESPEXT[*]	40%
E110RX_DOA[*]	20%
E110RX_RAM_SIZE[*]	15%
E110TX_RAM_SIZE[*]	10%

Table 5.4 Input Timing in the HCLK Domain (Cont.)

Input Pin	Input Setup cw001200_agflxr_2_0 with cw001124_1_0
HCLKEN	20%
IHRDATAEXT	10%
IHREADYOUTEXT	25%
IHRESPEXT[*]	15%
INTERRUPTS[*]	55%
MHADDR[*]	50%
MHBURST[*]	30%
MHBUSREQ	5%
MHLOCK	10%
MHPROT[*]	20%
MHSIZE[*]	25%
MHTRANS[*]	40%
MHWDATA[*]	30%
MHWRITE	35%
SRAMRDATA[*]	5%

Table 5.5 Input Timing in the HOST_CLK Domain

Input Pin	Input Setup cw001200_agflxr_2_0 with cw001124_1_0
CLKS	10%

Table 5.6 Input Timing in the MII_RXCLK Domain

Input Pin	Input Setup cw001200_agflxr_2_0 with cw001124_1_0
MII_RXD[*]	10%
MII_RXDV	10%
MII_RXER	5%

Table 5.7 Input Timing in the MII_TXCLK Domain

Input Pin	Input Setup cw001200_agflxr_2_0 with cw001124_1_0
E110TX_DOA[*]	10%
MII_COL	5%
MII_CRS	5%

Table 5.8 Input Timing in the PCLK Domain

Input Pin	Input Setup cw001200_agflxr_2_0 with cw001124_1_0
CTSn0	5%
CTSn1	5%
DCDn0	5%
DCDn1	5%
DSRn0	5%
DSRn1	5%
GPIODataIn[*]	10%
PCLKEN	25%

Table 5.8 Input Timing in the PCLK Domain (Cont.)

Input Pin	Input Setup cw001200_agflxr_2_0 with cw001124_1_0
RIn0	5%
RIn1	5%
SCL0_I	5%
SCL1_I	5%
SDA0_I	5%
SDA1_I	5%
SIN0	5%
SIN1	5%

Table 5.9 Input Timing in the TCK Domain

Input Pin	Input Setup cw001200_agflxr_2_0 with cw001124_1_0
TDI	10%
TMS	10%

5.3.2 Output Timing

Table 5.10, Table 5.11, Table 5.12, Table 5.13, Table 5.14, and Table 5.15 show the AC timing values for the Processor System for ARM926EJ-S output pins as a percentage of the maximum clock frequency in a given

technology. Because the IP is delivered as a Firm netlist, the output times represented are only estimates, and are valid for all technologies.

Table 5.10 Output Timing in the CLK Domain

Output Pin	Output Valid cw001200_agflxr_2_0 with cw001124_1_0
DBGACK	50%
nTDOEN	30%
RTCK	15%
STANDBYWFI	20%
TDO	40%

Table 5.11 Output Timing in the HCLK Domain

Output Pin	Output Valid cw001200_agflxr_2_0 with cw001124_1_0
BRHADDR[*]	10%
BRHBURST[*]	10%
BRHMASTLOCK	10%
BRHPROT[*]	10%
BRHSIZE[*]	10%
BRHTRANS[*]	10%
BRHWDATA[*]	10%
BRHWRITE	10%
DHADDR[*]	30%
DHBURST[*]	25%
DHMASTLOCK	10%
DHPROT[*]	25%
DHREADY	35%

Table 5.11 Output Timing in the HCLK Domain (Cont.)

Output Pin	Output Valid cw001200_agflxr_2_0 with cw001124_1_0
DHSEL	40%
DHSELCFG	40%
DHSIZE[*]	25%
DHTRANS[*]	30%
DHWDATA[*]	20%
DHWRITE	25%
E110_INT	15%
E110RX_AADR[*]	15%
E110RX_ENA	10%
E110TX_BADR[*]	10%
E110TX_DIB[*]	30%
E110TX_ENB	20%
E110TX_WEB	15%
IHADDR[*]	20%
IHBURST[*]	15%
IHMASTLOCK	10%
IHPROT[*]	15%
IHREADY	30%
IHSEL	20%
IHSIZE[*]	20%
IHTRANS[*]	10%
IHWRITE	10%
MHGRANT	30%
MHRDATA[*]	40%

Table 5.11 Output Timing in the HCLK Domain (Cont.)

Output Pin	Output Valid cw001200_agflxr_2_0 with cw001124_1_0
MHREADY	35%
MHRESP[*]	35%
nSRAMCS[*]	10%
nSRAMDOE[*]	10%
nSRAMOE	10%
nSRAMWE[*]	10%
SRAMADDR[*]	10%
SRAMWDATA[*]	10%

Table 5.12 Output Timing in the HOST_CLK Domain

Output Pin	Output Valid cw001200_agflxr_2_0 with cw001124_1_0
MII_MDC	5%
MII_MDO	5%
MII_MDOEN_n	5%

Table 5.13 Output Timing in the MII_RXCLK Domain

Output Pin	Output Valid cw001200_agflxr_2_0 with cw001124_1_0
E110RX_BADR[*]	5%
E110RX_DIB[*]	10%
E110RX_ENB	10%
E110RX_WEB	10%

Table 5.14 Output Timing in the MI_TXCLK Domain

Output Pin	Output Valid cw001200_agflxr_2_0 with cw001124_1_0
E110TX_AADR[*]	5%
E110TX_ENA	10%
MII_TXD[*]	5%
MII_TXEN	5%
MII_TXER	5%

Table 5.15 Output Timing in the PCLK Domain

Output Pin	Output Valid cw001200_agflxr_2_0 with cw001124_1_0
DTRn0	30%
DTRn1	30%
GPIODataDir[*]	10%
GPIODataOut[*]	10%
GPIOINTS[*]	15%
I2CINTR0	10%
I2CINTR1	10%
OUT1n0	30%
OUT1n1	30%
OUT2n0	30%
OUT2n1	30%
RTSn0	30%
RTSn1	30%
RXRDYn0	10%

Table 5.15 Output Timing in the PCLK Domain (Cont.)

Output Pin	Output Valid cw001200_agflxr_2_0 with cw001124_1_0
RXRDYn1	10%
SCL0_O_n	10%
SCL1_O_n	10%
SDA0_O_n	10%
SDA1_O_n	10%
SOUT0	15%
SOUT1	15%
TTPxMATCH	15%
TXRDYn0	10%
TXRDYn1	10%
UARTINTR0	10%
UARTINTR1	10%

5.3.3 Pass-Through Timing

The Processor System for ARM926EJ-S, when analyzed individually, contains several pass-through paths. These paths are defined in two ways: The port to and from an internal register; and the port to another port. In Section 5.3.1, “Input Timing,” the percentage of the clock for input setup of the input port to an internal register is reported.

Likewise in Section 5.3.2, “Output Timing,” the percentage of clock for output valid for an internal register to the output port is reported. In this section the AC timing value of the input port to the output port is reported. The rest of the clock period must be shared by the logic connected to the input and output ports.

Table 5.16 shows the AC timing values for the Processor System for ARM926EJ-S pass-through pins as a percentage of the maximum clock frequency in a given technology. Because the IP is delivered as a Firm netlist, the times represented are only estimates, and are valid for all

technologies. The *0.11 µm Processor System for ARM926EJ-S Integration Application Note* contains more information about these paths.

Table 5.16 Pass-Through Paths in the HCLK Domain

Input Pin	Output Pin	Pass-Through Time cw001200_agflxr_2_0 with cw001124_1_0
DHRDATACFG[*]	MHRDATA[*]	10%
DHRDATAEXT[*]	MHRDATA[*]	15%
DHREADYOUTCFG	DHREADY	20%
DHREADYOUTCFG	MHREADY	15%
DHREADYOUTEXT	DHREADY	20%
DHREADYOUTEXT	MHREADY	15%
DHRESPCFG[*]	MHRESP[*]	15%
DHRESPEXT[*]	MHRESP[*]	15%
GPIODataIn[*]	GPIOINTS[*]	10%
GPIODataIn[*]	MHRDATA[*]	15%
IHREADYOUTEXT	IHREADY	15%
MHADDR[*]	DHADDR[*]	10%
MHADDR[*]	DHSEL	20%
MHADDR[*]	DHSELCFG	20%
MHBURST[*]	DHBURST[*]	10%
MHPROT[*]	DHPROT[*]	10%

Table 5.16 Pass-Through Paths in the HCLK Domain (Cont.)

Input Pin	Output Pin	Pass-Through Time cw001200_agflxr_2_0 with cw001124_1_0
MHSIZE[*]	DHSIZE[*]	10%
MHTRANS[*]	DHTRANS[*]	10%
MHWDATA[*]	DHWDATA[*]	10%
MHWRITE	DHWRITE	10%
PCLKEN	DHREADY	10%
PCLKEN	MHREADY	10%