



## Universal Hexadecimal Counter

### AVAILABLE AS MILITARY SPECIFICATIONS

- MIL-STD-883, Paragraph 1.2.2 Compliant

### GENERAL DESCRIPTION

The AS10H536 is a high speed synchronous hexadecimal counter. This MECL 10H part which is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in powersupply current.

### FEATURES

- Counting frequency, 250 MHz minimum
- 900 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible
- Available in a 16-pin DIP package (C designator), CDIP2-T16 per MIL-STD-1835 and in a 16-pin Flatpack (F designator), CDFP4-F16 per MIL-STD-1835.

### BURN-IN CONDITIONS:

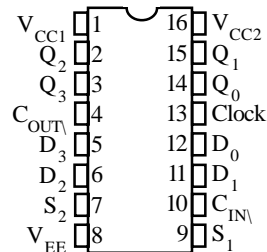
$V_{TT} = -2.0V \text{ MAX} / -2.2V \text{ MIN}$

$V_{EE} = -5.7V \text{ MAX} / -5.2V \text{ MIN}$

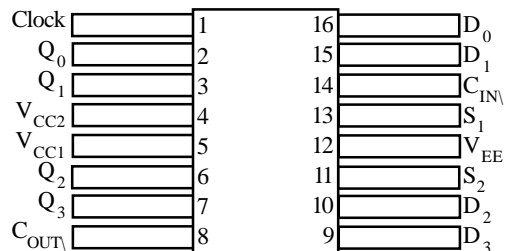
For more products and information please visit our web site at [www.austinsemiconductor.com](http://www.austinsemiconductor.com)

### PIN ASSIGNMENT (Top View)

#### 16-Pin Side Brazed DIP (C Designator)



#### 16-Pin Bottom Brazed FP (F Designator)



Function Select Table

$C_{IN}$	$S_1$	$S_2$	Operating Mode
Don't Care	L	L	Preset (Program)
L	L	H	Increment (Count Up)
H	L	H	Hold Count
L	H	L	Decrement (Count Down)
H	H	L	Hold Count
Don't Care	H	H	Hold (Stop Count)



**PIN ASSIGNMENTS  
(Ceramic DIP)**

FUNCTION	PIN #	BURN-IN (CONDITION C)
V <sub>CC1</sub>	1	GND
Q <sub>2</sub>	2	51 Ω to V <sub>TT</sub>
Q <sub>3</sub>	3	51 Ω to V <sub>TT</sub>
C <sub>OUT</sub> ∖	4	51 Ω to V <sub>TT</sub>
D <sub>3</sub>	5	GND
D <sub>2</sub>	6	GND
S <sub>2</sub>	7	OPEN
V <sub>EE</sub>	8	V <sub>EE</sub>
S <sub>1</sub>	9	OPEN
C <sub>IN</sub> ∖	10	OPEN
D <sub>1</sub>	11	GND
D <sub>0</sub>	12	GND
CLK	13	CP1
Q <sub>0</sub>	14	51 Ω to V <sub>TT</sub>
Q <sub>1</sub>	15	51 Ω to V <sub>TT</sub>
V <sub>CC2</sub>	16	GND

**PIN ASSIGNMENTS  
(Ceramic FP)**

FUNCTION	PIN #	BURN-IN (CONDITION C)
CLK	1	CP1
Q <sub>0</sub>	2	51 Ω to V <sub>TT</sub>
Q <sub>1</sub>	3	51 Ω to V <sub>TT</sub>
V <sub>CC2</sub>	4	GND
V <sub>CC1</sub>	5	GND
Q <sub>2</sub>	6	51 Ω to V <sub>TT</sub>
Q <sub>3</sub>	7	51 Ω to V <sub>TT</sub>
C <sub>OUT</sub> ∖	8	51 Ω to V <sub>TT</sub>
D <sub>3</sub>	9	GND
D <sub>2</sub>	10	GND
S <sub>2</sub>	11	OPEN
V <sub>EE</sub>	12	V <sub>EE</sub>
S <sub>1</sub>	13	OPEN
C <sub>IN</sub> ∖	14	OPEN
D <sub>1</sub>	15	GND
D <sub>0</sub>	16	GND

**ORDERING INFORMATION**

EXAMPLE: AS10H536C16MIL

Device Number	Package Type	Pin Count	Process*
AS10H536	C	16	MIL
AS10H536	F	16	MIL

**\*AVAILABLE PROCESSES**

MIL = Military Processing

-55°C to +125°C



# Universal Hexadecimal Counter AS10H536

Austin Semiconductor, Inc.

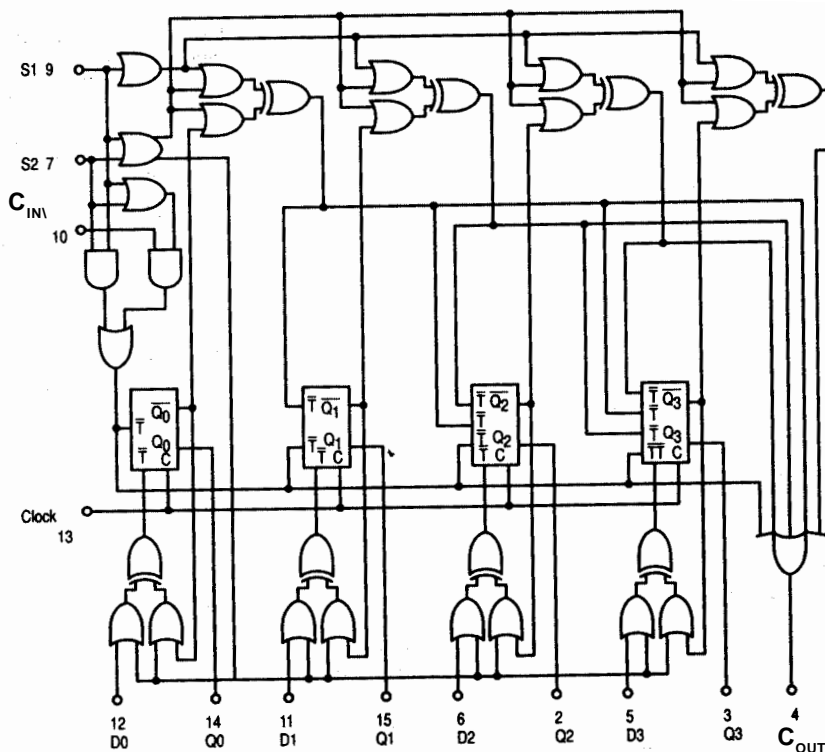
SEQUENTIAL TRUTH TABLE •												
S <sub>1</sub>	S <sub>2</sub>	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	Carry IN	Clock	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Carry OUT
L	L	L	L	H	H	∅	H	L	L	H	H	L
L	H	∅	∅	∅	∅	L	H	H	L	H	H	H
L	H	∅	∅	∅	∅	L	H	L	H	H	H	H
L	H	∅	∅	∅	∅	L	H	H	H	H	H	L
L	H	∅	∅	∅	∅	H	L	H	H	H	H	H
L	H	∅	∅	∅	∅	H	H	H	H	H	H	H
L	H	∅	∅	∅	∅	∅	H	H	H	H	H	H
L	L	H	H	L	L	∅	H	H	H	L	L	L
H	L	∅	∅	∅	∅	L	H	L	H	L	L	H
H	L	∅	∅	∅	∅	L	H	H	L	L	L	H
H	L	∅	∅	∅	∅	L	H	L	L	L	L	L
H	L	∅	∅	∅	∅	L	H	H	H	H	H	H

∅ = Don't Care

● Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.

●● A clock H is defined as a clock input transition from a low to a high logic level.

**FIGURE 1. Logic Diagram**



NOTES: Flip flops will toggle when all T\ inputs are LOW.



QUIESCENT LIMIT TABLE\*

\* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

Test Temperature	Test Voltage Values (Volts)									
	V <sub>IH1</sub>	V <sub>IL1</sub>	V <sub>IH2</sub>	V <sub>IL2</sub>	PS1	PS2	VEE1	VEE2	VEEL	VEEL
T <sub>A</sub> = 25 °C	-0.780	-1.950	-1.11	-1.48	+1.11	+0.31	-5.46	-4.94	-2.94	-2.94
T <sub>A</sub> = 125 °C	-0.650	-1.950	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94	-2.94
T <sub>A</sub> = -55 °C	-0.840	-1.950	-1.16	-1.51	+1.01	+0.28	-5.46	-4.94	-2.94	-2.94

SYM	PARAMETER	LIMITS						UNITS	TEST VOLTAGE APPLIED TO PINS BELOW												
		+25°C		+125°C		-55°C			Pinouts referenced are for DIP Package, Check Pin Assignments V <sub>CC</sub> =0V, Output Load=100Ω to -2.0V												
		Subgroup 1	Subgroup 2	Subgroup 1	Subgroup 2	Subgroup 1	Subgroup 2		V <sub>IH1</sub>	V <sub>IL1</sub>	V <sub>EE2</sub>	V <sub>EE1</sub>	V <sub>CC</sub>	P.U.T.							
V <sub>OH</sub>	High Output Voltage	MIN	MAX	MIN	MAX	MIN	MAX														
V <sub>OL</sub>	Low Output Voltage																				
V <sub>OH1</sub>	High Output Voltage																				
V <sub>OL1</sub>	Low Output Voltage																				
I <sub>EE</sub>	Power Supply Current																				
I <sub>IH</sub>	Input Current High																				
I <sub>IH1</sub>	Input Current High																				
I <sub>IH2</sub>	Input Current High																				
I <sub>IH3</sub>	Input Current High																				
I <sub>IL</sub>	Input Current Low																				



QUIESCENT LIMIT TABLE\*

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Test Temperature	Test Voltage Values (Volts)									
	V <sub>IH1</sub>	V <sub>IL1</sub>	V <sub>IH2</sub>	V <sub>IL2</sub>	PS1	PS2	VEE1	VEE2	VEEL	VEEL
T <sub>A</sub> = 25 °C	-0.780	-1.950	-1.11	-1.48	+1.11	+0.31	-5.46	-4.94	-2.94	-2.94
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Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
		+25 °C		+125 °C		-55 °C			Pinouts referenced are for DIL package, check Pin Assignments V <sub>CC</sub> = 2.0 V, Output Load = 100 Ω to GND							
		Subgroup 9	Subgroup 10	Subgroup 11	Subgroup 9	Subgroup 10	Subgroup 11		V <sub>IN</sub>	V <sub>OUT</sub>	PS1	PS2	V <sub>CC</sub>	VEEL	P.U.T.	
t <sub>TLH</sub>	Rise Time	0.7	2.1	0.7	2.3	0.7	2.3	ns	7, 13	4	11, 12	9, 10	1, 16	8	2, 3, 14, 15	
t <sub>FHL</sub>	Fall Time	0.7	2.1	0.7	2.3	0.7	2.3	ns	7, 13	4	11, 12	9, 10	1, 16	8	2, 3, 14, 15	
t <sub>pd</sub>	Propagation Delay															
	Clk to Q	0.7	3.2	0.7	3.5	0.7	3.5	ns	10	4	11, 12	9, 13	1, 16	8	2, 3, 14, 15	
	Clk to Carry Out	0.7	7.0	0.7	7.7	0.7	7.7	ns	10	4	11, 12	9, 13	1, 16	8	2, 3, 14, 15	
	Carry In to Carry Out	0.7	3.0	0.7	3.5	0.7	3.5	ns	10	4	11, 12	9, 13	1, 16	8	2, 3, 14, 15	
t <sub>SET</sub>	Setup Time															
	Data (D <sub>0</sub> to C)	2.0		2.0		2.0		ns	12, 13	14		7, 9	1, 16	8	2, 3, 14, 15	
	Select (S to C)	3.5		3.5		3.5		ns	12, 13	14		7, 9	1, 16	8	2, 3, 14, 15	
	Carry In (C <sub>IN</sub> to C)	2.0		2.0		2.0		ns	12, 13	14		7, 9	1, 16	8	2, 3, 14, 15	
	(C to C <sub>IN</sub> )	0.0		0.0		0.0		ns	12, 13	14		7, 9	1, 16	8	2, 3, 14, 15	
t <sub>HOLD</sub>	Hold Time															
	Data (D <sub>0</sub> to C)	0.0		0.0		0.0		ns	12, 13	14		7, 9	1, 16	8	2, 3, 14, 15	
	Select (S to C)	-0.5		-0.5		-0.5		ns	12, 13	14		7, 9	1, 16	8	2, 3, 14, 15	
	Carry In (C <sub>IN</sub> to C)	150		150		150		ns	12, 13	14		7, 9	1, 16	8	2, 3, 14, 15	
	(C to C <sub>IN</sub> )	2.0		2.2		2.2		ns	12, 13	14		7, 9	1, 16	8	2, 3, 14, 15	
f <sub>Count</sub>	Count Frequency	250		250		250		MHZ	12	13	9		1, 16	8	3, 14	