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AS1123

Constant-Current, 16-Channel LED Driver with Diagnostics

1 General Description

The AS1123 is designed to drive up to 16 LEDs through a fast serial interface and features 16 output constant current drivers and an on-chip diagnostic read-back function.

The high clock-frequency (up to 50MHz), adjustable output current, and flexible serial interface makes the device perfectly suited for high-volume transmission applications.

Output current is adjustable (up to 40mA/channel) using an external resistor (REXT).

The serial interface with Schmitt trigger inputs includes an integrated shift register. Additionally, an internal data register stores the currently displayed data.

The device features integrated diagnostics for over-temperature, open-LED, and shorted-LED conditions. Integrated registers store global fault status information during load as well as the detailed temperature/open-LED/shorted-LED diagnostics results.

The AS1123 also features a low-current diagnostic mode to minimize display flicker during fault testing.

The AS1123 is available in a 24-pin QSOP and a 24-pin TQFN (4x4mm) package.

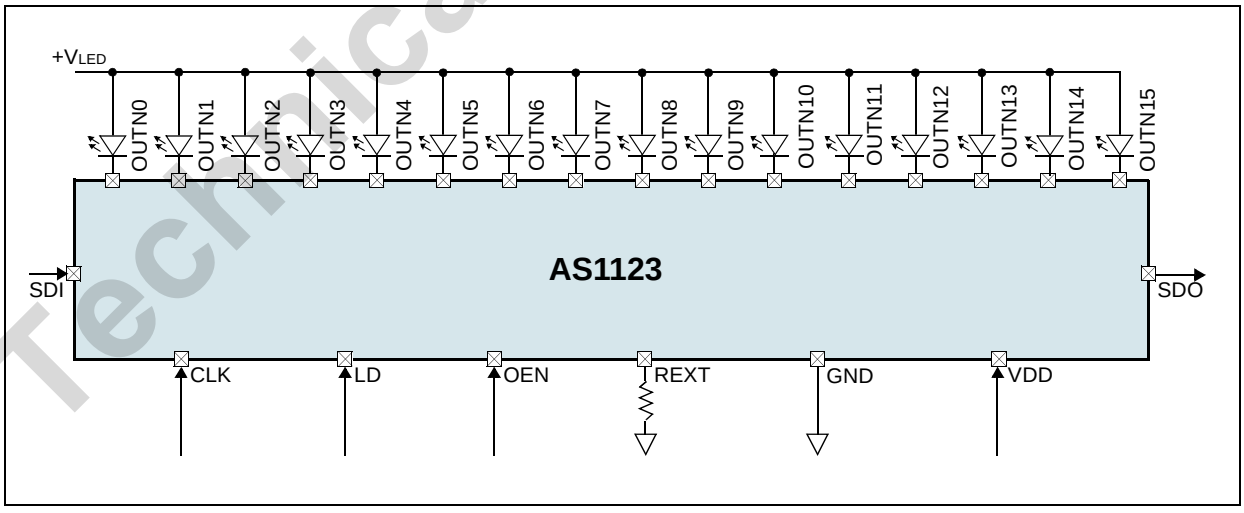
2 Key Features

- 16 Constant-Current Output Channels
- Excellent Output Current Accuracy
  - Between Channels: <±3%
  - Between Devices: <±3%
- Output Current Per Channel: 0.5mA to 40mA
- Over-Temperature, Open-LED, Shorted-LED Diagnostic Functions
- Low-Current Test Mode
- Global Fault Monitoring
- Fast Serial Interface: 50MHz
- Cascaded Configuration
- Extremely Fast Output Drivers Suitable for PWM
- Output Delay for controlling Inrush Current (on request)
- 24-pin QSOP and 24-pin TQFN (4x4mm) Package

3 Applications

The device is ideal for fixed- or slow-rolling displays using static or multiplexed LED matrix and dimming functions, large LED matrix displays, mixed LED display and switch monitoring, displays in elevators, public transports (underground, trains, buses, taxis, airplanes, etc.), large displays in stadiums and public areas, price indicators in retail stores, promotional panels, bar-graph displays, industrial controller displays, white good panels, emergency light indicators, and traffic signs.

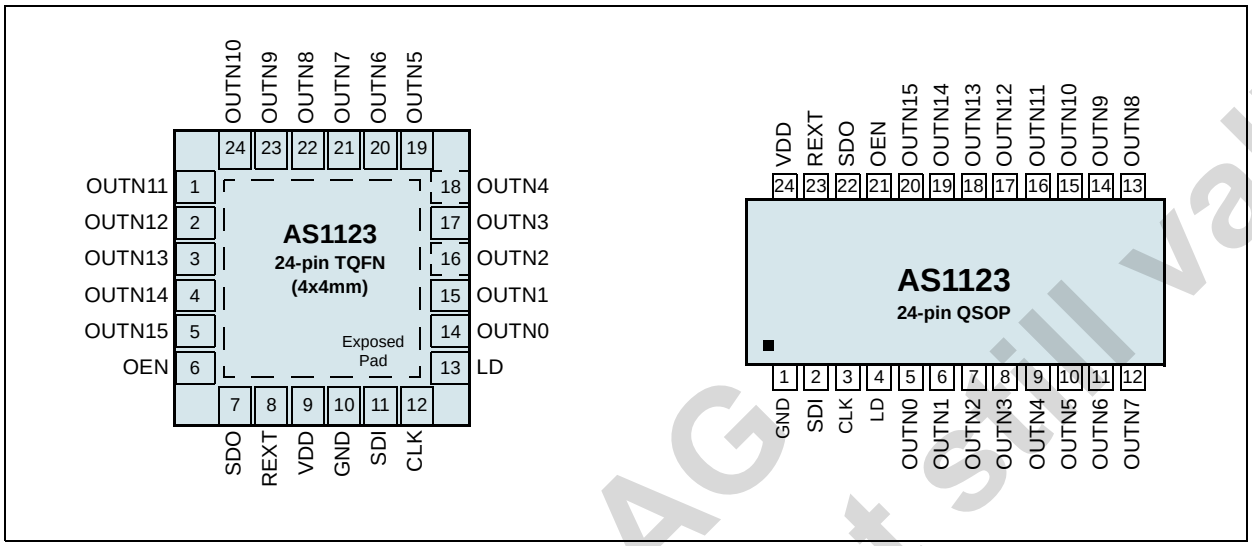
Figure 1. AS1123 - Typical Application Diagram



4 Pinout

Pin Assignments

Figure 2. Pin Assignments (Top View)



Pin Descriptions

Table 1. Pin Descriptions

Pin Number		Pin Name	Description
QSOP	TQFN		
1	10	GND	**Ground**
2	11	SDI	**Serial Data Input**
3	12	CLK	**Serial Data Clock**. The rising edge of the CLK signal is used to clock data into and out of the AS1123 shift register. In error mode, the rising edge of the CLK signal is used to switch error modes.
4	13	LD	**Serial Data Load.** Pull-down Resistor
5:20	1:5, 14:24	OUTN0:15	**Output Current Drivers**. These pins are used as LED drivers or for input sense for diagnostic modes. Data is transferred to the data register at the rising edge of these pins.
21	6	OEN	**Output Enable**. Pull-up Resistor. The active-low pin OEN signal can always enable output drivers to sink current independent of the AS1123 mode. 0 = Output drivers are enabled. 1 = Output drivers are disabled.
22	7	SDO	**Serial Data Output.** In normal mode SDO is latched out 8.5 clock cycles after SDI is latched in. In global error detection mode this pin indicates the occurrence of a global error. 0 = Global error mode returned an error. 1 = No errors.
23	8	REXT	**External Resistor Connection**. This pin connects through the external resistor (REXT) to GND, to setup the load current.
24	9	VDD	**Positive Supply Voltage**
-	Exposed Pad		**Exposed Pad.** This pin also functions as a heat sink. Solder it to a large pad or to the circuit-board ground plane to maximize power dissipation.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Section 6 Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
Electrical Parameters				
VDD to GND	0	7	V	
Input Voltage	-0.4	VDD+0.4	V	
Output Voltage	-0.4	7	V	
GND Pin Current		2000	mA	24-pin QSOP package
		2800	mA	24-pin TQFN (4x4mm) package
Input Current (latch-up immunity)	-100	+100	mA	Norm: JEDEC 78
Electrostatic Discharge				
Electrostatic Discharge HBM	+/- 1		kV	Norm: MIL 883 E method 3015
Temperature Ranges and Storage Conditions				
Thermal Resistance ΘJA		88	ºC/W	on PCB, 24-pin QSOP package
		23	ºC/W	on PCB, 24-pin TQFN (4x4mm) package
Junction Temperature		150	°C	
Storage Temperature	-55	150	ºC	
Package Body Temperature		+260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).
Humidity	5	85	%	Non-condensing
Moisture Sensitive Level	3			Represents a max. floor life time of 168h

6 Electrical Characteristics

VDD = +3.0V to +5.5V, Typical values are at TAMB = +25°(unless otherwise specified). All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Table 3. Electrical Characteristics

Symbol	Parameter		Condition	Min	Typ	Max	Unit
TAMB	Operating Ambient Temperature			-40		+85	°C
TJ	Operating Junction Temperature			-40		+125	°C
VDD	Supply Voltage			3.0		5.5	V
VDS	Output Voltage		OUTN0:15	0		5.5	V
IOUT	Output Current		OUTN0:15, *VDD = 5V*	0.5		40	mA
IOH			SDO	-1.0			
IOL			SDO	1.0			
VIH	Input Voltage	High Level	CLK, OEN, LD, SDI	0.7 x VDD		VDD + 0.3	V
VIL		Low Level		-0.3		0.3 x VDD	
IDS(OFF)	Output Leakage Current		OEN = 1, VDS = 5.5V			1.5	µA
VOL	Output Voltage	SDO	IOL = +1.0mA			0.4	V
VOH			IOH = -1.0mA	VDD - 0.4V			
IAV1	Device-to-Device Average Output Current from OUTN0 to OUTN15		VDS = 0.6V, VDD = Const., REXT = 470Ω	38.8		41.2	mA
ΔIAV1	Current Skew (Between Channels)		VDS ≥ 0.6V, VDD = Const., REXT = 470Ω		±1	±3	%
IAV2	Device-to-Device Average Output Current from OUTN0 to OUTN15		VDS = 0.5V, VDD > 3.3V, REXT = 1.87kΩ	9.6		10.4	mA
ΔIAV2	Current Skew (Between Channels)		VDS ≥ 0.5V, VDD = Const., REXT = 1.87kΩ		±1	±4	%
ILC	Low-Current Diagnosis Mode		VDS = 0.8V, VDD = 5.0V	0.4	0.6	0.8	mA
%/ΔVDS	Output Current vs. Output Voltage Regulation		VDS within 1.0 and 3.0V @ IOUT = 40mA		±0.7		%/V
%/ΔVDD	Output Current vs. Supply Voltage Regulation		VDD within 3.0 and 5.0V		±0.2		%/V
RIN(UP)	Pullup Resistance		OEN	250	500	800	kΩ
RIN(DOWN)	Pulldown Resistance		LD	250	500	800	kΩ
VTHL	Error Detection Threshold Voltage			0.25	0.3	0.45	V
VTHH	Error Detection Threshold Voltage (Level1 = default)		VDD = 3.0V		1.6		V
			VDD = 5.0V		2.7		
	Error Detection Threshold Voltage (Level2)		VDD = 3.0V		2.4		V
			VDD = 5.0V		4		
TOV1	Overtemperature Threshold Flag				150		ºC
IDD(OFF)	Supply Current		REXT = 470Ω, OUTN0:15 = Off		4	5.5	mA
			REXT = 1.87kΩ, OUTN0:15 = Off		2	3.5	
IDD(ON)			REXT = 470Ω, OUTN0:15 = On		15	18	
			REXT = 1.87kΩ, OUTN0:15 = On		5	7	

Switching Characteristics

V_{DD} = 3.0 to 5.5V, V_{DS} = 0.8V, V_{IH} = V_{DD}, V_{IL} = GND, R_{EXT} = 940Ω, V_{LOAD} = 4.0V, R_{LOAD} = 64Ω, C_{LOAD} = 10pF; The Switching Characteristics are guaranteed by design.

Table 4. Switching Characteristics for V_{DD} = 5V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{P1}	Propagation Delay Time (Without Staggered Output Delay)	CLK - SDO		5	10	ns
t_{P2}		LD - OUTN*n*		250	500	ns
t_{P3}		OEN - OUTN*n*		250	500	
t_{P4}	Propagation Delay Time				10	ns
$t_{W(CLK)}$	Pulse Width	CLK	15			ns
$t_{W(L)}$		LD	15			
$t_{W(OE)}$		OEN (@I_{OUT} < 40mA)	500			
t_R *	CLK Rise Time				500	ns
t_F *	CLK Fall Time				500	ns
t_{OR}	Output Rise Time of V_{OUT} (Turn Off)			tbd	500	ns
t_{OF}	Output Fall Time of V_{OUT} (Turn On)			tbd	500	ns
$t_{SU(D)}$	Setup Time for SDI		5			ns
$t_{H(D)}$	Hold Time for SDI		5			ns
$t_{SU(L)}$	Setup Time for LD		5			ns
$t_{H(L)}$	Hold Time for LD		5			ns
$t_{TESTING}$	OEN Time for Error Detection		2000			ns
t_{STAG}	Staggered Output Delay (only for AS1123B)			20	40	ns
$t_{SU(OE)}$	Output Enable Setup Time		20			ns
$t_{GSW(ERROR)}$	Global Error Switching Setup Time		10			ns
$t_{SU(ERROR)}$	Global Error Detection Setup Time		10			ns
$t_{P(I/O)}$	Propagation Delay Global Error Flag				5	ns
$t_{SW(ERROR)}$	Switching Time Global Error Flag				10	ns
f_{CLK}	Clock Frequency (Cascade Operation)				30	MHz
$t_{P3,ON}$	Low-Current Test Mode Propagation Delay Time	Turn ON		3	5	µs
$t_{P3,OFF}$		Turn OFF		0.05	0.1	µs
$t_{REXT2,1}$	External Resistor Reaction Time	Change from R_{EXT1} = 470Ω, I_{OUT1} = 40mA to R_{EXT2} = 4.7kΩ, I_{OUT2} = 4mA		0.5	1	µs
$t_{REXT2,1}$	External Resistor Reaction Time	Change from R_{EXT1} = 4.7kΩ, I_{OUT1} = 4mA to R_{EXT2} = 470Ω, I_{OUT2} = 40mA		0.5	1	µs

* If multiple AS1123 devices are cascaded and t_r or t_f is large, it may be critical to achieve the timing required for data transfer between two cascaded LED drivers.

7 Typical Operating Characteristics

VDD = +3.0V to +5.5V, TAMB = 25ºC (unless otherwise specified).

Figure 3. Output Current vs. Output Voltage

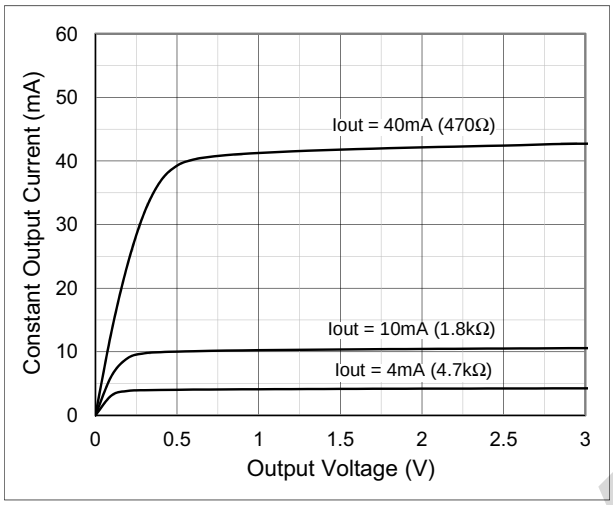


Figure 4. ICOC vs. Supply Voltage; REXT = 470Ω

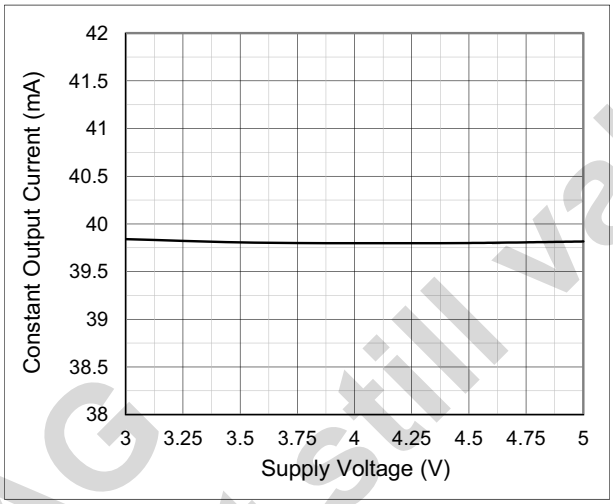


Figure 5. ICOC vs. Temperature; REXT = 470Ω

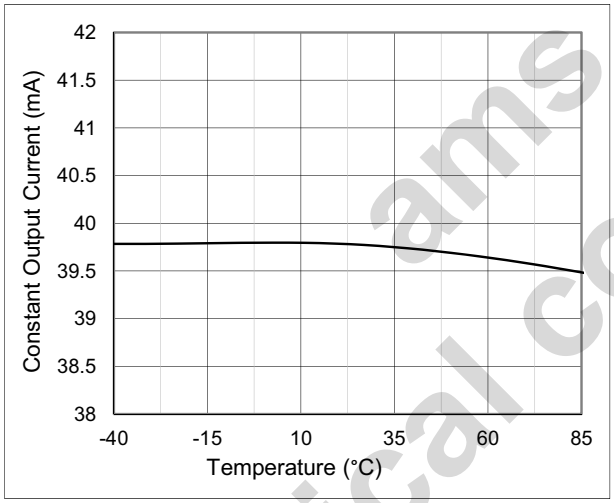


Figure 6. ICOC vs. Temperature; REXT = 1.8kΩ

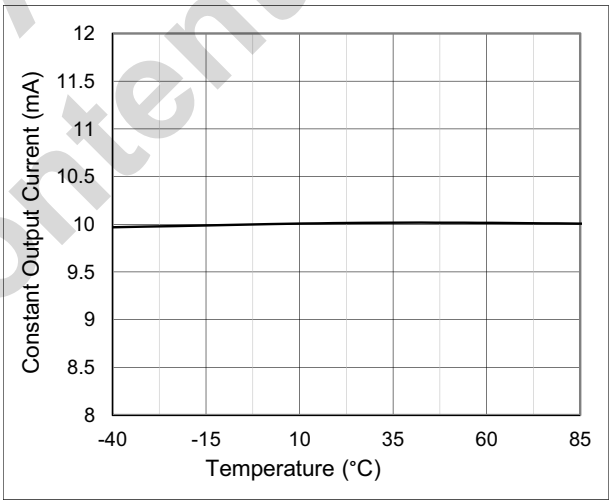
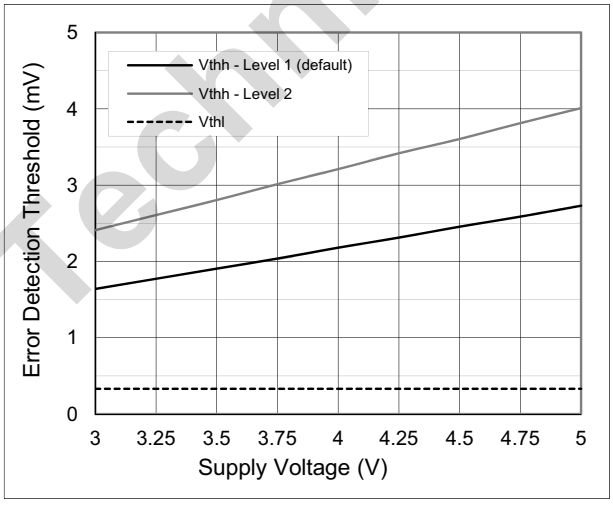


Figure 7. LED Error Detection Threshold vs. Supply Voltage



8 Detailed Description

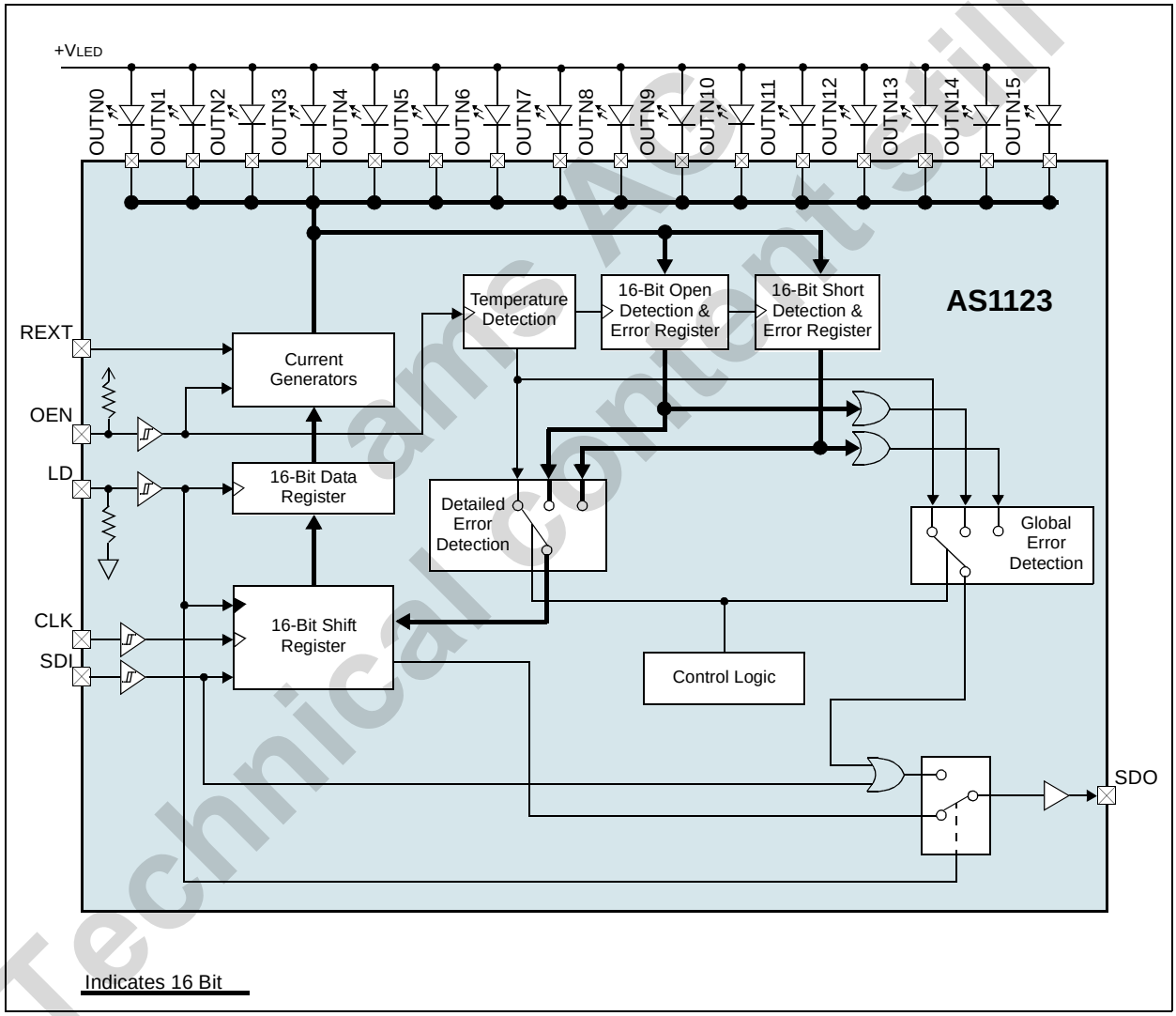
The AS1123 is designed to drive up to 16 LEDs through a fast serial interface and 16 constant-current output drivers. Furthermore, the AS1123 provides diagnostics for detecting open- or shorted-LEDs, as well as over-temperature conditions for LED display systems, especially LED traffic sign applications.

The AS1123 contains an 16-bit shift register and an 16-bit data register, which convert serial input data into parallel output format. At AS1123 output stages, sixteen regulated current sinks are designed to provide uniform and constant current with excellent matching between ports for driving LEDs within a wide range of forward voltage variations. External output current is adjustable from 0.5 to 40mA using an external resistor for flexibility in controlling the brightness intensity of LEDs. The AS1123 guarantees to endure 5.5V maximum at the outputs.

The serial interface is capable of operating at a minimum of 30 MHz, satisfying the requirements of high-volume data transmission.

Using a multiplexed input/output technique, the AS1123 adds additional functionality to pins SDO, LD and OEN. These pins provide highly useful functions (open- and shorted-LED detection, over-temperature detection), thus reducing pin count. Over-temperature detection will work on-the-run, whereas the open- and shorted-LED detection can be used on-the-run or in low-current diagnostic mode (see page 14).

Figure 8. AS1123 - Block Diagram



Serial Interface

Data accesses are made serially via pins SDI and SDO. At each CLK rising edge, the signal present at pin SDI is shifted into the first bit of the internal shift register and the other bits are shifted ahead of the first bit. The MSB is the first bit to be clocked in. In error-detection mode the shift register will latch-in the corresponding error data of temperature-, open-, and short-error register with each falling edge of LD.

The 16-bit data register will latch the data of the shift register at each rising edge of LD. This data is then used to drive the current generator output drivers to switch on the corresponding LEDs as OEN goes low.

Timing Diagrams

This section contains timing diagrams referenced in other sections of this data sheet.

Figure 9. Normal Mode Timing Diagram

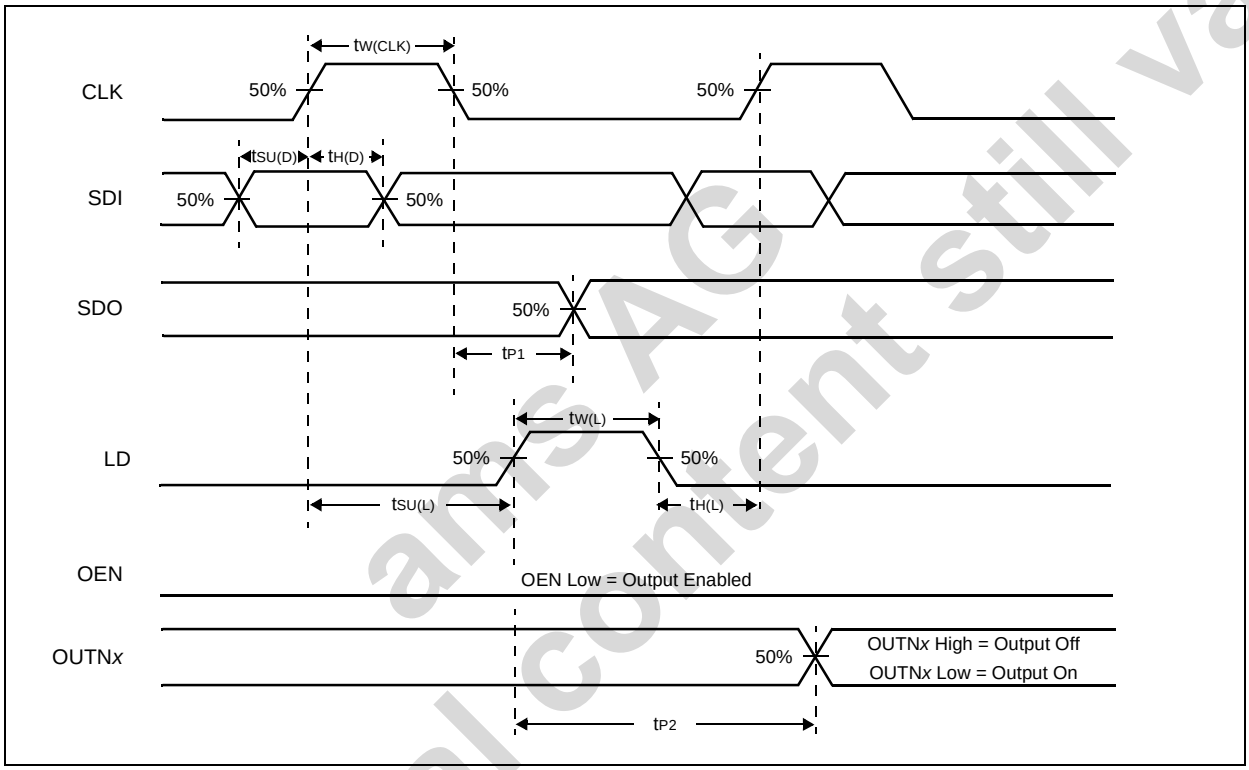


Figure 10. Output Delay Timing Diagram

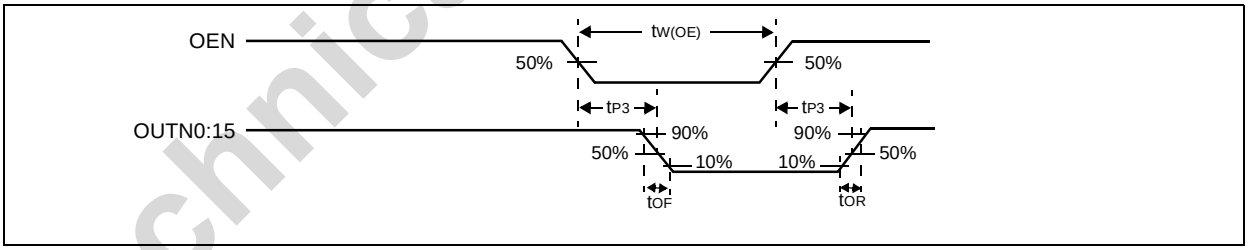


Figure 11. Data Input Timing Diagram

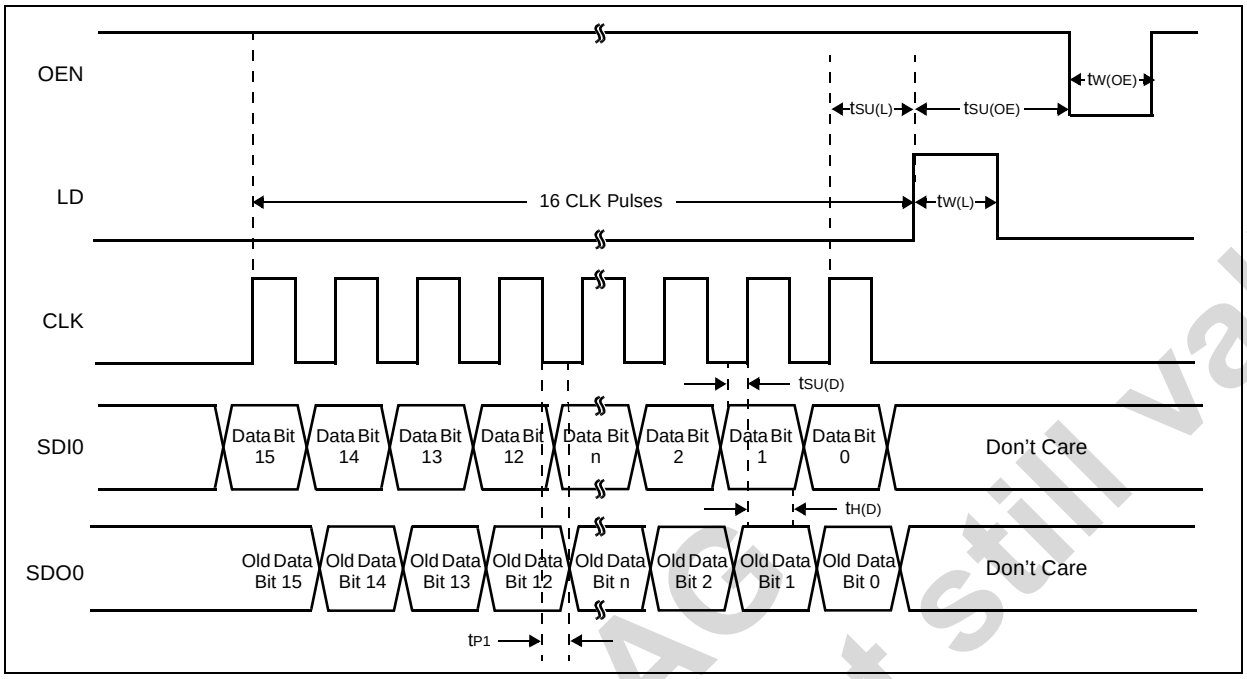


Figure 12. Data Input Example Timing Diagram

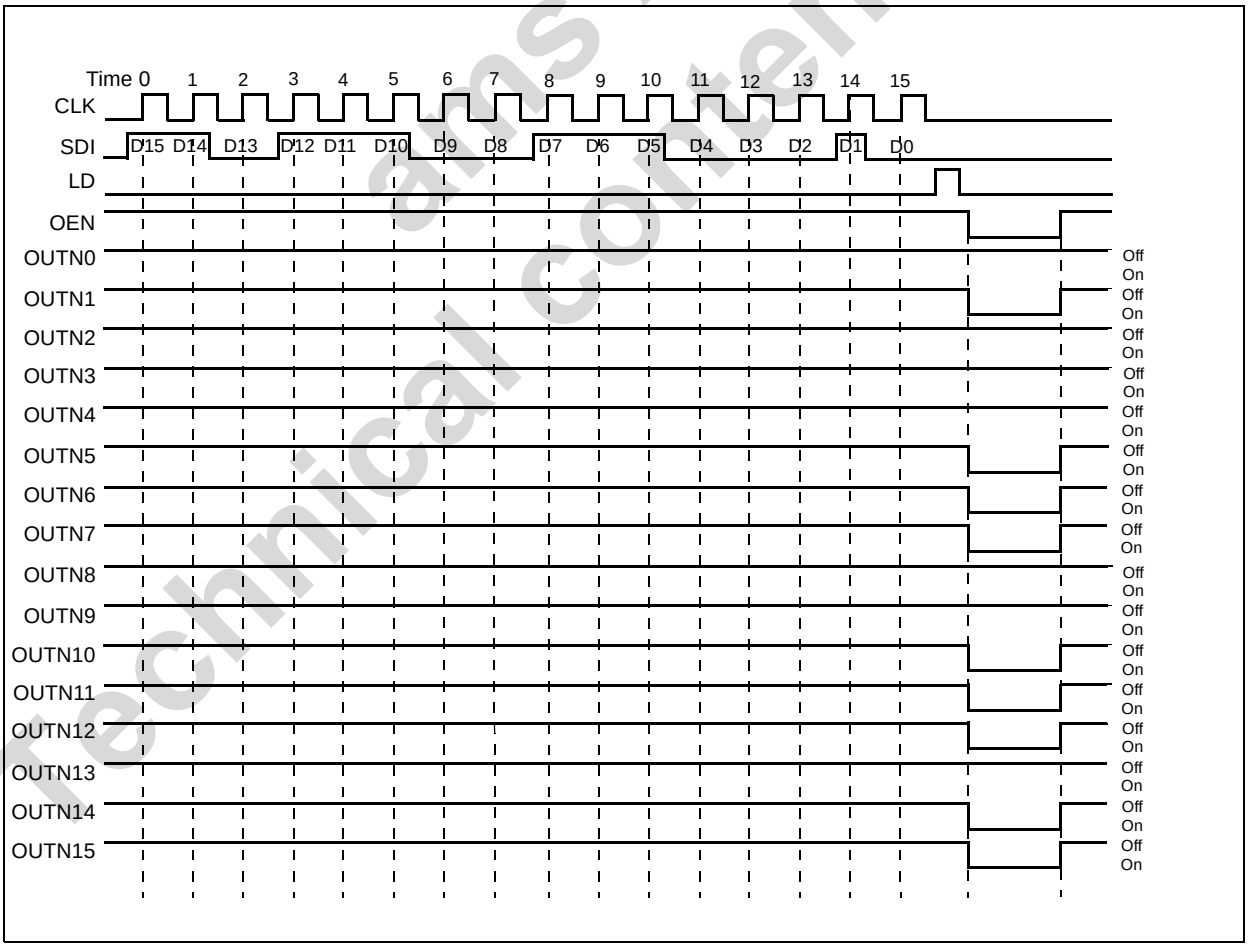
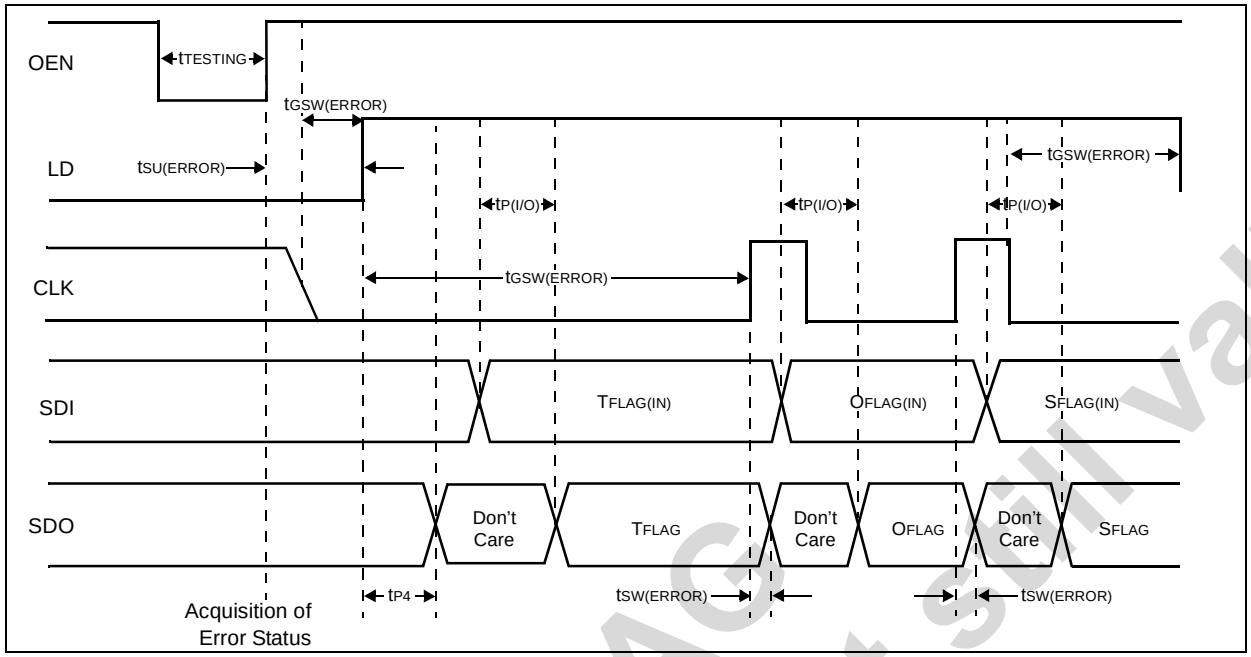


Figure 13. Switching Global Error Mode Timing Diagram



Error-Detection Mode

Acquisition of the error status occurs at the rising edge of OEN. Error-detection mode is started on the rising edge of LD when OEN is high. The CLK signal must be low when entering error detection mode. Error detection for open- and shorted-LEDs can only be performed for LEDs that are switched on during test time. To switch between error-detection modes clock pulses are needed (see Table 5).

Note: To test all LEDs, a test pattern that turns on all LEDs must be input to the AS1123.

Global Error Mode

Global error mode is entered when error-detection mode is started. Clock pulses during this period are used to select between temperature, open-LED, and shorted-LED tests, as well as low-current diagnostic mode and shutdown mode (see Table 5). In global error mode, an error flag (TFLAG, OFLAG, SFLAG) is delivered to pin SDO if any errors are encountered.

Table 5. Global Error Mode Selections

Clock Pulses	Output Port	Error-Detection Mode	Global Error Flag/Shutdown Condition
0	Don't Care	Over-Temperature Detection	TFLAG = SDO = 1: No over-temperature warning. TFLAG = SDO = 0: Over-temperature warning.
1	Enabled	Open-LED Detection	OFLAG = SDO = 1: No open-LED error. OFLAG = SDO = 0: Open-LED error.
2	Enabled	Shorted-LED Detection	SFLAG = SDO = 1: No shorted-LED error. SFLAG = SDO = 0: Shorted-LED error.
3	Don't Care	Low-Current Diagnostic Mode	
4	Don't Care	VTHH Level	SDI = 1: Level1, VTHH set to 54% VDD (default) SDI = 0: Level2, VTHH set to 80% VDD

Note: For a valid result SDI must be 1 for the first device.

If there are multiple AS1123s in a chain, the error flag will be gated through all devices. To get a valid result at the end of the chain, a logic 1 must be applied to the SDI input of the first device of the chain. If one device produces an error this error will show up after *n**tP(I/O) + tSW(ERROR) at pin SDO of the last device in the chain. This means it is not possible to identify which device in the chain produced the error. Therefore, if a global error occurs, the detailed error report can be run to identify which AS1123, or LED produced the error.

Note: When no error has occurred, the detailed error report can be skipped, setting LD and subsequently OEN low.

Error Detection Functions

Open-LED Detection

The AS1123 open-LED detection is based on the comparison between V_{DS} and V_{THL}. The open LED status is aquired at the rising edge of OEN and stored internally. While detecting open-LEDs the output port must be turned on. Open LED detection can be started with 1 clock pulse during error detection mode while the output port is turned on.

Note: LEDs which are turned off at test time cannot be tested and will be shown as a logic 1 in the detailed error report.

Table 6. Open LED Detection Modes

Output Port State	Effective Output Point Conditions	Detected Open-LED Error Status Code	Meaning
On	$V_{DS} < V_{THL}$	0	Open Circuit
On	$V_{DS} > V_{THL}$	1	Normal

Shorted-LED

The AS1123 shorted-LED detection is based on the comparison between V_{DS} and V_{THH}. The shortened LED status is acquired at the rising edge of OEN and stored internally. While detecting shorted-LEDs the output port must be turned on. Shorted-LED detection can be started with 2 clock pulses during error detection mode while the output port is turned on.

For valid results, the voltage at OUTN0:OUTN15 must be lower then V_{THH} under low-current diagnostic mode operating conditions. This can be achieved by reducing the V_{LED} voltage or by adding additional diodes, resistors or LED's.

Note: LEDs which are turned off at test time cannot be tested and will be shown as a logic 1 in the detailed error report.

Table 7. Shorted LED Detection Modes

Output Port State	Effective Output Point Conditions	Detected Shorted-LED Error Status Code	Meaning
On	$V_{DS} > V_{THH}$	0	Short Circuit
On	$V_{DS} < V_{THH}$	1	Normal

Overtemperature

Thermal protection for the AS1123 is provided by continuously monitoring the device's core temperature. The overtemperature status is acquired at the rising edge of OEN and stored internally.

Table 8. Overtemperature Modes

Output Port State	Effective Output Point Conditions	Detected Overtemperature Status Code	Meaning
Don't Care	Temperature > T_{OV1}	0	Overtemperature Condition
Don't Care	Temperature < T_{OV1}	1	Normal

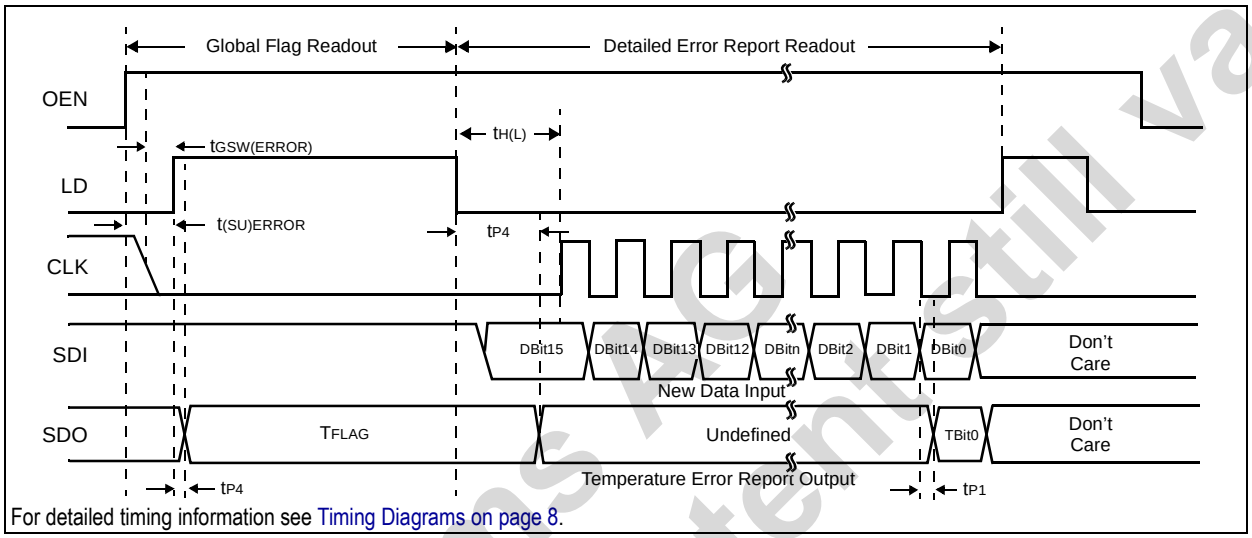
Detailed Error Reports

The detailed error report can be read out after global error mode has been run. At the falling edge of LD, the detailed error report of the selected test is latched into the shift register and can be clocked out with *n**16 clock cycles (*n* is the number of AS1123s in a chain) via pin SDO. At the same time new data can be written into the shift register, which is loaded on the next rising edge of pin LD. This pattern is shown at the output drivers, at the falling edge of OEN.

Detailed Temperature Warning Report

The detailed temperature warning report can be read out immediately after global error mode has been run. SDI must be 1 for the first device. Bit0 of the 16bit data word represents the temperature flag of the chip.

Figure 14. Detailed Temperature Warning Report Timing Diagram



For detailed timing information see Timing Diagrams on page 8.

Detailed Temperature Warning Report Example:

Consider a case where four AS1123s are cascaded in one chain. The detailed error report lists the temperatures for each device in the chain:

IC1:[70°] IC2:[85°] IC3:[170°] IC4:[60°]

In this case, IC3 is overheated and will generate a global error, and therefore 4*16 clock cycles are needed to write out the detailed temperature warning report, and optionally read in new data. The detailed temperature warning report would look like this:

XXXXXXXXXXXXXXX1 XXXXXXXXXXXXXXX1 XXXXXXXXXXXXXXX0 XXXXXXXXXXXXXXX1

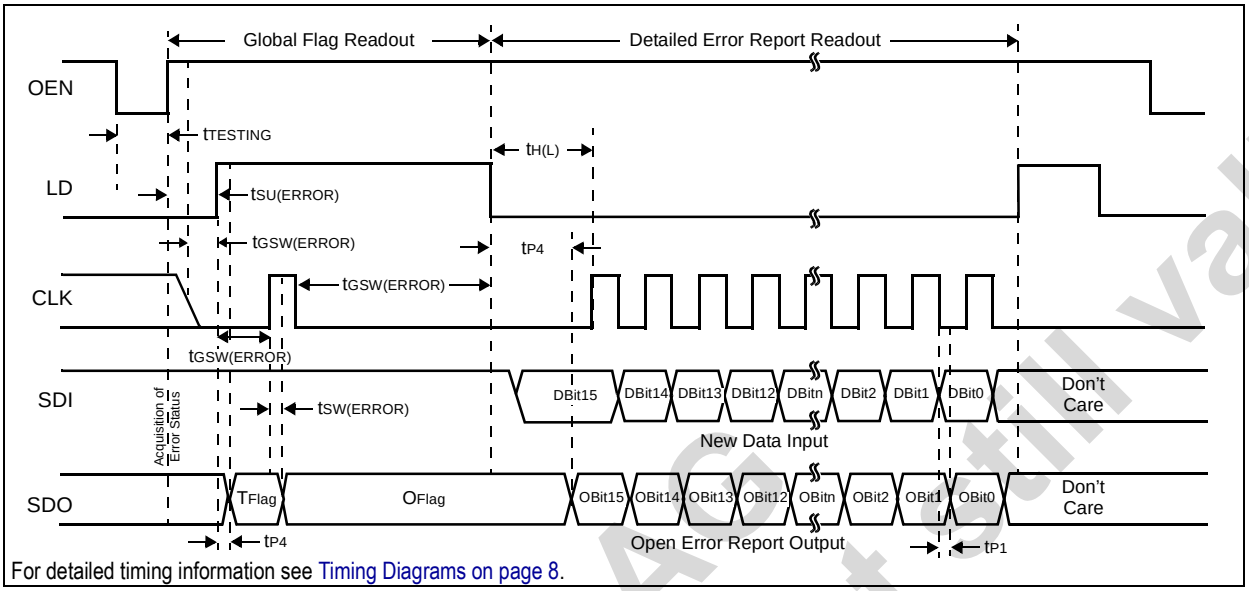
The 0 in the detailed temperature warning report indicates that IC3 is the device with the over-temperature condition.

Note: In an actual report there are no spaces in the output.

Detailed Open-LED Error Report

The detailed open-LED error report can be read out immediately after global error mode has been run. SDI must be 1 for the first device.

Figure 15. Detailed Open-LED Error Report Timing Diagram



For detailed timing information see Timing Diagrams on page 8.

Detailed Open-LED Error Report Example:

Consider a case where three AS1123s are cascaded in one chain. A 1 indicates a LED is on, a 0 indicates a LED is off, and an X indicates an open LED. The open-LED test is only applied to LEDs that are turned on. This test is used with a test pattern where all LEDs are on at test time.

IC1:[1111111111111111] IC2:[111XX11111111X11] IC3:[1111111111111111]

IC2 has three open LEDs switched on due to input. 3*16 clock cycles are needed to write the entire error code out. The detailed error report would look like this:

Input Data:	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
LED Status:	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 X X 1 1 1 1 1 1 1 1 X 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Failure Code:	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 0 0 1 1 1 1 1 1 1 1 0 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

Comparing this report with the input data indicates that IC2 is the device with two open LEDs at position 4 and 5 and one open LED at position 14. For such a test it is recommended to enter low-current diagnostic mode first (see Low-Current Diagnostic Mode on page 14) to reduce screen flickering.

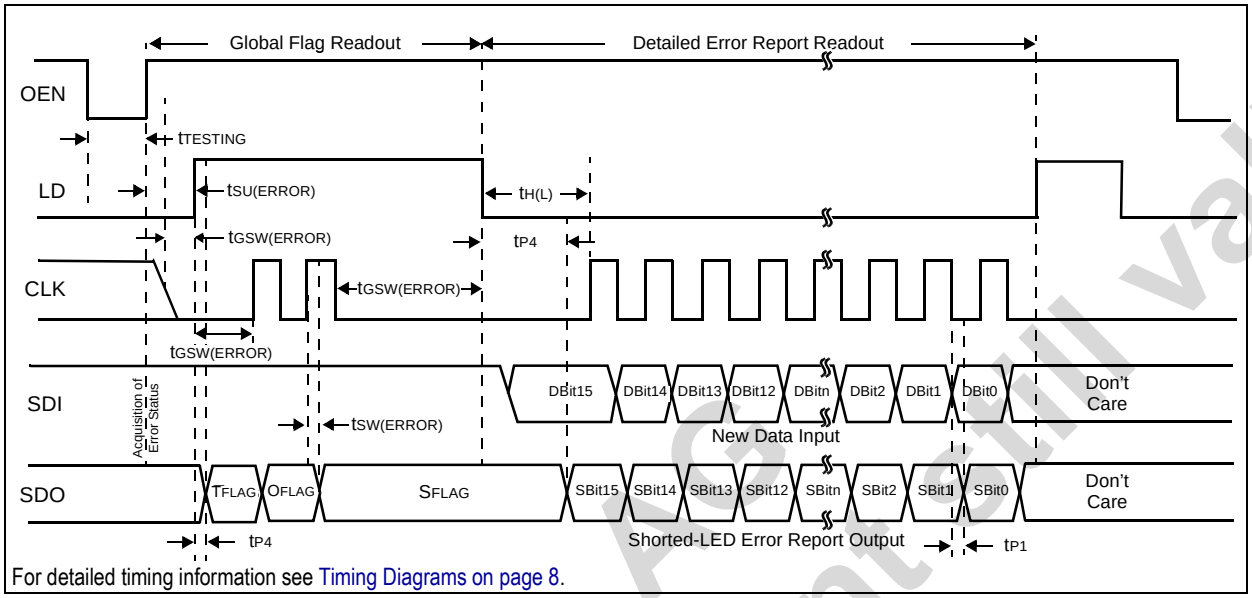
This test can be used also on-the-fly without using an all 1s test pattern (see Figure 19 on page 16).

Note: In an actual report there are no spaces in the output. LEDs turned off during test time cannot be tested and will show a logic 1 in the detailed error report.

Detailed Shorted-LED Error Report

The detailed shorted-LED error report can be read out immediately after global error mode has been run (see Global Error Mode on page 10). SDI must be 1 for the first device.

Figure 16. Detailed Shorted-LED Error Report Timing Diagram



Detailed Shorted-LED Error Report Example

Consider a case where three AS1123s are cascaded in one chain. A 1 indicates a LED is on, a 0 indicates a LED is off, and an X indicates a shorted LED. This test is used on-the-fly.

IC1:[11111XX111111111] IC2:[1111111111111111] IC3:[X100011111111111]

IC1 has two shorted LEDs which are switched on, IC3 has one shorted LED switched off due to input. 3*16 clock cycles are needed to write the entire error code out. The detailed error report would look like this:

Input Data:	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0 1 0 0 0 1 1 1 1 1 1 1 1 1 1 1
LED Status:	1 1 1 1 1 X X 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	X 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Failure Code:	1 1 1 1 1 0 0 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

Showing IC1 as the device with two shorted LEDs at position 6 and 7, and IC3 with one shorted LED at position 1. The shorted LED at position 1 of IC3 cannot be detected, since LEDs turned off at test time are not tested and will show a logic "1" at the detailed error report. To test all LEDs this test should be run with an all 1s test pattern. For a test with an all on test pattern, low-current diagnostic mode should be entered first to reduce on-screen flickering.

Note: In an actual report there are no spaces in the output. LEDs turned off during test time cannot be tested and will show a logic 1 in the detailed error report.

Low-Current Diagnostic Mode

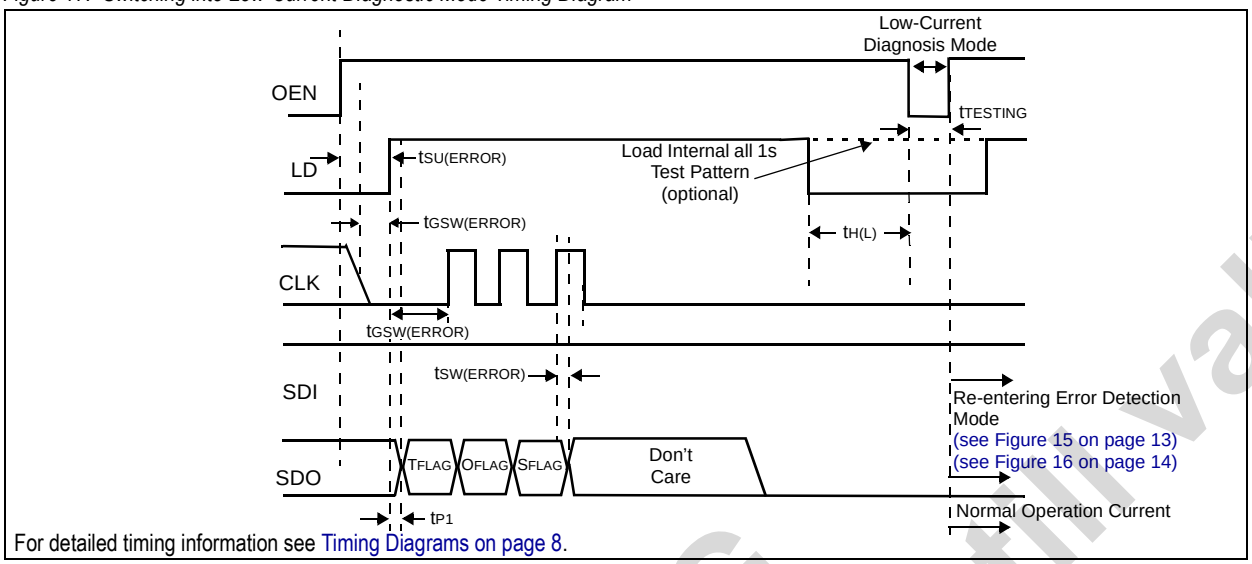
To run the open- or shorted-LED test, a test pattern must be used that will turn on each LED to be tested. This test pattern will cause a short flicker on the screen while the test is being performed. The low-current diagnostic mode can be initiated prior to running a detailed error report to reduce this on-screen flickering.

Note: Normally, displays using such a diagnostic mode require additional cables, resistors, and other components to reduce the current. The AS1123 has this current-reduction capability built-in, thereby minimizing the number of external components required.

Low-current diagnostic mode can be initiated via 3 clock pulses during error-detection mode. After the falling edge of LD, a test pattern displaying all 1s can be written to the shift register which will be used for the next error-detection test.

On the next falling edge of OEN, current is reduced to I_{LC}. With the next rising edge of OEN the current will immediately increase to normal levels and the detailed error report can be read out entering error-detection mode.

Figure 17. Switching into Low-Current Diagnostic Mode Timing Diagram

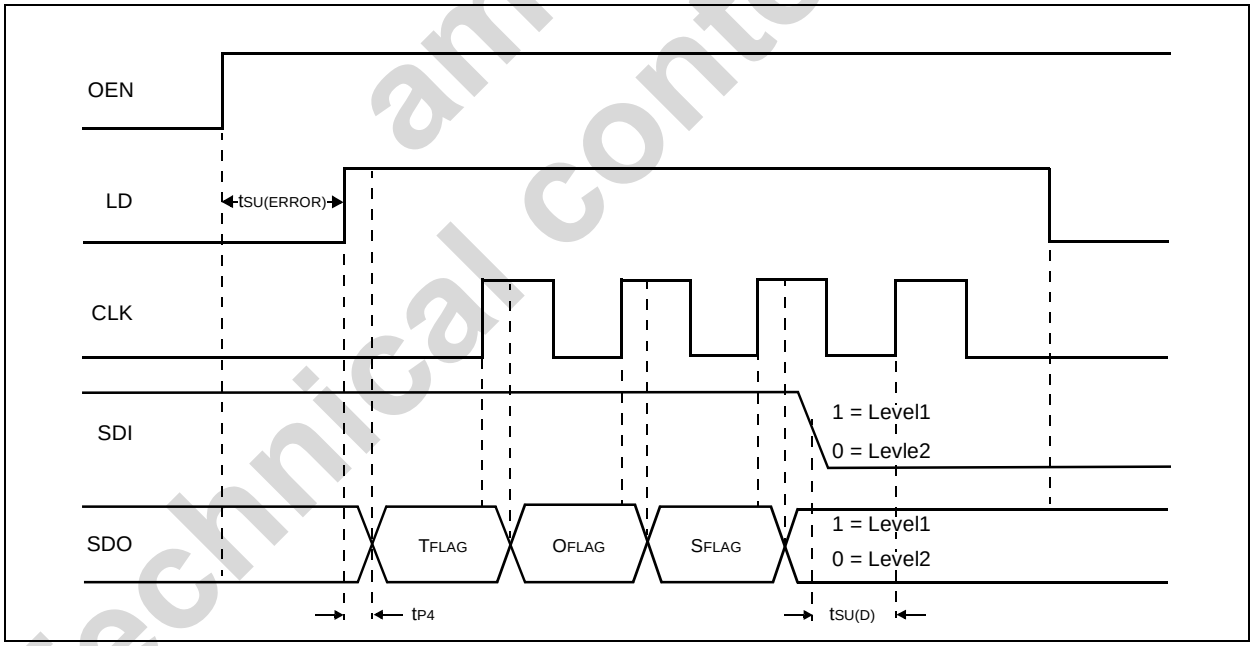


V_{THH} Level

Two different threshold levels of the error detection can be set via a bit. The bit can be entered via 4 clock pulses during error-detection mode. To set level 2 (V_{THH} is 80% of Vdd) a 0 must be placed at SDI after the rising edge of the 3rd clock pulse.

To set level 1 (V_{THH} is 54% of Vdd) a 1 must be placed at SDI after the 3rd clock pulse. The level 1/level 2 information will be latched through if multiple AS1123 devices are in a chain. At the rising edge of the 4th clock pulse the bit will be read out and the AS1123 is set to Level1 or Level2.

Figure 18. V_{THH} Level Timing Diagram



9 Application Information

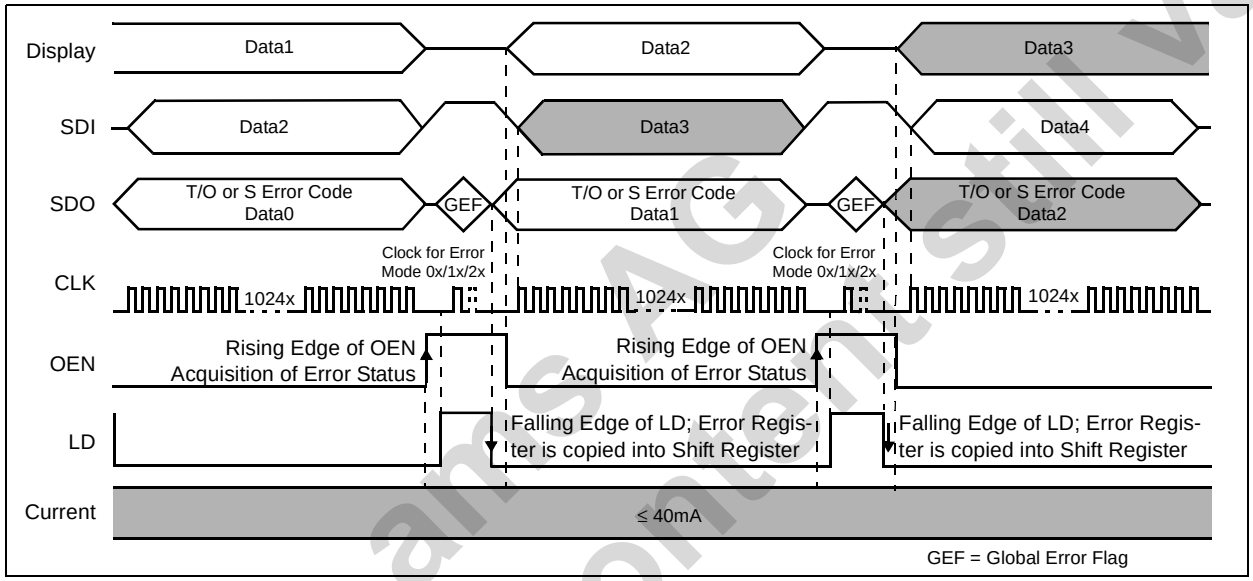
Error Detection

The AS1123 features two types of error detection. The error detection can be used on-the-fly, for active LEDs, without any delay, or by entering into low-current diagnosis mode.

Error Detection On-The-Fly

Error detection on-the-fly will output the status of active LEDs during operation. Without choosing an error mode this will output the temperature flag at every input/output cycle. Triggering one clock pulse for open or two clock pulses for short detection during error detection mode outputs the detailed open- or short-error report with the next input/output cycle (see Figure 19). LEDs turned off at test time are not tested and will show a logic "1" at the detailed error report.

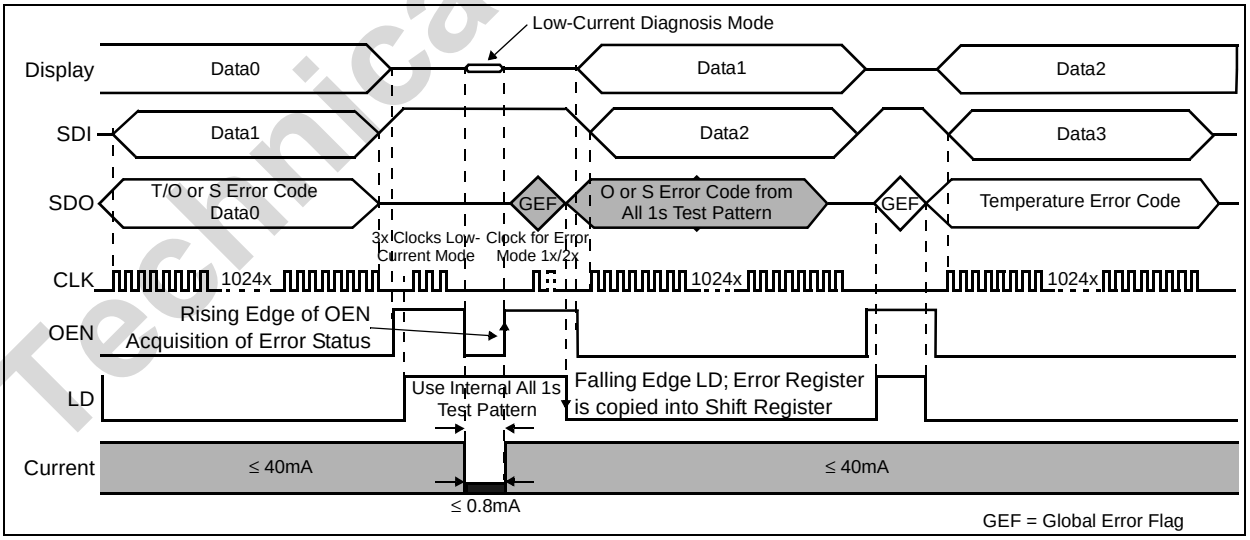
Figure 19. Normal Operation with Error Detection During Operation – 64 Cascaded AS1123s



Error Detection with Low-Current Diagnosis Mode

This unique feature of the AS1123 uses an internal all 1s test pattern for a flicker free diagnosis of all LEDs. This error detection mode can be started at the end of each input cycle (see Figure 20).

Figure 20. Low-Current Diagnosis Mode with Internal All 1s Test Pattern – 64 Cascaded AS1123s



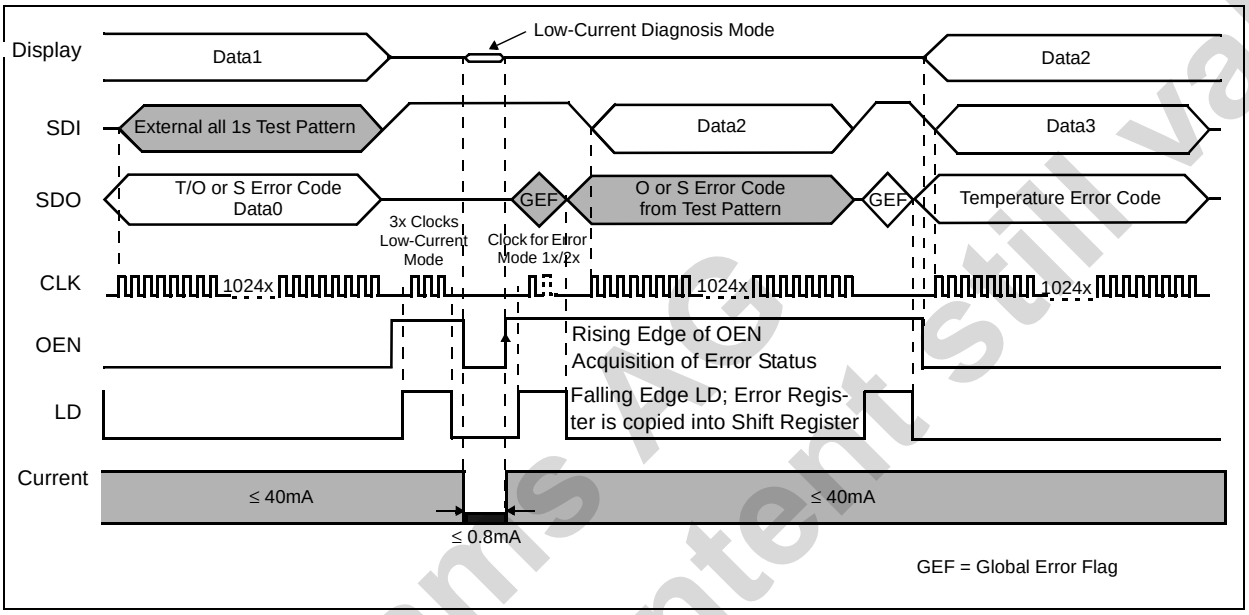
The last pattern written into the shift register will be saved before starting low-current diagnosis mode and can be displayed immediately after the test has been performed.

Low-current diagnostic mode is started with 3 clock pulses during error detection mode. Then OEN should be enabled for ≥2µs for testing. With the rising edge of OEN the LED test is stopped, and while LD is high the desired error mode can be selected with the corresponding clock pulses. After LD and OEN go low again the previously saved pattern can be displayed at the outputs.

With the next data input the detailed error code will be clocked out at pin SDO.

Note: See Figure 21 for use of an external test pattern.

Figure 21. Low-Current Diagnosis Mode with External Test Pattern – 64 Cascaded AS1123s

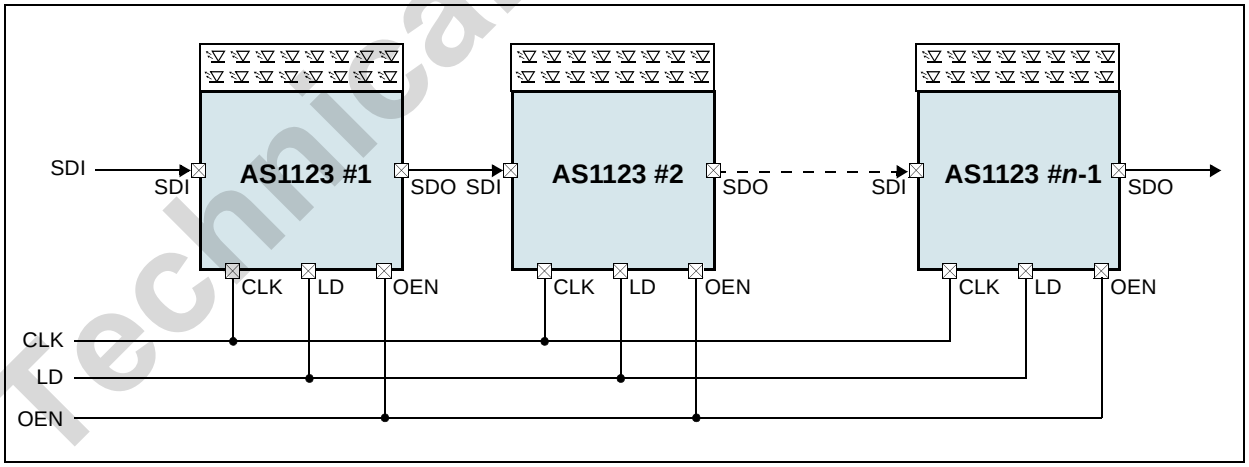


Cascading Devices

To cascade multiple AS1123 devices, pin SDO must be connected to pin SDI of the next AS1123 (see Figure 22). At each rising edge of CLK the LSB of the shift register will be written into the shift register SDI of the next AS1123 in the chain.

Note: When *n**AS1123 devices are in one chain, *n**16 clock pulses are needed to latch-in the input data.

Figure 22. Cascading AS1123 Devices



Constant Current

In LED display applications, the AS1123 provides virtually no current variations from channel-to-channel and from AS1123-to-AS1123. This is mostly due to 2 factors:

- While I_{OUT} ³ 10mA, the maximum current skew is less than ±3% between channels and less than ±3% between AS1123 devices.
- In the saturation region, the characteristic curve of the output stage is flat. Thus, the output current can be kept constant regardless of the variations of LED forward voltages (V_F).

Adjusting Output Current

The AS1123 scales up the reference current (I_{REF}) set by external resistor (R_{EXT}) to sink a current (I_{OUT}) at each output port. As shown the output current in the saturation region is extremely flat so that it is possible to define it as target current ($I_{OUT\ TARGET}$). $I_{OUT\ TARGET}$ can be calculated by:

$$V_{REXT} = 1.253V \quad (EQ\ 1)$$

$$I_{REF} = V_{REXT}/R_{EXT}\ (\text{if the other end of } R_{EXT} \text{ is connected to ground}) \quad (EQ\ 2)$$

$$I_{OUT\ TARGET} = I_{REF}*15 = (1.253V/R_{EXT})*15 \quad (EQ\ 3)$$

Where:

R_{EXT} is the resistance of the external resistor connected to pin REXT.
V_{REXT} is the voltage on pin REXT.

The magnitude of current (as a function of R_{EXT}) is around 40mA at 470Ω and 20mA at 940Ω.

Package Power Dissipation

The maximum allowable package power dissipation (PD) is determined as:

$$P_{D(MAX)} = (T_J - T_{AMB})/R_{TH(J-A)} \quad (EQ\ 4)$$

When 16 output channels are turned on simultaneously, the actual package power dissipation is:

$$P_{D(ACT)} = (I_{DD}*V_{DD}) + (I_{OUT}*Duty*V_{DS}*16) \quad (EQ\ 5)$$

Therefore, to keep $P_{D(ACT)} \leq P_{D(MAX)}$, the maximum allowed output current as a function of duty cycle is:

$$I_{OUT} = \{[(T_J - T_{AMB})/R_{TH(J-A)}] - (I_{DD}*V_{DD})\}/V_{DS}/Duty/16 \quad (EQ\ 6)$$

Where:

T_J = -40°C to +125°C

Delayed Outputs (only for AS1123B)

The AS1123B has graduated delay circuits between outputs. These delay circuits can be found between OUTN*n* and the constant current block.

The fixed delay time is 20 ns (typ) where OUTN0:3 has no delay, OUTN4:7 has 20ns delay, OUTN8:11 has 40ns delay and OUTN12:15 has 60ns delay. This delay prevents large inrush currents, which reduce power supply bypass capacitor requirements when the outputs turn on.

Switching-Noise Reduction

LED drivers are frequently used in switch-mode applications which normally exhibit switching noise due to parasitic inductance on the PCB.

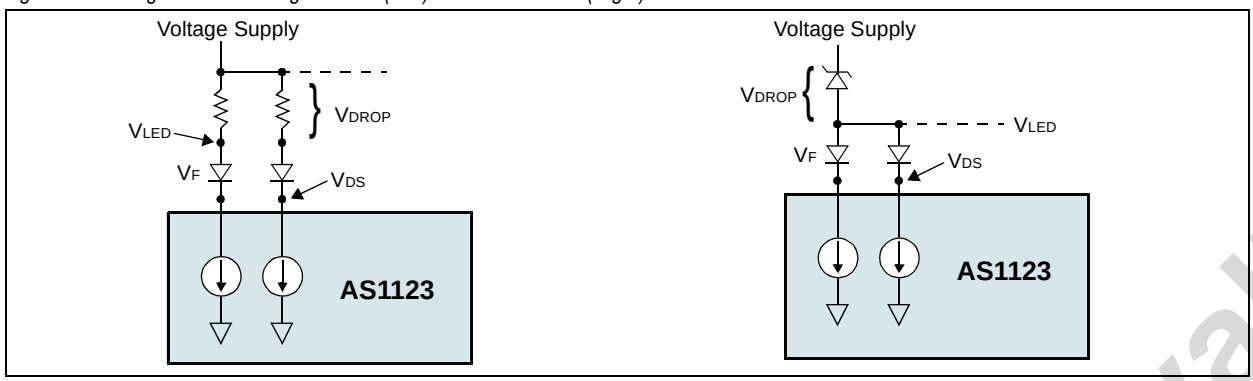
Load Supply Voltage

Considering the package power dissipation limits, the AS1123 should be operated within the range of V_{DS} = 0.4 to 1.0V.

For example, if V_{LED} is higher than 5V, V_{DS} may be so high that $P_{D(ACT)} > P_{D(MAX)}$ where $V_{DS} = V_{LED} - V_F$. In this case, the lowest possible supply voltage or a voltage reducer (V_{DROP}) should be used. The voltage reducer allows
$V_{DS} = (V_{LED} - V_F) - V_{DROP}$.

Note: Resistors or zener diodes can be used as a voltage reducer as shown in Figure 23 on page 19.

Figure 23. Voltage Reducer using Resistor (Left) and Zener Diode (Right)



10 Package Drawings and Markings

Figure 24. 24-pin QSOP Marking

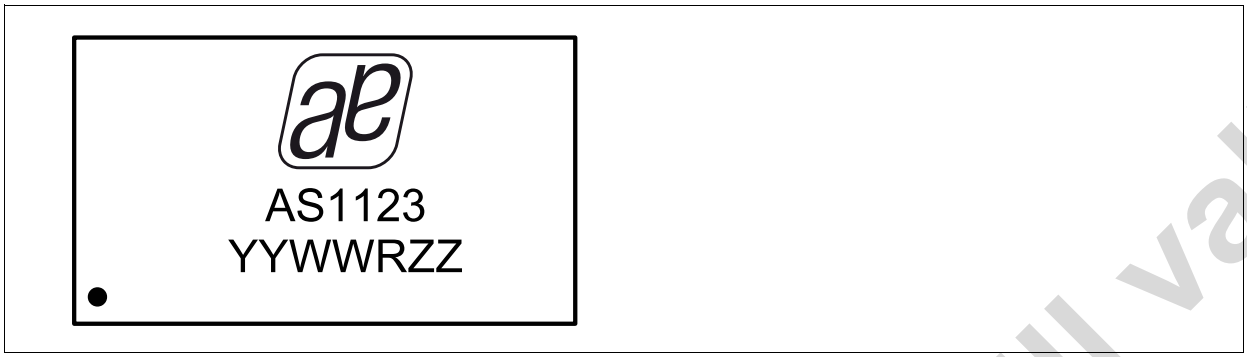


Figure 25. 24-pin TQFN (4x4mm) Marking

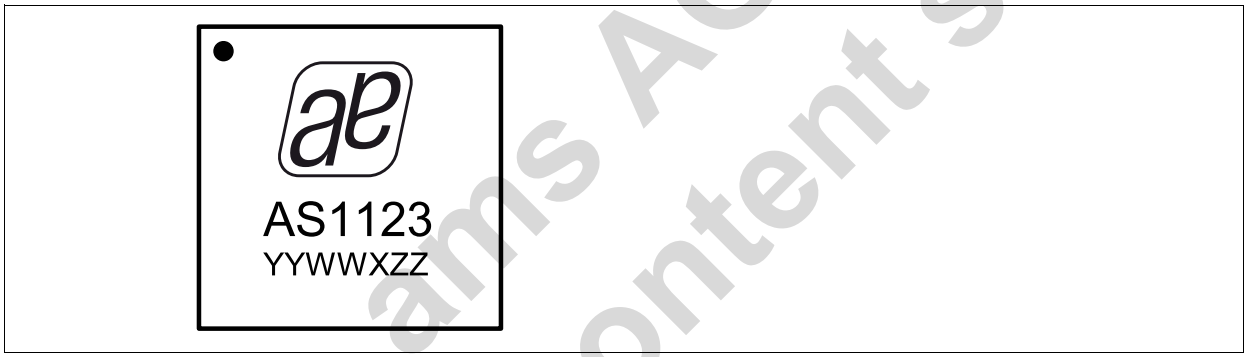
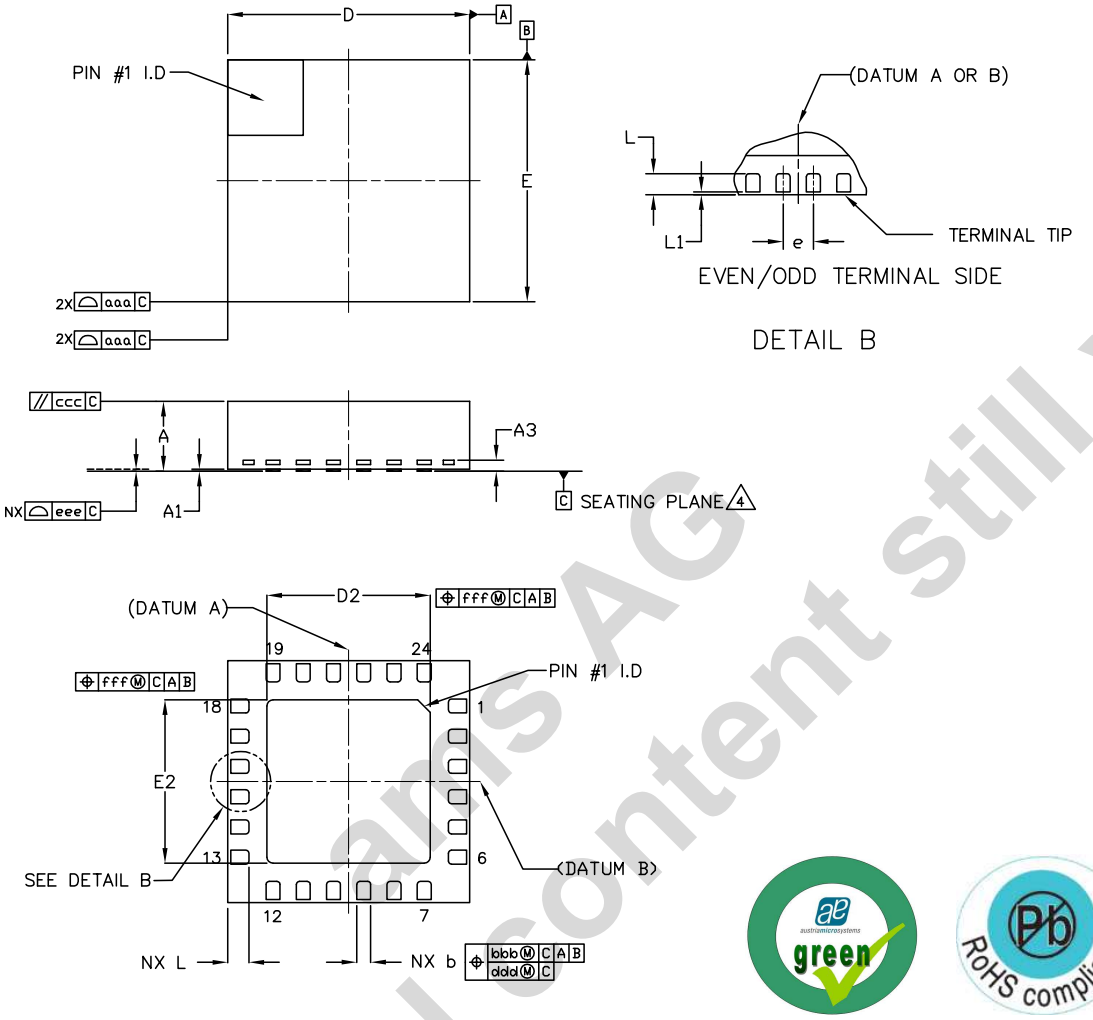


Table 9. Packaging Code YYWWRZZ or YYWWXZZ

YY	WW	R / X	ZZ
last two digits of the current year	manufacturing week	plant identifier	free choice / traceability code

Figure 26. 24-pin TQFN (4x4mm) Package



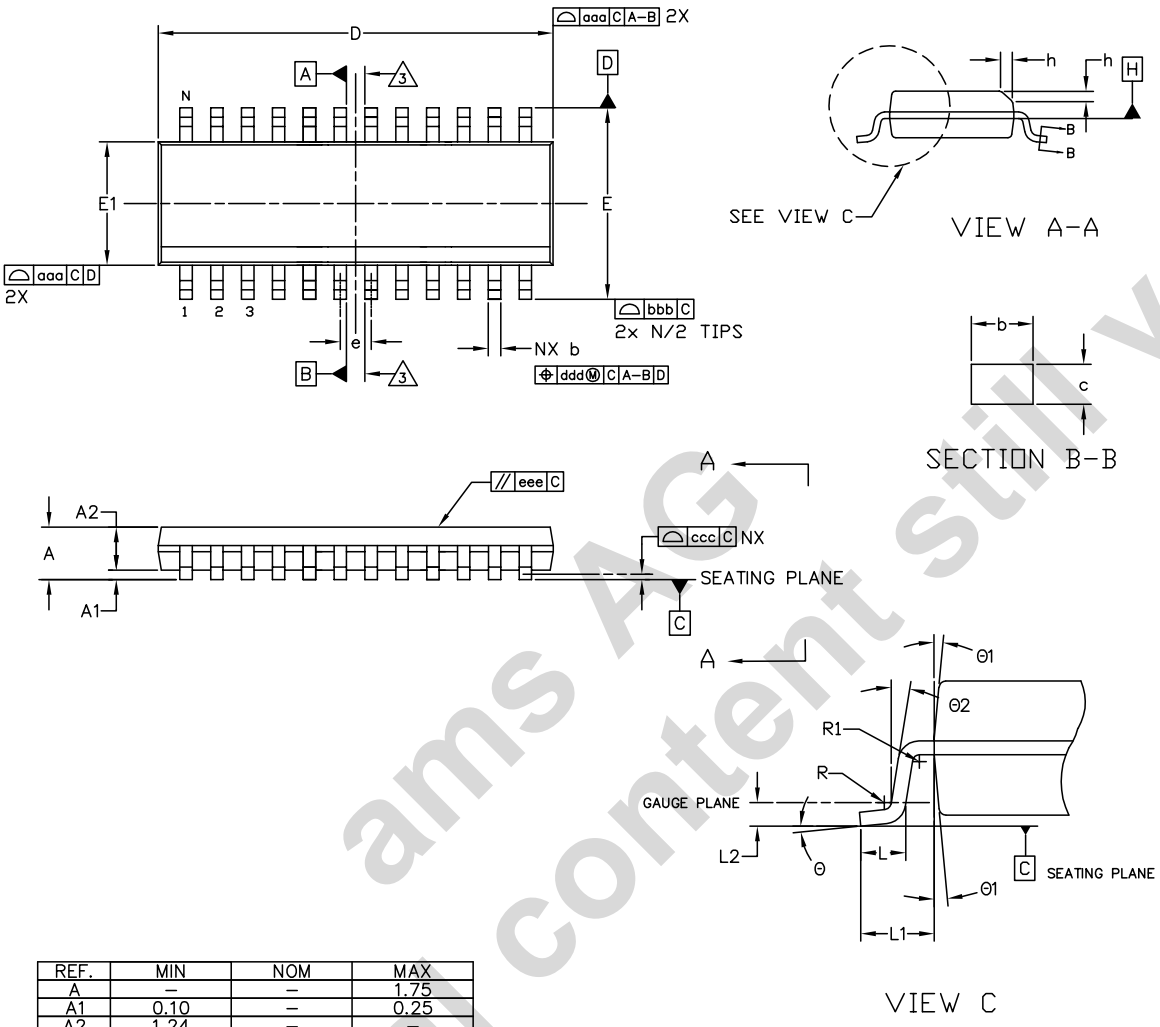
REF.	MIN	NOM	MAX
A	0.50	0.55	0.65
A1	0	0.02	0.05
A3	–	–	0.22
L	0.30	0.35	0.40
L1	0	–	0.15
b	0.18	0.25	0.35
D		4.00 BSC	
E		4.00 BSC	
e		0.50 BSC	
D2	2.70	2.80	2.90
E2	2.70	2.80	2.90
aaa	–	0.15	–
bbb	–	0.10	–
ccc	–	0.10	–
ddd	–	0.05	–
eee	–	0.08	–
fff	–	0.10	–
N		24	

NOTE:

1. DIMENSIONS & TOLERANCEING CONFIRM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGELS ARE IN DEGREES.
3. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP. DIMENSION L1 REPRESENTS TERMINAL FULL BACK FROM PACKAGE EDGE UP TO 0.15mm IS ACCEPTABLE.
4. COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.
5. RADIUS ON TERMINAL IS OPTIONAL.
6. N IS THE TOTAL NUMBER OF TERMINALS.

austriamicrosystems a leap ahead in analog			ASSEMBLY ENGINEERING	
			TITLE: SAWN TQFN, PULL BACK, 4x4x0.55mm, 24 LEAD, 2.80mm SQ. ePAD	REFERENCE DOCUMENT: JEDEC Mo – 248 LATEST REVISION
DRAWN: RH8	DATE: 2010.10.22	REV.: N/C		
CHECKED: GBO	DATE: 2010.10.22		DRAWING NO.: QAU	UNIT
APPROVED: MKR	DATE: 2010.10.22	SHEET: 1 OF 1	DIMENSION AND TOLERANCE	SCALE: NOT IN SCALE

Figure 27. 24-pin QSOP Package



REF.	MIN	NOM	MAX
A	–	–	1.75
A1	0.10	–	0.25
A2	1.24	–	–
b	0.20	–	0.30
c	0.15	–	0.25
D		8.66 BSC	
E		6.00 BSC	
E1		3.91 BSC	
e		0.635 BSC	
L	0.41	–	1.27
L1		1.04 REF	
L2		0.25 BSC	
R	0.08	–	–
R1	0.08	–	–
h	0.25	–	0.51
Θ	0°	–	8°
Θ1	5°	–	15°
Θ2	0°	–	–
aaa	–	0.10	–
bbb	–	0.20	–
ccc	–	0.10	–
ddd	–	0.18	–
eee	–	0.10	–
fff	–	0.15	–
N		24	

NOTE:

1. DIMENSIONS & TOLERANCEING CONFIRM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGELS ARE IN DEGREES.

3 DATUMS A & B TO BE DETERMINED AT DATUM H.

austriamicrosystems a leap ahead in analog		ASSEMBLY ENGINEERING	
		TITLE: QSOP 150MIL, 24 LEAD	REFERENCE DOCUMENT: JEDEC MO – 137 LATEST REVISION
DRAWN: RH8	DATE: 2011.03.01	REV.: N/C	
CHECKED: GBO	DATE: 2011.03.01	DRAWING NO.: QES	UNIT
APPROVED: MKR	DATE: 2011.03.01	SHEET: 1 OF 1	DIMENSION AND TOLERANCE / SCALE: NOT IN SCALE

11 Ordering Information

The device is available as the standard products shown in Table 10.

Table 10. Ordering Information

Ordering Code	Marking	Description	Delivery Form	Package
AS1123-BQFT	AS1123	Constant-Current, 16-Channel LED Driver with Diagnostics	Tape and Reel	24-pin TQFN (4x4mm)
AS1123-BTST	AS1123	Constant-Current, 16-Channel LED Driver with Diagnostics	Tape and Reel	24-pin QSOP
AS1123B*	AS1123B	Constant-Current, 16-Channel LED Driver with Diagnostics with controlled inrush Current	Tape and Reel	tbd

*) on request

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or find your local distributor at http://www.austriamicrosystems.com/distributor

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