GENERAL DESCRIPTION

The Akros Silicon AS1228 Single Chip Controller provides DC-DC Power Conversion for isolated and non-isolated power conversion applications over a wide input voltage range of 8.5-28 VDC. The current-mode controller architecture provides fast loop response, high efficiency, and low no-load power configurable for flyback, forward or buck topology power designs.

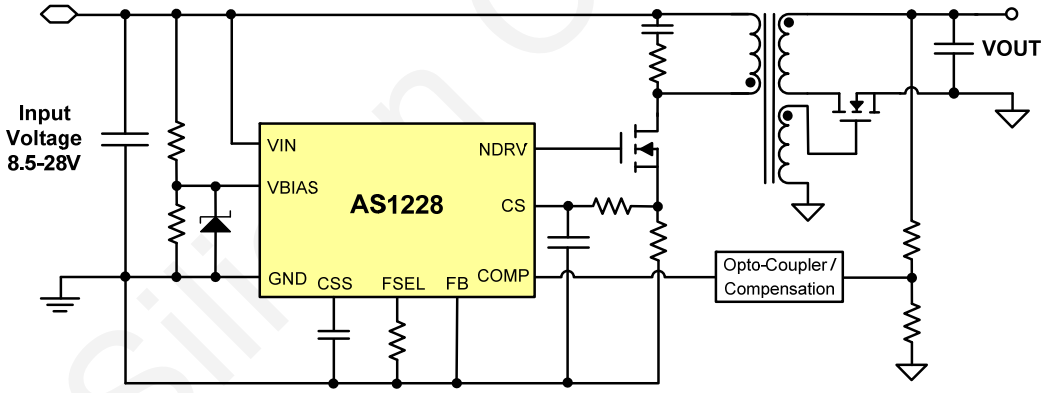
Features

- 8.5V to 28V Input Voltage
- High Efficiency Design Capable, 90% typical
- Low No-Load Power for Energy Star and EUP/CoC Compliant Designs
- Programmable PWM Frequency, 100-500 KHz
- Programmable Soft Start
- Over Temperature Protection
- Industrial Temperature Range, -40° to +85°C
- RoHS compliant 5x5 mm 20 lead QFN and Chip Scale Packaging (contact Akros for CSP details)

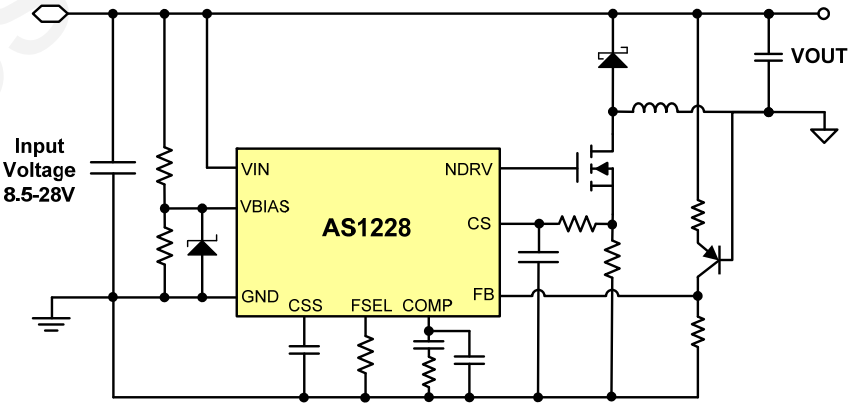
Typical Applications

- Consumer 12V, 24V Input Power Conversion (WiFi Access Points, Ethernet Switches, Set Top Boxes, DVR, Printers)
- Enterprise Router, Switch and Server Blades
- Isolated and Non-Isolated IBA Power Conversion
- Flyback, Forward and Buck Power Designs

Typical Isolated Synchronous Flyback Application



Typical Non-Isolated High Side Buck Application



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Status:	Preliminary Datasheet
Revision:	Version 0.25
Release Date:	September 27, 2010

Advance Datasheet: Document contains design specifications for initial product development.

Preliminary Datasheet: Document contains preliminary data and will be revised at a later date.

Final Datasheet: Document contains specifications on a product that is in final release.

PIN ASSIGNMENTS AND DESCRIPTIONS

Figure 1 - AS1228 Pin Assignments

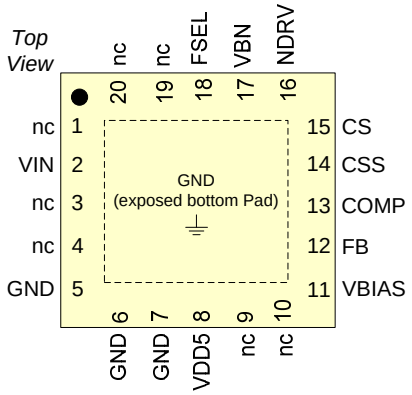


Table 1 - AS1228 Pin Descriptions

Pin	I/O[1]	Name	Description
2	P	VIN	Voltage input.
5	A	GND	Must be connected to exposed bottom side pad ground (GND).
6	A	GND	Must be connected to exposed bottom side pad ground (GND).
7	A	GND	Must be connected to exposed bottom side pad ground (GND).
8	O	VDD5	Internal 5 volts bus decoupling point.
11	A	VBIAS	Voltage bias input.
12	A	FB	DC-DC Controller feedback point.
13	A	COMP	DC-DC Controller error amplifier compensation network connection.
14	A	CSS	DC-DC Controller soft-start capacitor connection point.
15	A	CS	DC-DC Controller peak-current sense input (low side).
16	O	NDRV	DC-DC Controller N-MOSFET gate drive.
17	O	VBN	DC-DC Controller low-side supply decoupling.
18	I	FSEL	Frequency Select. This pin sets the switching frequency of the DC-DC converter.
Pad	P	GND	Device ground connection (exposed bottom side Pad).
1, 3, 4, 9, 10, 19, 20	-	nc	No connection. Must be left floating.

[1]Key: I = Input O = Output A = Analog signal P = Power

TEST SPECIFICATIONS

Unless otherwise noted Test Specifications apply over the full -40°C to 85°C operating temperature range.

Table 2 - Absolute Maximum Ratings

Description	Max Value[1]	Units
High-voltage pin (VIN) Under Transient conditions[4]	100	Volts
High-voltage pin (VIN) Steady-state with internal Surge Clamp	60	Volts
VDD5; VBIAS; FB; COMP; CSS; CS; NDRV; VBN; FSEL	6	Volts
ESD Ratings		
Human body model[2]	2	KV
ESD charged device model	500	V
ESD machine model	200	V
System level (contact/air) at RJ-45[3]	8/15	KV
Temperature		
Storage temperature	165	°C
Junction temperature	150	°C

[1] Absolute maximum ratings are limits beyond which damage to the device may occur.
[2] The human body model is as described in JESD22-A114.
[3] System ESD testing done per IEC61000-4-2.
[4] Transient conditions like system startup and other noise conditions. Device must not be exposed to sustained over-voltage condition at this level.

Table 3 - Normal Operating Conditions

Description	Min	Typical[1]	Max	Unit	Conditions
VIN	8.5V		28V		
Operating temperature range	-40		+85	°C	

[1] Typical specification; not 100% tested. Performance guaranteed by design and/or other correlation methods.

Table 4 - DC-DC Controller Electrical Characteristics

Description	Min	Typical[1]	Max	Units	Conditions
Operating current (at VIN)			TBD	mA	VIN = TBD, FOSC = TBD
FOSC (DC-DC switching frequency)	80	100	120	KHz	Rosc=178kΩ
	200	225	250		Rosc=100kΩ
	315	350	385		Rosc=53.6kΩ
	450	500	550		Rosc=36.8kΩ
FOSC temperature coefficient		0.12		%/C	
NDRV ROUT		1.2	3	Ω	Output drive resistance
NDRV voltage		4.7			NDRV voltage follows VBN power supply voltage

Description	Min	Typical[1]	Max	Units	Conditions
Gate drive dynamic response NDRV TR, TF		2.2 2		ns ns	10% - 90% with CLOAD = 1 nF
Max. NDRV duty cycle		80		%	Measured at 350KHz
Min. NDRV duty cycle		6	10	%	Measured at 350KHz
VBN		4.7		V	Internal supply voltage; sets VOH of NDRV.
Error amplifier reference voltage	1.45	1.5	1.55	V	Compared to input of the FB pin
VPK, peak current sense threshold voltage at CS	500	600	700	mV	IPEAK=VPK/RSENSE
Soft start ramp time		2		ms	Conditions: CSS=100nF
COMP source current		80		µA	FB = 0V, COMP=0V
COMP sink current		80		µA	FB = 5V, COMP=5V
Open loop voltage gain (Error amplifier)		80		dB	
Small signal unity-gain bandwidth		5		MHz	COMP connected to FB.
FB leakage (source or sink)		1		µA	
VBIAS pin voltage	5.4	5.6	5.8	V	
VBIAS current		75		µA	VBIAS voltage = 5.6V

[1] Typical specifications are not 100% tested. Performance guaranteed by design and/or other correlation methods.

Table 5 - Thermal Characteristics

Description	Min	Typical[1]	Max	Units	Conditions
Thermal shutdown temperature		165		°C	Above this Temp., the AS1228 is disabled.
Thermal shutdown hysteresis		40		°C	Temperature change required to restore full operation after thermal shutdown
Max. on-die operating temperature			140	°C	Maximum recommended operating temperature for normal operation
Thermal Resistance, Junction to Ambient, θ_{JA}		31		°C/W	20 lead QFN package
Thermal Resistance, Junction to Case, θ_{JC}		3.4		°C/W	20 lead QFN package

[1] Typical specifications are not 100% tested. Performance guaranteed by design and/or other correlation methods.

FUNCTIONAL DESCRIPTION

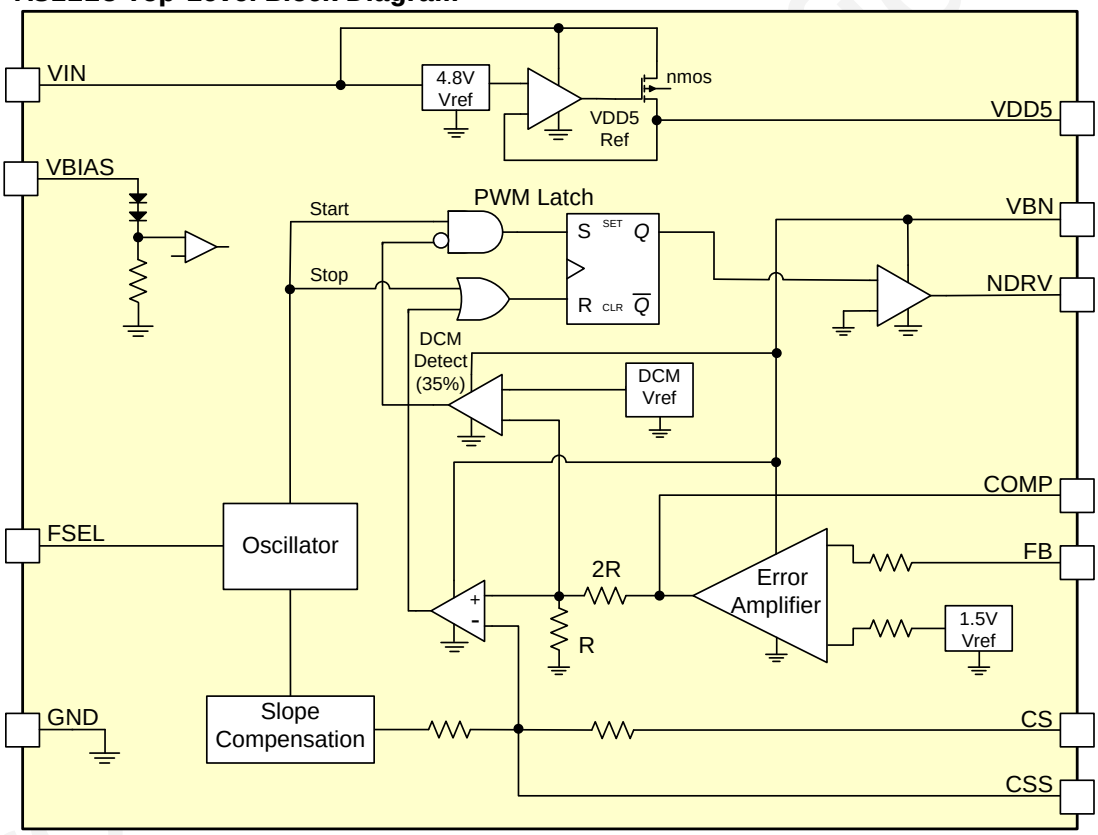
AS1228 Overview

The AS1228 DC-DC architecture is that of a current-mode controller, configurable with external components to fly-back, forward or buck topologies. Both non-isolated and isolated application topologies are supported.

The integrated DC-DC controller includes programmable soft start. Once input power is applied within the device VIN range, the DC-DC controller starts up. The controller provides a gate control signal, NDRV, for an external switching MOSFET and uses an external resistor to sense primary current in the transformer. It also provides an 80% duty cycle (max) programmable PWM switching frequency and a true voltage-output error amplifier.

As part of a full system level solution to control EMI, the device reduces switching noise by shaping the FET driver waveforms. Ground bounce is also reduced by minimizing dV/dt switching noise.

Figure 2 - AS1228 Top-Level Block Diagram



Programmable PWM Frequency

The FSEL pin allows the DC-DC converter switching frequency to be set externally. Placing a resistor between FSEL and GND sets the internal oscillator's frequency. Table 6 identifies resistor values for some commonly used switching frequencies.

Table 6 - PWM Switching Frequency Selection

Switching Frequency (KHz)	FSEL Resistor (KΩ, 1%)
100	178
225	100
350	53.6
500	36.8

Current-Limit/Current Sense

The DC/DC controller provides cycle-by-cycle current limiting, to ensure that transformer primary current limits are not exceeded. The maximum average current in the transformer primary is nominally set by internal duty-cycle limits.

Low Load Current Operation

If a low output power condition is detected the DC-DC Controller is put into a discontinuous current operation (DCM) mode.

Compensation and Feedback

For isolated applications, loop compensation and output voltage feedback is generally provided by an opto-isolator circuit, and the Feedback pin (FB) is tied to ground. In these applications, the COMP pin is pulled up to approximately 4.8V by an internal current source. This pull-up can be the termination for an opto-isolator, or, an additional resistor can be used in parallel.

For non-isolated applications, a resistive divider network, connected directly to the FB pin, senses the output voltage. The internal error amplifier is connected to a 1.5V reference voltage and the control loop will servo the FB pin to this voltage. A capacitive/resistive network connected to the COMP pin provides loop compensation.

Soft-Start Current Limit

Internal circuitry automatically ramps up the inrush current by limiting the maximum current allowed in the transformer primary magnetizing inductance per clock cycle. The amount of time required to perform a soft start cycle is determined by the CSS capacitor. A value of 330nF provides approximately 7ms of soft startup ramp time.

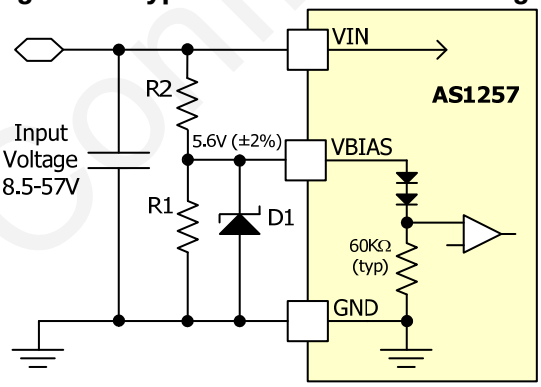
Thermal Limit / Protection

The AS1228 provides internal thermal protection by monitoring die temperature and reducing maximum current or disconnecting power as needed to prevent pre-set thermal limits from being exceeded. Two-stage thermal current limiting is implemented, which reduces the operating current limit by 50% when the die temperature reaches 145°C, and disables the power MOSFET switch above 165°C. Normal current limits in both cases are re-applied when the die temperature returns below 125°C.

Deriving VBIAS from VIN

A VBIAS input (5.6V, ±2%) is required for device operation. Figure 3 shows a typical external component design using the VIN power source to create VBIAS.

Figure 3 - Typical VBIAS from VIN Design



An appropriate ratio of R1 and R2 resistors should be used to ensure proper operation across all supply voltages. Though single values of R1 and R2 can be used across the whole local supply voltage range of 8.5V to 28V, if the application has a narrower input voltage range then the resistor values can be adjusted to minimize power consumption. See Table 7 for some typical external component values.

Table 7 - Typical VBIAS External Component Values

Local Voltage Range (V)	R2 (KΩ)	R1 (KΩ)
8.5-28	2.74	4.02
20-28	11.3	4.02
D1: 5.6V Zener (±2%, max)		

APPLICATION INFORMATION

For detailed applications documentation please refer to the separate Akros application note #TBD, the AS12xx Design and Layout Guide.

Isolated DC-DC Topologies

The DC-DC controller can be configured in several different isolated power topologies.

Flyback topology is chosen when a minimum number of external components is desired, or, there is a large step-down and the output voltage is < 7V. The Forward mode is chosen when lower switching noise is desired.

Either of these isolated topologies can be designed for synchronous or non-synchronous operation based on system requirements. A typical high-efficiency Isolated Synchronous Flyback design is shown in Figure 4.

Non-Isolated Topologies

A Buck topology is used in non-isolated applications, which uses an inductor for energy storage instead of a transformer.

Buck designs typically have the smallest overall board component footprint.
Figure 5 shows a typical non-synchronous high side Buck converter design. Since the FB voltage is input power ground referenced, the feedback signal must be level-shifted back down to the input power ground. This is accomplished by the PNP transistor and associated resistors.

Figure 4 - Typical Isolated Synchronous Flyback Application

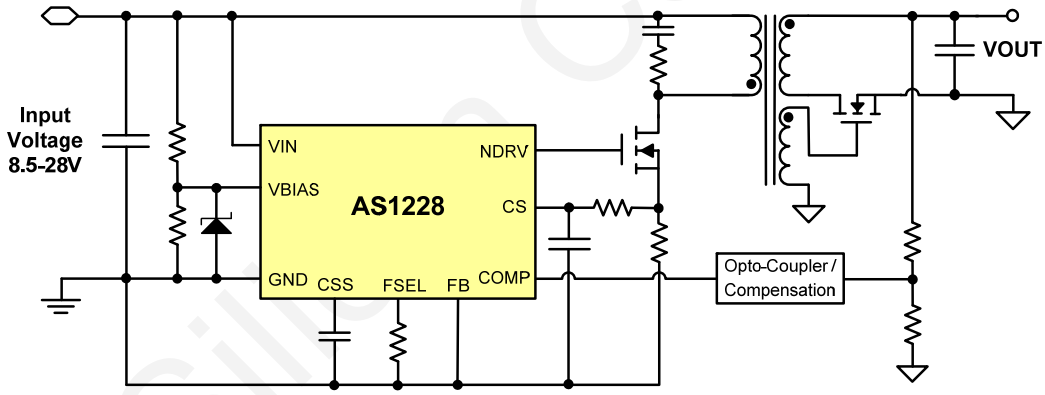
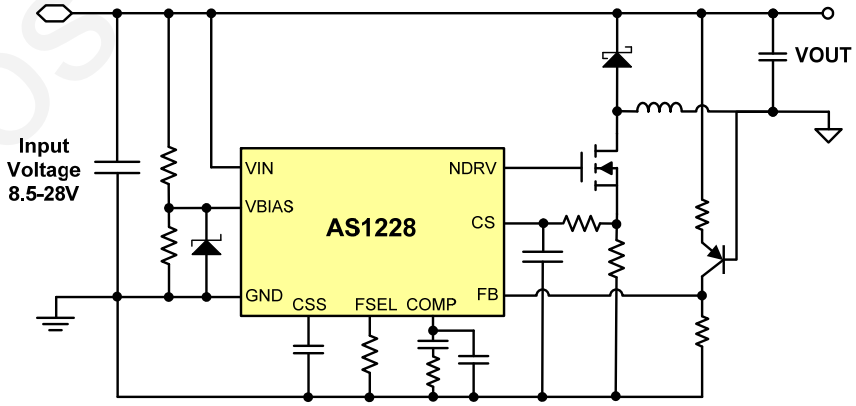


Figure 5 - Typical Non-Isolated High Side Buck Application



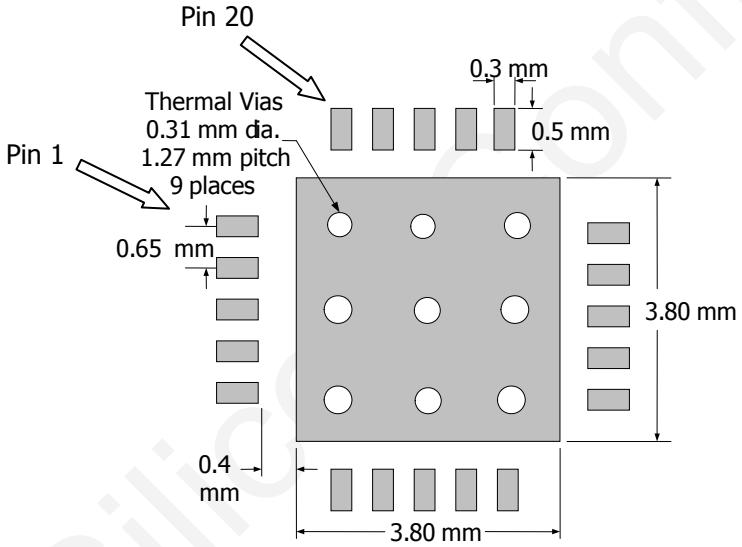
THERMAL DE-RATING AND BOARD LAYOUT CONSIDERATIONS

The AS1228 is capable of operation to 85 ºC (ambient) without forced cooling. A thermal pad on the underside of the package dissipates generated heat.

If the PCB landing pattern is properly designed, the QFN package should exhibit a thermal resistance of Θ_{JA}=31°C/W. For adequate heat dissipation, the board layout must include a ground pad which provides both the ground connection and dissipates the heat energy produced in the chip. Thermal vias are used to draw heat away from the QFN package and transfer it to the backside of the system PCB.

The recommended PCB layout for the AS1228 is shown in Figure 6.

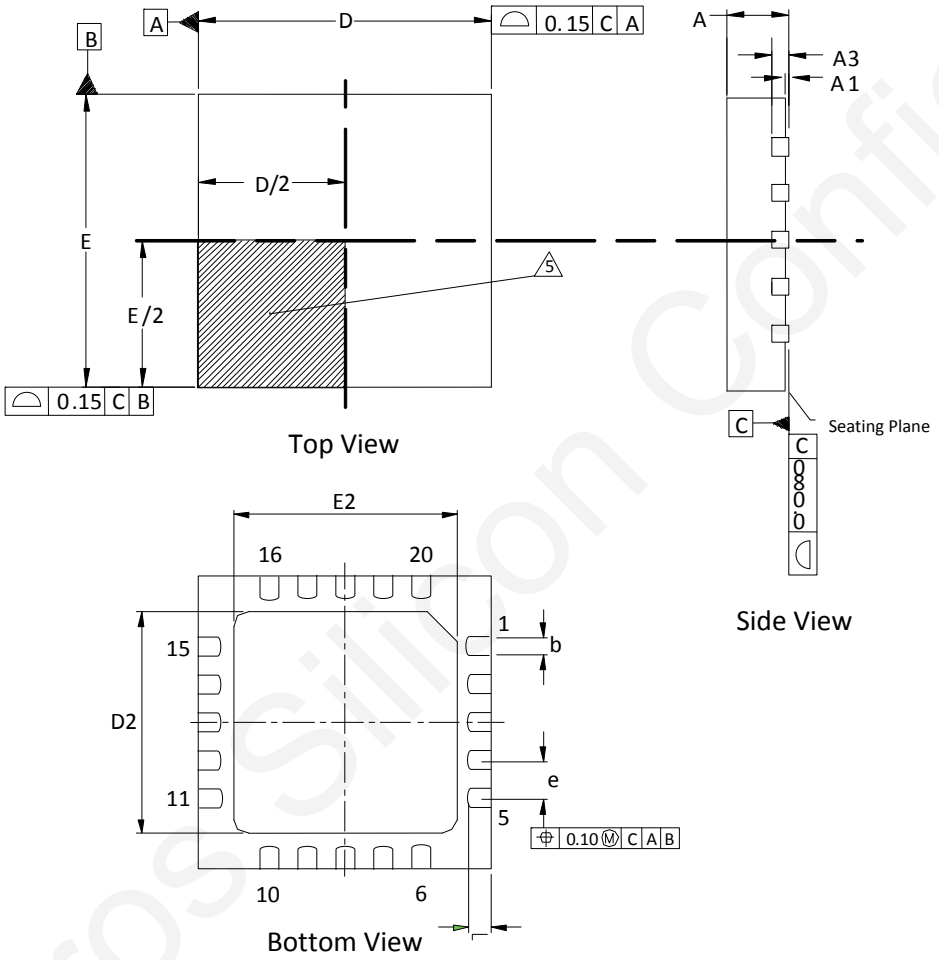
Figure 6 - AS1228 PCB Footprint (top view)



PHYSICAL DIMENSIONS

Figure 7 – AS1228 Physical Dimensions

20 Pin QFN Package, 5mm X 5mm
For Chip Scale Packaging (CSP) details please contact Akros



Common Dimensions			
	MIN.	NOM.	MAX
A	0.80	0.85	0.95
A1	0.00	0.02	0.04
A3		0.20 REF.	
D	4.85	5.00	5.15
D2	3.70	3.80	3.90
E	4.85	5.00	5.15
E2	3.70	3.80	3.90
L	0.35	0.40	0.45
N		20L	
b	0.25	0.30	0.35
e		0.650 BSC	
JEDEC		MO-220-VHHC-2	

NOTES

1. Controlling dimensions in mm.
2. Dimension tolerances are ± 0.1 (angular tolerance ± 3°) unless otherwise specified.
3. All dimensions and tolerances conform to ANSI 14.5M-1994.
4. Co-planarity applies to exposed pad as well as the terminals.
5. Pin 1 location may be identified by either a mold or marked feature.
6. JEDEC reference MO-220.

CONTACT INFORMATION

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