DataSheet

AS1353, AS1356
Linear Low-Dropout 150mA Voltage Regulators

1 General Description

The AS1353/AS1356 are high-performance, fixed-voltage linear LDOs designed for use with capacitors of 1 to 10µF. The devices can deliver superior performance even under low dropout conditions when the power transistor operates in linear mode.

The integrated P-channel MOSFET output allows the devices to maintain a low supply-current at loads of up to150mA. A shutdown mode includes logic-controlled circuitry which reduces shutdown current to less than 1µA (max).

Integrated over-temperature and over-current protection circuitry switches the devices off in case of thermal overload or output short-circuit conditions.

The AS1353/AS1356 are optimized for low equivalent-series resistance (ESR) output capacitors. Additionally, all devices contain reversed battery protection which disconnects the internal circuitry and parasitic diodes if the battery is connected incorrectly.

The AS1356 also features power-OK circuitry which can be used to monitor output regulation.

All devices also feature an integrated error amplifier and built-in 1.25V reference, and output current is limited (380mA typ) via the on-chip current limiting circuitry.

Multiple output voltages are available as standard products: 3.6, 3.3, 3.0, 2.7, 2.5, or 1.5V. All devices are available in a 5-pin SOT23 package.

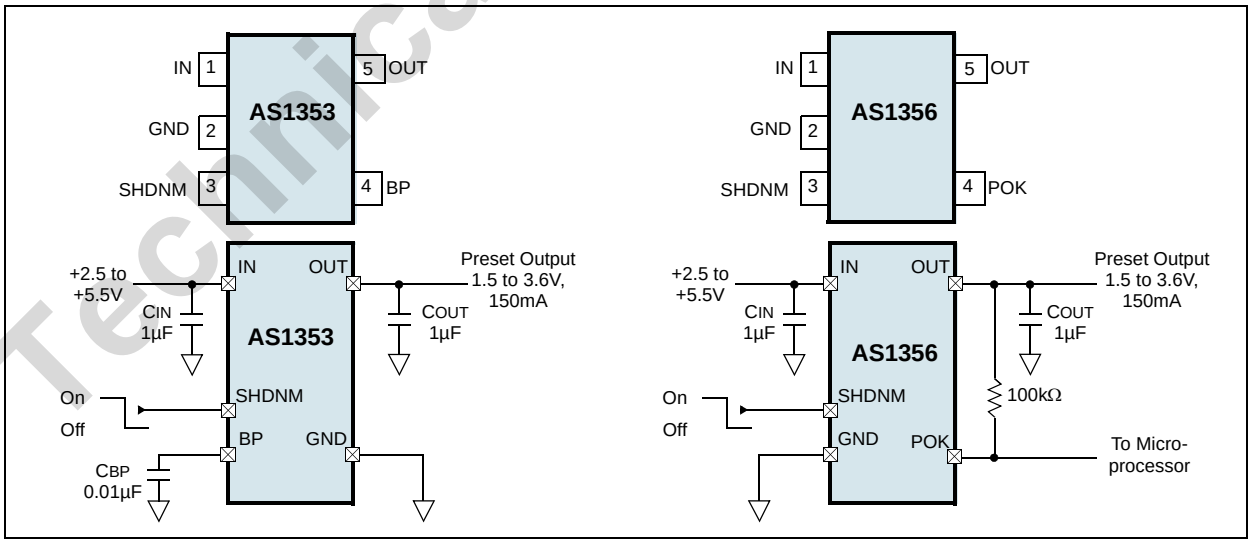
2 Key Features

- Ultra-Low Dropout Voltage: 40mV @ 100mA load
- Output Voltage Range: +1.5 to +3.6V (100mV steps)
- Max Output Current: 150mA
- Output Voltage Accuracy: ±1%
- Low Shutdown Current: 1µA
- High PSRR: 60dB at 100Hz
- Integrated Overtemperature/Overcurrent Protection
- Reverse-Battery Protection (AS1353/AS1356)
- Power-OK Output (AS1356)
- Minimal External Components Required
- Operating Temperature Range: -40 to +85°C
- 5-pin SOT23 Package

3 Applications

The devices are ideal for powering cordless and mobile phones, MP3 players, CD and DVD players, PDAs, handheld computers, digital cameras, and any other hand-held and/or battery-powered device.

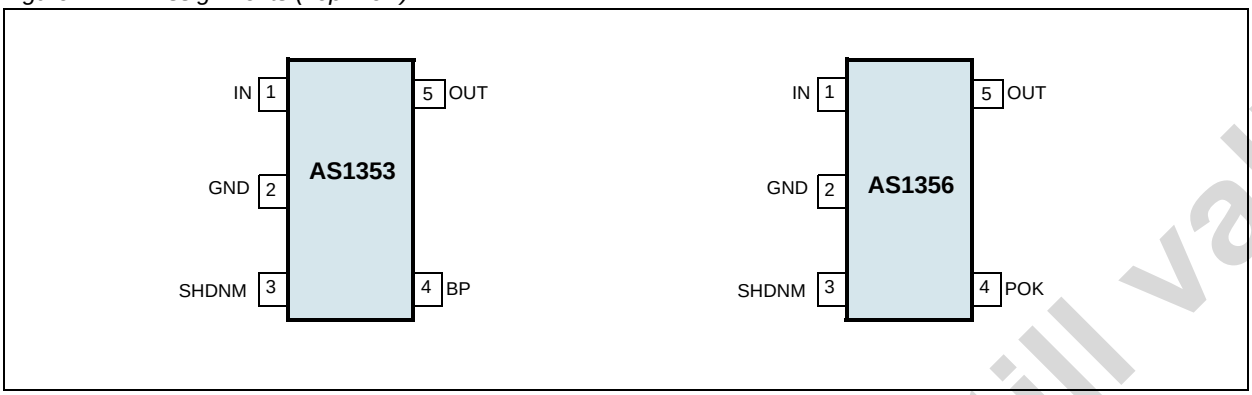
Figure 1. Pinout and Application Diagrams



4 Pinout

Pin Assignments

Figure 2. Pin Assignments (Top View)



Pin Descriptions

Table 1. AS1353 Pin Descriptions

Pin Number	Pin Name	Description
1	IN	**LDO Input**. Supply voltage can range from 2.5 to 5.5V. Bypass with a 1µF capacitor to GND (see Capacitor Selection and Regulator Stability on page 10).
2	GND	**Ground**. This pin also functions as a heat sink. Solder to a large pad or the circuit-board ground plane to maximize power dissipation.
3	SHDNM	**Active-Low Shutdown Input**. A logic low reduces the supply current to < 1µA. **Note:** Connect to IN for normal operation.
4	BP	**Reference-Noise Bypass**. Bypass with a low-leakage, 0.01µF ceramic capacitor for reduced noise at the output.
5	OUT	**LDO Output**. Fixed 1.5, 2.5, 2.7, 3.0, 3.3, and 3.6V output. Sources up to 150mA.

Table 2. AS1356 Pin Descriptions

Pin Number	Pin Name	Description
1	IN	**LDO Input**. Input voltage can range from 2.5 to 5.5V. Bypass with 1µF to GND (see Capacitor Selection and Regulator Stability on page 10).
2	GND	**Ground**. This pin also functions as a heat sink. Solder to a large pad or the circuit-board ground plane to maximize power dissipation.
3	SHDNM	**Active-Low Shutdown Input**. A logic low reduces the supply current to < 1µA. **Note:** Connect to pin IN for normal operation.
4	POK	**Power-OK Output**. Active-low, open-drain output indicates an out-of-regulation condition. Connect a 100kΩ pull-up resistor to pin OUT for logic levels. **Note:** Leave this pin unconnected if the power-OK feature is not used.
5	OUT	**LDO Output**. Fixed 1.5, 2.5, 2.7, 3.0, 3.3, and 3.6V output. Sources up to 150mA.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 3 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Section 6 Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Typ	Units	Comments
IN, SHDNM to GND	-7	+7		V	
SHDNM to IN	-7	+0.3		V	
POK, BP, OUT to GND	-0.3	V_{IN} + +0.3		V	
Output Short-Circuit Duration	Indefinite			V	
Continuous Power Dissipation (T_{AMB} = +70ºC)		571		mW	Derate 7.1mW/ºC above +70ºC
Operating Temperature Range	-40	+85		ºC	
Junction Temperature		+150		ºC	Internally limited
Θ_{JA}		+140		ºC/W	
Storage Temperature Range	-65	+150		ºC	
Package Body Temperature		+260		ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for non-hermetic Solid State Surface Mount Devices"*

6 Electrical Characteristics

(V_{IN} = $V_{OUT(Nominal)}$ + 1V, SHDNM = IN, T_{AMB} = -40 to +85ºC (unless otherwise specified). Typical values are at T_{AMB} = +25ºC. Limits are 100% production tested at T_{AMB} = +25ºC.

Table 4. Electrical Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IN}	Input Voltage			2.5		5.5	V
	Output Voltage Accuracy	T_{AMB} = +25ºC, I_{OUT} = 100µA		-1		1	%
		T_{AMB} = -40 to +85ºC, I_{OUT} = 100µA to 150mA		-3		3	
I_{OUT}	Maximum Output Current			150			mA
I_{LIM}	Current Limit			160	380		mA
I_Q	Ground Pin Current	I_{OUT} = 100µA			70	180	µA
		I_{OUT} = 150mA			115		
V_{IN} - V_{OUT}	Dropout Voltage [1]	I_{OUT} = 100µA			0.05		mV
		I_{OUT} = 50mA			20		
		I_{OUT} = 100mA			40	100	
		I_{OUT} = 150mA			60		
ΔV_{LNR}	Line Regulation	V_{IN} = 2.5V or (V_{OUT} + 0.1) to 4.5V, I_{OUT} = 1mA		-0.2	0	0.2	%/V
		V_{IN} = 2.5V or (V_{OUT} + 0.1) to 5.5V, I_{OUT} = 1mA		-0.8	0	0.8	
ΔV_{LDR}	Load Regulation	I_{OUT} = 100µA to 150mA, C_{OUT} = 1µF			0.001	0.02	%/mA
en	Output Voltage Noise	C_{OUT} = 1µF, f = 10Hz to 100kHz, C_{BP} = 0.01µF	AS1353		30		μV_{RMS}
		C_{OUT} = 1µF, f = 10Hz to 100kHz	AS1356		110		
PSRR	Output Voltage AC Power-Supply Rejection Ratio	f = 100Hz, C_{OUT} = 1µF, (C_{BP} = 0.01µF, AS1353)			60		dB
Shutdown [2]							
t_{ON}	Exit Delay from Shutdown [3,4]	C_{BP} = 0.01µF, no load (AS1353)			30	150	µs
I_{OFF}	Shutdown Supply Current	SHDNM = GND	T_{AMB} = +25ºC		0.01	1	µA
			T_{AMB} = +85ºC		0.04		
V_{IH}	SHDNM Input Threshold	V_{IN} = 2.5 to 5.5V		2.0			V
V_{IL}						0.4	
I_{SHDNM}	SHDNM Input Bias Current	SHDNM = IN or GND	T_{AMB} = +25ºC		0.03	100	nA
			T_{AMB} = +85ºC		0.2		
Power-OK Output (AS1356 only)							
V_{POK}	Power-OK Voltage Threshold	I_{OUT} = 0, V_{OUT} falling		92	95	97	% V_{OUT}
		Hysteresis, I_{OUT} = 0			1		
V_{OL}	POK Output Voltage Low	I_{SINK} = 1mA				0.4	V
	POK Output Leakage Current	0 ≤ V_{POK} ≤ 5.5V, V_{OUT} in regulation				1	µA
Thermal Protection							
T_{SHDNM}	Thermal Shutdown Temperature	AS1353			150		ºC
		AS1356			165		
ΔT_{SHDNM}	Thermal Shutdown Hysteresis	AS1353			15		ºC
		AS1356			20		ºC

1. Dropout voltage = V_{IN} - V_{OUT} when V_{OUT} is 100mV < V_{OUT} for V_{IN} = V_{OUT} +0.5V (applies only to output voltages ≥ 2.5V).
2. The rise and fall time of the shutdown signal must not exceed 1ms.
3. The delay time is defined as time required to set V_{OUT} to 95% of its final value.
4. Guaranteed by design.

7 Typical Operating Characteristics

VOUT = +3.0V, VIN = +3.6V, CIN = COUT = 1µF, SHDNM = IN, TAMB = +25ºC (unless otherwise specified)

Figure 3. Ground Pin Current vs. Input Voltage

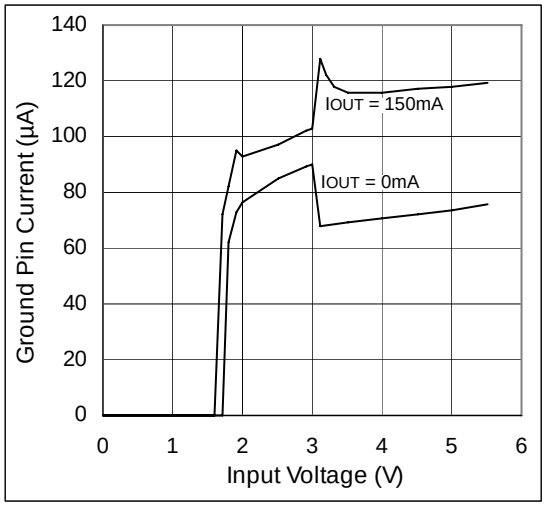


Figure 4. Ground Pin Current vs. Output Load

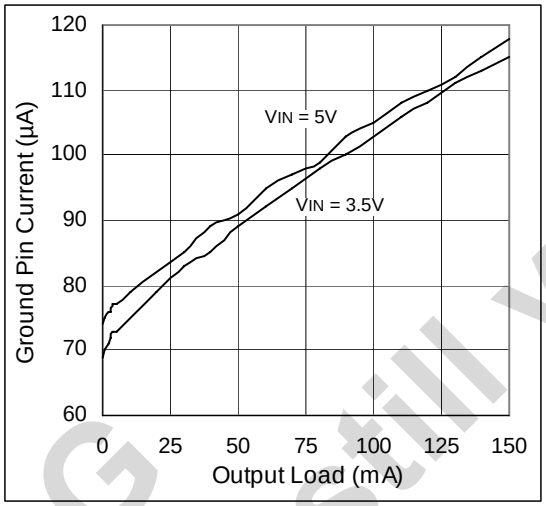


Figure 5. Ground Pin Current vs. Temperature

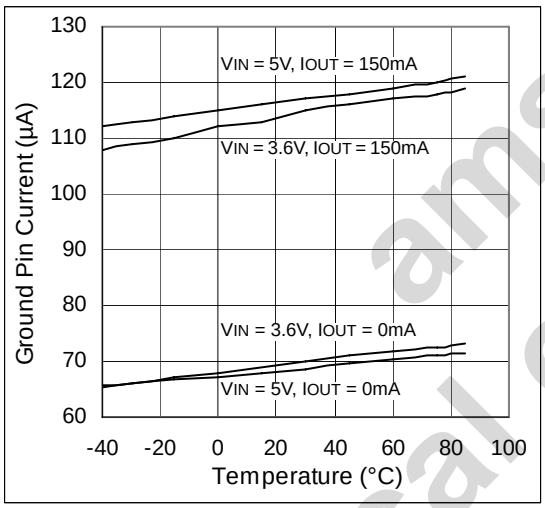


Figure 6. Output Voltage vs. Input Voltage

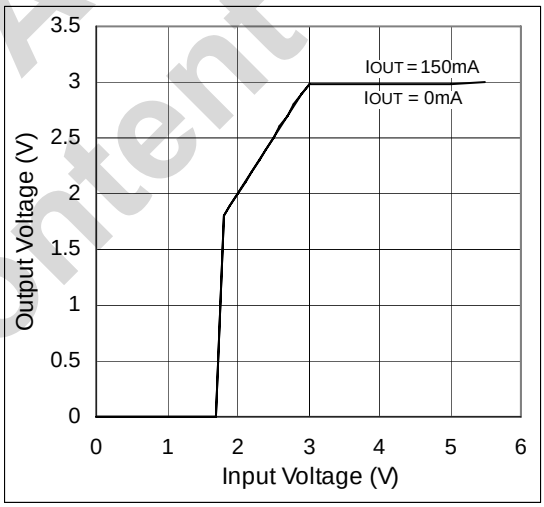


Figure 7. Output Voltage vs. Output Load

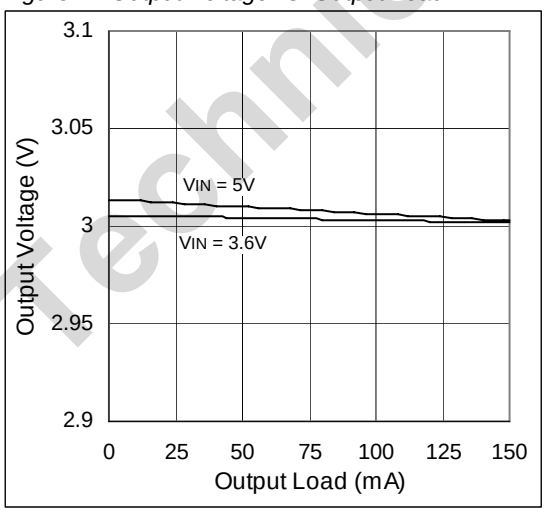


Figure 8. Output Voltage vs. Temperature

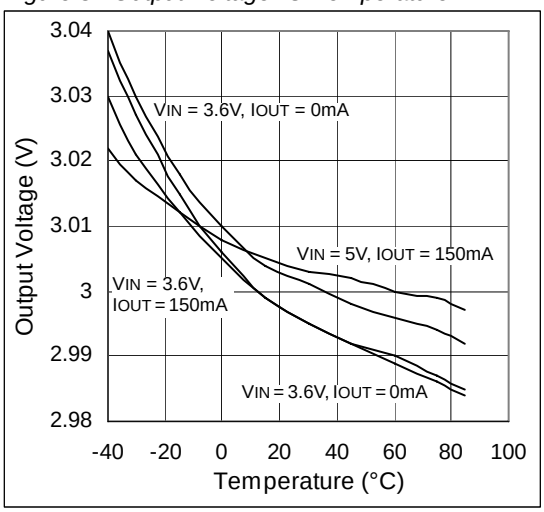


Figure 9. Dropout Voltage vs. Output Load

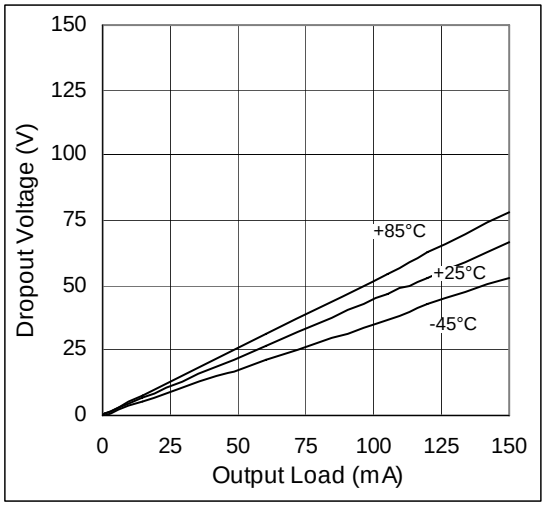


Figure 10. PSRR vs. Frequency

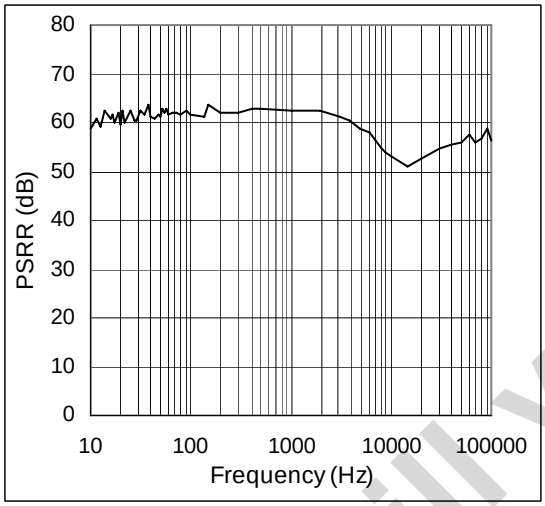
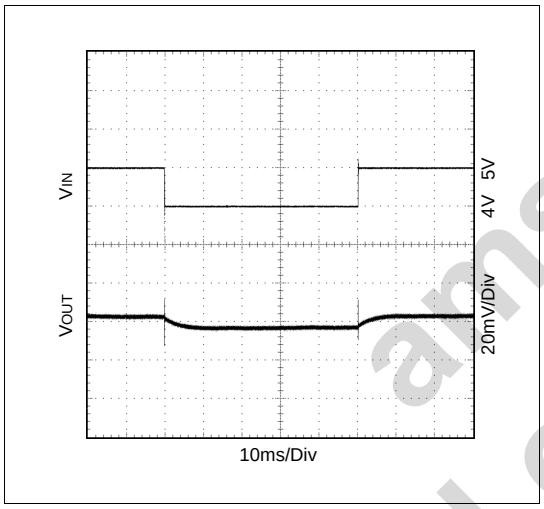


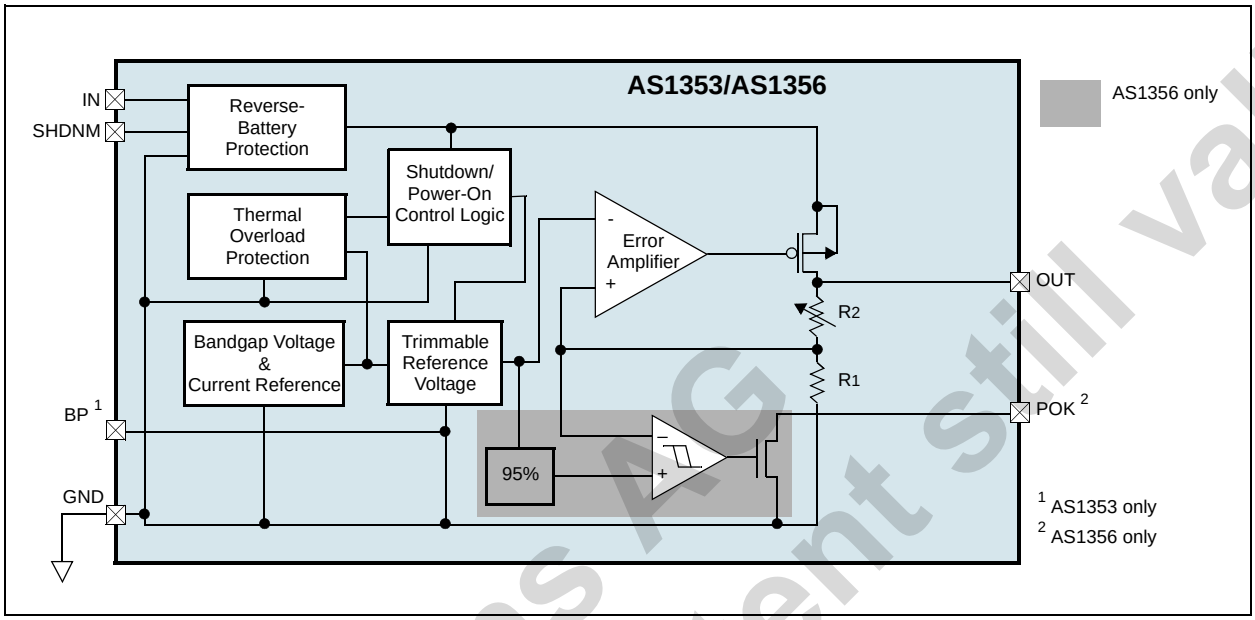
Figure 11. Line Transient Response; IOUT = 50mA



8 Detailed Description

The AS1353/AS1356 are low-dropout, low-quiescent-current linear regulators intended for LDO regulator applications where output current load requirements range from no load to 150mA. All devices come standard with fixed output voltages of 1.5 to 3.6V (see Ordering Information on page 12).

Figure 12. Block Diagram



As illustrated in Figure 12, the devices comprise a 1.25V reference, error amplifier, P-channel MOSFET pass transistor, power-OK comparator, internal feedback voltage divider, current limiter, reverse-battery protection, thermal sensor and shutdown logic.

The 1.25V bandgap reference is connected to the inverting input of the error amplifier. The error amplifier compares this reference with the feedback voltage and amplifies the difference. If the feedback voltage is lower than the reference voltage, the P-channel MOSFET gate is pulled lower, allowing more current to pass to the output, and increases the output voltage. If the feedback voltage is too high, the pass-transistor gate is pulled up, allowing less current to pass to the output. The output voltage feeds back through an internal resistor voltage divider connected to pin OUT.

Output Voltages

Standard products are factory-set with output voltages of from 1.5 to 3.6V. A two-digit suffix of the part number identifies the nominal output voltage (see Ordering Information on page 12).

Non-standard devices are available. Contact austriamicrosystems AG for more information.

Internal P-Channel MOSFET Pass Transistor

The integrated 0.5Ω (typ) P-channel MOSFET pass transistor requires no base drive, which reduces quiescent current significantly, and does not exhibit the problems associated with PNP-based regulators, such as dropout when the pass transistor saturates or high base-drive currents under large load conditions.

The devices consume only 115µA quiescent current in dropout, light-load, or heavy-load applications (see Typical Operating Characteristics on page 6).

Power-OK

The AS1356's power-ok circuitry is built around an N-channel MOSFET. The circuitry monitors the voltage on pin 5 (OUT) and if the voltage goes out of regulation (e.g. during dropout, current limit, or thermal shutdown) pin POK goes low.

The power-OK feature is not active during shutdown and provides a power-on-reset (POR) function that can operate down to V_{IN} = 1V. A capacitor to GND may be added to generate a POR delay.

To obtain a logic-level output, connect a pull-up resistor from pin POK to pin OUT. Larger values for this resistor will help minimize current consumption; a 100kΩ resistor is perfect for most applications (see Figure 13).

Reverse-Battery Protection

The AS1353/AS1356 contain integrated reverse-battery protection circuitry which monitors the polarity of pins IN and SHDNM and disconnects the internal circuitry and parasitic diodes if the battery is connected incorrectly. Reverse supply current is limited to 1mA if V_{IN} = V_{SHDNM} falls below ground. Load current is also limited when V_{IN} or V_{SHDNM} are reverse biased with respect to ground.

Current Limiting

The AS1353/AS1356 include current limiting circuitry to protect against short-circuit conditions. The circuitry monitors and controls the gate voltage of the P-channel MOSFET, limiting the output current to 380mA (typ). The P-channel MOSFET output can be shorted to ground for an indefinite period of time without damaging the device.

Noise Reduction

The AS1353 uses an external 0.01µF bypass capacitor (C_{BP}) at pin BP to reduce output noise. An internal pre-charge circuit is used to reduce start-up time.

The use of C_{BP} > 0.01µF improves noise performances but increases start-up time.

Thermal-Overload Protection

The devices are protected against thermal runaway conditions by the integrated thermal sensor circuitry. Thermal shutdown is an effective means to prevent die overheating since the power transistor is the principle heat source in the device.

If the junction temperature exceeds 165ºC (typ, AS1356) or 150ºC (typ, AS1353), the thermal sensor starts the shutdown logic, at which point the P-channel MOSFET is switched off. After the device temperature has dropped by approximately 20ºC, the thermal sensor will turn the P-channel MOSFET on again. Note that this will be exhibited as a pulsed output under continuous thermal-overload conditions.

Note: The absolute maximum junction-temperature rating of +150ºC should not be exceeding during continual operation.

Operating Region and Power Dissipation

Maximum power dissipation is determined by the thermal resistance of the case and circuit board, the temperature difference between the die junction and ambient air, and the rate of air flow. The power dissipation of the device is calculated by:

$$P = I_{OUT} (V_{IN} - V_{OUT}) \quad (EQ\ 1)$$

Maximum power dissipation is calculated by:

$$P_{MAX} = (T_J - T_{AMB}) / (\Theta_{JB} + \Theta_{JA}) \quad (EQ\ 2)$$

Where:

T_J - T_{AMB} is the temperature difference between the device die junction and the surrounding air.

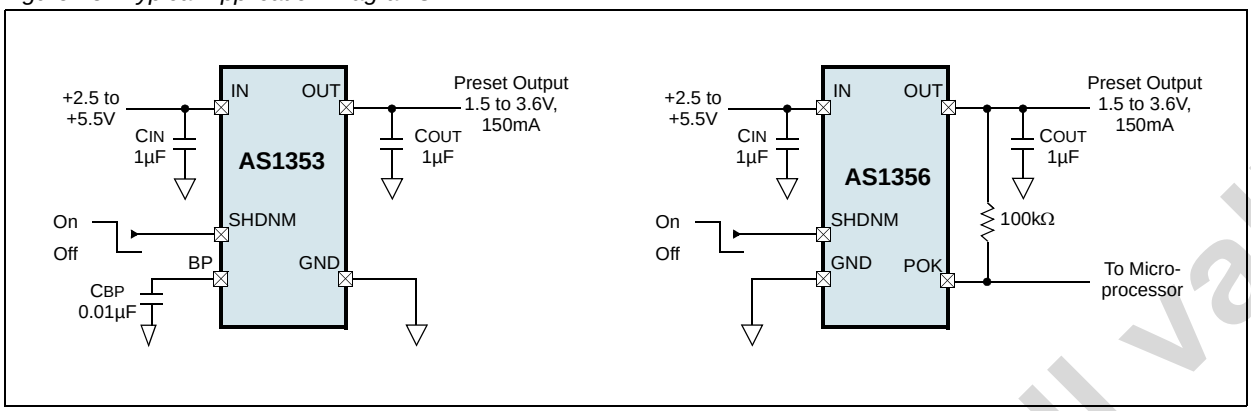
Θ_{JB} or Θ_{JC} is the thermal resistance of the package.

Θ_{JA} is the thermal resistance through the printed circuit board, copper traces, and other materials to the surrounding air.

Note: Pin GND is a multi-function pin providing a connection to the system ground and acting as a heat sink. This pin should be connected to the system ground using a large pad or ground plane.

9 Typical Application

Figure 13. Typical Application Diagrams



Capacitor Selection and Regulator Stability

Ceramic capacitors are highly recommended as they offer distinct advantages over their tantalum and aluminum electrolytic components.

For stable operation with load currents up to 150mA over the entire device temperature range, use a 1µF (min) ceramic output capacitor with an ESR <0.2Ω.

Use large output capacitor values (10µF max) to reduce noise and improve load transient-response, stability and power-supply rejection.

Note: Some ceramic capacitors exhibit large capacitance and ESR variations with variations in temperature. Z5U and Y5V capacitors may be required to ensure stability at temperatures below T_{AMB} = -10ºC. With X7R or X5R capacitors, a 1µF capacitor should be sufficient at all operating temperatures.

Power Supply Rejection Ratio

The AS1353/AS1356 are designed to deliver low dropout voltages and low quiescent currents. Power-supply rejection is 60dB (typ) at low frequencies. To improve power supply-noise rejection and transient response, increase the values of the input and output bypass capacitors (see Figure 13).

The Typical Operating Characteristics (page 6) show the device line- and load-transient responses. See the Power-Supply Rejection Ratio vs. Frequency graph in the Typical Operating Characteristics section (page 6) for further details.

Dropout Voltage

For standard products with output voltage greater than the minimum V_{IN} (2.5V), the minimum input-output voltage differential (dropout voltage) determines the lowest usable supply voltage. This determines the useful end-of-life battery voltage in battery-powered systems.

The dropout voltage is a function of the P-MOSFET drain-to-source on-resistance multiplied by the load current, and is calculated by:

$$V_{DROPOUT} = V_{IN} - V_{OUT} = R_{DS(ON)} \times I_{OUT} \quad \text{(EQ 3)}$$

Where:

$R_{DS(ON)}$ is the drain-to-source on-resistance.

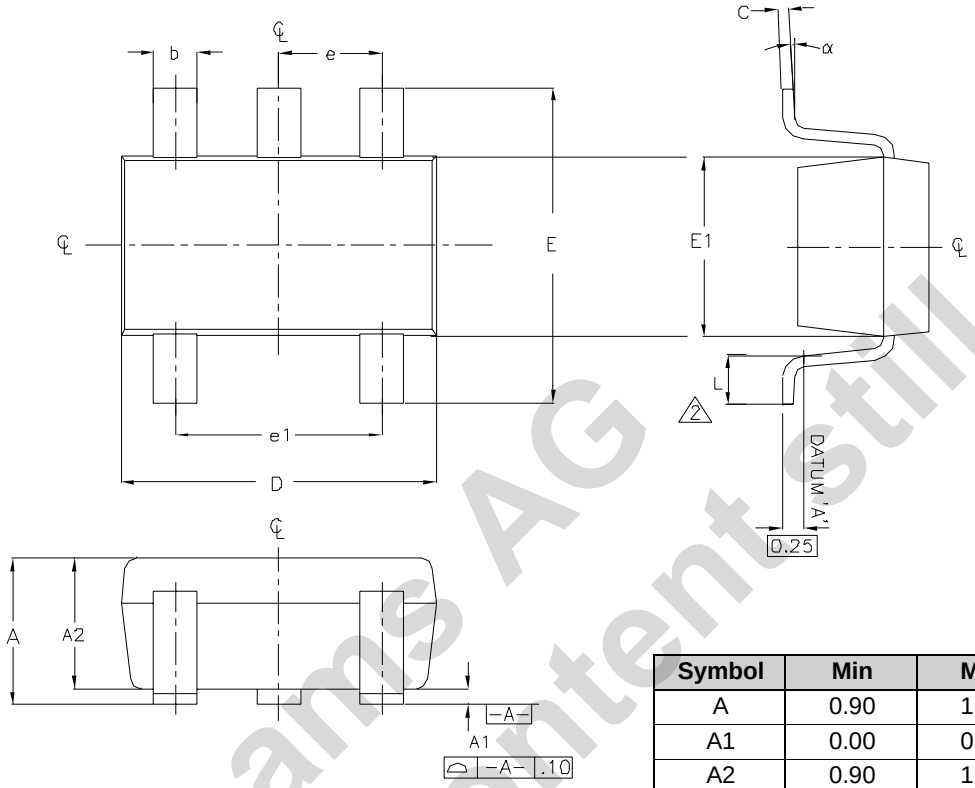
I_{OUT} is the supply current.

See Typical Operating Characteristics (page 6) for further information.

10 Package Drawings and Markings

The AS1353/AS1356 are available in a 5-pin SOT23 package.

Figure 14. 5-pin SOT23 Package



Notes:

1. All dimensions in millimeters.
2. Foot length measured at intercept point between datum A and lead surface.
3. Package outline exclusive of mold flash and metal burr.
4. Package outline inclusive of solder plating.
5. Complies with EIAJ SC74.
6. PKG ST 0003 Rev A supersedes SOT23-D-2005 Rev C.

Symbol	Min	Max
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.30	0.50
C	0.09	0.20
D	2.80	3.05
E	2.60	3.00
E1	1.50	1.75
L	0.30	0.55
e	0.95 REF	
e1	1.90 REF	
α	0º	8º

11 Ordering Information

The devices are available as the following standard products.

Type	Marking	Description	Delivery Form	Package
AS1353-15-T	ASD8	LDO 150mA, Reverse-Battery Protection, 1.5V	Tape and Reel	5-pin SOT23
AS1353-18-T	ASD9	LDO 150mA, Reverse-Battery Protection, 1.8V	Tape and Reel	5-pin SOT23
AS1353-26-T	ASHB	LDO 150mA, Reverse-Battery Protection, 2.6V	Tape and Reel	5-pin SOT23
AS1353-28-T	ASHC	LDO 150mA, Reverse-Battery Protection, 2.8V	Tape and Reel	5-pin SOT23
AS1353-30-T	ASHD	LDO 150mA, Reverse-Battery Protection, 3.0V	Tape and Reel	5-pin SOT23
AS1353-33-T	ASHE	LDO 150mA, Reverse-Battery Protection, 3.3V	Tape and Reel	5-pin SOT23
AS1353-36-T	ASI8	LDO 150mA, Reverse-Battery Protection, 3.6V	Tape and Reel	5-pin SOT23
AS1356-27-T	ASHM	LDO 150mA, Reverse-Battery Protection,with Power-OK, 2.7V	Tape and Reel	5-pin SOT23
AS1356-33-T	ASHO	LDO 150mA, Reverse-Battery Protection,with Power-OK, 3.3V	Tape and Reel	5-pin SOT23

Non-standard versions are available with a minimum order of 30,000 units. Contact austriamicrosystems for availability of non-standard versions.

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