AS1358 / AS1359

150mA/300mA, Ultra-Low-Noise, High-PSRR Low Dropout Regulators

1 General Description

The AS1358 / AS1359 are ultra-low-noise, low-dropout linear regulators specifically designed to deliver up to 150/300mA continuous output current, and can achieve a low 140mV dropout for 300mA load current. The LDOs are designed and optimized to work with low-cost, small-capacitance ceramic capacitors.

The devices are available as the standard products listed in Table 1.

Table 1. Standard Products

Model	Load Current	Output Voltage
AS1358	150mA	Preset – 1.5V to 4.5V
AS1359	300mA	Preset – 1.5V to 4.5V

An integrated P-channel MOSFET pass transistor allows the devices to maintain extremely low quiescent current (40µA).

The AS1358 / AS1359 uses an advanced architecture to achieve ultra-low output voltage noise of 9µVRMS and a power-supply rejection-ratio of better than 80dB (up to 10kHz).

The AS1358 / AS1359 requires only 1µF output capacitor for stability at any load. When the LDO is disabled, current consumption drops below 500nA.

The devices are available in a TSOT23 5-pin package.

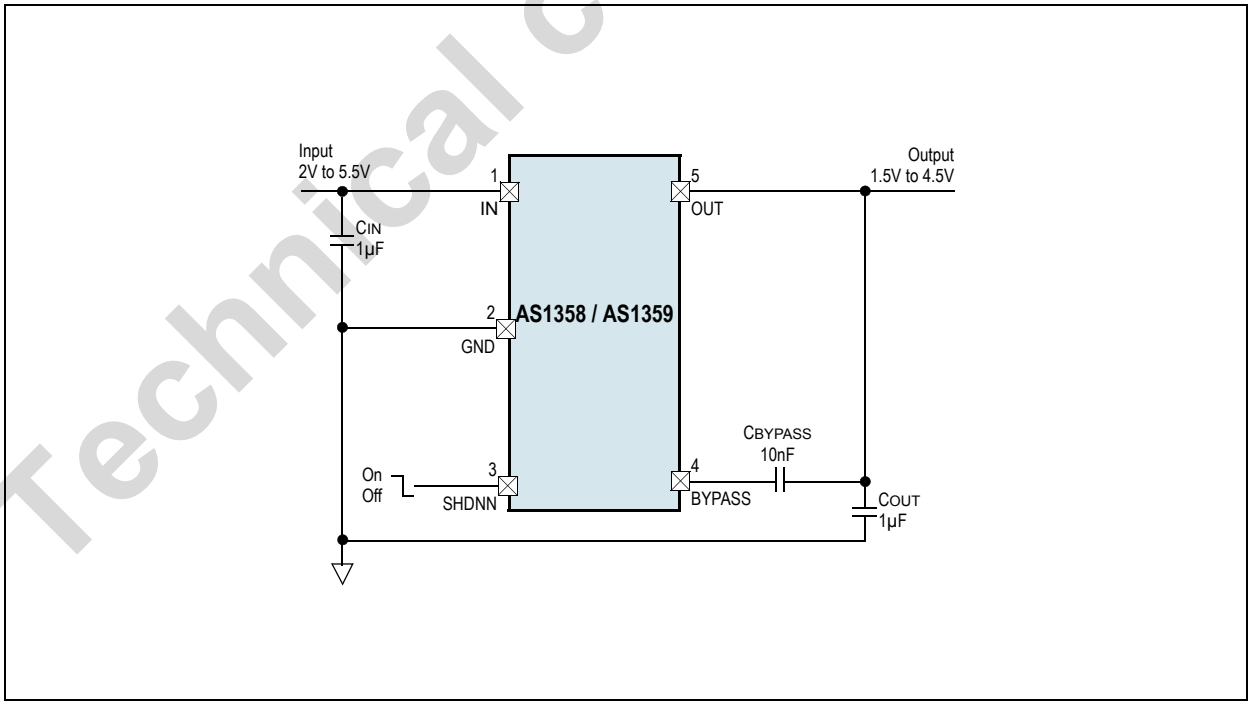
2 Key Features

- Preset Output Voltages: 1.5V to 4.5V (in 50mV steps)
- Output Noise: 9µVRMS @ 100Hz to 100kHz
- Power-Supply Rejection Ratio: 92dB @ 1kHz
- Low Dropout: 140mV @ 300mA Load
- Stable with 1µF Ceramic Capacitor for any Load
- Guaranteed 150mA / 300mA Output
- 1.25V Internal Reference
- Extremely-Low Quiescent Current: 40µA
- Excellent Load/Line Transient
- Overcurrent and Thermal Protection
- TSOT23 5-pin Package

3 Applications

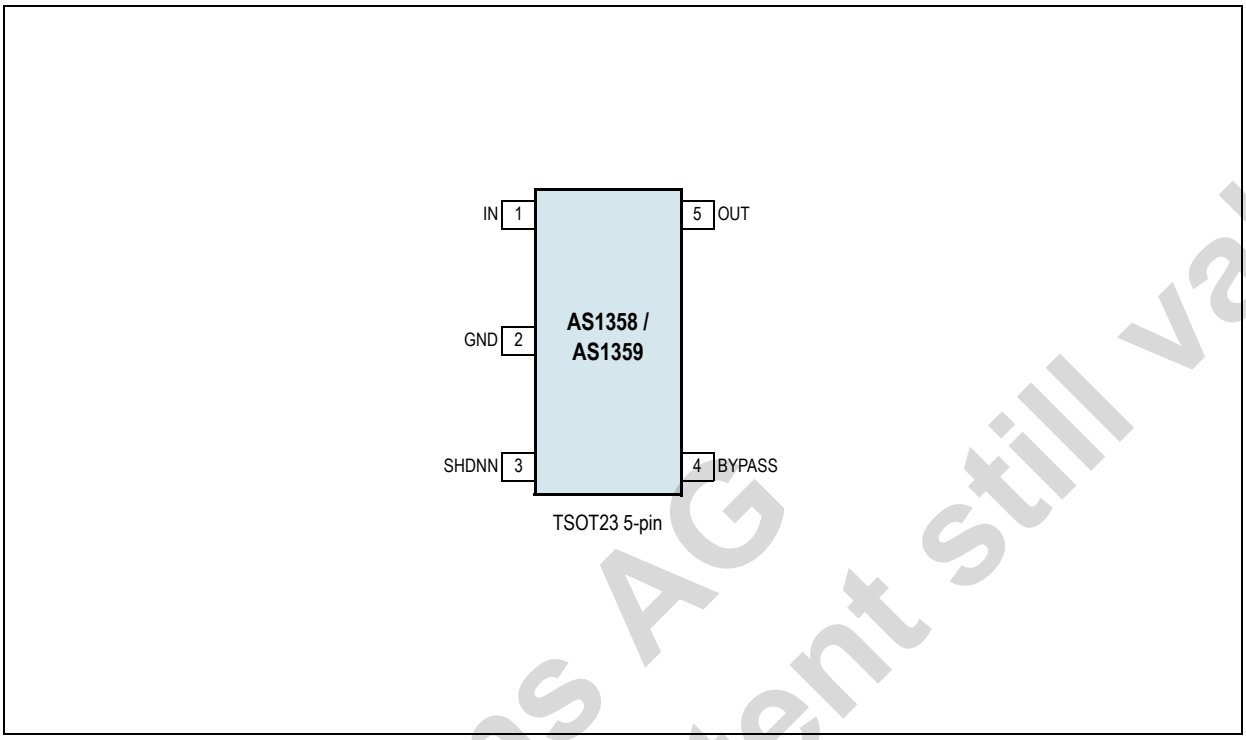
The devices are ideal for mobile phones, wireless phones, PDAs, handheld computers, mobile phone base stations, Bluetooth portable radios and accessories, wireless LANs, digital cameras, personal audio devices, and any other portable, battery-powered application.

Figure 1. Typical Application Circuit



4 Pin Assignments

Figure 2. Pin Assignments (Top View)



4.1 Pin Descriptions

Table 2. Pin Descriptions

Pin Number	Pin Name	Description
1	IN	**Unregulated Input Supply.**
2	GND	**Ground.** Provides the electrical connection to system ground and also serves as a heat sink. Connect pin GND to the system ground using a large pad or ground plane.
3	SHDNN	**Shutdown.** Pull this pin low to disable the LDO.
4	BYPASS	**Noise Bypass for Low-Noise Operation.** Connect a 10nF capacitor from this pin to **OUT**. **Note:** This pin is shorted to GND in shutdown mode.
5	OUT	**Regulated Output Voltage.** Bypass this pin with a capacitor to GND.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 3 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
IN to GND	-0.3	+7	V	
OUT, SHDNN to GND	-0.3	IN +0.3	V	
BYPASS to GND	-0.3	OUT +0.3	V	
Output Short-Circuit Duration		Infinite		
Thermal Resistance ΘJA		201.7	ºC/W	Junction-to-ambient thermal resistance is very dependent on application and board-layout. In situations where high maximum power dissipation exists, special attention must be paid to thermal dissipation during board design.
Operating Temperature Range	-40	+85	ºC	
Junction Temperature		+125	ºC	
Storage Temperature Range	-65	+150	ºC	
Package Body Temperature		+260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020D "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).

6 Electrical Characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed by production tests or SQC (Statistical Quality Control) methods.

V_{IN} = V_{OUT} +0.5V, C_{IN} = 1µF, C_{OUT} = 1µF, C_{BYPASS} = 10nF, T_{AMB} = -40 to +85ºC (unless otherwise specified).
Typical values are at T_{AMB} = +25ºC.

Table 4. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IN}	Input Voltage Range		2		5.5	V
	Output Voltage Accuracy	I_{OUT} = 1mA, T_{AMB} = +25ºC	-0.5		+0.5	%
		I_{OUT} = 100µA to 150mA, T_{AMB} = +25ºC (AS1358)	-0.75		+0.75	
		I_{OUT} = 100µA to 300mA, T_{AMB} = +25ºC (AS1359)	-1.0		+1.0	
		I_{OUT} = 100µA to 150mA, (AS1358)	-1.5		+1.5	
		I_{OUT} = 100µA to 300mA, (AS1359)	-2.0		+2.0	
I_{OUT}	Maximum Output Current	AS1358	150			mA
		AS1359	300			
I_{LIMIT}	Current Limit	AS1358, OUT = 90% of nom., T_{AMB} = +25ºC		270		mA
		AS1359, OUT = 90% of nom., T_{AMB} = +25ºC		510		
	Dropout Voltage [1]	$V_{OUT} \geq$ 3V, I_{OUT} = 150mA		70	95	mV
		$V_{OUT} \geq$ 3V, I_{OUT} = 300mA, (AS1359 only)		140	200	
		2.5V $\leq V_{OUT} <$ 3V, I_{OUT} = 150mA		90	120	
		2.5V $\leq V_{OUT} <$ 3V, I_{OUT} = 300mA, (AS1359 only)		170	230	
		2.0V $\leq V_{OUT} <$ 2.5V, I_{OUT} = 150mA		140	190	
		2.0V $\leq V_{OUT} <$ 2.5V, I_{OUT} = 300mA, (AS1359 only)		270	350	
I_Q	Quiescent Current	I_{OUT} = 0.05mA		40	90	µA
		$V_{IN} = V_{OUTNOM}$ - 0.1V, I_{OUT} = 0mA		150	250	
V_{LNR}	Line Regulation	V_{IN} = (V_{OUT} +0.5V) to 5.5V, I_{OUT} = 0.1mA		0.02		%/V
V_{LDR}	Load Regulation	I_{OUT} = 1 to 150mA / 300mA		0.0005		%/mA
I_{SHDNN}	Shutdown Supply Current	SHDNN = 0V		9	500	nA
PSRR	Ripple Rejection	f = 1kHz, I_{OUT} = 10mA		92		dB
		f = 10kHz, I_{OUT} = 10mA		80		
		f = 100kHz, I_{OUT} = 10mA		62		
	Output Noise Voltage (RMS)	f = 100Hz to 100kHz, I_{LOAD} = 0 to 150mA / 300mA		9		µV
Shutdown						
	Shutdown Exit Delay [2]	R_{LOAD} = 50Ω			300	µs
	SHDNN Logic Low Level	V_{IN} = 2V to 5.5V			0.4	V
	SHDNN Logic High Level	V_{IN} = 2V to 5.5V	1.5			V
Thermal Protection						
T_{SHDNM}	Thermal Shutdown Temperature			160		ºC
ΔT_{SHDNM}	Thermal Shutdown Hysteresis			15		ºC

1. Dropout is defined as V_{IN} - V_{OUT} when V_{OUT} is 100mV below the value of V_{OUT} for V_{IN} = V_{OUT} + 0.5V
2. Time needed for V_{OUT} to reach 90% of final value

7 Typical Operating Characteristics

V_{IN} = V_{OUT} + 0.5V, C_{IN} = C_{OUT} = 1µF, C_{BYPASS} = 10nF, T_{AMB} = 25°C (unless otherwise specified).

Figure 3. Output Voltage vs. Input Voltage

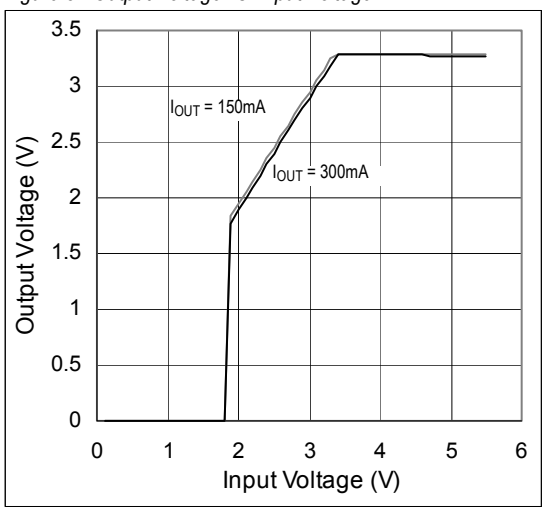


Figure 4. Output Voltage Accuracy vs. Load Current

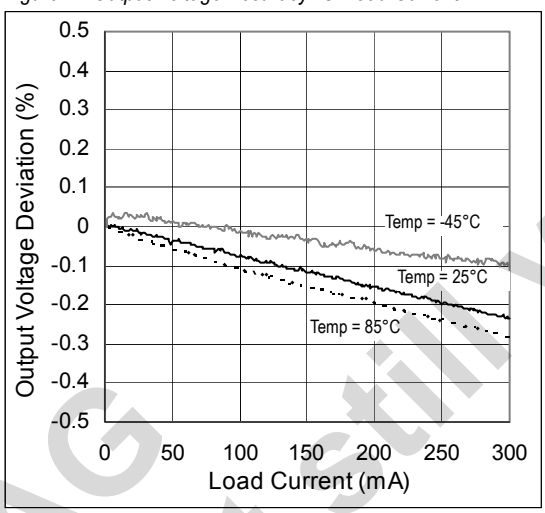


Figure 5. Output Voltage Accuracy vs. Temperature

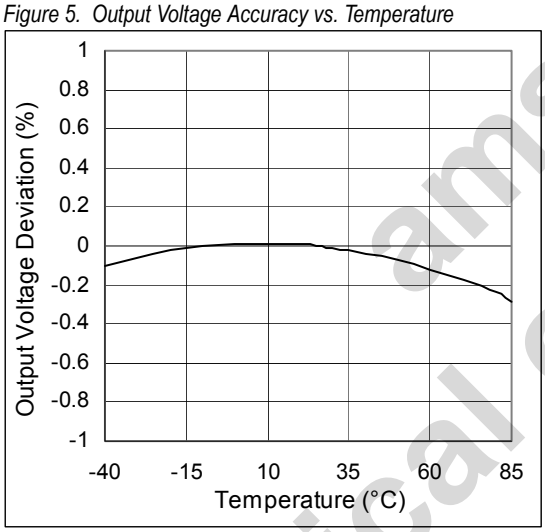


Figure 6. Dropout Voltage vs. Load Current

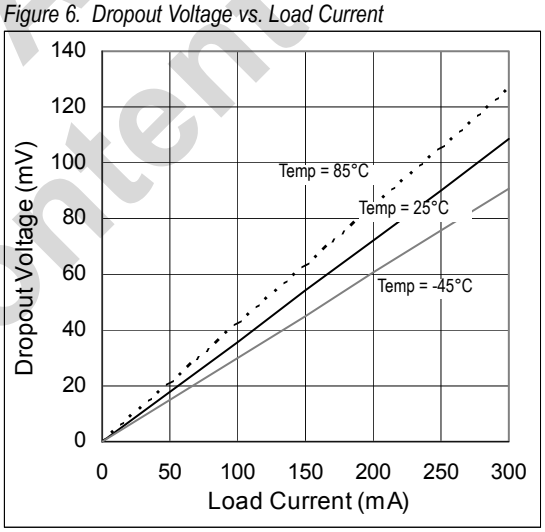


Figure 7. Dropout Voltage vs. Output Voltage

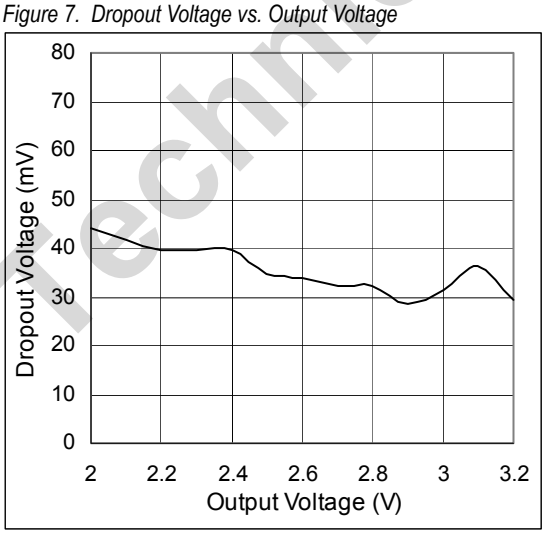


Figure 8. Ground Pin Current vs. Input Voltage

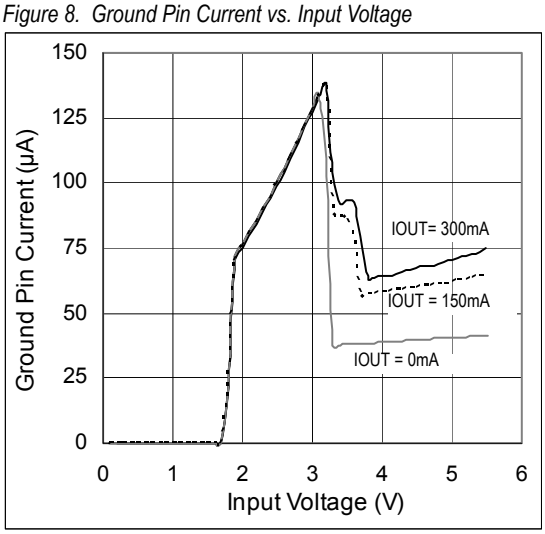


Figure 9. Ground Pin Current vs. Load Current

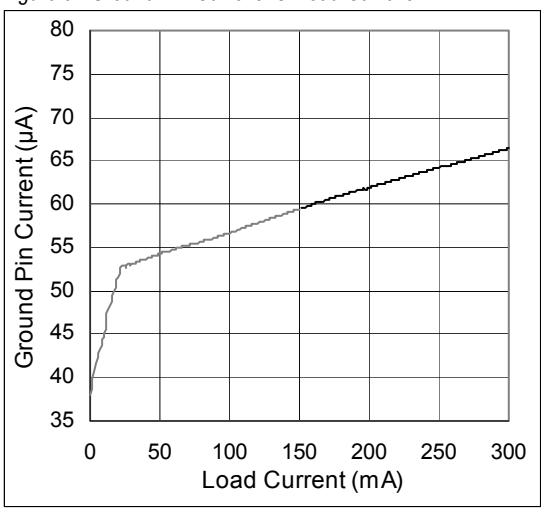


Figure 10. Ground Pin Current vs. Temperature

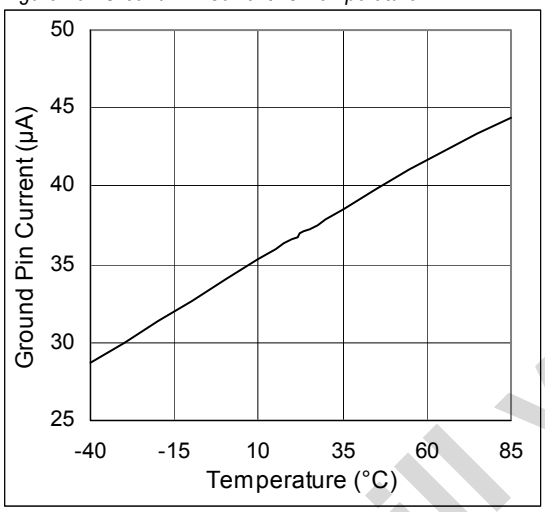


Figure 11. PSRR vs. Frequency; I_{OUT} = 10mA

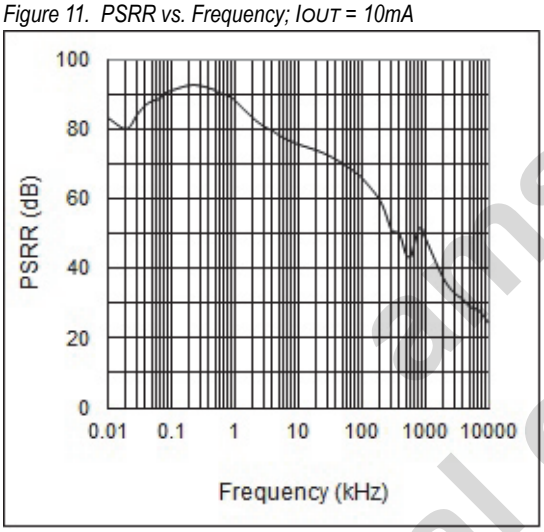


Figure 12. Output Noise Spectral Density vs. Frequency

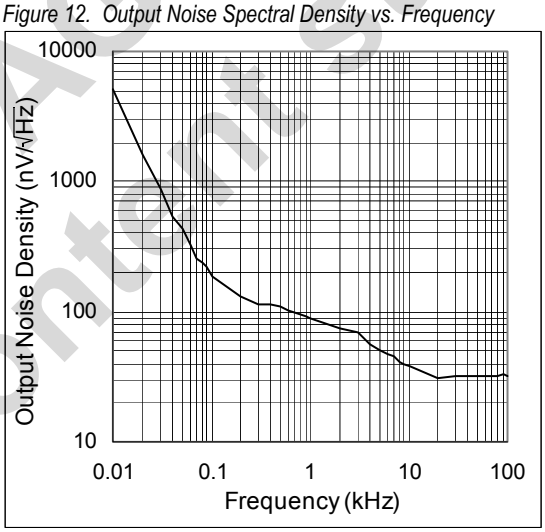


Figure 13. Output Noise vs. Bypass Capacitance

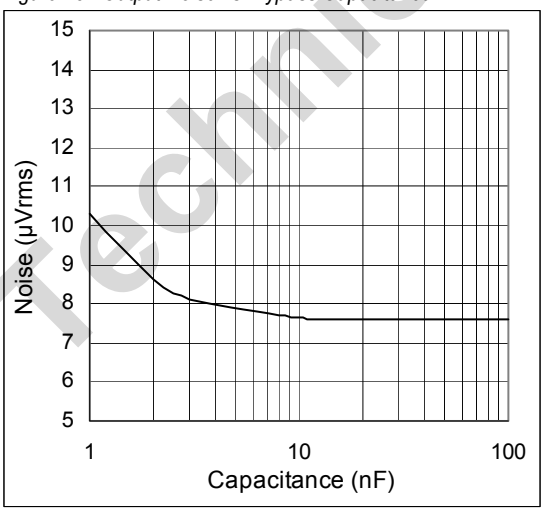


Figure 14. Load Transient Response, V_{IN} = 3.8V, V_{OUT} = 3.3V

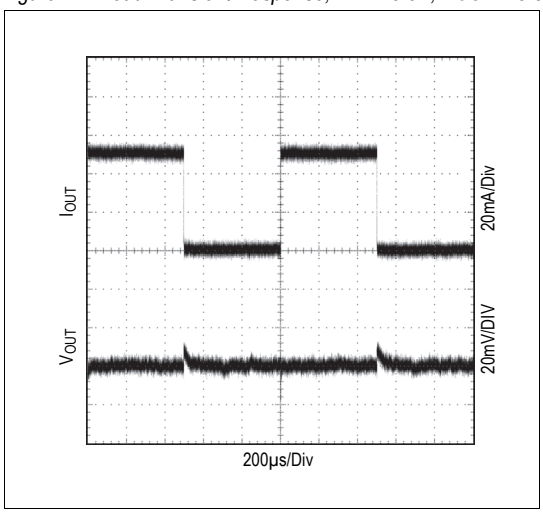


Figure 15. Load Transient Response near Dropout, V_{IN} = 3.4V, V_{OUT} = 3.3V

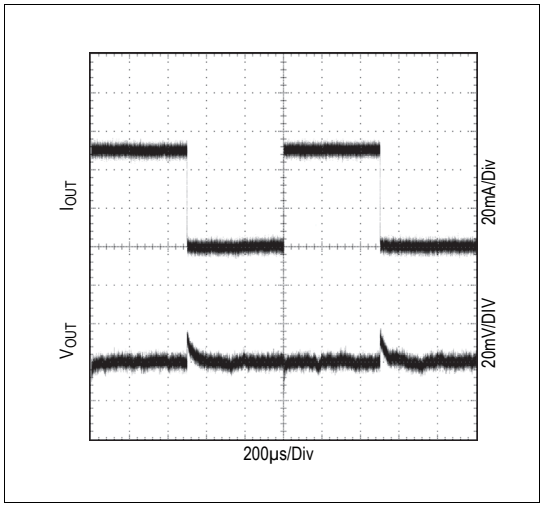


Figure 16. Line Transient Response

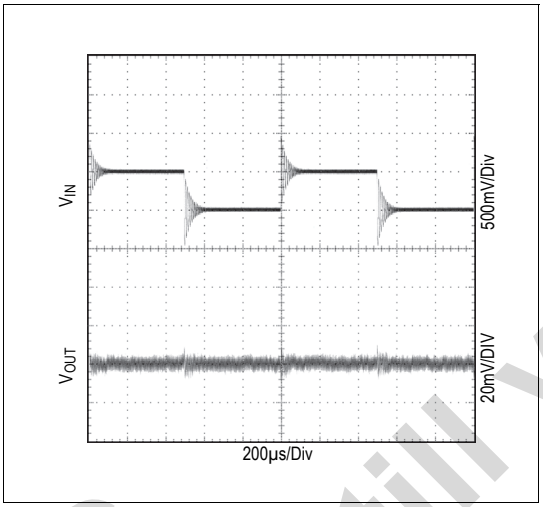
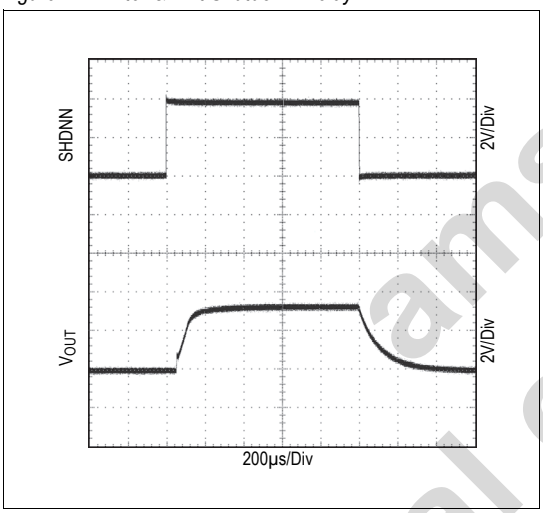


Figure 17. Enter & Exit Shutdown Delay



8 Detailed Description

The AS1358 / AS1359 are ultra-low-noise, low-dropout, low-quiescent current linear-regulators specifically designed for space-limited applications. The devices are available with preset output voltages from 1.5V to 4.5V in 50mV increments.

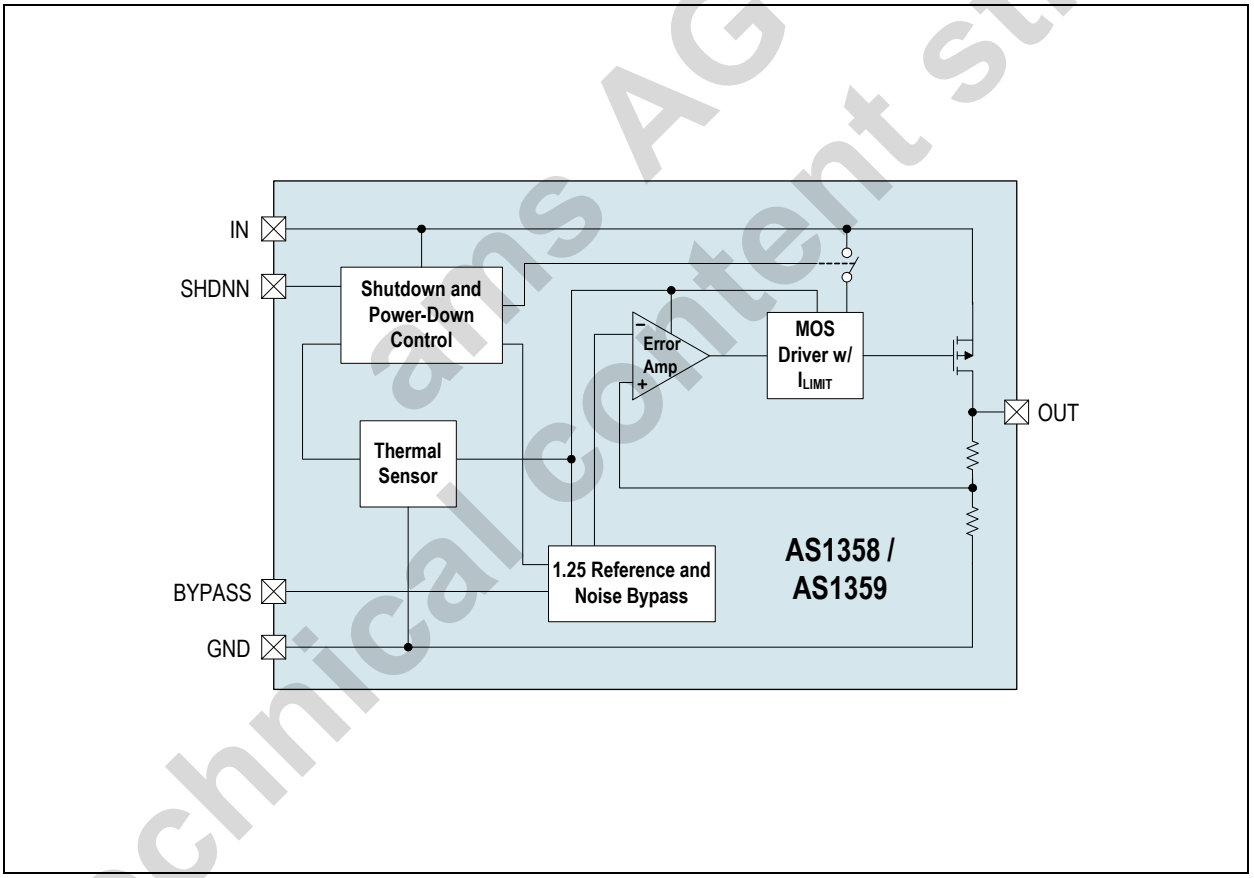
These devices can supply loads up to 150mA / 300mA. As shown in Figure 18, the AS1358 / AS1359 consist of an integrated bandgap core and noise bypass circuitry, error amplifier, P-channel MOSFET pass transistor, and internal feedback voltage-divider.

Figure 18 shows the block diagram of the AS1358 / AS1359. It identifies the basics of a series linear regulator employing a 0.5Ω (typ) P-Channel MOSFET as the control element. A stable voltage reference (REF in Figure 18) is compared with an attenuated sample of the output voltage. Any difference between the two voltages (reference and sample) creates an output from the error amplifier that drives the series control element to reduce the difference to a minimum. The error amplifier incorporates additional buffering to drive the relatively large gate capacitance of the series pass P-channel MOSFET, when additional drive current is required under transient conditions. Input supply variations are absorbed by the series element and output voltage variations with loading are absorbed by the low output impedance of the regulator.

The AS1358 / AS1359 deliver preset output voltages from 1.5V to 4.5V, in 50mV increments (see Ordering Information on page 15).

The output voltage is fed back through an internal resistor voltage-divider connected to pin OUT. An external bypass capacitor connected to pin BYPASS reduces noise at the output. Startup time is minimized by internal power-on circuitry which pre-charges C_{BYPASS}. Additional blocks include a current limiter, thermal sensor, and shutdown logic.

Figure 18. AS1358 / AS1359 Block Diagram



9 Application Information

9.1 Dropout Voltage

Dropout is the input to output voltage difference, below which the linear regulator ceases to regulate. At this point, the output voltage change follows the input voltage change. Dropout voltage may be measured at different currents and, in particular at the regulator maximum one. From this is obtained the MOSFET maximum series resistance over temperature etc. More generally:

$$V_{DROPOUT} = I_{LOAD} \times R_{SERIES} \quad \text{(EQ 1)}$$

Dropout is probably the most important specification when the regulator is used in a battery application. The dropout performance of the regulator defines the useful “end of life” of the battery before replacement or re-charge is required.

Figure 19. Graphical Representation of Dropout Voltage

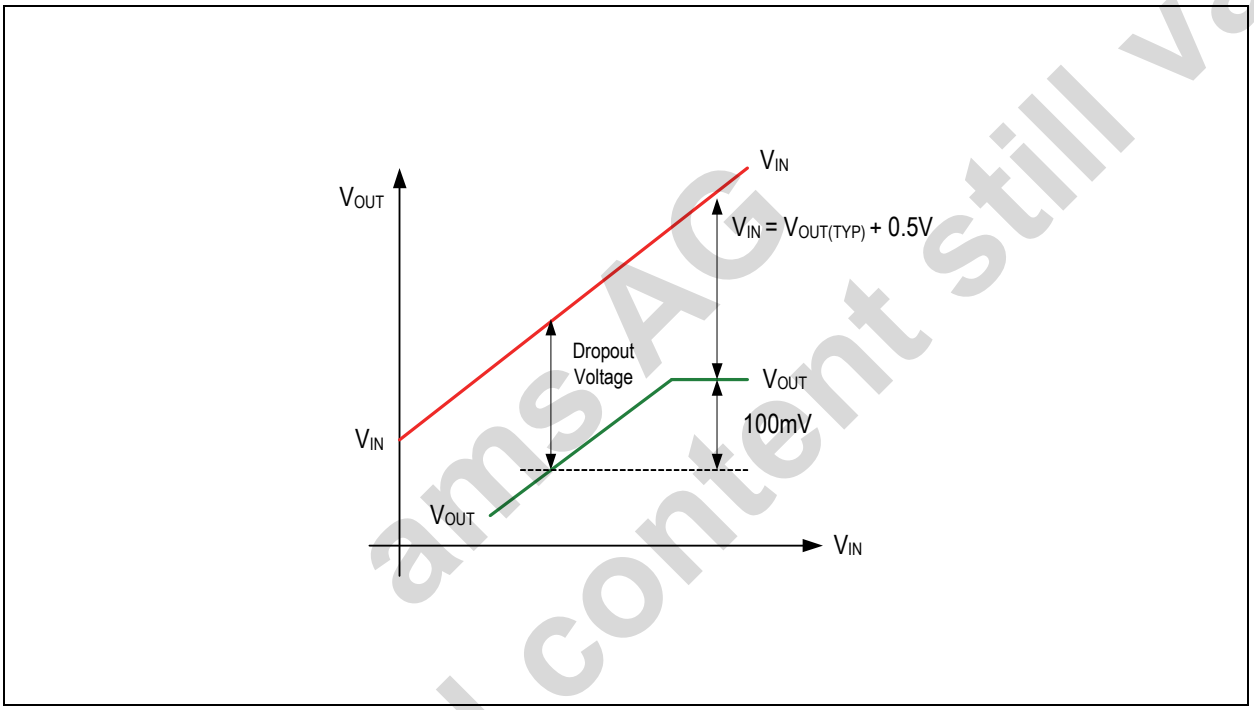


Figure 19 shows the variation of VOUT as VIN is varied for a certain load current. The practical value of dropout is the differential voltage (VOUT-VIN) measured at the point where the LDO output voltage has fallen by 100mV below the nominal, fully regulated output value. The nominal regulated output voltage of the LDO is that obtained when there is 500mV (or greater) input-output voltage differential.

9.2 Efficiency

Low quiescent current and low input-output voltage differential are important in battery applications amongst others, as the regulator efficiency is directly related to quiescent current and dropout voltage. Efficiency is given by:

$$\textit{Efficiency} = \frac{V_{LOAD} \times I_{LOAD}}{V_{IN}(I_Q + I_{LOAD})} \times 100\ \% \quad \text{(EQ 2)}$$

Where:
I_Q = Quiescent current of LDO

9.3 Power Dissipation

Maximum power dissipation (PD) of the LDO is the sum of the power dissipated by the internal series MOSFET and the quiescent current required to bias the internal voltage reference and the internal error amplifier, and is calculated as:

$$PD_{(MAX)}(Seriespass) = I_{LOAD(MAX)}(V_{IN(MAX)} - V_{OUT(MIN)}) \ Watts \quad (EQ\ 3)$$

Internal power dissipation as a result of the bias current for the internal voltage reference and the error amplifier is calculated as:

$$PD_{(MAX)}(Bias) = V_{IN(MAX)}I_Q \ Watts \quad (EQ\ 4)$$

Total LDO power dissipation is calculated as:

$$PD_{(MAX)}(Total) = PD_{(MAX)}(Seriespass) + PD_{(MAX)}(Bias) \ Watts \quad (EQ\ 5)$$

9.4 Junction Temperature

Under all operating conditions, the maximum junction temperature should not be allowed to exceed 125ºC (unless the data sheet specifically allows). Limiting the maximum junction temperature requires knowledge of the heat path from junction to case (θ_{JC}ºC/W fixed by the IC manufacturer), and adjustment of the case to ambient heat path (θ_{CA}ºC/W) by manipulation of the PCB copper area adjacent to the IC position.

Figure 20. Package Physical Arrangements

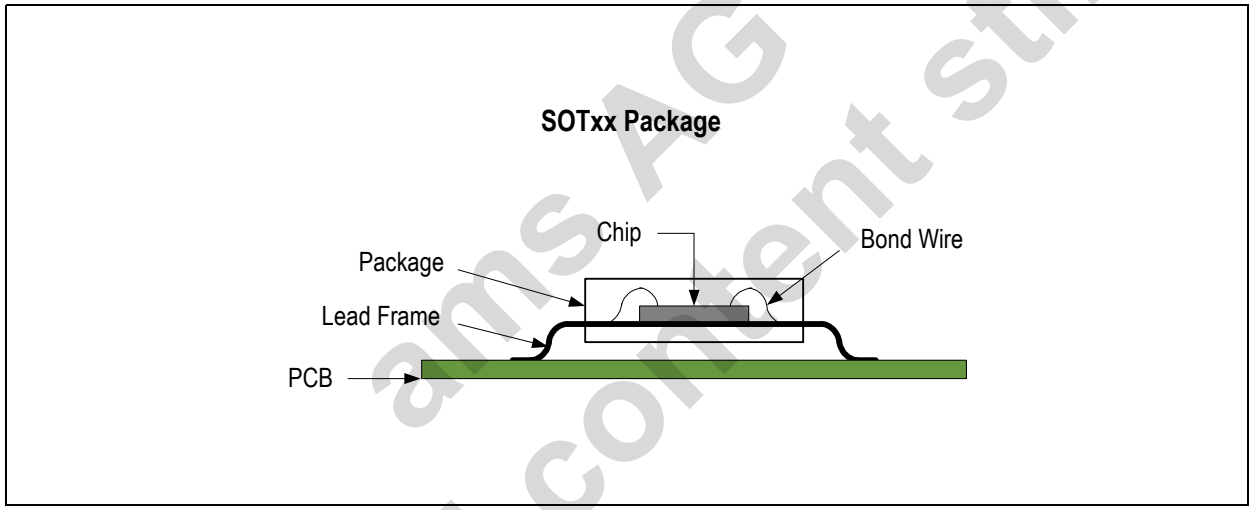
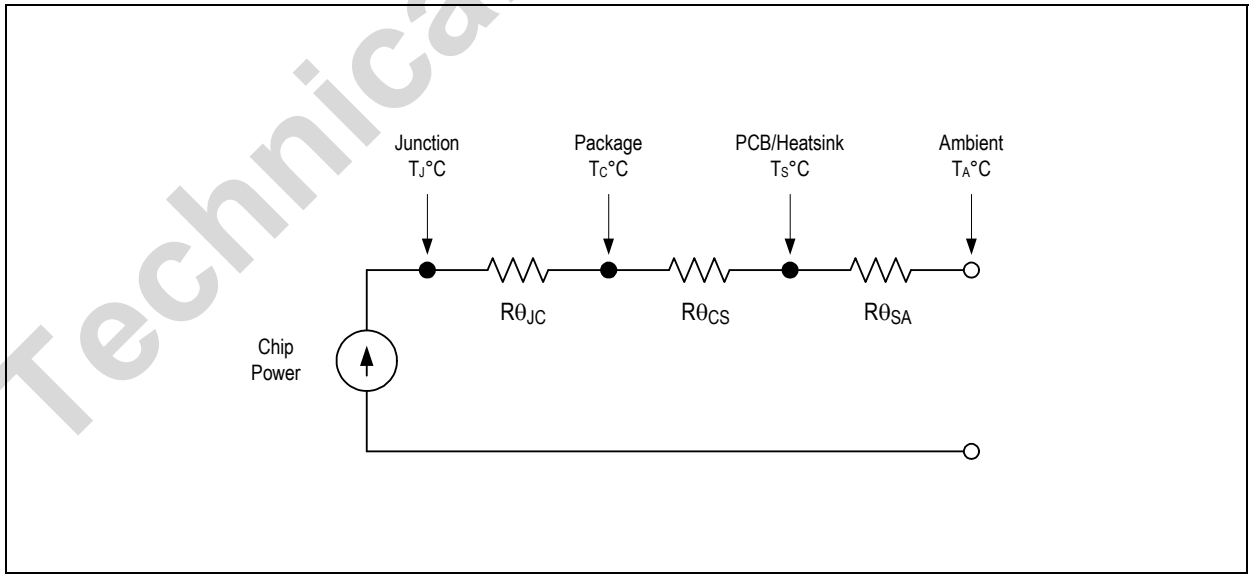


Figure 21. Steady State Heat Flow Equivalent Circuit



Total Thermal Path Resistance:

$$R\theta_{JA} = R\theta_{JC} + R\theta_{CS} + R\theta_{SA} \quad \text{(EQ 6)}$$

Junction Temperature (T_JºC) is determined by:

$$T_J = (PD_{(MAX)} \times R\theta_{JA}) + T_{AMB} \ ºC \quad \text{(EQ 7)}$$

9.5 Explanation of Steady State Specifications

9.5.1 Line Regulation

Line regulation is defined as the change in output voltage when the input (or line) voltage is changed by a known quantity. It is a measure of the regulator's ability to maintain a constant output voltage when the input voltage changes. Line regulation is a measure of the DC open loop gain of the error amplifier. More generally:

$$\text{Line Regulation} = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \text{ and is a pure number} \quad \text{(EQ 8)}$$

In practise, line regulation is referred to the regulator output voltage in terms of % / VOUT. This is particularly useful when the same regulator is available with numerous output voltage trim options.

$$\text{Line Regulation} = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \times \frac{100}{V_{OUT}} \text{ \% / V} \quad \text{(EQ 9)}$$

9.5.2 Load Regulation

Load regulation is defined as the change of the output voltage when the load current is changed by a known quantity. It is a measure of the regulator's ability to maintain a constant output voltage when the load changes. Load regulation is a measure of the DC closed loop output resistance of the regulator. More generally:

$$\text{Load Regulation} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \text{ and is units of ohms } (\Omega) \quad \text{(EQ 10)}$$

In practise, load regulation is referred to the regulator output voltage in terms of % / mA. This is particularly useful when the same regulator is available with numerous output voltage trim options.

$$\text{Load Regulation} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \times \frac{100}{\Delta V_{OUT}} \text{ \% / mA} \quad \text{(EQ 11)}$$

9.5.3 Setting Accuracy

The regulator is supplied pre-trimmed, so that the output voltage accuracy is fully defined in the output voltage specification.

9.5.4 Total Accuracy

Away from dropout, total steady state accuracy is the sum of setting accuracy, load regulation and line regulation. Generally:

$$\text{Total \% Accuracy} = \text{Setting \% Accuracy} + \text{Load Regulation \%} + \text{Line Regulation \%} \quad \text{(EQ 12)}$$

9.6 Explanation of Dynamic Specifications

9.6.1 Power Supply Rejection Ratio (PSRR)

Known also as Ripple Rejection, this specification measures the ability of the regulator to reject noise and ripple beyond DC. PSRR is a summation of the individual rejections of the error amplifier, reference and AC leakage through the series pass transistor. The specification, in the form of a typical attenuation plot with respect to frequency, shows up the gain bandwidth compromises forced upon the designer in low quiescent current conditions. Generally:

$$PSSR = 20Log\frac{\delta V_{OUT}}{\delta V_{IN}} \text{ dB using lower case } \delta \text{ to indicate AC values} \quad \text{(EQ 13)}$$

Power supply rejection ratio is fixed by the internal design of the regulator. Additional rejection must be provided externally.

9.6.2 Output Capacitor ESR

The series regulator is a negative feedback amplifier, and as such is conditionally stable. The ESR of the output capacitor is usually used to cancel one of the open loop poles of the error amplifier in order to produce a single pole response. Excessive ESR values may actually cause instability by excessive changes to the closed loop unity gain frequency crossover point. The range of ESR values for stability is usually shown either by a plot of stable ESR versus load current, or a limit statement in the datasheet.

Some ceramic capacitors exhibit large capacitance and ESR variations with temperature. Z5U and Y5V capacitors may be required to ensure stability at temperatures below T_{AMB} = -10ºC. With X7R or X5R capacitors, a 1.0µF capacitor should be sufficient at all operating temperatures.

Larger output capacitor values (2.2µF max) help to reduce noise and improve load transient-response, stability and power-supply rejection.

9.6.3 Input Capacitor

An input capacitor at V_{IN} is required for stability. It is recommended that a 1.0µF capacitor be connected between the AS1358 / AS1359 power supply input pin V_{IN} and ground (capacitance value may be increased without limit subject to ESR limits). This capacitor must be located at a distance of not more than 1cm from the V_{IN} pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

9.6.4 Noise

The regulator output is a DC voltage with noise superimposed on the output. The noise comes from three sources; the reference, the error amplifier input stage, and the output voltage setting resistors. Noise is a random fluctuation and if not minimized in some applications, will produce system problems. The AS1358/9 architecture provides enhance noise reduction when an external 10nF capacitor is connected between Bypass and Output pins, and 1µF connected as the output capacitor.

The leakage current going into the BYPASS pin should be less than 10nA. Increasing the capacitance slightly decreases the output noise. Values above 0.1µF and below 0.001µF are not recommended.

9.6.5 Transient Response

The series regulator is a negative feedback system, and therefore any change at the output will take a finite time to be corrected by the error loop. This “propagation time” is related to the bandwidth of the error loop. The initial response to an output transient comes from the output capacitance, and during this time, ESR is the dominant mechanism causing voltage transients at the output. More generally:

$$\delta V_{TRANSIENT} = \delta I_{OUTPUT} \times R_{ESR} \quad \textit{Units are Volts, Amps, Ohms.} \qquad \textit{(EQ 14)}$$

Thus an initial +50mA change of output current will produce a -12mV transient when the ESR=240mΩ. Remember to keep the ESR within stability recommendations when reducing ESR by adding multiple parallel output capacitors.

After the initial ESR transient, there follows a voltage droop during the time that the LDO feedback loop takes to respond to the output change. This drift is approximately linear in time and sums with the ESR contribution to make a total transient variation at the output of:

$$\delta V_{TRANSIENT} = \delta I_{OUTPUT} \times \left(R_{ESR} + \frac{T}{C_{LOAD}} \right) \quad \textit{Units are Volts, Seconds, Farads, Ohms.} \qquad \textit{(EQ 15)}$$

Where:
C_{LOAD} is output capacitor
T = Propagation delay of the LDO

This shows why it is convenient to increase the output capacitor value for a better support for fast load changes. Of course the formula holds for t < “propagation time”, so that a faster LDO needs a smaller cap at the load to achieve a similar transient response. For instance 50mA load current step produces 50mV output drop if the LDO response is 1usec and the load cap is 1µF.

There is also a steady state error caused by the finite output impedance of the regulator. This is derived from the load regulation specification discussed above.

9.6.6 Turn On Time

This specification defines the time taken for the LDO to awake from shutdown. The time is measured from the release of the enable pin to the time that the output voltage is within 5% of the final value. It assumes that the voltage at V_{IN} is stable and within the regulator Min and Max limits. Shutdown reduces the quiescent current to very low, mostly leakage values (<1µA).

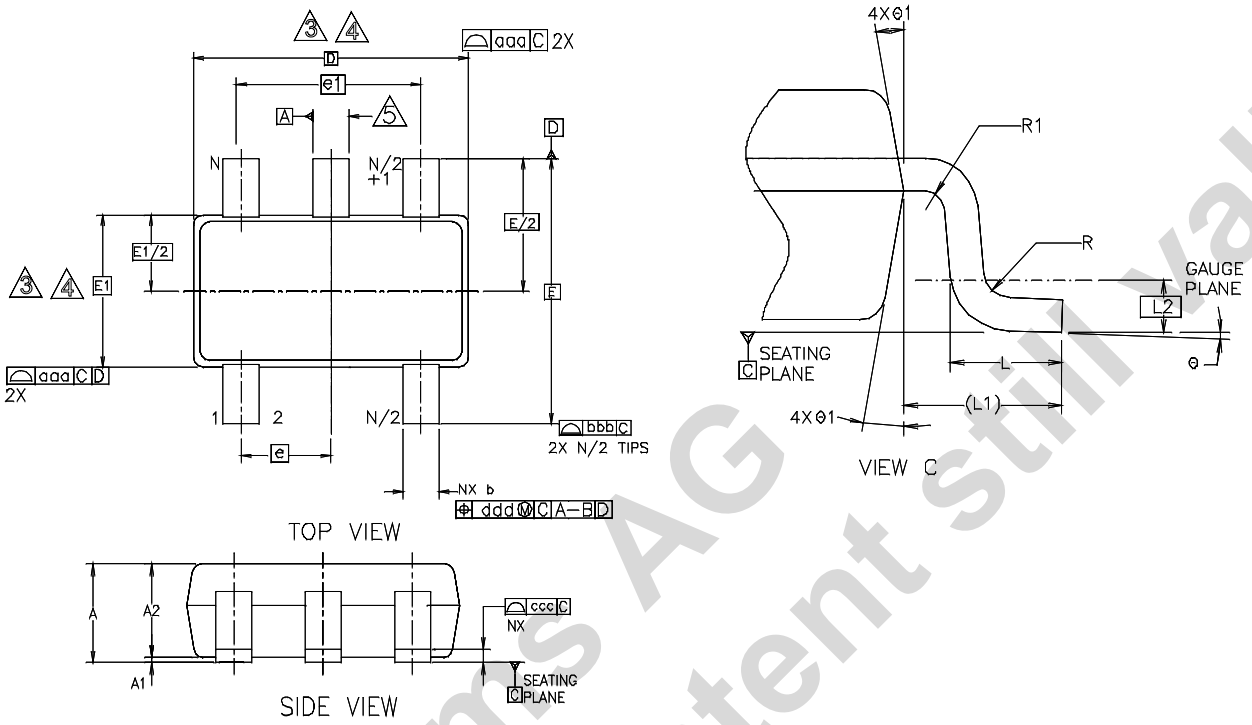
9.6.7 Thermal Protection

To prevent operation under extreme fault conditions, such as a permanent short circuit at the output, thermal protection is built into the device. Die temperature is measured, and when a 160ºC threshold is reached, the device enters shutdown. When the die cools sufficiently, the device will restart (assuming input voltage exists and the device is enabled). Hysteresis of 15ºC prevents low frequency oscillation between start-up and shutdown around the temperature threshold.

10 Package Drawings and Markings

The devices are available in a TSOT23 5-pin package.

Figure 22. TSOT23 5-pin Package



Symbol	Min	Typ	Max	Notes		Symbol	Min	Typ	Max	Notes
A			1.00			L	0.30	0.40	0.50	
A1	0.01	0.05	0.10			L1		0.60REF		
A2	0.84	0.87	0.90			L2		0.25BSC		
b	0.30		0.45			N		5		
b1	0.31	0.35	0.39			R	0.10			
c	0.12	0.15	0.20			R1	0.10		0.25	
c1	0.08	0.13	0.16			θ	0°	4°	8°	
D		2.90BSC		3,4		θ1	4°	10°	12°	
E		2.80BSC		3,4		**Tolerances of Form and Position**				
E1		1.60BSC		3,4		aaa		0.15		
e		0.95BSC				bbb		0.25		
e1		1.90BSC				ccc		0.10		
						ddd		0.20		

Notes:

1. Dimensioning and tolerancing conform to *ASME Y14.5M - 1994.*
2. Dimensions are in millimeters.
3. Dimension D does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0.15mm per end. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.15mm per side. Dimensions D and E1 are determined at datum H.
4. The package top can be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but include any mistmatches between the top of the package body and the bottom. D and E1 are determined at datum H.

Revision History

Revision	Date	Owner	Description
1.4	-	afe	Initial revisions
1.5	13 Jun, 2012		

Note: Typos may not be explicitly mentioned under revision history.

11 Ordering Information

The devices are available as the standard products shown in Table 5.

Table 5. Ordering Information

Ordering Code	Marking	Output Current	Output Voltage	Delivery Form	Package
AS1358-BTTT-15	ASLI	150mA	1.5V	Tape and Reel	TSOT23 5-pin
AS1358-BTTT-18	ASLJ	150mA	1.8V	Tape and Reel	TSOT23 5-pin
AS1358-BTTT-25	ASLK	150mA	2.5V	Tape and Reel	TSOT23 5-pin
AS1358-BTTT-26	ASLL	150mA	2.6V	Tape and Reel	TSOT23 5-pin
AS1358-BTTT-27	ASLM	150mA	2.7V	Tape and Reel	TSOT23 5-pin
AS1358-BTTT-28	ASLN	150mA	2.8V	Tape and Reel	TSOT23 5-pin
AS1358-BTTT-285	ASLO	150mA	2.85V	Tape and Reel	TSOT23 5-pin
AS1358-BTTT-30	ASLP	150mA	3.0V	Tape and Reel	TSOT23 5-pin
AS1358-BTTT-33	ASLQ	150mA	3.3V	Tape and Reel	TSOT23 5-pin
AS1358-BTTT-45	ASLR	150mA	4.5V	Tape and Reel	TSOT23 5-pin
AS1359-BTTT-15	ASLS	300mA	1.5V	Tape and Reel	TSOT23 5-pin
AS1359-BTTT-18	ASLT	300mA	1.8V	Tape and Reel	TSOT23 5-pin
AS1359-BTTT-25	ASLU	300mA	2.5V	Tape and Reel	TSOT23 5-pin
AS1359-BTTT-26	ASLV	300mA	2.6V	Tape and Reel	TSOT23 5-pin
AS1359-BTTT-27	ASLW	300mA	2.7V	Tape and Reel	TSOT23 5-pin
AS1359-BTTT-28	ASLX	300mA	2.8V	Tape and Reel	TSOT23 5-pin
AS1359-BTTT-285	ASLY	300mA	2.85V	Tape and Reel	TSOT23 5-pin
AS1359-BTTT-30	ASLZ	300mA	3.0V	Tape and Reel	TSOT23 5-pin
AS1359-BTTT-31	ASSA	300mA	3.1V	Tape and Reel	TSOT23 5-pin
AS1359-BTTT-33	ASL0	300mA	3.3V	Tape and Reel	TSOT23 5-pin
AS1359-BTTT-45	ASL1	300mA	4.5V	Tape and Reel	TSOT23 5-pin

Non-standard devices from 1.5V to 4.5V are available in 50mV steps. For more information and inquiries contact http://www.austriamicrosystems.com/contact

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