AS1701, AS1706

1.6W Audio Power Amplifiers

DataSheet

1 General Description

The AS1701 and AS1706 are 1.6W bridged audio power amplifiers that provide excellent circuit reliability, providing a very low-cost solution by eliminating external components when used with 2.7 to 5.5V-powered circuits.

The devices have superb total harmonic distortion (THD) at high-power output and excellent power supply rejection with 4- and 8Ω-loads.

Integrated over-temperature and over-current protection circuitry switch the devices off in case of an output short-circuit. A digital input allows the devices to automatically switch into shutdown mode. Click- and pop-suppression circuitry reduces audible clicks and pops during power-up and shutdown. The gain (A_V) of the devices is controlled using external resistors.

The AS1701/AS1706 are available in an 8-pin MSOP package.

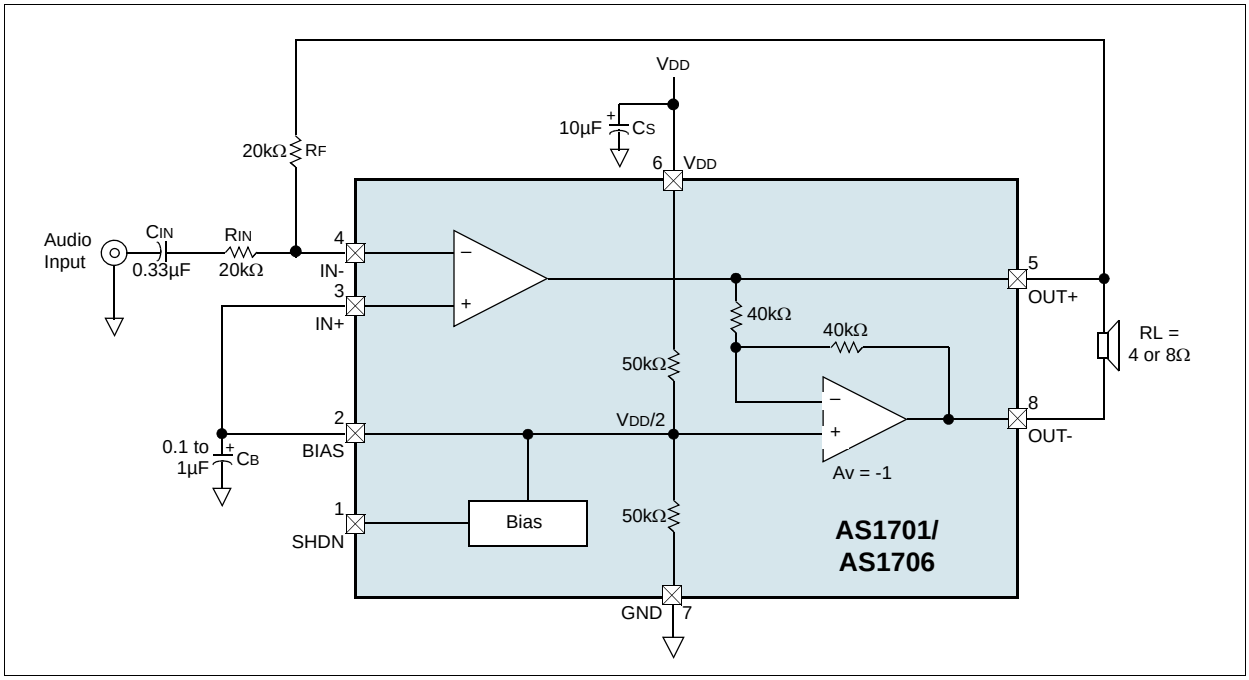
2 Key Features

- 2.7 to 5.5V (V_{DD}) Single-Supply Operation
- Very High PSRR: Greater Than 65dB @ 217Hz
- THD+Noise: 1.6W into 4Ω at 1%
- No Output Coupling Capacitors Required
- External Gain Configuration Capability
- Low-Power Shutdown Mode: 10nA
- Click and Pop Suppression
- Over-Temperature and Over-Current Protection
- Operating Temperature Range: -40 to +85°C
- 8-pin MSOP Package

3 Applications

The AS1701/AS1706 are ideal as audio front-ends for battery powered audio devices such as MP3 and CD players, mobile phones, PDAs, portable DVD players, and any other hand-held battery-powered device.

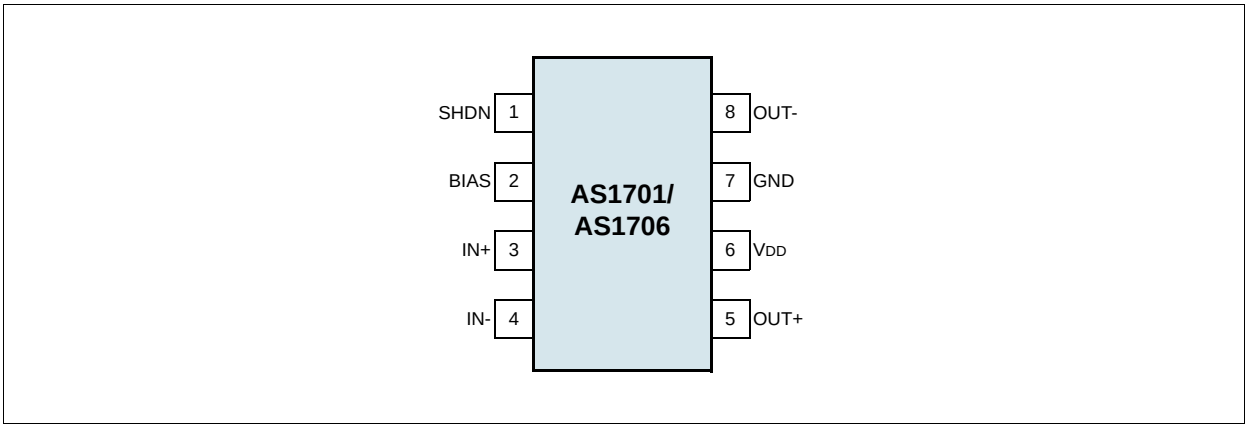
Figure 1. Typical Configuration Block Diagram



4 Pinout

Pin Assignments

Figure 2. Pin Assignment – 8-Pin MSOP Package (Top View)



Pin Descriptions

Table 1. Pin Descriptions

Pin	Name	Description
1	SHDN	**Shutdown**. Connect this pin to GND for the AS1701 (active-high); connect this pin to V_{DD} for the AS1706 (active-low).
2	BIAS	**DC Bias Bypass**
3	IN+	**Non-Inverting Input**
4	IN-	**Inverting Input**
5	OUT+	**Positive Differential Output**
6	V_{DD}	**Power Supply**
7	GND	**Ground**
8	OUT-	**Negative Differential Output**

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Unit	Comments
V_{DD} to GND	-0.3	+7	V	
Any Other Pin to GND	-0.3	V_{DD} + 0.3	V	
Input Current (Latchup Immunity)	-100	100	mA	*JEDEC 78*
Continuous Power Dissipation		362	mW	T_{AMB} = 70ºC, Derate 4.5mW/ºC Above +70ºC
Electro-Static Discharge (ESD)		1	kV	*HBM MIL-Std883E 3015.7 Methods*
Operating Temperature Range (T_{AMB})	-40	+85	ºC	
Storage Temperature Range	-65	+150	ºC	
Soldering Conditions		+260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".*

6 Electrical Characteristics

All specifications are 100% tested at T_{AMB} = +25ºC.

5V Operation

V_{DD} = 5V, R_L = ∞, C_{BIAS} = 0.1µF to GND, SHDN = GND, T_{AMB} +25ºC (unless otherwise specified).

Table 3. DC Electrical Characteristics – 5V Operation

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Supply Voltage Range	V_{DD}	Inferred from PSRR Test		2.7		5.5	V
Supply Current [1]	I_{DD}	T_{AMB} = -40 to +85ºC			6.8	10.4	mA
Shutdown Supply Current	I_{SHDN}	SHDN = V_{DD}			0.01	1	µA
SHDN Threshold		V_{IH}		V_{DD} x 0.7			V
		V_{IL}				V_{DD} x 0.3	
Common-Mode Bias Voltage [2]	VBIAS			V_{DD}/2 - 5%	V_{DD}/2	V_{DD}/2 + 5%	V
Output Offset Voltage	V_{OS}	Av = 2, IN- = OUT+, IN- = BIAS			±1	±10	mV
Power Supply Rejection Ratio	PSRR	Inputs Grounded, V_{RIPPLE} = 200mVp-p, R_L = 4Ω, V_{IN-} = V_{IN+} = V_{BIAS}	217Hz		65		dB
			1kHz		63		
Output Power [3]	P_{OUT}	R_L = 4Ω, THD+N = 1%, f_{IN} = 1kHz			1.6		W
		R_L = 8Ω, THD+N = 1%, f_{IN} = 1kHz		0.8	1.2		
Total Harmonic Distortion+Noise	THD+N	A_V = 2, R_L = 4Ω, f_{IN} = 1kHz, P_{OUT} = 1.3W			0.09		%
		A_V = 2, R_L = 8Ω, f_{IN} = 1kHz, P_{OUT} = 1W			0.05		
Thermal-Shutdown Threshold					145		ºC
Thermal-Shutdown Hysteresis					9		ºC
Power-Up/Enable from Shutdown Time	t_{PU}				150		ms
Shutdown Time	t_{SHDN}				1		µs
Turn-Off Transient	V_{POP}				20		mV

1. Quiescent power supply current is specified and tested without loads on the outputs. Quiescent power supply current depends on the offset voltage when a practical load is connected to the device.
2. Common-mode bias voltage is the voltage on pin BIAS and is nominally V_{DD}/2.
3. Guaranteed by design.

3V Operation

V_{DD} = 3V, R_L = ∞, C_{BIAS} = 0.1µF to GND, SHDN = GND, T_{AMB} +25ºC (unless otherwise specified).

Table 4. DC Electrical Characteristics – 3V Operation

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Supply Current [1]	I_{DD}	T_{AMB} = -40 to +85ºC			6	10	mA
Shutdown Supply Current	I_{SHDN}	SHDN = V_{DD}			0.01	1	µA
Output Power [2]	P_{OUT}	R_L = 4Ω, THD+N = 1%, f_{IN} = 1kHz			0.6		W
		R_L = 8Ω, THD+N = 1%, f_{IN} = 1kHz			0.4		
Power Supply Rejection Ratio	PSRR	V_{RIPPLE} = 200mVp-p, R_L = 8Ω, V_{IN-} = V_{IN+} = V_{BIAS}	217Hz		65		dB
			1kHz		63		
Total Harmonic Distortion +Noise	THD+N	A_V = 2, R_L = 4Ω, f_{IN} = 1kHz, P_{OUT} = 500mW			0.09		%
		A_V = 2, R_L = 8Ω, f_{IN} = 1kHz, P_{OUT} = 350mW			0.06		

1. Quiescent power supply current is specified and tested without loads on the outputs. Quiescent power supply current depends on the offset voltage when a practical load is connected to the device.
2. Guaranteed by design.

7 Typical Operating Characteristics

Figure 3. THD + Noise vs. Output Power; VDD = 3V, RL = 4Ω, Av = 2

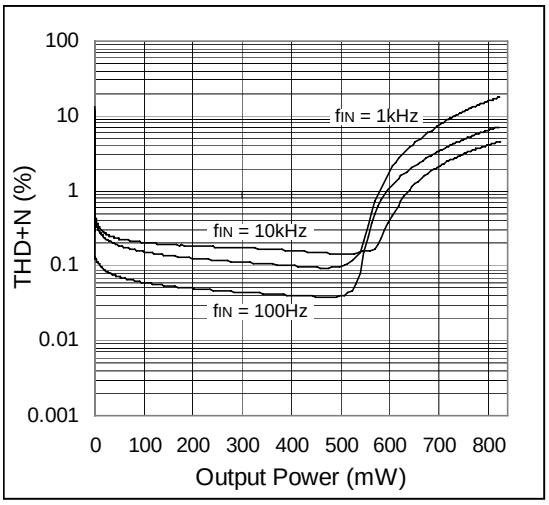


Figure 4. THD + Noise vs. Output Power; VDD = 3V, RL = 8Ω, Av = 2

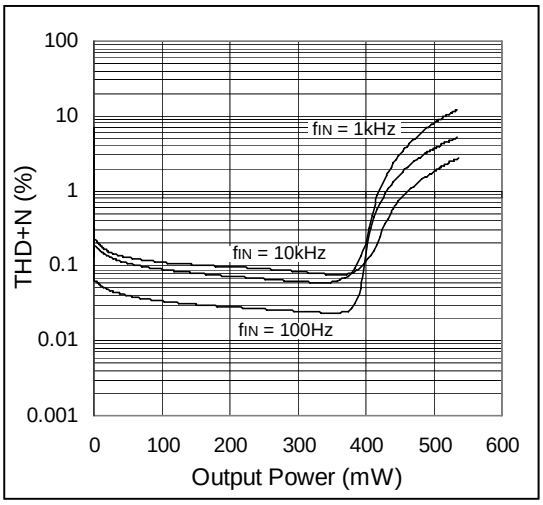


Figure 5. THD + Noise vs. Output Power; VDD = 3V, RL = 4Ω, Av = 4

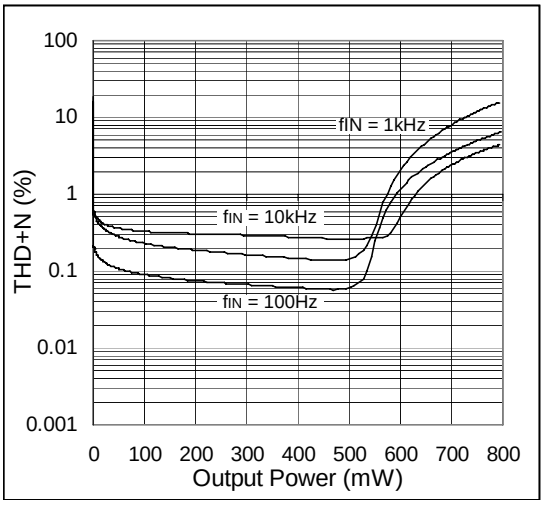


Figure 6. THD + Noise vs. Output Power; VDD = 3V, RL = 8Ω, Av = 4

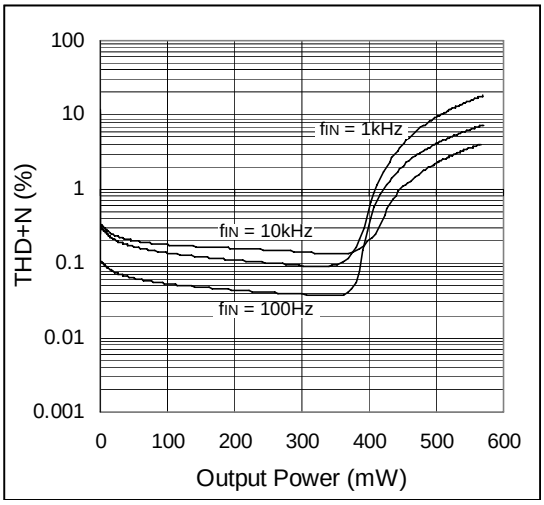


Figure 7. THD + Noise vs. Output Power; VDD = 5V, RL = 4Ω, Av = 2

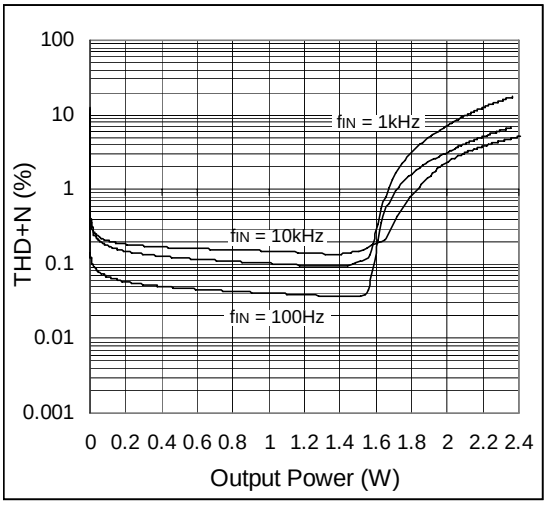


Figure 8. THD + Noise vs. Output Power; VDD = 5V, RL = 8Ω, Av = 2

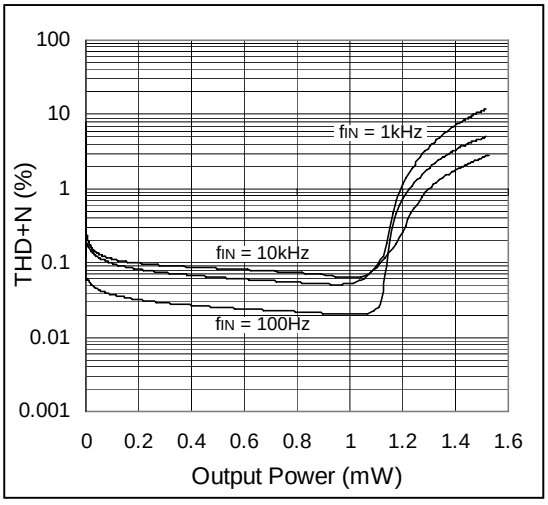


Figure 9. THD + Noise vs. Output Power; VDD = 5V, RL = 4Ω, Av = 4

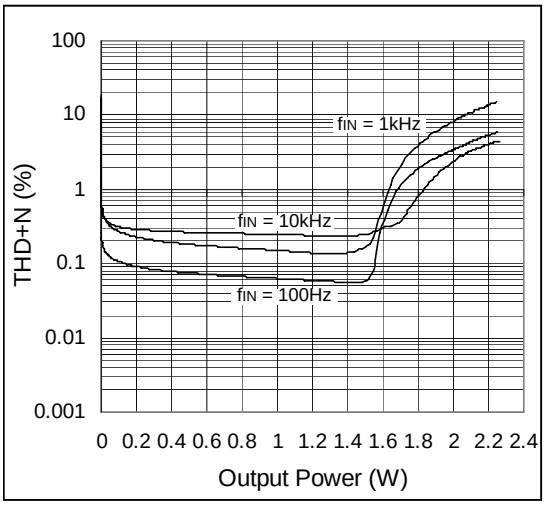


Figure 10. THD + Noise vs. Output Power; VDD = 5V, RL = 8Ω, Av = 4

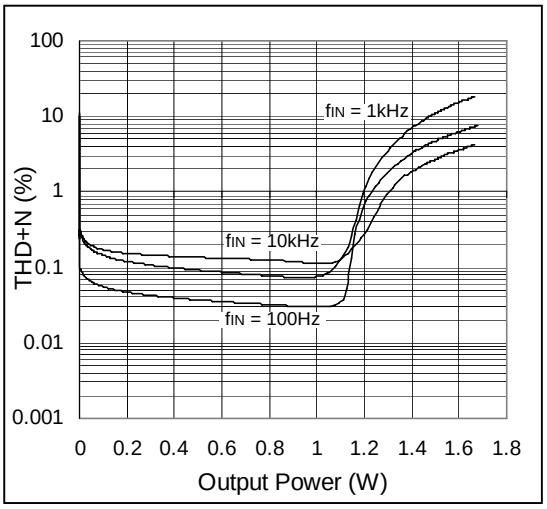


Figure 11. THD + Noise vs. Frequency; VDD = 3V, RL = 4Ω, Av = 2

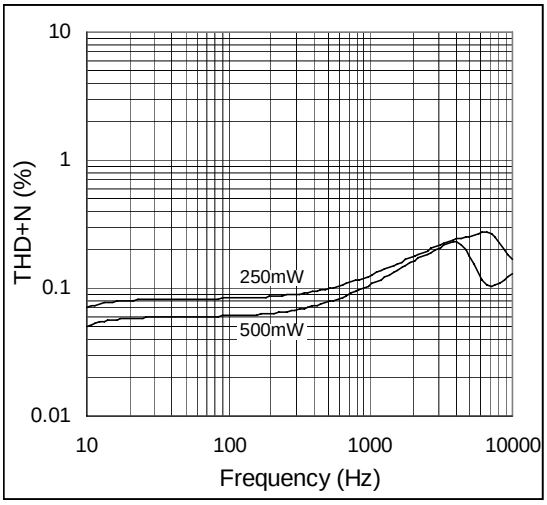


Figure 12. THD + Noise vs. Frequency; VDD = 3V, RL = 8Ω, Av = 2

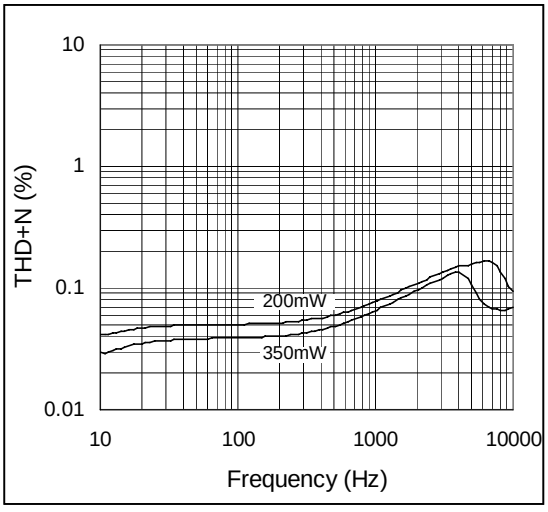


Figure 13. THD + Noise vs. Frequency; VDD = 5V, RL = 4Ω, Av = 2

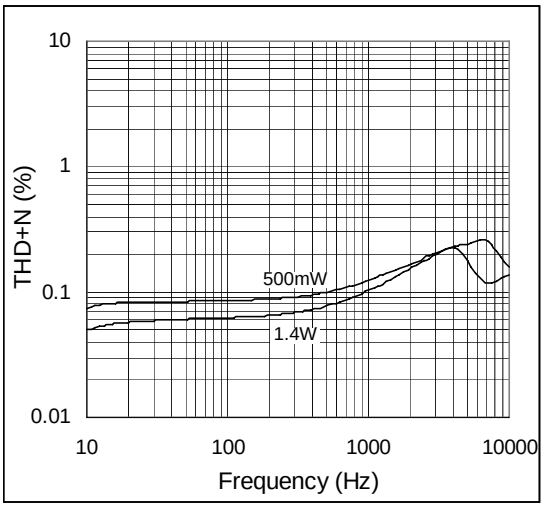


Figure 14. THD + Noise vs. Frequency; VDD = 5V, RL = 8Ω, Av = 2

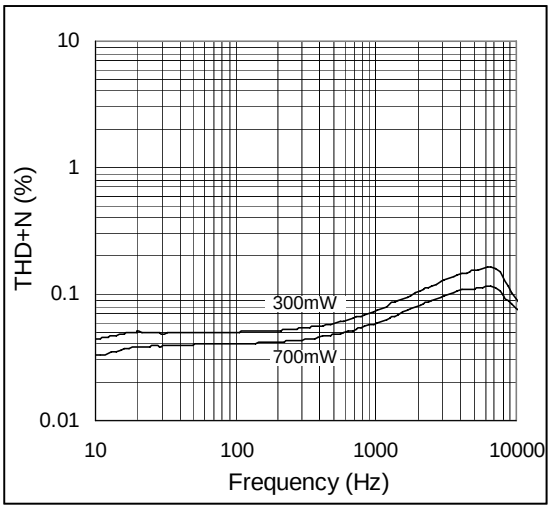


Figure 15. THD + Noise vs. Frequency; VDD = 5V, RL = 4Ω, Av = 4

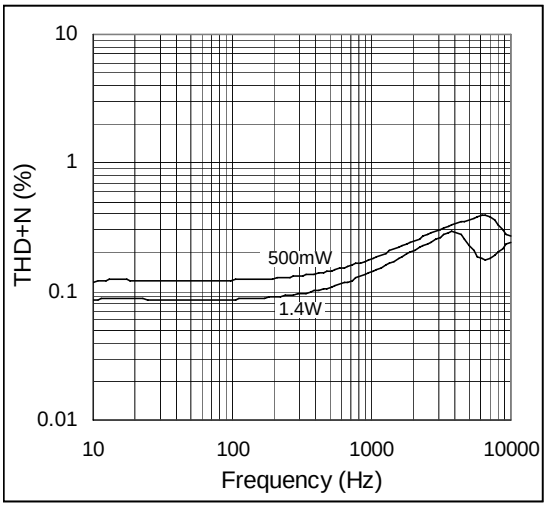


Figure 16. THD + Noise vs. Frequency; VDD = 5V, RL = 8Ω, Av = 4

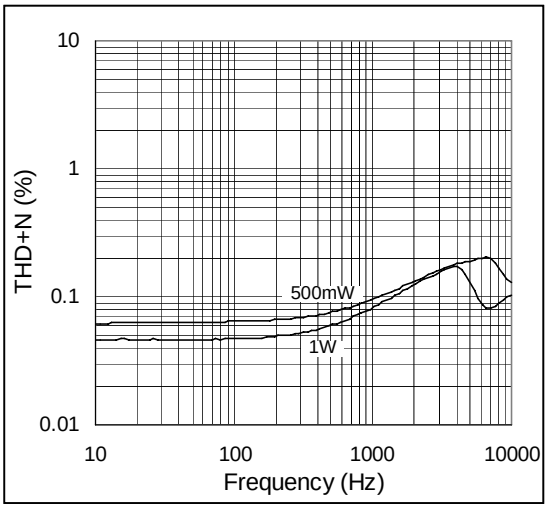


Figure 17. Power Dissipation vs. POUT; VDD = 5V, Av = 2, RL = 4Ω, f = 1kHz, THD+N<1%

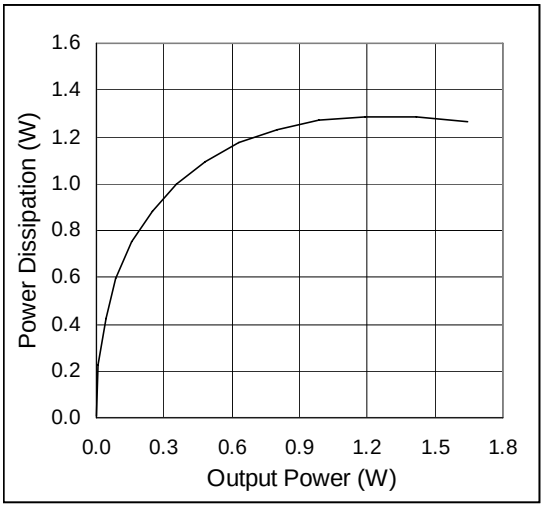


Figure 18. Power Dissipation vs. POUT; VDD = 3V Av = 2, RL = 4Ω, f = 1kHz, THD+N<1%

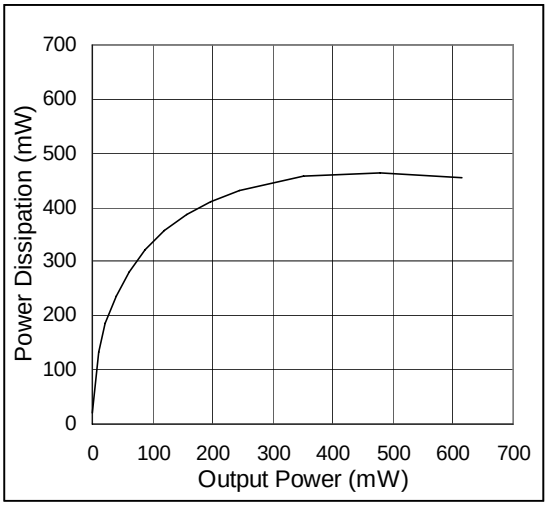


Figure 19. Power Dissipation vs. POUT; VDD = 5V, Av = 2, RL = 8Ω, f = 1kHz, THD+N<1%

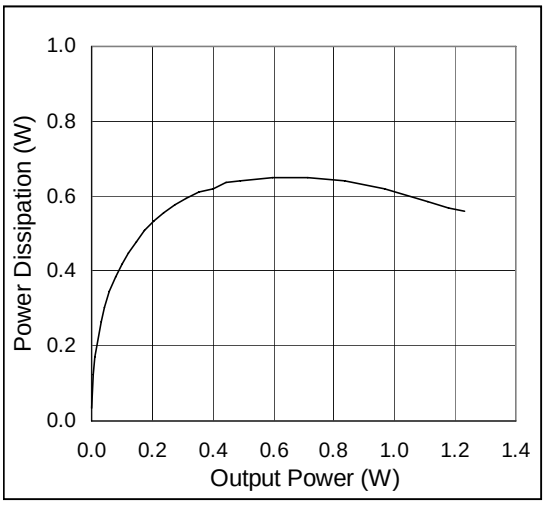


Figure 20. Power Dissipation vs. POUT; VDD = 3V Av = 2, RL = 8Ω, f = 1kHz, THD+N<1%

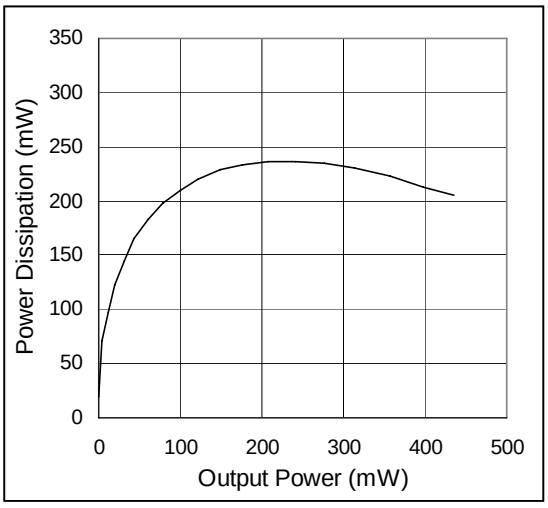


Figure 21. Output Power vs. Supply Voltage; f = 1kHz, RL = 4Ω, Av = 2

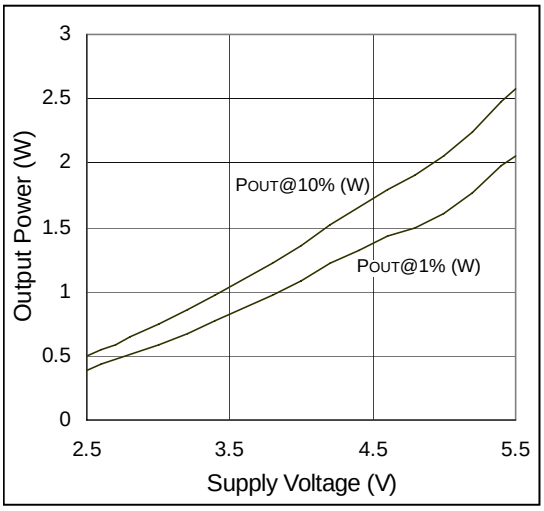


Figure 22. Output Power vs. Supply Voltage; f = 1kHz, RL = 8Ω, Av = 2

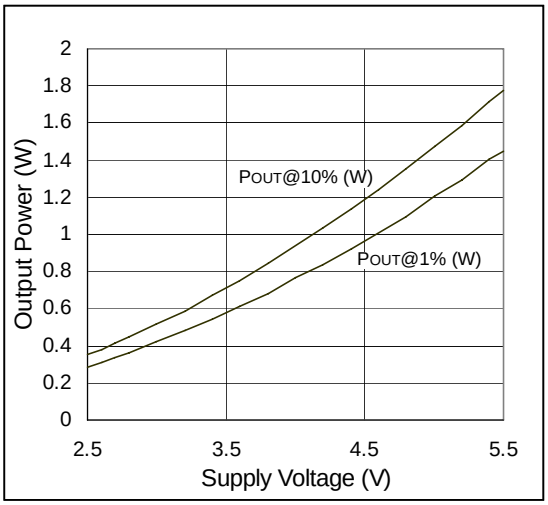


Figure 23. PSRR vs. Frequency; VRIPPLE = 200mVPP CBP = CIN = 1µF, RL = 4Ω, Av = 2, In1 Grounded

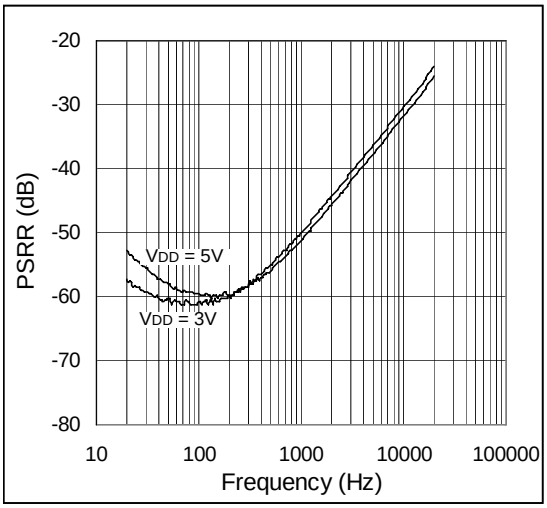


Figure 24. PSRR vs. Frequency; VRIPPLE = 200mVPP CBP = CIN = 1µF, RL = 4Ω, Av = 2, Floating Input

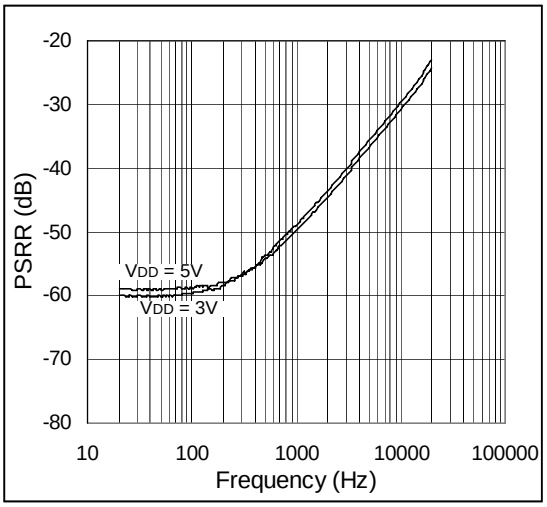


Figure 25. PSRR vs. Frequency; VRIPPLE = 200mVPP CBP = CIN = 1µF, RL = 4Ω, Av = 2, Inputs Grounded

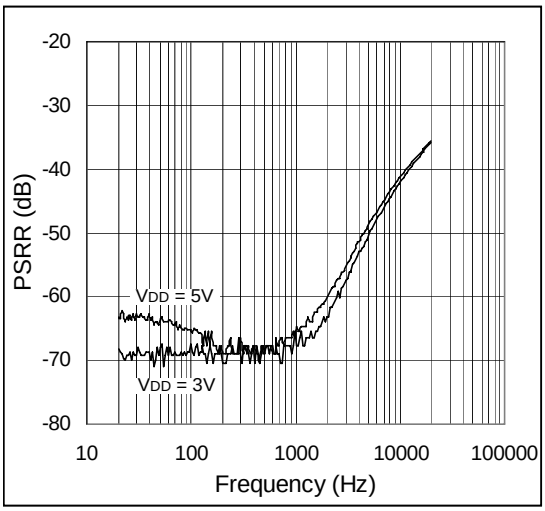


Figure 26. Supply Current vs. Temperature

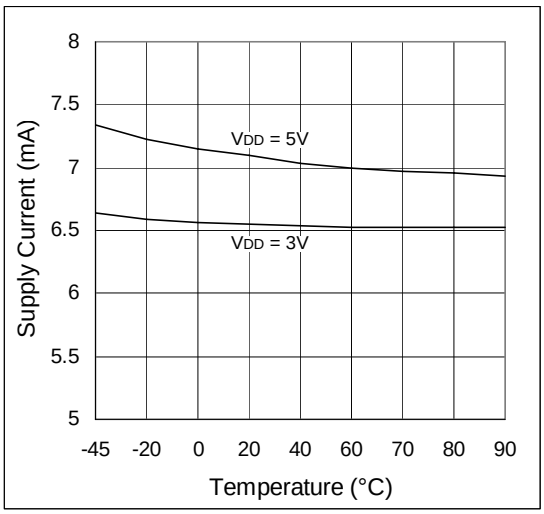


Figure 27. Output Power vs. Load Resistance; V_{DD} = 5V

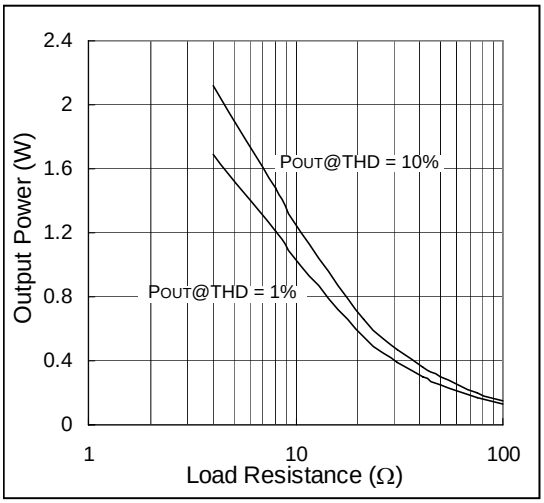
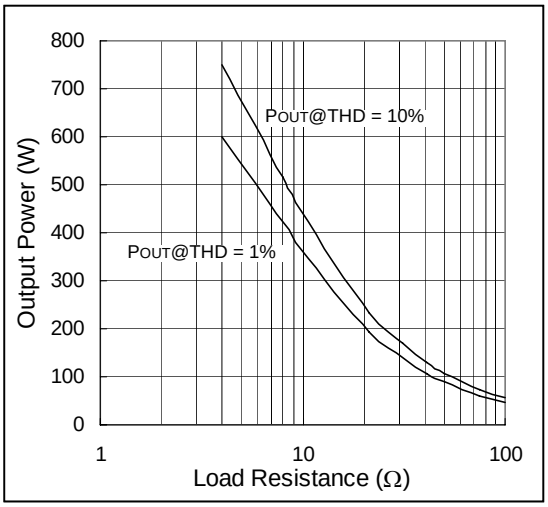


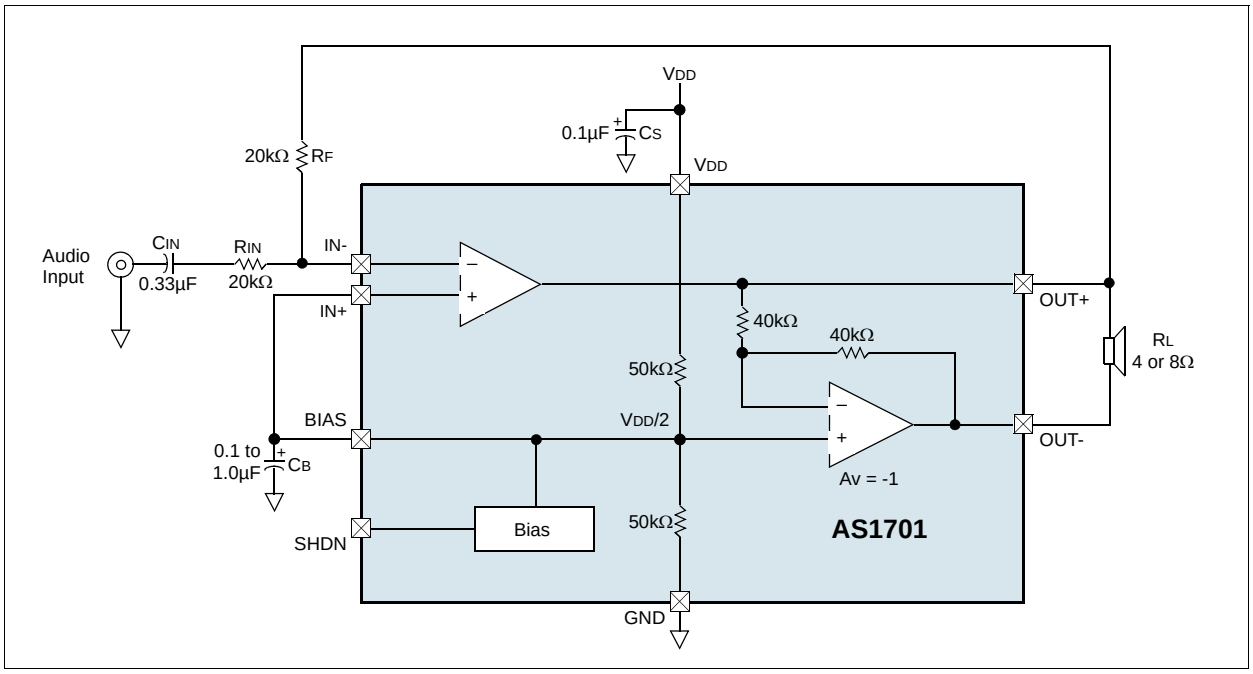
Figure 28. Output Power vs. Load Resistance; V_{DD} = 3V



8 Detailed Description

The AS1701/AS1706 bridged audio power-amplifiers can deliver 1.6W into 4Ω while operating from a single 2.7 to 5.5V supply. The devices consist of two high-output-current operational amplifiers configured as a bridge-tied load (BTL) amplifier as shown in Figure 29.

Figure 29. AS1701 Typical Configuration Block Diagram



The gain of the devices is set by the closed-loop gain of the input operational amplifier. As shown in Figure 29, the output of the first amplifier serves as the input to the second amplifier, which is configured as an inverting unity-gain follower in both devices. This results in two outputs, identical in magnitude, and 180° out-of-phase.

Bias

The devices operate from a single 2.7 to 5.5V supply and contain an internally generated, common-mode bias voltage of:

$$V_{DD}/2 \qquad \text{(EQ 1)}$$

referenced to ground. Bias provides click-and-pop suppression and sets the DC bias level for the audio outputs. For selection of the value for the bias bypass capacitor (C_{BIAS}), see Bias Bypass Capacitor on page 13. Pin BIAS is internally connected to the non-inverting input of one amplifier, and should be connected to the non-inverting input of the other amplifier for proper signal biasing (see Figure 29).

Shutdown

The integrated 100nA, low-power shutdown circuitry reduces quiescent current consumption. As shutdown commences, the bias circuitry is automatically disabled, the device outputs go high impedance, and bias is driven to GND.

Note: Connect SHDN to GND for the AS1701 (active-high); connect SHDN to V_{DD} for the AS1706 (active-low).

Current Limit

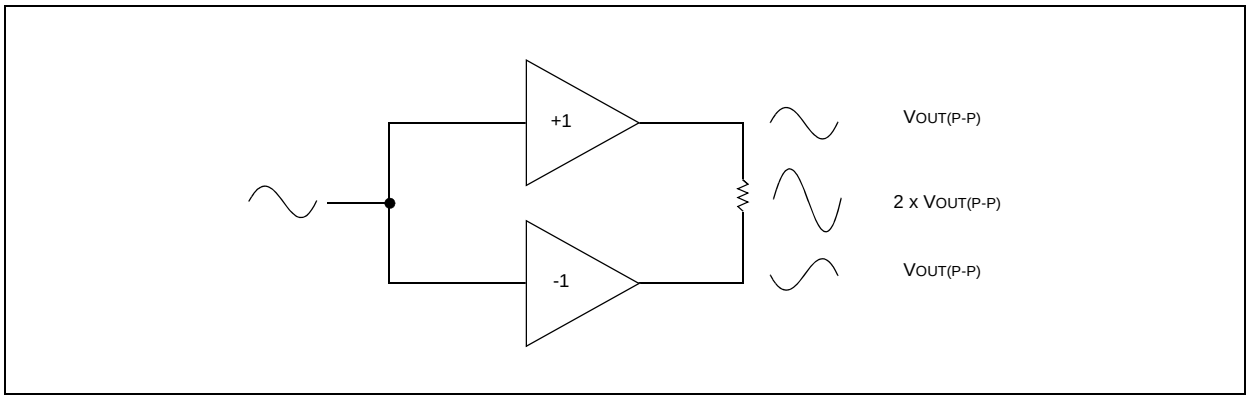
The AS1701/AS1706 current limit circuitry protects the device during output short-circuit and overload conditions. When both amplifier outputs are shorted to either V_{DD} or GND, the short-circuit protection is enabled and the amplifier enters a pulsing mode, reducing the average output current to a safe level. The amplifier remains in this mode until the short-circuit or overload condition is corrected.

9 Application Information

BTL Amplifier

The AS1701/AS1706 are designed to drive loads differentially in a bridge-tied load (BTL) configuration.

Figure 30. Bridge-Tied Load Configuration



Driving the load differentially doubles the output voltage (illustrated in Figure 30) compared to a single-ended amplifier under similar conditions. Thus, the differential gain of the device is twice the closed-loop gain of the input amplifier. The effective gain is calculated by:

$$A_{VD} = 2 \times \frac{R_F}{R_{IN}} \qquad \text{(EQ 2)}$$

Substituting 2 x $V_{OUT(P-P)}$ into (EQ 3) and (EQ 4) yields four times the output power due to doubling of the output voltage.

$$V_{RMS} = \frac{V_{OUT(P-P)}}{2\sqrt{2}} \qquad \text{(EQ 3)}$$

$$P_{OUT} = \frac{V_{RMS}^2}{R_L} \qquad \text{(EQ 4)}$$

Since the differential outputs are biased at mid-supply, there is no net DC voltage across the load, eliminating the need for the large, expensive, performance degrading DC-blocking capacitors required by single-ended amplifiers.

Power Dissipation and Heat Sinking

Normally, the devices dissipate a significant amount of power. The maximum power dissipation is given in Table 2 as Continuous Power Dissipation, or it can be calculated by:

$$P_{DISSPKF(MAX)} = \frac{T_{J(MAX)} - T_A}{\Theta_{JA}} \qquad \text{(EQ 5)}$$

where $T_{J(MAX)}$ is +150°C, T_{AMB} (see Table 2) is the ambient temperature, and Θ_{JA} is the reciprocal of the derating factor in °C/W.

The increased power delivered by a BTL configuration normally results in increased internal power dissipation versus a single-ended configuration. The maximum internal power dissipation for a given V_{DD} and load is calculated by:

$$P_{DISSPKF(MAX)} = \frac{2V_{DD}^2}{\pi^2 R_L} \qquad \text{(EQ 6)}$$

If the internal power dissipation exceeds the maximum allowed for a given package, power dissipation can be reduced by increasing the ground plane heat-sinking capabilities and increasing the size of the traces to the device (see Layout and Grounding Considerations on page 14). Additionally, reducing V_{DD}, increasing load impedance, and decreasing ambient temperature can reduce device power dissipation.

The integrated thermal-overload protection circuitry limits the total device power dissipation. Note that if the junction temperature is ≥ +145°C, the integrated thermal-overload protection circuitry will disable the amplifier output stage. If the junction temperature is reduced by 9ºC, the amplifiers will be re-enabled.

Note: A pulsing output under continuous thermal overload results as the device heats and cools.

Efficiency

Efficiency of the AS1701/AS1706 is calculated by taking the ratio of the power delivered to the load, to the power consumed from the power supply. Output power is calculated by:

$$P_{OUT} = \frac{V_{PEAK}^2}{\pi^2 R_L} \quad \text{(EQ 7)}$$

where V_{PEAK} is half the peak-to-peak output voltage. In BTL amplifier configurations, the supply current waveform is a full-wave rectified sinusoid with the magnitude proportional to the peak output voltage and load.

Calculate the supply current and power drawn from the power supply by:

$$I_{DD} = \frac{2V_{PEAK}}{\pi R_L} \quad \text{(EQ 8)}$$

$$P_{IN} = V_{DD} \frac{2V_{PEAK}}{\pi R_L} \quad \text{(EQ 9)}$$

The efficiency of the AS1701/AS1706 is:

$$\eta = \frac{P_{OUT}}{R_{IN}} = \pi \sqrt{\frac{\frac{P_{OUT} R_L}{2}}{2V_{DD}}} \quad \text{(EQ 10)}$$

Component Selection

Gain-Setting Resistors

External feedback resistors R_F and R_{IN} (see Figure 1 on page 1) set the gain of the device as:

$$A_{VD} = 2 \times \frac{R_F}{R_{IN}} \quad \text{(EQ 11)}$$

Optimum output offset is achieved when R_F = 20kΩ. Device gain can be varied by changing the value of R_{IN}.

If used in a high-gain configuration (greater than 8V/V), a feedback capacitor may be required to maintain stability (see Figure 1 on page 1). C_F and R_F limit the bandwidth of the device, preventing high-frequency oscillations.

Note: Ensure that the pole created by C_F and R_F is not within the frequency band of interest.

Input Filter

Input capacitor CIN (if used), in conjunction with RIN, forms a high-pass filter that removes the DC bias from an incoming signal. CIN allows the amplifier to bias the signal to an optimum DC level. Assuming zero source impedance, the -3dB point of the high-pass filter is given by:

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}} \quad \text{(EQ 12)}$$

Select the value for RIN as specified in Gain-Setting Resistors on page 12. Choose the value for CIN such that f-3dB is well below the lowest frequency of interest. Setting f-3dB too high can affect the low-frequency response of the device. Capacitors with dielectrics that have low-voltage coefficients such as tantalum or aluminum electrolytic should be used, since capacitors with high-voltage coefficients, such as ceramics, can increase distortion at low frequencies.

Note: Other considerations when designing the input filter include the overall constraints of the system, the frequency band of interest, and click-and-pop suppression. Although hi-fi audio specifies a flat gain response between 20Hz and 20kHz, portable voice reproduction devices such as mobile phones and two-way radios only need address the frequency range of the human voice (~ 300Hz to 3.5kHz). Additionally, speakers used in portable devices typically have poor response below 150Hz. In practice, the input filter may not need to be designed for the 20Hz to 20kHz range, which could save PCB space and design costs since only small capacitors would be required.

Bias Bypass Capacitor

The bias bypass capacitor, CBIAS, improves PSRR and THD+N by reducing power supply noise at the common-mode bias node, and serves as the primary click- and pop-suppression component. CBIAS is fed from an internal 25kΩ source, and controls the rate at which the common-mode bias voltage rises at power-up and falls during shutdown. For optimal click- and pop-suppression, ensure that the input capacitor (CIN) is fully charged (ten time constants) before CBIAS.

The value of CBIAS for best click- and pop-suppression is given by:

$$C_{BIAS} \leq 10 \frac{C_{IN} R_{IN}}{25k\Omega} \quad \text{(EQ 13)}$$

Note: A larger CBIAS value yields higher PSRR.

Click- and Pop-Less Operation

AC-coupling capacitors (CIN) along with CBIAS facilitate click- and pop-less power-up and shutdown. The value of CBIAS determines the rate at which the mid-rail bias voltage rises on power-up and falls when entering shutdown.

On power-up, CIN is charged to its quiescent DC voltage through the RF from the output. The current generated creates a voltage transient at the amplifier output, which can result in an audible pop. Minimizing the value of CIN reduces this effect, optimizing click-and-pop suppression.

For more information see Bias on page 10 and Bias Bypass Capacitor on page 13.

Supply Bypassing

Proper power supply bypassing – connect a 0.1µF ceramic capacitor in parallel with a 10µF ceramic capacitor from VDD to GND – will ensure low-noise, low-distortion performance of the device. Additional bulk capacitance can be added as required.

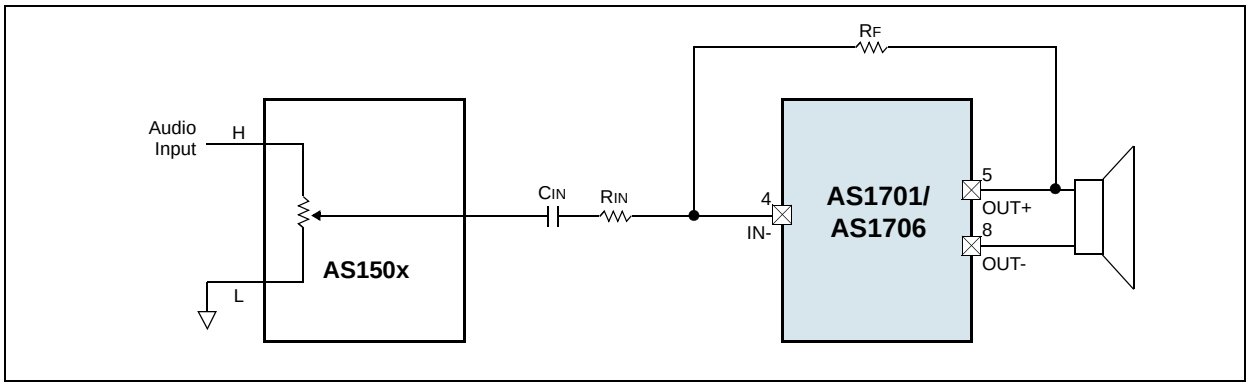
Note: Place the capacitors as close to the device as possible.

Volume Control

The addition of a digital potentiometer (AS1500 family) used as an input attenuator, can provide simple volume control for the AS1701/AS1706.

Connect the high terminal of the AS150x to the audio input, the low terminal to ground and the AS150x wiper to CIN (as shown in Figure 31). Setting the wiper to the top position passes the audio signal unattenuated; setting the wiper to the lowest position fully attenuates the input.

Figure 31. Volume Control Configuration



For more information on the AS1500 family of digital potentiometers, refer to the latest version of the AS150*x* data sheet, available from the austriamicrosystems website http://www.austriamicrosystems.com.

Layout and Grounding Considerations

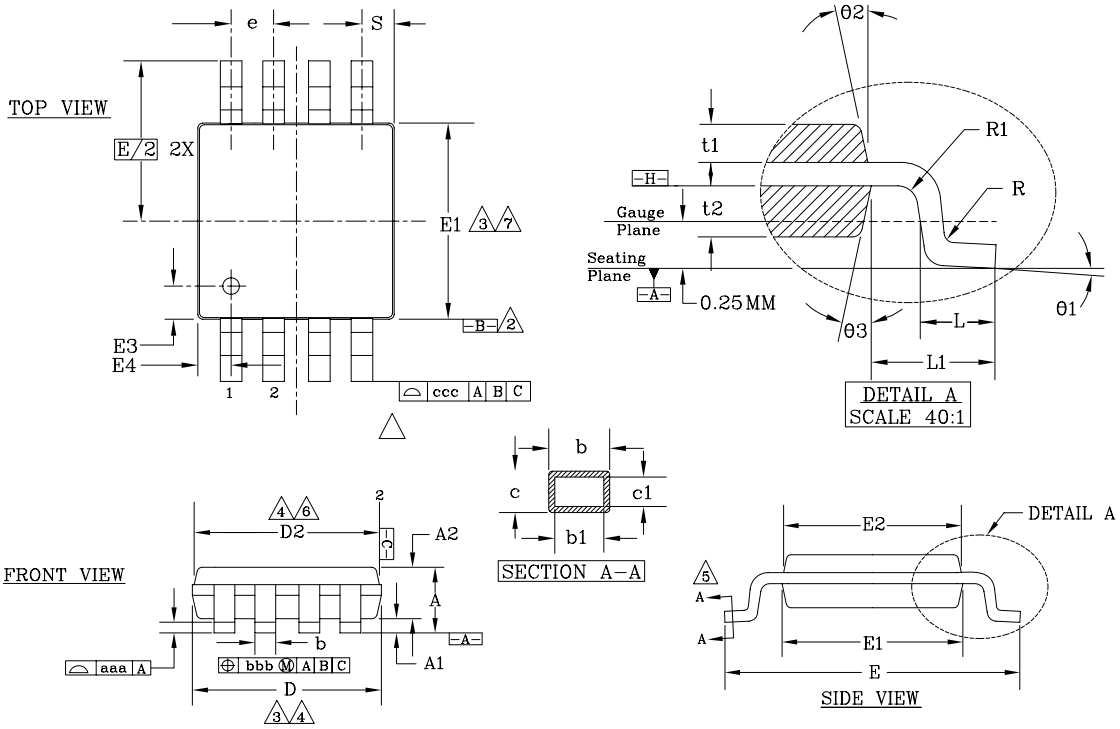
Well designed PC board layout is essential for optimizing device performance. Use large traces for the power supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance and route heat away from the device.

Sufficient grounding improves audio performance, minimizes crosstalk between channels, and prevents digital switching noise from coupling onto the audio signal.

Refer to Power Dissipation and Heat Sinking on page 11 for heat sinking considerations.

10 Package Drawings and Markings

Figure 32. 8-pin MSOP Package



Symbol	Millimeters	± Tolerance	Symbol	Millimeters	± Tolerance
A	1.10	Max	b	0.33	+0.07 to -0.08
A1	0.10	±0.05	b1	0.30	±0.05
A2	0.86	±0.08	c	0.18	±0.05
D	3.00	±0.10	c1	0.15	+0.03 to -0.02
D2	2.95	±0.10	θ1	3.0º	±3.0º
E	4.90	±0.15	θ2	12.0º	±3.0º
E1	3.00	±0.10	θ3	12.0º	±3.0º
E2	2.95	±0.10	L	0.55	±0.15
E3	0.51	±0.13	L1	0.95 BSC	
E4	0.51	±0.13	aaa	0.10	
R	0.15	+0.15 to -0.08	bbb	0.08	
R1	0.15	+0.15 to -0.08	ccc	0.25	
t1	0.31	±0.08	e	.65 BSC	
t2	0.41	±0.08	S	.525 BSC	

Notes:

1. All dimensions are in millimeters (angle in degrees), unless otherwise specified.
2. Datums B and C to be determined at datum plane H.
3. Dimensions D and E1 are to be determined at datum plane H.
4. Dimensions D2 and E2 are for top package and D and E1 are for bottom package.
5. Cross section A-A to be determined at 0.13 to 0.25mm from the lead tip.
6. Dimensions D and D2 do not include mold flash, protrusion, or gate burrs.
7. Dimension E1 and E2 do not include interlead flash or protrusion.

11 Ordering Information

The devices are available as the standard products shown in Table 5.

Table 5. Ordering Information

Part Number	Description	SHDN	Delivery Form	Package Type
AS1701	1.6W Audio Power Amplifier	Active-High	Tube	8-pin MSOP
AS1701-T	1.6W Audio Power Amplifier	Active-High	Tape and Reel	8-pin MSOP
AS1706	1.6W Audio Power Amplifier	Active-Low	Tube	8-pin MSOP
AS1706-T	1.6W Audio Power Amplifier	Active-Low	Tape and Reel	8-pin MSOP

Copyrights

Disclaimer

Devices sold by austriamicrosystems AG are covered by the warranty and patent indemnification provisions appearing in its Term of Sale. austriamicrosystems AG makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. austriamicrosystems AG reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with austriamicrosystems AG for current information. This product is intended for use in normal commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically not recommended without additional processing by austriamicrosystems AG for each application. For shipments of less than 100 parts the manufacturing flow might show deviations from the standard production flow, such as test flow or test location.

The information furnished here by austriamicrosystems AG is believed to be correct and accurate. However, austriamicrosystems AG shall not be liable to recipient or any third party for any damages, including but not limited to personal injury, property damage, loss of profits, loss of use, interruption of business or indirect, special, incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data herein. No obligation or liability to recipient or any third party shall arise or flow out of austriamicrosystems AG rendering of technical or other services.

Contact Information

Headquarters
austriamicrosystems AG
A-8141 Schloss Premstaetten, Austria

Tel: +43 (0) 3136 500 0
Fax: +43 (0) 3136 525 01

For Sales Offices, Distributors and Representatives, please visit:

http://www.austriamicrosystems.com/contact