AS1713

DataSheet

Difference Amplifier, 10MHz, 10V/µs, Rail-to-Rail I/O with Shutdown

1 General Description

The AS1713 is a low cost cmos difference amplifier providing extended common mode voltage range for a single rail 5V supply. Resistor trimming during final test ensures a typical common mode rejection of 60dB. Low input bias currents, 10MHz gain bandwidth, low total harmonic distortion (THD) and a rail-to-rail output drive capability of typically 200mA (@ 5V supply) provide support for a number of signal processing applications such as audio line receivers, ground loop breakers and current sensing. Linearity is suitable for 12bit ADC measurement.

A classical single amplifier approach ensures that the differential gain is determined by a simple ratio of two internal resistors. A fixed gain of x1 is available.

Single ended input resistance is equalised (10kΩ ±10%) at each input terminal. This feature provides additional common mode rejection when long balanced input cables connect at the input.

A EN pin reduces the quiescent current of the device.

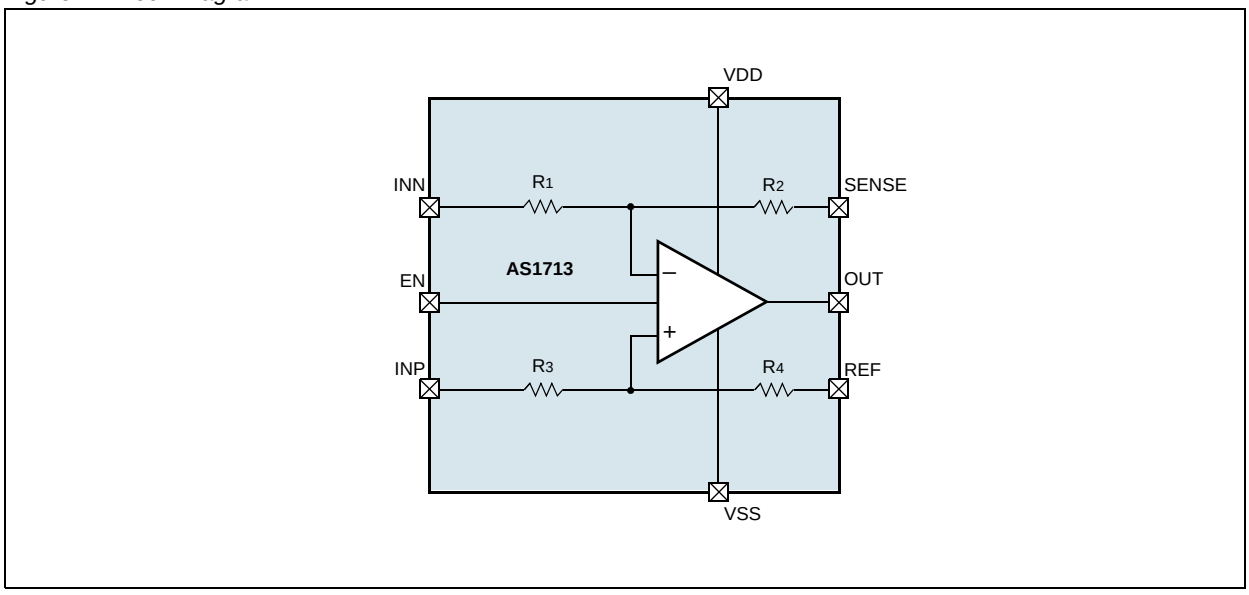
2 Key Features

- Constant Output Drive Capability: 50mA
- Rail-to-Rail Input and Output
- Supply Current: 1.6mA
- Single-Supply Operation: 2.7 to 5.5V
- Voltage Gain: 1
- Gain-Bandwidth Product: 10MHz
- High Slew Rate: 10V/µs
- Power-Supply Rejection Ratio: -70dB
- Common Mode Rejection Ratio: -60dB
- No Phase Reversal for Overdriven Inputs
- Unity-Gain Stable for Capacitive Loads: Up to 100pF
- Shutdown Mode Current: 1nA
- MLPD (2x2mm) 8-pin package

3 Applications

The device is ideal for headphone amplifiers with ground interference rejection, infotainment high drive audio line buffers with ground interference rejection, audio differential-to-single-ended conversion and instrumentation amplifier back-end.

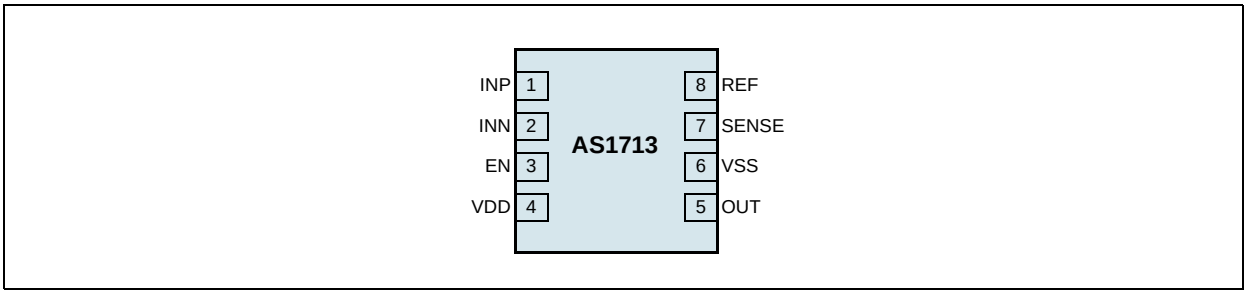
Figure 1. Block Diagram



4 Pinout

Pin Assignments

Figure 2. Pin Assignments (Top View)



Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Pin Name	Description
1	INP	**Non-inverting Input.**
2	INN	**Inverting Input.**
3	EN	**Active-Low Enable Input.** A logic low on this pin shuts down the device. V_{SS}: device in shutdown. V_{DD}: normal operation.
4	VDD	**Positive Supply Input.**
5	OUT	**Amplifier Output.**
6	VSS	**Negative Supply Input.** This pin must be connected to ground in single-supply applications.
7	SENSE	**Sense Input.** Ground this pin when external inverting gain control is required.
8	REF	**Reference Input.** Reference to non-inverting input resistor network.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
Supply Voltage (V_{DD} to V_{SS})		+7	V	
Supply Voltage (All Other Pins)	V_{SS} - 0.3	V_{DD} + 0.3	V	
Output Short-Circuit Duration to V_{DD} or V_{SS}		1	s	
Thermal Resistance Θ_{JA}	33		ºC/W	on PCB
ESD	1		kV	*HBM MIL-Std. 883E 3015.7* methods
Operating Temperature Range	-40	+85	ºC	
Storage Temperature Range	-65	+150	ºC	
Junction Temperature		+150	ºC	
Package Body Temperature		+260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).

6 Electrical Characteristics

DC Electrical Characteristics

V_{DD} = 2.7V, V_{SS} = 0V, V_{CM} = V_{DD}/2, V_{OUT} = V_{DD}/2, R_{LOAD} = Infinite, V_{EN} = V_{DD}, T_{AMB} = -40 to +85ºC. Typical values at T_{AMB} = 25°C.

Table 3. DC Electrical Characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Unit
V_{DD}	Supply Voltage Range	Inferred from Power Supply Rejection Ratio Test		2.7		5.5	V
V_{OFFSET}	Input Offset Voltage			-1.5		+1.5	mV
R_{SEIN}	Single-Ended Input Resistance			9	10	11	kΩ
V_{CM}	Common Mode Input Voltage Range	Inferred from Common Mode Rejection Ratio[1]		V_{SS}		V_{DD}	V
CMRR	Common Mode Rejection Ratio	V_{SS} < V_{CM} < V_{DD}		-45	-60		dB
PSRR	Power Supply Rejection Ratio	V_{DD} = 2.7 to 5.5V		-60	-70		dB
R_{OUT}	Shutdown Output Impedance	V_{EN} = 0V			130		Ω
$V_{OUT-SHDNN}$	Shutdown Output Voltage	V_{EN} = 0V, R_{LOAD} = 2kΩ to V_{DD}			170	400	mV
	Output Voltage Swing	V_{DD} - V_{OH} or V_{OL} - V_{SS}	R_{LOAD} = 32Ω		350	650	mV
			R_{LOAD} = 200Ω		70	120	
			R_{LOAD} = 2kΩ		9	20	
V_{OUT}	Output Voltage	V_{DD} - V_{OH} or V_{OL} - V_{SS}	I_{LOAD} = 10mA, V_{DD} = 2.7V		55	100	mV
			I_{LOAD} = 50mA, V_{DD} = 5V		100	200	
I_{OUT}	Output Source/Sink Current	V_{DD} = 2.7V, V- = V_{CM}, V+ = V_{CM}±100mV			100		mA
		V_{DD} = 5.0V, V- = V_{CM}, V+ = V_{CM}±100mV			200		
I_{DD}	Quiescent Supply Current	V_{DD} = 2.7V, V_{CM} = V_{DD}/2			1.6	3.2	mA
		V_{DD} = 5.0V, V_{CM} = V_{DD}/2			2.3	4.6	
$I_{DD-SHDNN}$	Shutdown Supply Current	V_{EN} = 0V, V_{DD} = 2.7V			1	2000[1]	nA
	EN Logic Threshold	Shutdown Mode			V_{SS} + 0.3		V
		Normal Operation			V_{DD} - 0.3		
	EN Input Bias Current	V_{SS} < V_{EN} < V_{DD}			50		pA

1. Guaranteed by design.

AC Electrical Characteristics

V_{DD} = 2.7V, V_{SS} = 0V, V_{CM} = V_{DD}/2, V_{OUT} = V_{DD}/2, R_{LOAD} = Infinite, V_{EN} = V_{DD}, T_{AMB} = -40 to +85ºC. Typical values at T_{AMB} = 25°C.

Table 4. AC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
GBWP	Gain-Bandwidth Product	V_{CM} = V_{DD}/2		4		MHz
f_C	Cut-off Frequency			8.5		MHz
SR	Slew Rate			5		V/µs
PM	Phase Margin			60		deg
GM	Gain Margin[1]			10		dB
THD+N	Total Harmonic Distortion Plus Noise	f = 10kHz, V_{OUT} = 2V_{P-P}, A_{VCL} = 1V/V		60		dBc
C_{IN}	Input Capacitance			2		pF
en	Voltage-Noise Density[1]	f = 1kHz		40		nV/√Hz
		f = 10kHz		30		
	Capacitive-Load Stability	A_{VCL} = 1V/V, no sustained oscillations		100		pF
t_{SHDN}	Shutdown Time			1		µs
t_{ENABLE}	Enable Time from Shutdown			7		µs
t_{ON}	Power-Up Time			20		ns

1. Guaranteed by design.

7 Typical Operating Characteristics

V_{DD} = 2.7V; V_{SS} = 0V, V_{CM} = V_{DD}/2, V_{OUT} = V_{DD}/2, R_{LOAD} = ∞, V_{EN} = V_{DD} T_{AMB} = +25ºC (unless otherwise specified).

Figure 3. Gain and Phase vs. Frequency

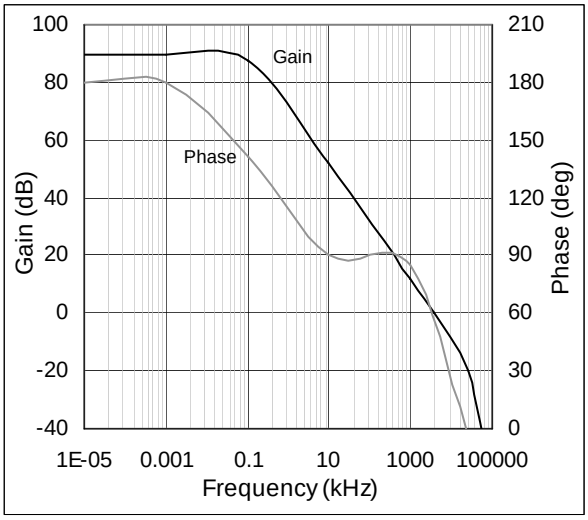


Figure 4. Gaind and Phase vs. freq.; C_{LOAD} = 100pF

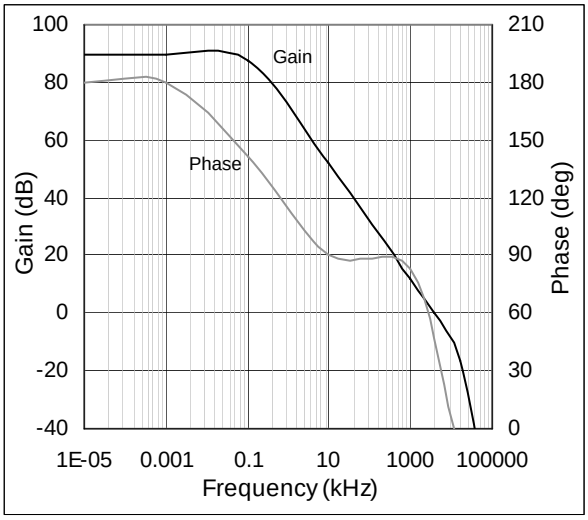


Figure 5. PSRR vs. Frequency

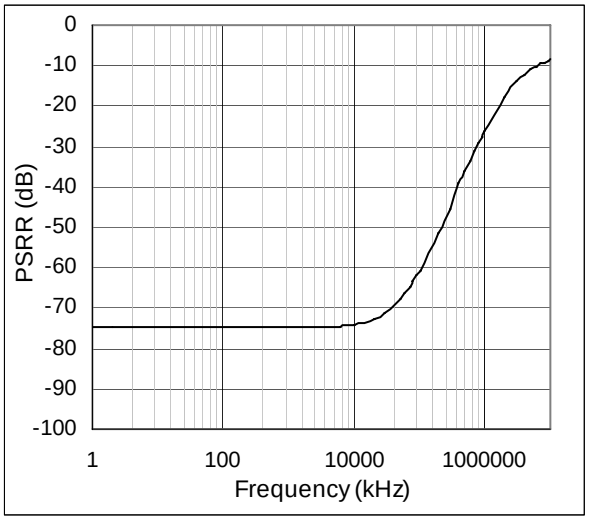


Figure 6. CMRR vs. Frequency

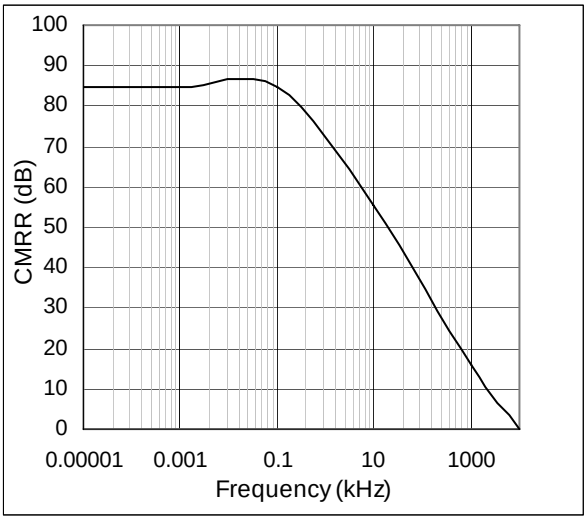


Figure 7. Supply Current vs. Temperature

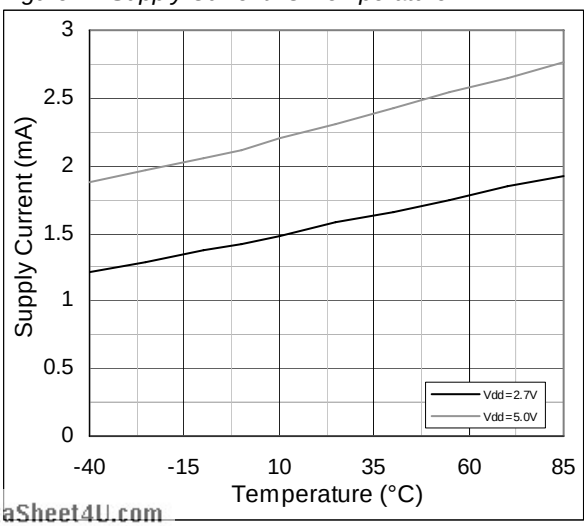


Figure 8. Shutdown Current vs. Temperature

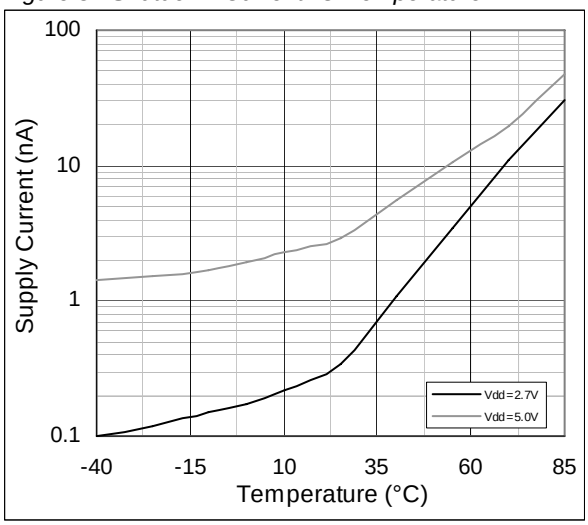


Figure 9. Supply Current vs. CMRR

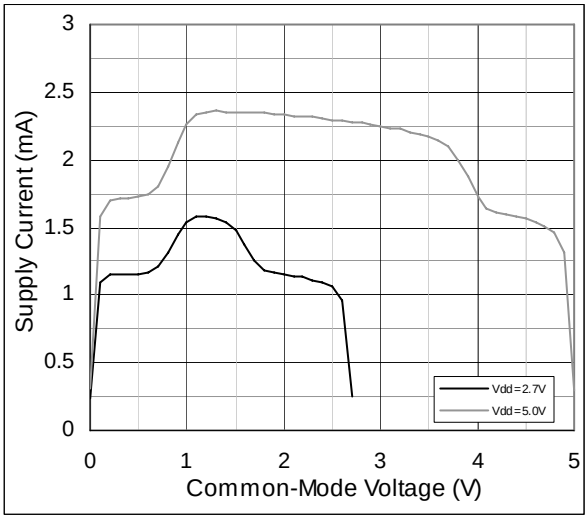


Figure 10. Input Voltage Noise vs. Frequency

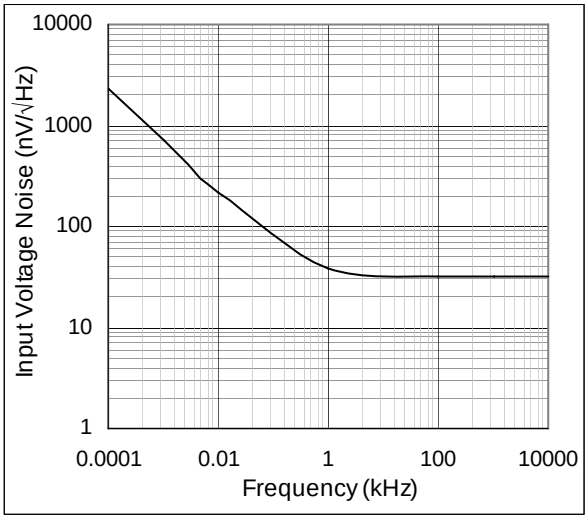


Figure 11. Output Swing High vs. Temp.; V_{DD} = 2.7V

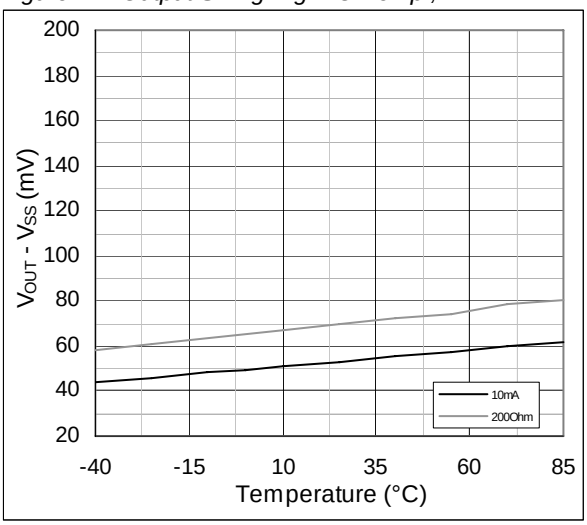


Figure 12. Output Swing Low vs. Temp.; V_{DD} = 2.7V

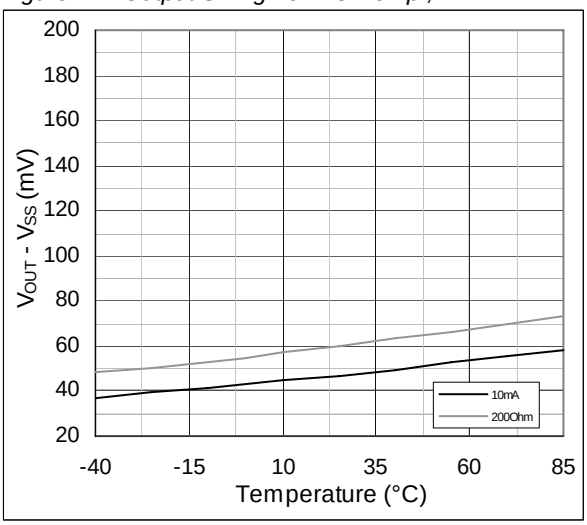


Figure 13. Output Swing High vs. Temp.; V_{DD} = 5.5V

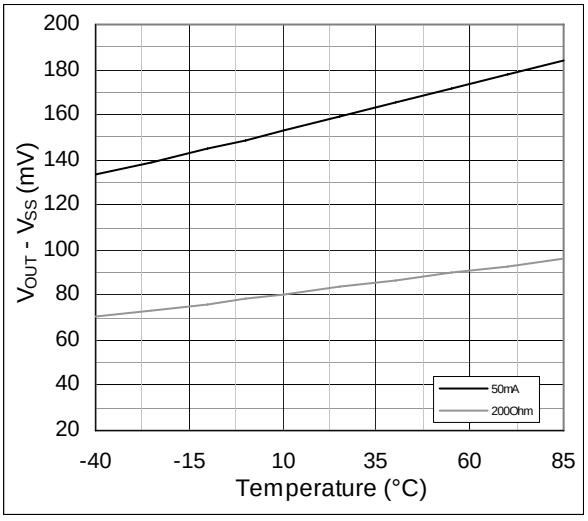


Figure 14. Output Swing Low vs. Temp.; V_{DD} = 5.5V

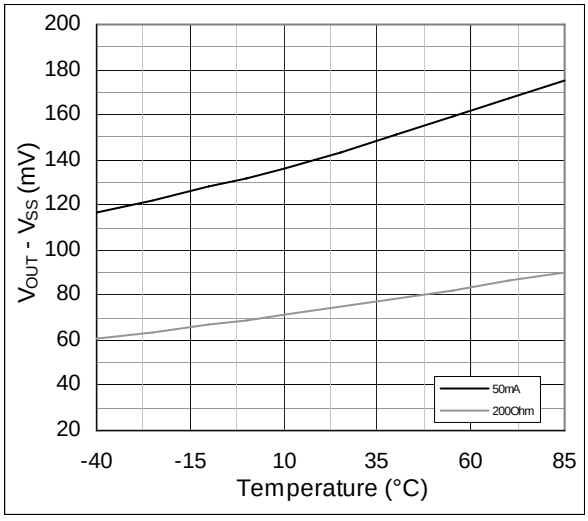


Figure 15. VOUT vs. IOUT, sourcing

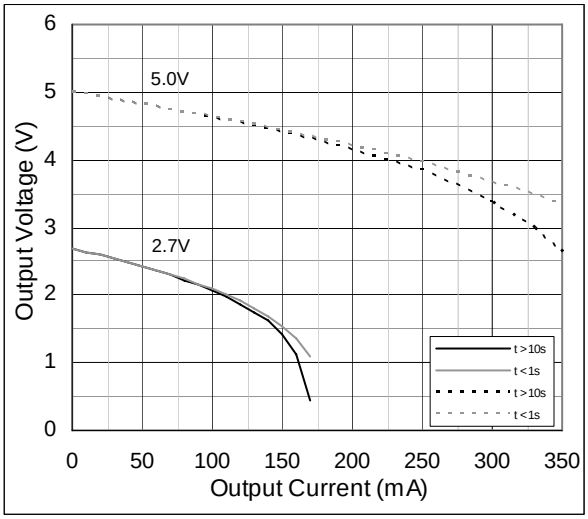


Figure 16. VOUT vs. IOUT, sinking

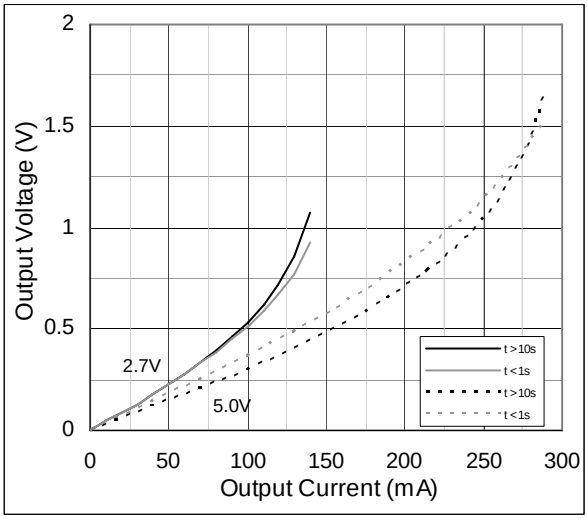


Figure 17. Transient Response; VIN = 100mV, CLOAD = 10pF

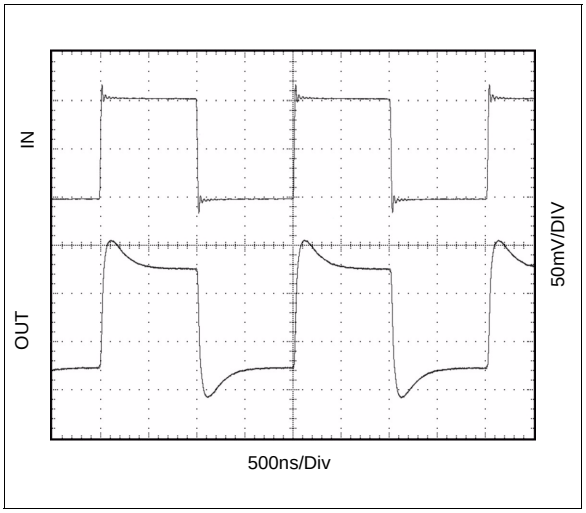


Figure 18. Transient Response; VIN = 100mV, CLOAD = 100pF

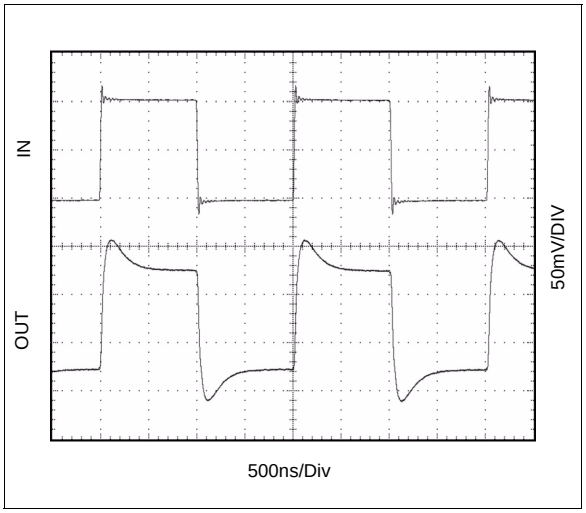


Figure 19. Transient Response; VIN = 1V, CLOAD = 10pF

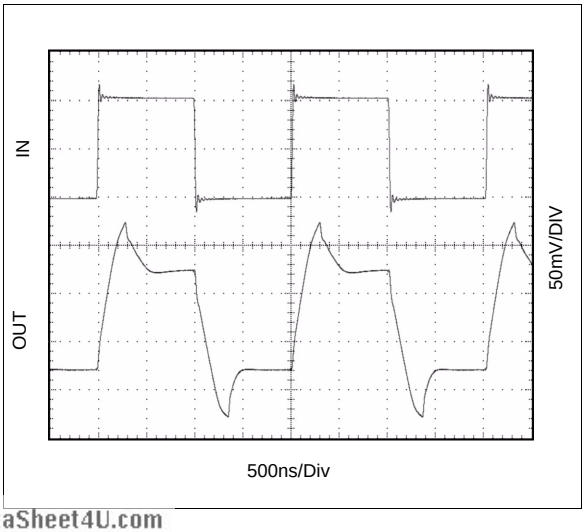


Figure 20. Transient Response; VIN = 1V, CLOAD = 100pF

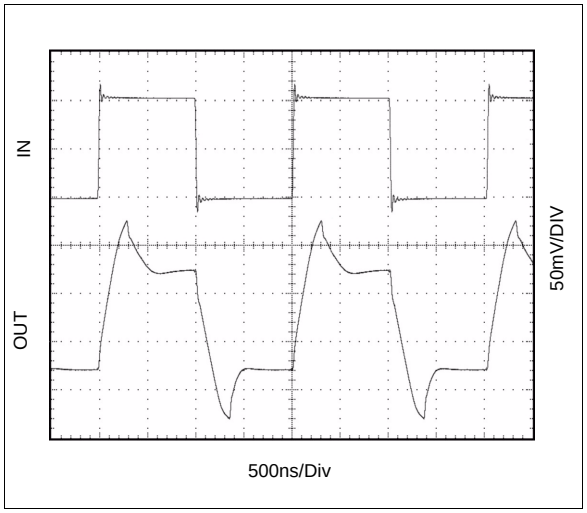


Figure 21. Transient Response; V_{IN} = 2V, C_{LOAD} = 10pF

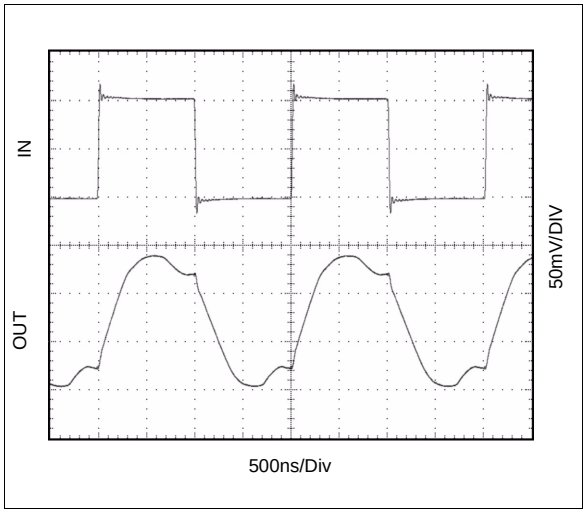
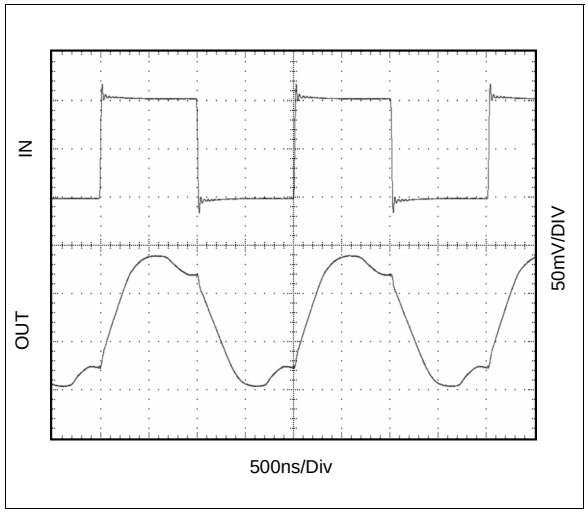


Figure 22. Transient Response; V_{IN} = 2V, C_{LOAD} = 100pF



8 Application Information

Ground Loop Interference Suppression:

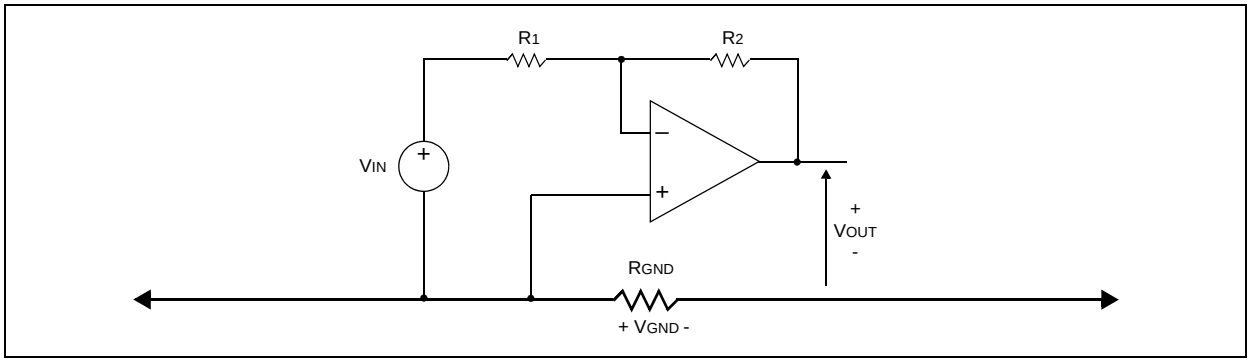
In real life situations the signal source and the amplifier are often located a distance apart, but still share the same ground arrangement with a number of other circuits. The ground system is never perfect as it has a small distributed resistance, capacitance and inductance. Thus, the ground appears as a distributed impedance.

As a various current flow into and out of the ground system exists, a small voltage drop will inevitably occur, causing different voltages within the ground. In Figure 23 and Figure 24, R_{GND} denotes the ground resistance between the input signal ground and the output signal ground. The voltage drop across R_{GND} should ideally have no effect on individual circuit performance.

In the single ended inverting amplifier shown in Figure 23, the amplifier sees V_{IN} and V_{GND} in series, so the amplifier output is:

$$V_{OUT} = - [R_2/R_1] [V_{IN}+V_{GND}] \quad \text{(EQ 1)}$$

Figure 23. Single Ended Inverting Amplifier

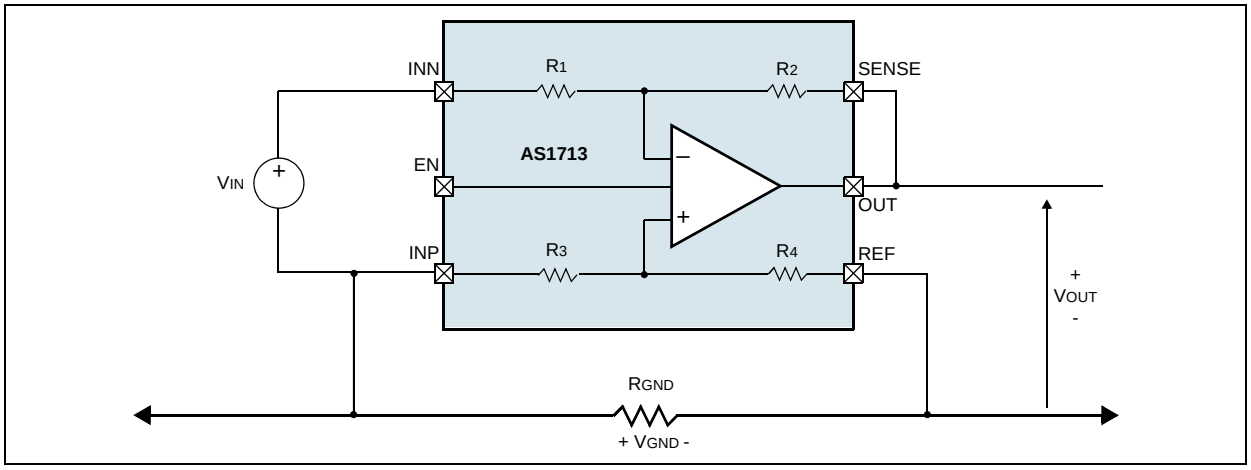


V_{GND} is part of the output expression and is known as ground loop interference, ground bounce or even common impedance crosstalk. In some situations this interference signal can be close to or the same value as the wanted input signal such as in sensor applications.

A difference amplifier is a simple method used to reduce the effect of ground interference. V_{IN} is regarded as a differential input signal, and V_{GND} a common mode signal. From Figure 24, the amplifier output is:

$$V_{OUT} = - [R_2/R_1] V_{IN} \quad \text{(EQ 2)}$$

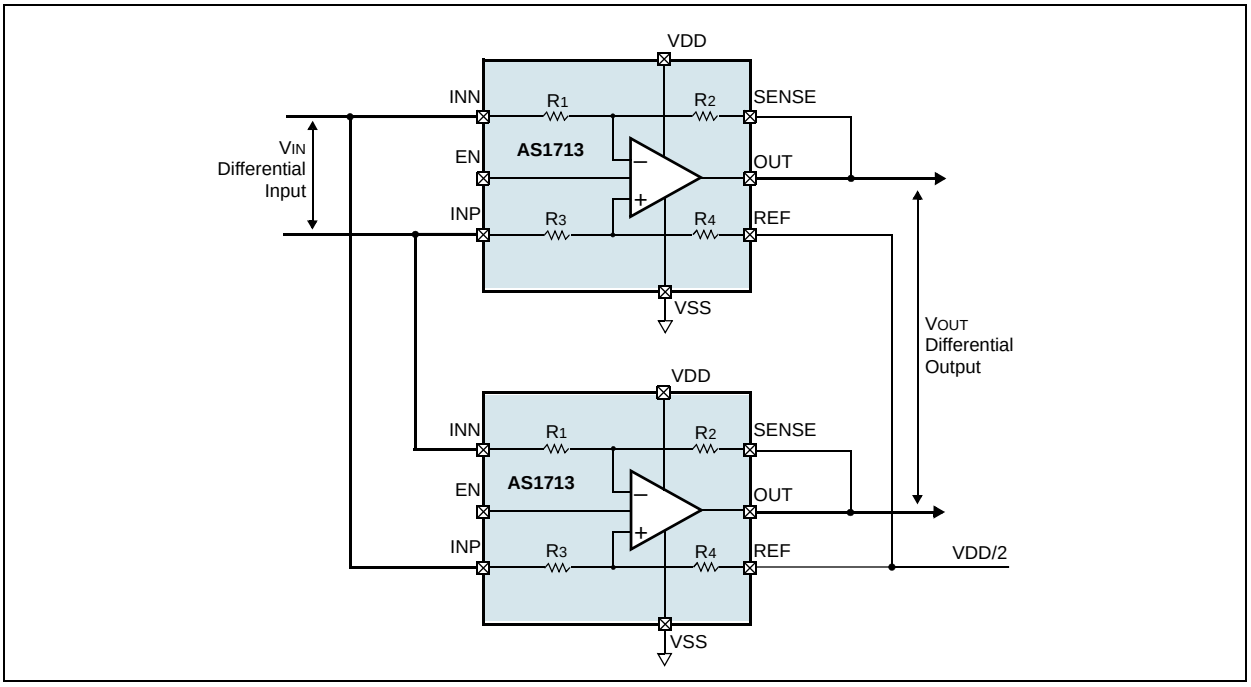
Figure 24. Difference Amplifier



The additional cost of extra matched resistors is offset by the rejection of the unwanted common mode ground interference.

Differential Input / Output Buffer

Figure 25. Differential Input / Output Buffer



Rail-to-Rail Input Stage

The AS1713 CMOS op amps have parallel connected n- and p-channel differential input stages that combine to accept a common-mode range extending to both supply rails. The n-channel stage is active for common-mode input voltages typically greater than (V_{SS} + 1.2V), and the p-channel stage is active for common-mode input voltages typically less than (V_{DD} - 1.2V).

Rail-to-Rail Output Stage

The minimum output is within millivolts of ground for single- supply operation, where the load is referenced to ground (V_{SS}). Figure 26 shows the input voltage range and the output voltage swing of an AS1713 connected as a voltage follower. The maximum output voltage swing is load dependent although it is guaranteed to be within 500mV of the positive rail (V_{DD} = 2.7V) even with maximum load (32Ω to ground) as shown in Figure 27.

Figure 26. Rail-to-Rail Input / Output Range; V_{IN} = V_{DD} = 3.0V, R_{LOAD} = 100kΩ

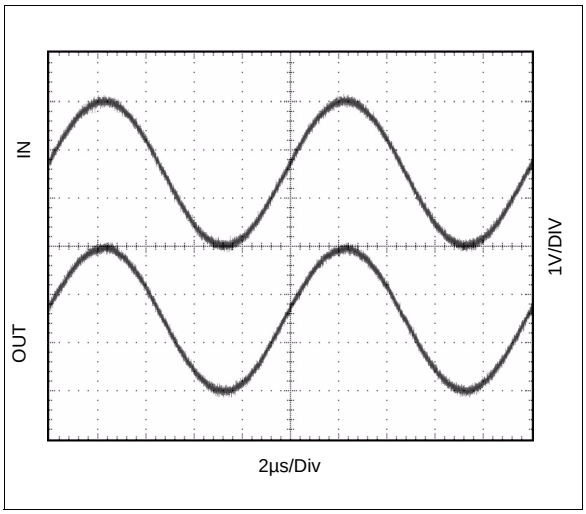
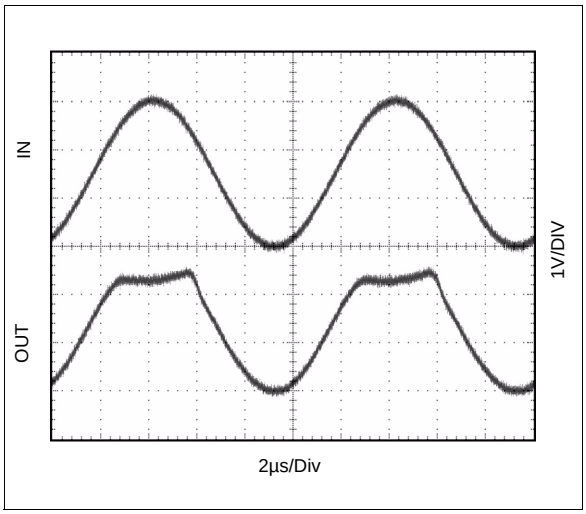


Figure 27. Rail-to-Rail Input / Output Range; V_{IN} = V_{DD} = 3.0V, R_{LOAD} = 32Ω



Note: The absolute maximum ratings (see page 3) for power dissipation and output short-circuit duration (10s, max) must be adhered since the output current can exceed 200mA (see Typical Operating Characteristics on page 6).

Shutdown

When EN is pulled to low, the supply current drops to 0.5µA, the amplifier is disabled and the output is driven to Vss. Pulling EN to high enables the amplifier. When exiting shutdown, there is a 6µs delay before the amplifier output becomes active.

Note: Because the output is actively driven to Vss in shutdown, any pullup resistor on the output causes a current drain from the supply.

Power-Up

The AS1713 typically settle within 5µs after power-up.

Power Supplies and Layout

The AS1713 can operate from a single 2.7V to 5.5V supply or from dual ±1.35V to ±2.5V supplies. Good design improves device performance by decreasing the amount of stray capacitance at the op amp inputs/outputs.

- For single-supply operation, bypass the power supply with a 0.1µF ceramic capacitor.
- For dual-supply operation, bypass each supply to ground.
- Decrease stray capacitance by placing external components close to the op amp pins, minimizing trace and lead lengths.

9 Package Drawings and Markings

Figure 28. MLPD (2x2mm) 8-pin Package

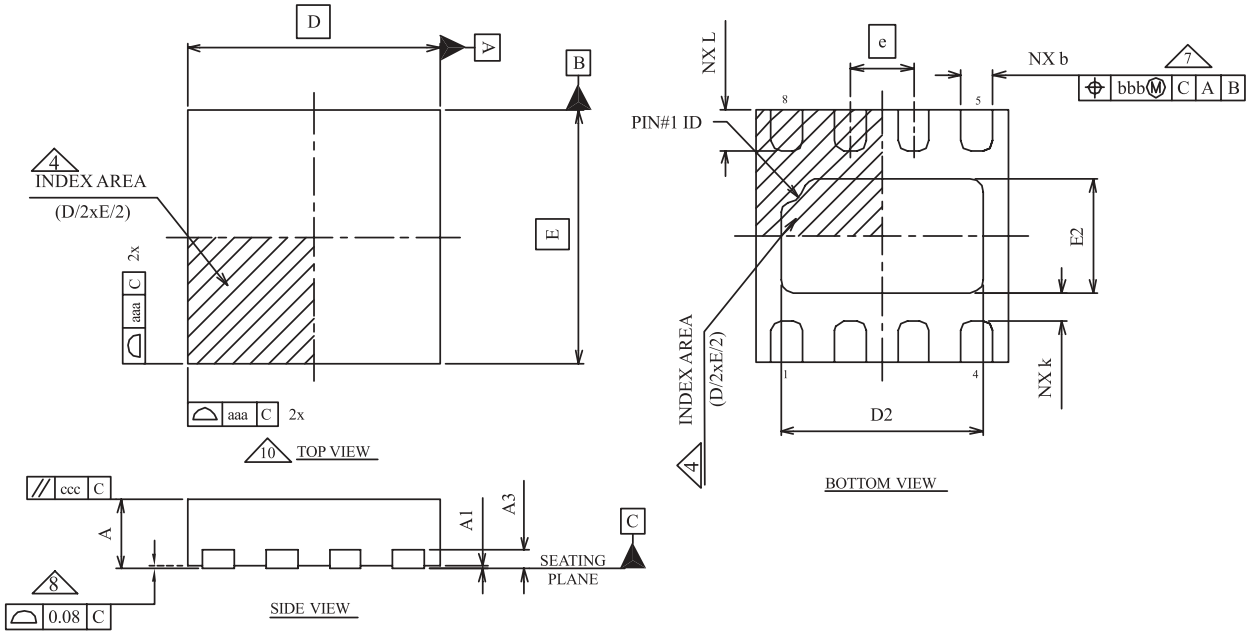


Table 5. MLPD (2x2mm) 8-pin package Dimensions

Symbol	Min	Typ	Max	Symbol	Min	Typ	Max
A	0.51	0.55	0.60	**D**		2.00	
A1	0.00	0.02	0.05	**E**		2.00	
A3		0.15 ref		**D2**	1.45	1.60	1.70
aaa		0.15		**E2**	0.75	0.90	1.00
bbb		0.10		**L**	0.225	0.325	0.425
ccc		0.10		**N**		8	
k	0.20			**ND**		4	
b	0.20	0.25	0.30	**NE**		--	
e		0.50					

Notes:

1. Dimensioning and tolerancing conform to *ASME Y14.5M-1994*.
2. All dimensions are in millimeters, angle is in degrees.
3. Terminal #1 identifier and terminal numbering convention shall conform to JESD 95-1 SPP-012. Details of terminal #1 identifier are optional, but must be located within the area indicated. The terminal #1 identifier may be either a mold, embedded metal or mark feature.
4. Dimension **b** applies to metallized terminal and is measured between 0.15 and 0.30mm from terminal tip.

10 Ordering Information

The device is available as the standard products shown in Table 6.

Table 6. Ordering Information

Model	Marking	Description	Delivery Form	Package
AS1713-BTDT	ABB	Difference Amplifier, 10MHz, 10V/µs, Rail-to-Rail I/O with Shutdown	Tape and Reel	MLPD (2x2mm) 8-pin

All devices are RoHS compliant and free of halogene substances.

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