AS1860 — 60W/90W PoE PD Controllers with HV Isolation and Quad DC-DC Outputs

GENERAL DESCRIPTION

The AS1860 integrates Akros *GreenEdge*™ Isolation technology with next generation Power-over-Ethernet (PoE) PD and integrated isolated high speed digital communication to deliver up to 90W to an isolated secondary side comprising of four independent outputs. Delivering 90W enables a new range of PoE PD capabilities and solutions which greatly expands the markets for PoE.

The AS1860's 90W capability is fully backwards compatible with Type 1 (IEEE® 802.3af) and Type 2 (IEEE® 802.3at) compliant PD. This is integrated with high-voltage isolation and quad-output digital power DC-DC converters – resulting in a complete PoE & Power management solution in a single device with minimal external components.

In addition to enabling digital PoE power conversion, Akros *GreenEdge*™ isolation enables direct digital management of both isolated Primary power and Secondary system power for real time end-to-end Green Power application capabilities.

TYPICAL APPLICATIONS

- Voice-over-IP (VoIP) phones
- Wireless LAN & WiMAX access points (WAP)
- Pan, Tilt, Zoom (PTZ) Cameras, IP cameras
- Thin-client and notebook computers
- Fiber-to-the-home (FTTH) terminals
- Point-of-sale (PoS) terminals, RFID readers

FEATURES

PoE PD Controller

- Fully Integrated 60/90W PD controller
- Backwards compatible with Type 1 and Type 2 IEEE® 802.3af/at Compliant PD
- 60/90W power up can be controlled by PSE or AS1860
- AS1860 will control safe 60/90W delivery from "Dumb" sources
- 4-pair power detection & secondary side logic notification
- Automatic Type 1, Type2 & 60W PoE detection in HW & I²C Modes
- Low Resistance PD Power FET Switch (0.5Ω typical)

Primary-Side DC-DC Controller

- High-efficiency DC-DC Controller with Digital Optimization
- Primary-Secondary High-voltage integrated Digital Isolation
- Programmable Primary Clock Frequency
- Local-power operation down to 9.5V

Secondary-Side Power Outputs

- Programmable PWM Frequencies synched to External Clock
- Output #1: Sync Controller with programmable power-FET timing for high efficiency at both light and full load
- Outputs #2 & #3: Buck Regulators w/2A FETs
- Output #4: DC-DC Controller for Buck, Boost, or LED Boost platform applications

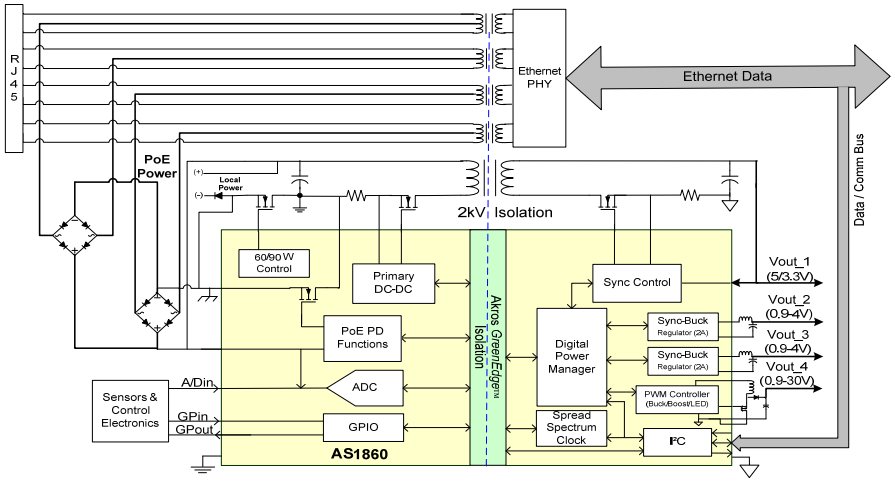
Power Management

- Hardware programmable start-up power sequencing
- Primary-side power monitoring & control from Secondary-side
- Individual output Power-Good management
- Voltage margining for each output
- Primary GPIO/ADC controlled via Secondary GPIO or I²C
- 5V µC-compatible with interrupt on alarm services
- Programmable watchdog timer

EMC Compliance and Protection

- Slew-rate-controlled power drivers
- Multi-phased PWM clocking, with External Sync clock option
- Optional spread-spectrum clocking available for all PWMs
- Over-current, Under/Over-voltage and Short-circuit Protection
- High-temperature warning and shutdown
- Meets IEC 61000-4-2/3/4/5/6, IEC60747, IEC 60950, DIN EN60747-5-2 (VDE0884), & UL1577 requirements for EMC compliance and basic isolation to 2120 VDC (1500 VRMS)
- 100V Process for PoE transient voltage robustness

SIMPLIFIED APPLICATION DIAGRAM



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PIN ASSIGNMENTS AND DESCRIPTIONS

Figure 1 - AS1860 Pin Assignments

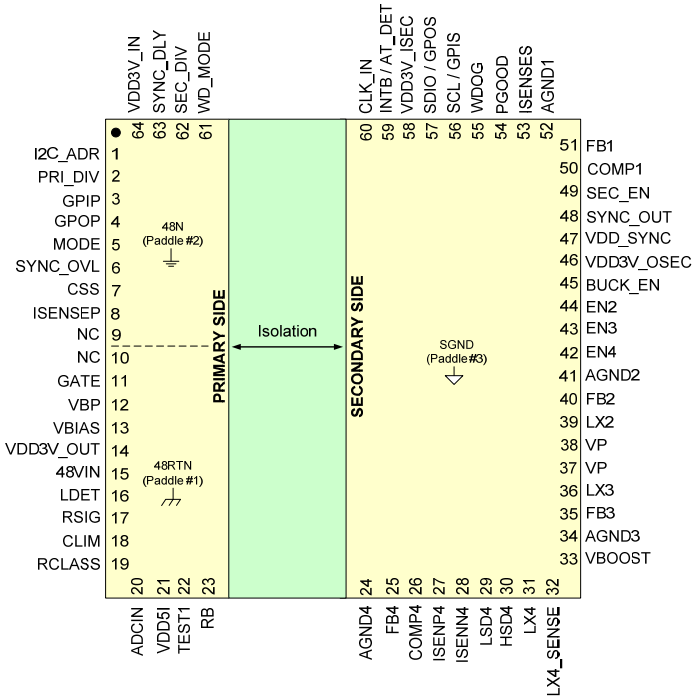


Table 1 - AS1860 Signal Descriptions - Primary Side

Pin	Name	I/O[1]	Description
Primary-Side: PD Controller			
15	48VIN	P	AS1860 startup power input.
Paddle #1	48RTN	P	Input power return. One of three bottom side device connections, 48RTN (Paddle #1) is connected to the internal PD Power MOSFET source. 48RTN is connected to 48N (Paddle #2) via this internal inrush current limiting power MOSFET.
Paddle #2	48N	P	Primary-side Transformer power return. One of three bottom side device connections, 48N (Paddle #2) provides the power return for the DC-DC controller transformer primary. 48N is connected to the internal PD Power MOSFET drain. 48N is connected to 48RTN via this internal inrush current limiting power MOSFET.
16	LDET	D, I	Local Power Enable Input. Enables use of local power for the DC-DC controller and disables PD functions. When activated this disables the PoE PD signature capability that normally uses the RSIG signature resistor. Refer to Figure 3 for a typical LDET circuit configuration and Table 16 for resistor values. If Local power detection is not required, connect LDET to 48VIN. Note that LDET must NOT be tied to 48RTN. In Software mode, the LDET status can be read from the PD Status & Control Register.
19	RCLASS	A	PoE Classification Resistor. See Table 14 for resistor value. Connect the classification resistor between this input and the 48RTN (Paddle #1). The resistor is automatically disconnected after a valid PD classification.
17	RSIG	A, I	PoE Signature Resistor. Connect a 26.7KΩ signature resistor from RSIG to 48VIN. This resistor is automatically disconnected after a valid PD detection.
18	CLIM	I	Sets internal PD Power MOSFET current limit in PoE operation mode; should be pulled either High (VDD5I) or Low (48RTN). In Local Mode (LDET active), CLIM is not used. High = VDD5I = ILIM_AT (see Electrical Characteristics) Low = 48RTN = ILIM_AF (see Electrical Characteristics)
Primary-Side: Common Power Pins			
12	VBP	P	Internal bias node, decouple with an external capacitor to VBIAS.
13	VBIAS	P	Bias voltage input (typically from a power transformer winding).

14	VDD3V_OUT	P	Primary-side supply voltage source (3.3 volts). This supply can be used for additional external circuits on the primary side that are referenced to 48N, see Electrical Characteristics for supply limits.
64	VDD3V_IN	P	Primary-side input supply voltage (3.3 volts) normally connected to VDD3_OUT.
21	VDD5I	P	Low power node that can be used to supply 48RTN referenced devices, see Electrical Characteristics for supply limits. Must be decoupled with an external capacitor.
23	RB	I, PU	PD Controller state machine Power-on-Reset, connect to 48RTN with external capacitor.
Primary-Side: DC-DC Controller			
7	CSS	A	Primary-side PWM Soft Start input, decouple to 48N with an external capacitor.
11	GATE	A	Primary-side external Power FET gate drive.
8	ISENSEP	A	Current sense input, also used to set Primary PWM current limit (with external resistor).
63	SYNC_DLY	A	Along with SYNC_OVL this signal sets Primary and Secondary-side primary sync delay timing for Output #1. Connecting a resistor to ground (48N) from this input will optimize output efficiency for a given PD power level or Sync Power-FET choice. See Table 19 for resistor value selection and other details.
6	SYNC_OVL	A	Along with SYNC_DLY this signal sets Primary and Secondary-side primary sync overlap timing for Output #1. Connecting a resistor to ground (48N) from this input will optimize output efficiency for a given PD power level or Sync Power-FET choice. See Table for resistor value selection and other details.
Primary-Side: Clock Dividers			
2	PRI_DIV	A, I	Primary PWM frequency divider input. Connect an external resistor (5%) from this input to ground to set the Primary PWM clock divider. Used in either internal or external (if the CLK_IN input is active) clocking operation. Note that the Primary PWM clocking rate is a function of both PRI_DIV and SEC_DIV divider ratios. See Device Description, Figure 4 and Table 17 for details.
62	SEC_DIV	A, I	Secondary PWM frequency divider input. Connect an external resistor (5%) from this input to ground to set the Secondary PWM clock divider for either internal or external (if the CLK_IN input is active) PWM clocking operation. Note that the Secondary PWM clocking rate is a function of this SEC_DIV divider ratio. See PWM Clock Generation description for details.
Primary-Side: Inputs & Outputs			
3	GPIP	I, PU	General purpose digital input on primary side, referenced to 48N. See GPIO operation.
4	GPOP	O	General purpose digital output on primary side, referenced to 48N. See GPIO operation.
20	ADCIN	A, I	General purpose ADC input, referenced to 48RTN.
1	I2C_ADR	A, I	Sets the AS1860 I^2C device address. One of 8 possible Device addresses is configured by connecting a resistor on this input to ground (48N). As a result of the chosen resistor, 3 bits of available addressing for the device are configured. See Table 20 for resistor values and other details.
61	WD_MODE	I	Watchdog Timer mode. Enables/disables watchdog timer and sets timer period, operation also varies with MODE input setup. **For Hardware Mode Operation:** WD_MODE = Low (connect to 48N): watchdog off. WD_MODE = Capacitor to 48N: A 1 second timeout generates a PGOOD output transition. WD_MODE = High (connect to VDD3V_OUT): A 32 second timeout generates a PGOOD output transition. **For Software Mode Operation:** WD_MODE = Low (connect to 48N): watchdog off. WD_MODE = Capacitor to 48N: Power-on enables watchdog usage and counter starts (at max count) after PGOOD indicates good power. Use the Watchdog Timeout Register to change timeout count. Watchdog servicing is via Hardware or I^2C commands. WD_MODE = High (connect to VDD3V_OUT): Power-on enables watchdog usage but waits for software to enable before starting. Use Watchdog Timeout Register for timeout length (reset to max). Watchdog servicing is via Hardware pin or I^2C commands.

5	MODE	I	The MODE pin selects the device operation mode at power-on. **For Hardware Mode Operation:** – Mode 1 = Reset mode o Mode 1 is selected by holding the MODE pin Low (MODE to 48N). – Mode 2 = HW Operating Mode o Mode 2 is selected with a pull-up resistor (17.8KΩ max) from MODE to VDD3V_OUT plus a required power-on reset capacitor from MODE to 48N. **For Software Mode Operation:** – Mode 1 = Reset mode o Mode 1 is selected by holding the MODE pin Low (MODE to 48N). – Mode 2 = SW Operating Mode with I²C device address per I2C_ADR pin setting o Mode 2 is selected with a required power-on reset capacitor from MODE to 48N.
Primary-Side: Miscellaneous			
22	TEST1		Must be pulled down to 48RTN with a resistor (4.7KΩ-100KΩ).
9, 10	NC		No User Connection. Must be floated.

[1] I = Input, O = Output, I/O = Bidirectional, PU = Internal pull-up, PD = Internal pull-down, P = Power, A = Analog, D = Digital, OD = Open drain

Table 2 - AS1860 Signal Descriptions - Secondary Side

Pin	Name	I/O[1]	Description
Secondary-Side: Common Power Pins			
Paddle #3	SGND	P	Secondary-side ground connection. One of three bottom side device connections, SGND (Paddle #3) is the Secondary-side ground connection.
37, 38	VP	P	#2, #3, #4 DC-DC regulators and controller power inputs, internally connected together. Must be connected externally to the same source, nominally Output #1
46	VDD3V_OSEC	P	Internal Buck power regulator output. Must be decoupled and used for the VDD3V_ISEC (pin 58) power source. VDD3V_OSEC can also be used for additional 3.3V secondary-side platform power (pull-ups, etc.); see Electrical Characteristics for supply limits.
58	VDD3V_ISEC	P	Secondary-side 3.3V power input. This must be sourced from VDD3V_OSEC (pin 46).
Secondary-Side: Synchronous Rectification Controller (Output #1)			
47	VDD_SYNC	A	Sync FET power decoupling node. Decouple with an external capacitor, VDD_SYNC to SGND. This node is nominally 5V.
51	FB1	A	Controller voltage feedback input.
53	ISENSES	A	Controller secondary-side sync switches node current sense. Sensed signal is used to control the external secondary-side power FET, making it an efficient power diode.
50	COMP1	A	Controller compensation network connection.
48	SYNC_OUT	A	Controller sync gate drive output. Used for secondary-side synchronization in conjunction with the primary-side controller.
52	AGND1	P	Controller secondary-side sense ground, used for both differential feedback and differential current sensing. Should be routed differentially, as the pairs of FB1 & AGND1 and ISENSES & AGND1.
Secondary-Side: Regulator (Output #2)			
41	AGND2	P	Sense ground for the Output #2, should be routed together with FB2 for differential feedback sensing and then tied to ground at the feedback resistor. If Output #2 is not used, AGND2 should still be tied to SGND.
39	LX2	A	Regulator switches node output. If Output #2 is not used, float LX2 (no user connection).
40	FB2	A	Regulator voltage feedback input, also used to disable Output #2 (see EN2).

44	EN2	D, I, PU	Hardware enables control for DC-DC regulator #2. A capacitor to ground applied to this input is required for buck reset before start up. This capacitor also sets the regulator delay start time, complimenting the internal fixed soft-start time. If Output #2 is not used, apply a Low (SGND) to this input, and connect FB2 to VP to fully disable the regulator.
Secondary-Side: Regulator (Output #3)			
34	AGND3	P	Sense ground for the Output #3, should be routed together with FB3 for differential feedback sensing and then tied to ground at the feedback resistor. If Output #3 is not used, AGND3 should still be tied to SGND.
36	LX3	A	Regulator switches node output. If Output #3 is not used, float LX3 (no user connection).
35	FB3	A	Regulator voltage feedback input, also used to disable Output #3 (see EN3).
43	EN3	D, I, PU	Hardware enables control for DC-DC regulator #3. A capacitor to ground applied to this input is required for buck reset before start up. This capacitor also sets the regulator delay start time, complimenting the internal fixed soft-start time. If Output #3 is not used, apply a Low (SGND) to this input, and connect FB3 to VP to fully disable the regulator.
Secondary-Side: Buck or Boost Controller (Output #4)			
45	BUCK_EN	D, I	Selects between Buck and Boost mode of operation for Output #4. Low = SGND = Boost. High = Buck If Output #4 is not used, tie BUCK_EN to SGND.
33	VBOOST	A	Boost voltage decoupling node. Decouple with a capacitor to LX4 when Output #4 is in Buck mode. When operating Output #4 in Boost mode, this input should be connected to Output #1. If Output #4 is not used, VBOOST should be tied to VP.
30	HSD4	A	High Side external Power FET gate Drive. If Output #4 is not used HSD4 should be left floating with no user connection.
29	LSD4	A	Low Side external Power FET gate Drive. If Output #4 is not used LSD4 should be left floating with no user connection.
24	AGND4	P	Sense ground for Controller #4, together with FB4 used for differential feedback sensing at the feedback divider. If Output #4 is not used, AGND4 should still be tied to SGND.
27	ISENP4	A	Positive current sense input. If Output #4 is not used, ISENP4 should be tied to SGND.
28	ISENN4	A	Negative current sense input. If Output #4 is not used, ISENN4 should be tied to SGND.
25	FB4	A	Controller voltage feedback input, also used to disable output (see EN4).
42	EN4	D, I, PU	Enable control for Controller #4. A capacitor to ground applied to this input is required for proper Controller #4 power-on reset and start up. This capacitor also sets the controller delay start time, complimenting the internal fixed soft-start time. If Output #4 is not used, apply a Low (SGND) to this input, and connect FB4 to VP to fully disable the controller.
26	COMP4	A	Controller compensation network connection. If Output #4 is not used COMP4 should be left floating with no user connection.
31	LX4	A	Controller switch sense input. If not used (typical for Boost and LED Boost applications) LX4 should be tied to SGND.
32	LX4_SENSE	A	Remote sense for LX4, used for differential sensing. Should be routed differentially with LX4 (Buck mode). If not used (typical for Boost and LED Boost applications) LX4_SENSE should be tied to SGND.
Secondary-Side: I^2C Interface (or I/O in Hardware Mode)			
57	SDIO / GPOS	OD	SDIO in Software mode, used for I^2C bi-directional data input/output. GPOS in Hardware mode, this output reflects the GPIP pin state (from the primary side).
56	SCL / GPIS	I / I	SCL in Software mode, used as the I^2C clock input. GPIS in Hardware mode is an input that drives the GPOP pin state (on the primary-side).

59	INTB / AT_DET	OD	INTB in Software Mode. The I^2C interface interrupts output, active low. The open drain output allows user defined voltage output high level. AT_DET in Hardware Mode. It is the PoE+ (802.3at) PSE detect indication output. A High level output indicates connection to either a Type 2 PSE or to a Local Power supply. The output is open drain, active High. If a Type 1 PSE is connected, the output of AT_DET remains in the inactive state (Low).
Secondary Side: Inputs & Outputs			
60	CLK_IN	I, PU	DC coupled clock input for timing of Primary and Secondary DC-DC regulators & controllers if synchronizing to an external time source is desired. Nominally sourced from the local Ethernet master clock.
54	PGOOD	OD	Logical "AND" of global power good & watchdog status. High = All enabled voltages (#1 with any or all of #2, #3, and #4) are within voltage spec and there is presently no watchdog timeout. Low = one or more of enabled voltages out of spec, or, the watchdog has timed out. Note that PGOOD operation is different for Hardware and Software modes of operation (selected by the MODE input). For Hardware mode PGOOD operation details see HW Mode Power Monitoring (PGOOD). For Software mode PGOOD operation details see SW Mode Power Status Monitoring (PGOOD).
55	WDOG	I	Watchdog timer input, used for hardware reset of the watchdog timer (if enabled). Serviced with a transition of either polarity.
Secondary I/O: Miscellaneous			
49	SEC_EN	I, PU	Secondary-side Enable. A capacitor on this input to SGND is required.

[1] I = Input, O = Output, I/O = Bidirectional, PU = Internal pull-up, PD = Internal pull-down, P = Power, A = Analog, D = Digital, OD = Open drain

TEST SPECIFICATIONS

Table 3 - Absolute Maximum Ratings

Parameter	Max	Unit
48VIN, 48N, RSIG: to 48RTN	100 [1]	V
48VIN: to 48N	100 [1]	V
48VIN, 48N, RSIG: to 48RTN (under steady-state conditions)	60 [2]	V
48VIN: to 48N (under steady-state conditions)	60 [2]	V
GATE, VBIAS, VBP: to 48N	20	V
LDET: to 48VIN	no more than 6V less than 48VIN	V
RCLASS, CLIM, RB, VDD5I: to 48RTN	6	V
ADCIN to 48RTN	4	V
VDD3V_OUT, VDD3V_IN: to 48N	4	V
ISENSEP, CSS, SYNC_DLY, SYNC_OVL, MODE, GPIP, GPOP, PRI_DIV, I2C_ADR, SEC_DIV, WD_MODE: to 48N	4	V
VBOOST: to SGND	12	V
VP, LX2, LX3, LX4, LX4_SENSE, FB1, FB2, FB3, FB4: to SGND	6	V
CLK_IN, ISENSES, SEC_EN, COMP1, AGND1, PGOOD, VDD3V_ISEC, VDD3V_OSEC: to SGND	4	V
VDD_SYNC, SYNC_OUT, INTB/AT_DET, SCL/GPIS, SDIO/GPOS, WDOG: to SGND	6	V
AGND2, AGND3, AGND4, COMP4, ISENP4, ISENN4, LSD4, HSD4, EN2, EN3, EN4, BUCK_EN: to SGND	6	V
ESD Rating, Human body model (per JESD22-A114)	2	kV
ESD charged device model	500	V
ESD machine model	200	V
ESD System level (contact/air) at RJ-45 (per IEC61000-4-2)	8/15	kV
Storage Temperature	165	°C
Operating Junction Temperature	125	°C

[1] The AS1860 has a fast internal surge clamp for transient conditions such as system startup and other noise conditions; the device must not be exposed to sustained over-voltage condition at this level.
[2] Under steady state conditions; higher voltage level is acceptable under transient conditions.
Unless otherwise noted all Test Specifications apply over the full -40°C to 85°C operating temperature range.
CAUTION: *Exceeding the maximum ratings specified in this table may cause permanent damage to the device.*

Table 4 - Normal Operating Conditions

Parameter	Min	Typ[1]	Max	Unit	Conditions
VIN_AF	37	48	57	V	Measured at the Network Interface
VIN_AT	42.5	48	57	V	Measured at the Network Interface
VAUX (optional local power)	9.5		57	V	Measured at 48VIN for full VLDET range (referenced to 48N)
Thermal Resistance, Junction to Case, θ_{JC}		5		°C/W	Operating Junction Temperature 125°C, max
Thermal Resistance, Junction to Ambient, θ_{JA}		20		°C/W	Operating Junction Temperature 125°C, max
Operating temperature range	-40		85	°C	

[1] Typical specifications not 100% tested. Performance guaranteed by design and/or other correlation methods.

Table 5 - PD Section Electrical Characteristics

Symbol	Parameter	Min	Typ[1]	Max	Unit	Conditions[2]
IINRUSH_AF	Inrush current limit - AF PD		120		mA	13W
IINRUSH_AT	Inrush current limit - AT PD		240		mA	30W
ILIM_AF	PoE current limit - AF PD	350	400	500	mA	13W, CLIM = 48RTN
ILIM_AT	PoE current limit - AT PD	720	750	1000	mA	30W, CLIM = VDD5I

RDS_ON	PD Power MOSFET Switch on Resistance		0.5	0.9	Ω	As measured between 48RTN and 48N with source of 48V and 200ma current.
VRESET_MIN	Minimum reset voltage level			2.81	V	Measured at the Network Interface[2].
VSIGMIN	Minimum Signature voltage			2.7	V	
VSIGMAX	Maximum Signature voltage	10.1			V	
VCLASSMIN	Minimum Classification voltage			14.5	V	In classification, the AS1860 sinks current as defined in Table 14, measured at the Network Interface[2].
VCLASSMAX	Maximum Classification voltage	20.5			V	
VMARKMIN	Min Mark Event voltage		5.2	6.90	V	Measured at the Network Interface[2].
VMARKMAX	Max Mark Event voltage	10			V	
IMARK	Mark Event current	0.5	2.1	4	mA	
VCLASSRSET	Classification Reset threshold	2.81	5.2	6.90	V	
VACT	Full power activation UVLO threshold, voltage rising		37	42	V	
VDEACT	Full power de-activation UVLO threshold, voltage falling	30			V	

[1] Typical values at: Ta = 25°C, Vin = 48VDC. Typical specifications not 100% tested. Performance guaranteed by design and/or other correlation methods.
[2] All measurements at the Network Interface are before the PD diodes (assuming a 1.2V drop across the PD diodes).

Table 6 - Primary Side Digital, I/O, and A/D Electrical Characteristics

Symbol	Parameter	Min	Typ[1]	Max	Unit	Conditions
VDD3V_OUT	Voltage from internally generated 3V source.	3.0	3.3	3.6	V	External bias-winding for VBIAS must be in use. Decouple VDD3V_OUT with 4.7µF cap. Referenced to 48N.
IVDD3V_OUT	Current output from internally generated 3V source.			5	mA	
VDD3V_IN	3V primary side voltage input.	3.0	3.3	3.6	V	Supplied by VDD3_OUT, Referenced to 48N.
VDD5I	Voltage from internally generated 5V node.	4.0	5	6.0	V	Decouple with 1.5µF cap, referenced to 48RTN.
IVDD5I	Current output from internally generated 5V node.			5	mA	
VHGPOP	GPOP voltage output – high	3.0			V	Current at GPOP = 1.0 mA (VDD3V_IN=3.3V, referenced to 48N).
VLGPOP	GPOP voltage output – low			0.4	V	Current at GPOP = -1.0 mA (VDD3V_IN=3.3V, referenced to 48N).
VHGPIP	GPIP voltage input - high	2.0			V	(VDD3V_IN=3.3V, referenced to 48N).
VLGPIP	GPIP voltage input - low			0.8	V	(VDD3V_IN=3.3V, referenced to 48N).
TGPIO	Primary side GPIO pin latency to register update.			10[2]	ms	Independent of I²C clock speed. Pin I/O is automatic to and from I²C registers.
TADCIN	ADCIN pin latency to register update.			10[2]	ms	
VADCIN	ADCIN voltage range	0		2.5	V	Referenced to 48RTN.
RADCIN	ADCIN resolution			8	bits	
ADCERROR	ADCIN total unadjusted error			±TBD[3]	LSB	
ILADCIN	ADCIN input leakage current			100[2]	nA	
CADCIN	ADCIN input capacitance			0.3[2]	pF	

[1] Typical values at: Ta = 25°C, Vin = 48VDC. Typical specifications not 100% tested. Performance guaranteed by design and/or other correlation methods.
[2] Guaranteed by design. Not tested in production.
[3] Includes offset, full-scale, and linearity.

Table 7 - Primary Side DC-DC Controller Electrical Characteristics

Symbol	Parameter	Min	Typ[1]	Max	Unit	Conditions
VIN_AF	Type 1 PD input voltage	37	48	57	V	Measured at the Network Interface
VIN_AT	Type 2 PD input voltage	42.5	48	57	V	Measured at the Network Interface
VAUX	Input Voltage, Local Power Mode	9.5		57	V	Measured at 48VIN (referenced to 48N) over full VLDET range
VLDET_ON	Local input voltage threshold for Local Power Mode - ON	48VIN -2.4V			V	See Table 3 for Absolute Maximum Rating for LDET (referenced to 48VIN).
VLDET_OFF	Local input voltage threshold for Local Power Mode - OFF			48VIN-1.2V	V	
VBIAS	External bias source voltage	8[2]		14[2]	V	Sets VOH of GATE.
FPWM1L	Low end of Primary PWM switching frequency range		104		KHz	Set by external resistors on PRI_DIV and SEC_DIV pins see Table 17.
FPWM1H	High end of Primary PWM switching frequency range		512		KHz	Set by external resistors on PRI_DIV and SEC_DIV pins see Table 17.
FOSC1	PWM1 clock frequency accuracy	-20		+20	%	See Table 17 for frequency.
FPWM1T	PWM switching frequency temperature coefficient		0.12		%/C°	Refer to Table 17 for PWM Frequency.
RH_GATE	GATE drive impedance		6		Ω	High side output drive resistance, Source.
RL_GATE			6		Ω	Low side output drive resistance, Sink.
VPK1P	Peak current sense threshold voltage at ISENSEP		395		mV	Ipeak = VPK1P / RISENSEP.
DMAX1	Primary PWM Maximum duty cycle	80[3]			%	
DMIN1	Primary PWM Minimum duty cycle			10[3]	%	

[1] Typical values at: Ta = 25°C, Vin = 48VDC. Typical specifications not 100% tested. Performance guaranteed by design and/or other correlation methods.
[2] Guaranteed by characterization. Not tested in production.
[3] Guaranteed by design. Not tested in production.

Table 8 - Secondary Side Sync Controller (Output #1) Electrical Characteristics

Symbol	Parameter	Min	Typ[1]	Max	Unit	Conditions
VSYNC_OUT	SYNC_OUT voltage	4.5	5	6	V	
RH_SYNC	SYNC_OUT Source Impedance			2.5	Ω	Source
RL_SYNC	VDD_SYNC = 5V			2.5	Ω	Sink
VMR1	Output 1 voltage margining range		±5		%	Software mode, see Table 37.
VREF1	FB1 voltage reference	0.98	1.0	1.02	V	
ILEA1	Error amp leakage			1[2]	µA	
Gm1	Feedback Transconductance (Siemens)	150	225	350	µS	

[1] Typical values at: Ta = 25°C, Vin = 48VDC. Typical specifications not 100% tested. Performance guaranteed by design and/or other correlation methods.
[2] Guaranteed by design. Not tested in production.

Table 9 - Secondary Side DC-DC Regulators (Outputs #2, #3) Electrical Characteristics

Symbol	Parameter	Min	Typ[1]	Max	Unit	Conditions
VP	Input Voltage at both VP pins	2.97		5.5	V	Nominally from Output #1
VOUT23_MIN	Output Voltage - Min		0.8		V	
VOUT23_MAX	Output Voltage - Max		VP-0.7		V	
TEN23_DLY	External EN2/3 power-on delay (cap on the EN2/3 pin)	8[2]			ms	SEC_EN cap = 10nF (typical)
VEN23_ON	EN2/3 threshold – On	0.75	0.82	1.0	V	Low to high transition
VEN23H	EN2/3 hysteresis	100		200	mV	
FPWM23L	Low end of PWM2 / PWM3 switching frequency range		500		KHz	Set by external resistors on PRI_DIV and SEC_DIV pins see Table 17.
FPWM23H	High end of PWM2 / PWM3 switching frequency range		2000		KHz	Set by external resistors on PRI_DIV and SEC_DIV pins see Table 17.
FOSC23	PWM2 / PWM3 clock frequency accuracy	-20		+20	%	See Table 17 for frequency.
DMAX23	PWM2/3 Maximum duty cycle	85[2]			%	
DMIN23	PWM2/3 Minimum duty cycle			10[2]	%	
IOUT23	Output Current	0		2[2]	A_{RMS}	RMS output current.
RPFET23	P-Channel Rdson, #2 and #3 Outputs			180[2]	mΩ	VP = 5.0V
RNFET23	N-Channel Rdson, #2 and #3 Outputs			120[2]	mΩ	VP = 5.0V
LXLI23	LX2, LX3 Leakage Current		0.1	1[2]	µA	
LXIM23	Output #2, #3 Current Limit	3[2]			A_{PEAK}	Peak output current.
VMR23	Outputs #2, #3 voltage margining range		-8 / +6		%	Software mode, see Table 37 and Table 38.
VREF23	FB2 and FB3 Reference Voltage	784	800	816	mV	
ILFB23	FB2 and FB3 Leakage Current			0.2[2]	µA	
IL_EN23	EN2/EN3 Leakage Current	9	10	11	µA	
IOFF23	#2 and #3 Regulator Shutdown Current		0.1	1.0[2]	µA	EN2, EN3 in disabeled mode

[1] Typical values at: Ta = 25°C, Vin = 48VDC. Typical specifications not 100% tested. Performance guaranteed by design and/or other correlation methods.
[2] Guaranteed by design. Not tested in production.

Table 10 - Secondary Side DC-DC Controller (Output #4) Electrical Characteristics

Symbol	Parameter	Min	Typ[1]	Max	Unit	Conditions
VOUT4_MIN_BUCK	Buck Output Voltage – Min		0.8		V	
VOUT4_MAX_BUCK	Buck Output Voltage – Max		VP-0.7		V	
VOUT4_MAX_BOOST	Boost Output Voltage - Max		30V		V	
TEN4_DLY	External EN4 power-on delay (cap on the EN4 pin)	8[2]			ms	SEC_EN cap = 10nF (typical)
VEN4_ON	EN4 Threshold – On	0.75	0.82	1.0	V	Low to high transition

VEN4_H	EN4 hysteresis	100		200	V	High to low transition
VBUCK_EN_HI	BUCK_EN input voltage threshold - high	2.0			V	
VBUCK_EN_LOW	BUCK_EN input voltage threshold - low			0.8	V	
FPWM4L	Low end of PWM4 switching frequency range		125		KHz	1/4 of internal Buck frequency. Set by external resistors on PRI_DIV and SEC_DIV pins; see Table 17.
FPWM4H	High end of PWM4 switching frequency range		500		KHz	
FOSC4	PWM4 clock frequency accuracy	-20		+20	%	See Table 17 for frequency.
RH_HSD4	HSD4 drive impedance		4		Ω	High side output drive resistance, Source
RL_HSD4			4		Ω	High side output drive resistance, Sink
RH_LSD4	LSD4 drive impedance		4		Ω	Low side output drive resistance, Source
RL_LSD4			4		Ω	Low side output drive resistance, Sink
VPK4N	Peak current sense threshold voltage at max load (ISENP4 – INSENN4)		60		mV	IL max
VPK4SS	Peak current sense threshold voltage at short circuit (ISENP4 – ISENN4)		90		mV	current limit (typically 50% above IL max)
DMAX4	PWM4 Maximum duty cycle	85[2]			%	
DMIN4	PWM4 Minimum duty cycle			10[2]	%	
ILLX4	LX4 Leakage Current		0.1	1[2]	µA	
VMR4	Output #4 Voltage Margining Range		-8 / +6		%	Software mode, see Table 37 and Table 38.
VREF4	FB4 Reference Voltage	784	800	816	mV	
ILFB4	FB4 Leakage Current			0.2[2]	µA	
IL_EN4	EN4 Leakage Current	9	10	11	µA	
Gm4	Feedback Transconductance	50	78	95	µS	Units in µSiemens.
IOFF4	#4 Controller Shutdown Current		0.1	1.0[2]	µA	EN4 in disable mode

[1] Typical values at: Ta = 25°C, VP = 5VDC. Typical specifications not 100% tested. Performance guaranteed by design and/or other correlation methods.
[2] Guaranteed by design. Not tested in production.

Table 11 - Secondary Side Digital I/O and I²C Electrical Characteristics

Symbol	Parameter	Min	Typ[1]	Max	Unit	Conditions
VDD3V_OSEC	Internally generated 3V source, referenced to SGND.	3.0	3.3	3.6	V	
IVDD3V_OSEC	VDD3V_OSEC current output (internally generated 3V source), referenced to SGND.			5	mA	
VDD3V_ISEC	Power Supply Input Voltage	3.0	3.3	3.6	V	Sourced from VDD3V_OSEC
FCLK_IN	External Clock Input Frequency	23.75	25	26.25	MHz	
VCLK_IN_HI	CLK_IN input voltage threshold - high	2.0			V	
VCLK_IN_LOW	CLK_IN input voltage threshold - low			0.8	V	
IOINTB	INTB/AT_DET open drain current drive	1			mA	With $V_{PULL-UP}$ = TBD and $R_{PULL-UP}$ = TBDKΩ, V_{INTB} (typ) = TBD
IOPG	PGOOD open drain current drive	1			mA	With $V_{PULL-UP}$ = TBD and $R_{PULL-UP}$ = TBDKΩ, V_{PGOOD} (typ) = TBD
TPGOOD	PGOOD minimum pulse output (High-Low-High)	10[2]			ms	
TWDOG	Watchdog minimum reset pulse width (WDOG pin)	100[2]			ns	
VHGPOS	GPOS voltage output – high (referenced to SGND)	3.0			V	Current at GPOS = 1.0 mA (VDD3V_ISEC=3.3V, referenced to SGND)
VLGPOS	GPOS voltage output – low (referenced to SGND)			0.4	V	Current at GPOS = -1.0 mA (VDD3V_ISEC=3.3V, referenced to SGND)
VHGPIS	GPIS voltage input – high (referenced to SGND)	2.0			V	(referenced to SGND)
VLGPIS	GPIS voltage input – low (referenced to SGND)			0.8	V	(referenced to SGND)
FSCL	I²C Clock Frequency	10		400	KHz	5V tolerant input
VIH	I²C HIGH level input voltage	1.4			V	5V tolerant input
VILI2C	I²C LOW level input voltage			0.5	V	5V tolerant input
VOLI2C	I²C Output low voltage for pull-up voltage (VDD)			0.4 0.2VDD	V V	VDD > 2V, 2 mA sink VDD < 2V, 2 mA sink
CDIO	Capacitance for each Digital I/O pin			10[2]	pF	

[1] Typical values at: Ta = 25°C, Vin = 48VDC. Typical specifications not 100% tested. Performance guaranteed by design and/or other correlation methods.
[2] Guaranteed by design. Not tested in production.

Table 12 - Thermal Protection Electrical Characteristics

Symbol	Parameter	Min	Typ[1]	Max	Unit	Conditions
T_{SD}	Thermal shutdown temperature		140		°C	Above this temperature, the AS1860 is disabled.
T_{I2C}	Thermal warning temperature for I^2C warning		115		°C	
T_{HYS}	Thermal shutdown hysteresis		40		°C	Temperature change required to restore full operation after thermal shutdown

[1] Typical values at: Ta = 25°C, Vin = 48VDC. Typical specifications not 100% tested. Performance guaranteed by design and/or other correlation methods.

Table 13 - Isolation Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
IIO_ISO	Input-output insulation			1.0[1]	µA	RH (Relative Humidity) = 45%, Ta = 25°C, t = 5s leakage current VIO_ISO = 2250 VDC
VISO_DC	Withstand insulation voltage DC	2120[1]			VDC	RH ≤ 50%, Ta = 25°C, t = 1 min
VISO_AC	Withstand insulation voltage AC	1500[1]			V_{RMS}	RH ≤ 50%, Ta = 25°C, t = 1 min
RIO_ISO	Resistance (input to output)		TBD[1]	TBD[1]	Ω	VIO = 250 VDC
CM	Common mode transient		10.0[2]		kV/µs	

[1] Device is considered a two terminal device: Primary pins are shorted together and Secondary pins are shorted together.
[2] All outputs to remain within ±3% tolerance during transient.

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 2 - Vin=38V 12V 2.5A Start Up

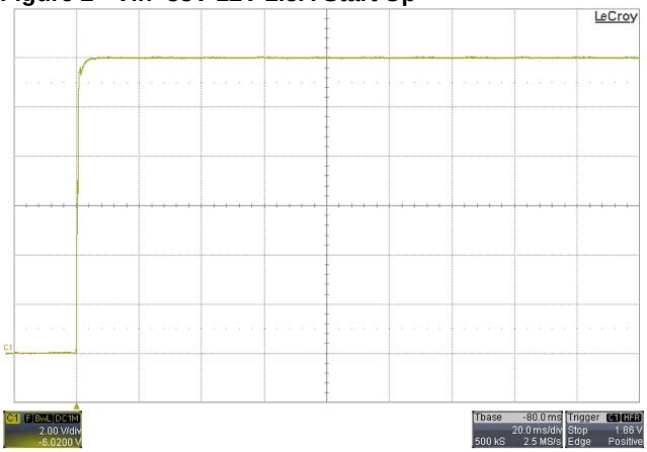


Figure 3 - Vin=40V_12V_2.5A _Start Up with el load

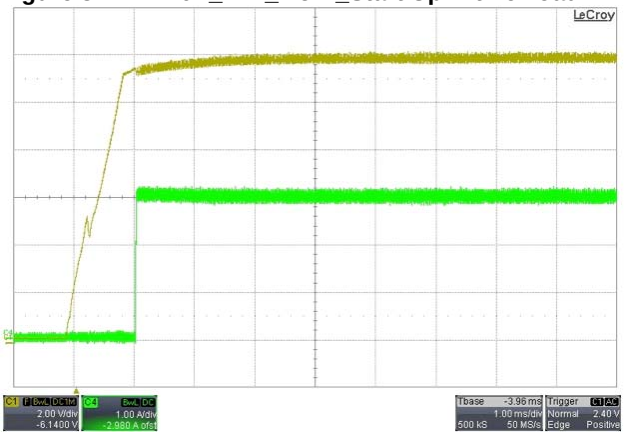


Figure 4 - Vin=57V_12V_3A _Start Up with el load

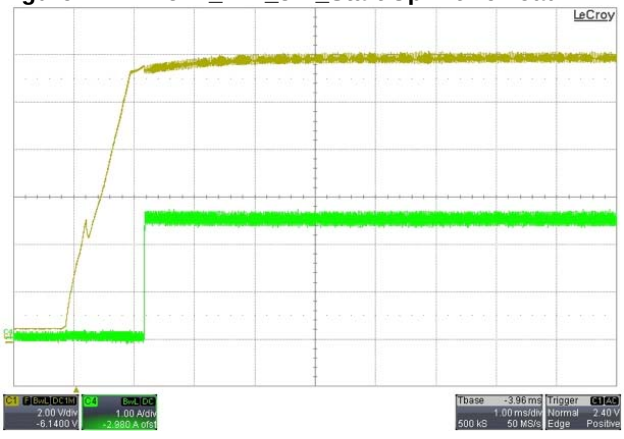


Figure 5 - Vin=48V_12V_3A _Start Up with el load

Figure 6 - Vin=48V_12V_3A _Start Up

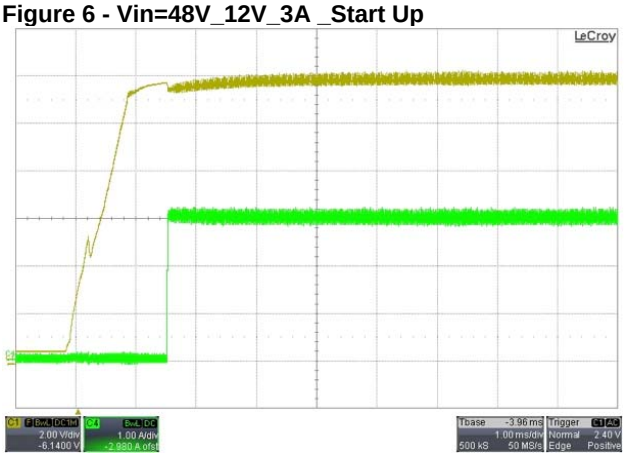


Figure 7 - Vin=57V_12V_3A _Start Up

FUNCTIONAL DESCRIPTION

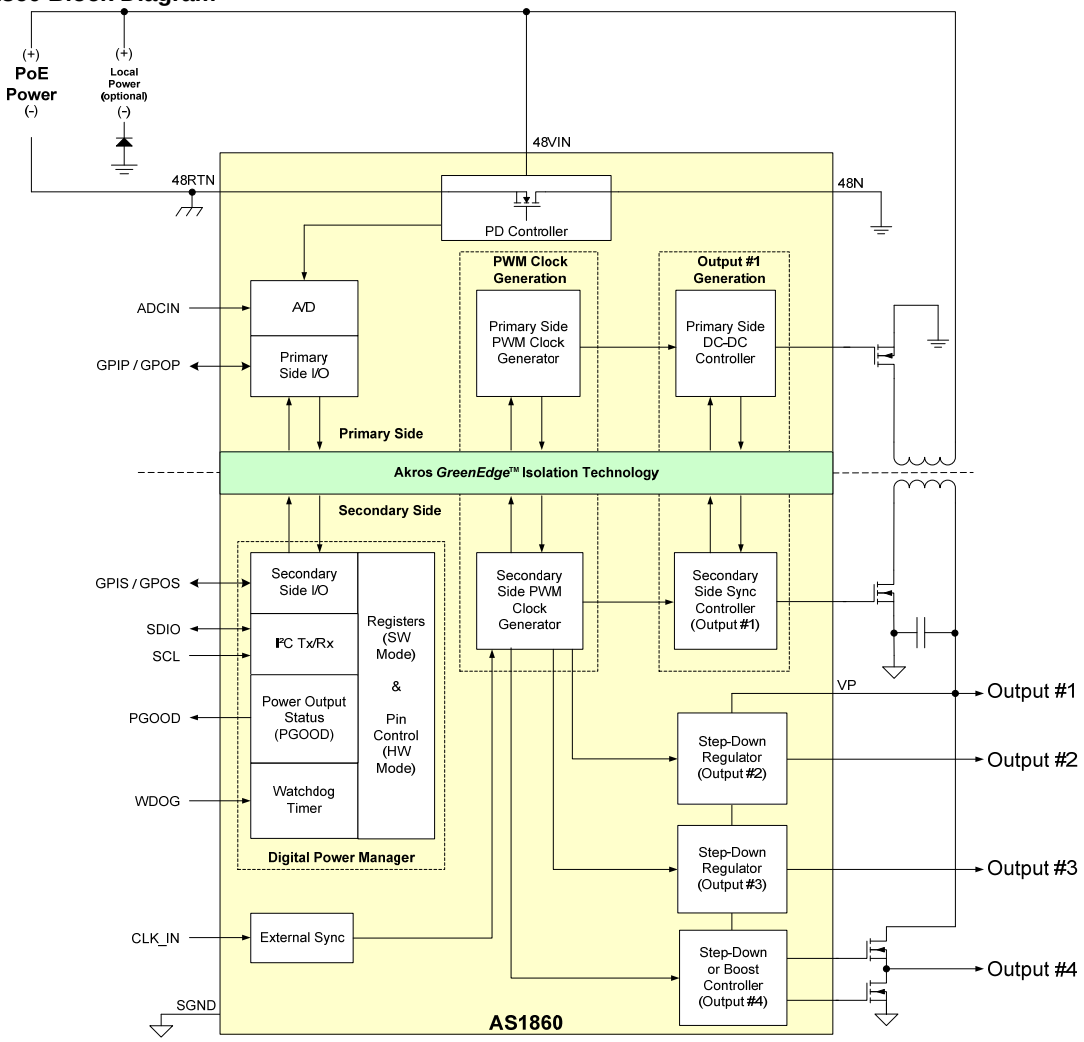
Figure 8 shows the block diagram of the AS1860. The individual blocks are described in greater detail in the following paragraphs.

(Please also refer to these separate Akros documents for the AS1860: AN080 for a detailed Design Guide and AN082 for a detailed Software Users Guide.)

ISOLATION

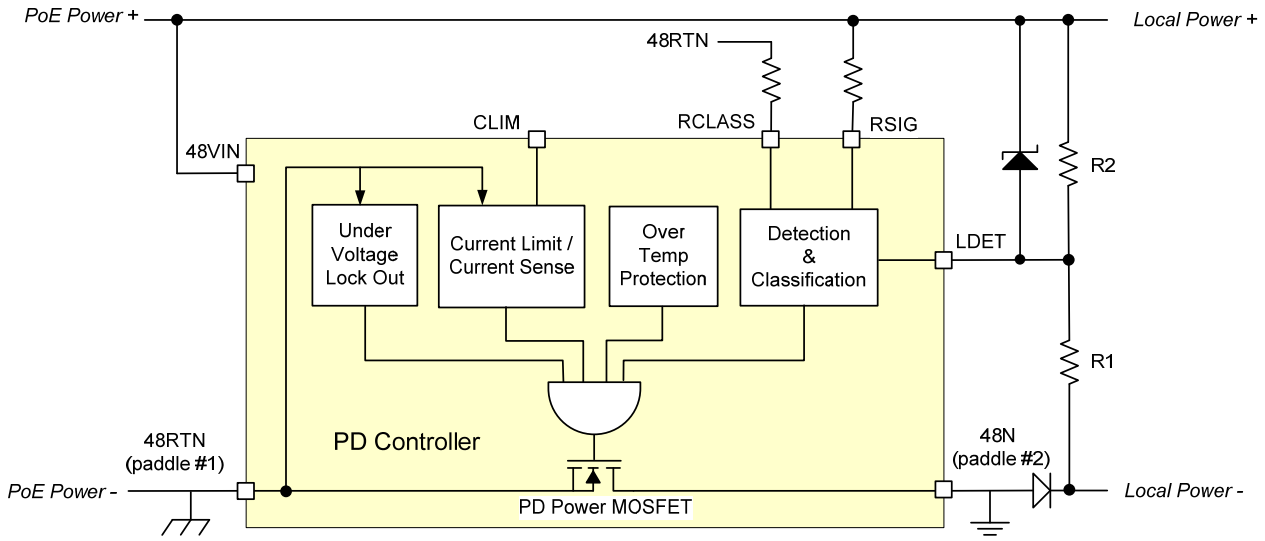
As shown in Figure 8, the AS1860 is divided internally into Primary and Secondary sides. All signals that interconnect the Primary and Secondary sides are isolated using Akros *GreenEdge*™ technology eliminating the need for opto-isolators in both analog power control loop and the digital I²C paths between Primary and Secondary ground planes.

Figure 8 - AS1860 Block Diagram



PD CONTROLLER

Figure 9 - AS1860 PD Controller Block Diagram



The AS1860 contains a fully integrated PD Controller (see Figure 9) that meets all system requirements for the IEEE® 802.3 standard for Ethernet, and, all PD power management requirements for IEEE® Standards 802.3af and 802.3at and for the emerging 60/90W standard. 60W/90W power delivery can be implemented in a number of ways using the AS1860's flexible architecture. See the Power over Ethernet overview on page 43 in this datasheet for additional PoE information.

PD Power MOSFET

Ethernet power source current is controlled with an integrated low-leakage, low RDSON, NMOS power MOSFET that is used to connect the 48RTN and 48N ground planes. If necessary the FET is throttled back or switched off to protect the AS1860 from damage due to problematic voltage, current, or temperature related conditions. For power levels greater than the AF or AT standards, an external power FET is placed in parallel with the internal FET. Gate control of this external FET is detailed in the 60/90W applications section.

Under-voltage Lockout (UVLO)

The UVLO circuitry detects low power source voltage conditions and disconnects the power MOSFET to protect the PD (see full power voltage activation and deactivation threshold specifications in the PD Electrical Characteristics).

PoE Current Limit/Current Sense

Current Limit/Current Sense circuitry minimizes on-device temperature peaks by limiting both inrush current and operating current. It monitors the current via an integrated sense circuit that regulates the gate voltage to the PD Power MOSFET.

This inrush current limiting maintains the cable voltage above the turn-off threshold as the input capacitor charges, an action that aids in preventing the PSE from going into current limit mode.

The PoE current limit is set by the CLIM input pin during PoE operating modes. When CLIM is set Low (48RTN) current is limited to 350mA (min); when High, 720mA (min). If the maximum primary current is exceeded, control of the internal PD Power MOSFET is used to protect the system from overload. In Local Power mode (LDET active), this CLIM based current control is not used (primary side external FET sensed current control can always be used).

Over-temperature Protection

If die temperature exceeds 140°C (typ) the AS1860 is shut down. Power is automatically reapplied when the die temperature returns to 100°C (typ).

PD Operating States

The AS1860 has five states of PD operation:

- ***Reset*** - The classification state machine is reset, and all circuitry blocks are disabled.
- ***Signature Detection*** - The PD signature resistance is applied across the input.
- ***Classification*** - The AS1860 indicates power requirements to the PSE.
- ***Idle*** - This state is entered after classification, where it remains until full-power input voltage is applied.
- ***ON*** - The PD is enabled, and supplies power to the DC-DC controller and the local application circuitry. In this state the PD also provides a Maintain Power Signature (MPS) state as required by the IEEE® PoE standard.

As the supply voltage from the PSE increases from 0V, the AS1860 transitions through these operating states:

These five operating states have specific transition criteria per the IEEE® PoE standard.

PD Reset State
When the voltage supplied to the AS1860 drops below VRESET_MIN, the device enters the reset state. In reset state, the AS1860 consumes very little power, the power supply to the PD is disconnected and state condition reverts to pre-classification.

PD Signature Detection State
During signature detection, the PSE applies a voltage to read the PD power signature and validates the PD as standards compliant.

To ascertain the power signature the PSE applies two voltages in the signature voltage range and extracts a signature resistance value from the I-V slope. The AS1860 signature resistance is specified by an external resistor connected between the RSIG pin and the 48VIN pin. A 26.7kΩ external signature resistor is recommended.

Upon successful detection of the PD by a PSE the AS1860 disconnects the external signature resistor at the RSIG pin to conserve power.

PD Classification State
Each class represents a power allocation level for the PD and allows the PSE to manage power requirements between multiple PDs. The AS1860 supports both IEEE® Std. 802.3af, and two event classification per IEEE® Std. 802.3at (PoE+), see Figure 29.

The AS1860 allows the user to set required classification current via an external resistor connected between the RCLASS pin and 48RTN (Paddle #1). See Table 14 for recommended RCLASS resistor values.

During the classification state the PSE presents a voltage between 14.5V and 20.5V which the AS1860 terminates in the RCLASS resistor resulting in a PSE measurable current, Iclass.

Table 14 - Classification Map

Class	Power (Watts)	Iclass	Rclass
0	0.44-12.95	0 - 4 mA	2.05MΩ, 1%
1	0.44-3.84	9 - 12 mA	221kΩ, 1%
2	3.84-6.49	17 - 20 mA	115kΩ, 1%
3	6.49-12.95	26 - 30 mA	75kΩ, 1%
4	12.96-25.5	36 - 44 mA	49.9kΩ, 1%

Upon successful classification of the PD by a PSE the AS1860 disconnects the external classification resistor at the RCLASS pin.

PD Idle State
In the Idle state (between Classification and the ON state) the AS1860 current is limited to monitoring circuitry needed for detection of the ON state threshold.

PD ON State
At a voltage of 42V or higher the AS1860 enters the ON state and full power is available via the DC-DC Controller.
In IEEE® PoE compliant systems the PSE remotely detects either a DC or AC Maintain Power Signature (MPS) state in the PD platform. If either the PD PoE DC current is less than 10mA or the PD input AC impedance is above 26.25KΩ the PSE may disconnect power. To guarantee such a power disconnect the PD PoE DC current must be <5mA, and, the AC impedance must be >2MΩ.

AT Detection Operation

The AS1860 has both software (I^2C register bit) and hardware (AT_DET pin) capabilities to indicate a PoE Plus platform operating mode.
The AT_DET detect feature (either pin or software) provides an indication when a PoE+ Power Source is available to the system, from either an Ethernet cable to a Type 2 PSE or via use of Local Power Supply using the LDET input pin. In the case of hardware mode the AT_DET pin can be used to directly drive an LED indicator. Since this pin is on the secondary side of the AS1860 the user can interface it directly to the PD system controller without additional interfacing isolation circuitry. A typical platform usage of AT_DET is to self-configure the PD platform based on available power.

If not operating on Local Power, the AT_DET indicator stays low during the PD Reset, Detection and Classification phases. This indicator will be set high once the PD recognizes completion of the 2-event Physical Layer Classification as initiated by a Type 2 PSE. The pin will remain high and be reset to zero after the occurrence of a PD Reset State (48VIN < 2.7V) or a power-down event. AT_DET remains low if the PSE partner is identified to be Type 1 during the classification phase.

Local Power Source

As mentioned above the AS1860 may also be powered from a DC source other than the Ethernet line. This local source is detected when the voltage at the LDET pin is 2 volts (typ) below the voltage at pin 48VIN. When such a local power is present the AS1860 will disable the power FET and thereby disconnect from the PoE power source.

When operating in Local Power mode the AT_DET pin does not indicate the far end PSE, and is always HIGH (see Table 15).

Refer to Figure 9 and Table 16 for typical LDET external resistor designs to match the specified Local Power configuration.

Table 15 - AT_DET and LDET Operation

LDET Mode	AT_DET Indication	
	PSE = Type 1	PSE = Type 2
LDET = Inactive (PoE power usage)	LOW	HIGH
LDET = Active (Local Power usage)	HIGH	HIGH

Table 16 - Typical LDET External Resistor Design

Local Adaptor or Local Voltage Requirement	Typical LDET Voltage Range to Cover Adaptor(s)	R1[1] (Ω)	R2[1] (Ω)
12V, 18V	10.8-22 VDC	47K	15.6K
18V, 24V, 30V	14-32 VDC	47K	10K
30V, 36V, 48V	26-57 VDC	47K	5K

[1] **Note:** See Figure 3 on 23.

The maximum voltage allowed from 48VIN to LDET is 6.0V; refer to Table 3 on 7. Therefore some LDET input range requirements (beyond those shown in Table 16) might require the use of a Zener, 5.1V typical, as shown in Figure 3 on 23.

PWM CLOCK GENERATION

Figure 10 shows the AS1860 PWM Clock Generation block diagram. During power-up, local oscillators on both sides of the isolation boundary provide separate clocks for Primary-side and Secondary-side PWMs. After power-up internal cross-isolation management automatically transitions all AS1860 PWM clocks such that the Secondary-side oscillator becomes the master, and sources multi-phase clocks to both Primary and Secondary PWMs.

PWM Clock Frequency Configuration

Frequencies of all AS1860 PWM clocks are set with resistors connected to the PRI_DIV and SEC_DIV pins as shown in Table 17.

External Clock Source (CLK_IN)

For additional EMI management, the CLK_IN pin provides an optional input for an external clock source to govern overall device timing. If used the local Secondary-side oscillator is slaved to CLK_IN, therefore Primary-side and Secondary-side PWM clocks are slaved to CLK_IN after power-up. The CLK_IN frequency should be 25MHz, and it is recommended that the Ethernet PHY clock be used.

EMI Performance Control

A multi-phase clocking technique is used to generate clocks for the Primary DC-DC controller and all Outputs (1-4). This improves Electromagnetic (EM) radiation performance by reducing common mode noise and also reduces the size of external capacitors.

Note that in Software mode, PBRS randomization and Fractional-N modulation clocking is available for additional EM performance to reduce PWM clock induced harmonics in the power supply.

Figure 10 - PWM Clock Generation Block Diagram

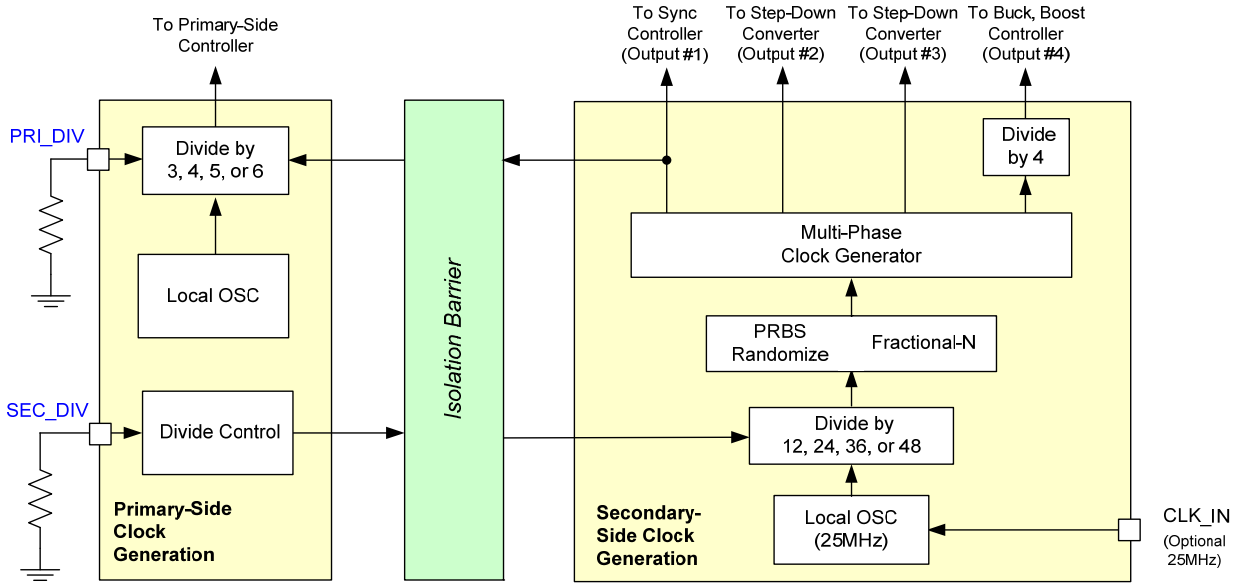


Table 17 - PWM Clock Rate Configuration

AS1860 Master Clock Rate = Internal (or 25MHz if using CLK_IN)		PRI_DIV Resistor (Ω)			
		12.4K	43.2K	68.1K	100.0K
SEC_DIV Resistor (Ω)	Outputs #2/#3/#4 PWM Clock Rates (MHz)	Output #1 PWM Clock Rate (KHz)			
12.4K	2.08 / 2.08 / 0.520	reserved	521	417	347
43.2K	1.04 / 1.04 / 0.260	347	260	208	174
68.1K	0.69 / 0.69 / 0.173	231	174	139	116
100.0K	0.52 / 0.52 / 0.130	174	130	104	reserved

Power Output #1

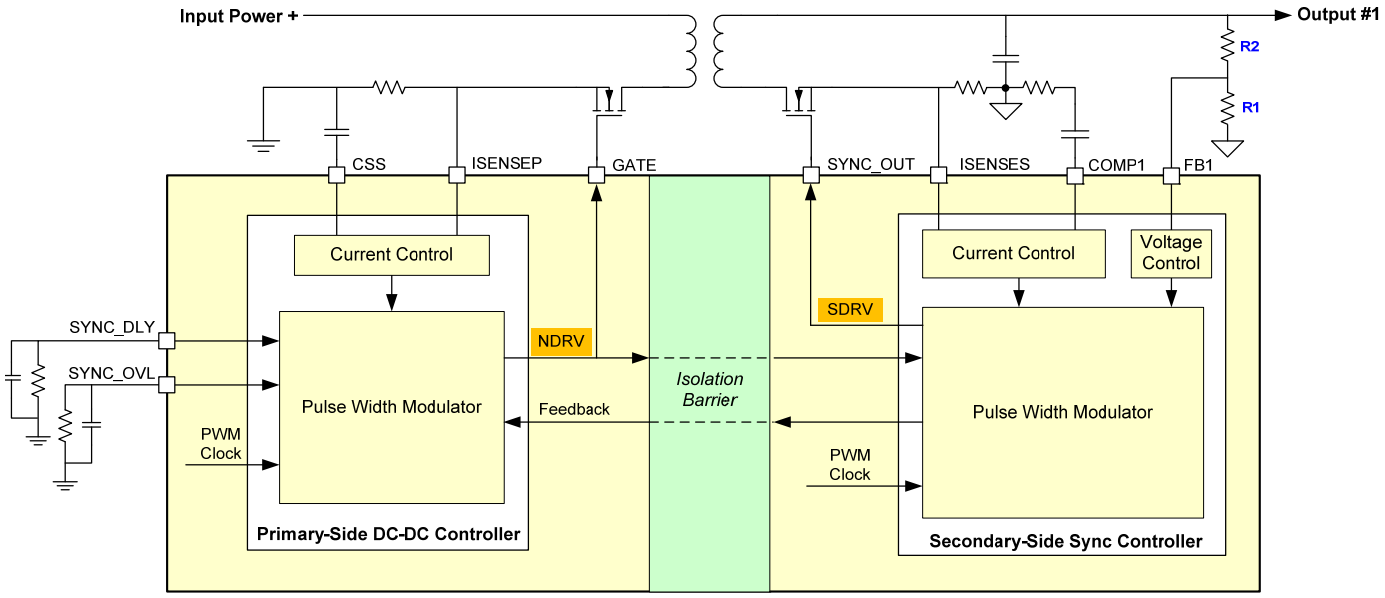
Output #1 is the main AS1860 power output and is typically used to supply the DC power that generates Outputs #2 thru #4. As described in the previous section, the Primary and Secondary-side PWM clocks are generated and automatically synchronized across the integrated isolation barrier. Figure 11 shows a typical synchronous Fly back design topology for Output #1.

Three power control loop operations take place:

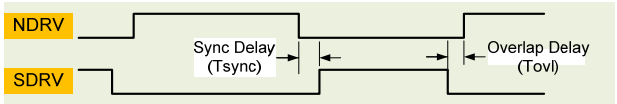
- Primary-side DC-DC controller FET driver switches the primary-side power FET from a loop error controlled PWM.
- Secondary-side sync controller FET driver switches the Secondary-side power FET to complete the Flyback power transfer cycle.
- The automated AS1860 isolation management transmits Secondary-side loop feedback to the Primary-side PWM.

A typical isolated synchronous Flyback application is shown in more detail in Figure 36.

Figure 11 - Power Output #1 Block Diagram



NDRV and SDRV timing delays, Sync Delay & Overlap Delay, are based on SYNC_DLY and SYNC_OVL resistor settings. These internally generated delays can be used to cost effectively optimize an Isolated Synchronous Flyback Design.



Primary-side DC-DC Controller

The Primary-side DC-DC Controller is a current-mode DC-DC controller which is easily configured with a minimal set of external components. Isolation is provided by the internal Akros *GreenEdge*™ circuitry which eliminates the need for external opto-isolators.

In PoE operation, the Primary-side DC-DC Controller operates from a PD Power MOSFET switched power input (48N, see Figure 2) and includes: an externally controlled soft start; a fixed (after resistor programming) frequency PWM; and a true voltage output error amplifier. In local

power operation 48N is sourced directly.

Soft-Start Inrush Current Limit

Internal circuitry automatically controls the inrush current ramp by limiting the maximum current allowed in the transformer primary at startup. The amount of time required to perform this soft-start cycle is determined by a capacitor on the CSS pin. A CSS capacitor of 330nF provides approximately 7ms of soft startup ramp time.

Current-Limit and Current Sense

The primary side controller provides cycle-by-cycle current limiting to ensure the transformer primary current limits are not exceeded through use of an external resistor on ISENSEP. In addition, the maximum average current in the transformer primary is set by internal PWM duty cycle limits.
A short-circuit event is declared by the primary controller if this ISENSEP sensed current limit is triggered on more than 50% of the clock cycles within any 64 cycle window. Once a short-circuit event has been declared, Output #1 will shut off for 1024 cycles before a restart is attempted. This process will repeat indefinitely until the output short is removed.

Secondary-side Sync Controller

The efficiency of Output #1 can be optimized by designing a non-overlapping solution for the external FETs on the Primary side and Secondary side of the PD power transformer. The FET sync and overlap delays, as shown in Figure 5, are controlled by the designer to compensate for rise, fall, and delay times for both Primary and Secondary-side external power FETs. See Table 18 and note the delay timing limit: (Tsync + Tovl) ≤ 25ns.

The required resistors at SYNC_DLY and SYNC_OVL to implement the desired Tsync and Tovl timing are then calculated; see an example in Table 19. The filter capacitors to SGND for these pins (see Figure 5) are 1nF, typical.

Table 18 - Sync & Overlap Delay Timing Limit

Sync Delay (ns)	Overlap Delay (ns)	Delay Timing Limit (ns)
Tsync	**Tovl**	(**Tsync** + **Tovl**) ≤ 25ns

Table 19 - SYNC_DLY & SYNC_OVL Resistor Calculation Example

Desired SYNC Delay (ns)	Desired Overlap Delay (ns)	Delay Timing Limit Check (ns)	SYNC_DLY Resistor Required (Ω)	SYNC_OVL Resistor Required (Ω)
Tsync	**Tovl**	(**Tsync** +**Tovl**)≤ 25ns	R_{SYNC_DLY} = (**Tsync** + **Tovl**) x 2KΩ	R_{SYNC_OVL} = **Tovl** x 2KΩ
10ns	15ns	Ok	50KΩ	30KΩ

Compensation and Loop Feedback

The primary output (Output #1) has two power compensation and feedback mechanisms:
– Adaptive slope compensation
– Primary-Secondary (feedback based) control loop
The adaptive slope compensation automatically provides an optimized ramp framework for the overall loop performance, there are no user settings required.
For the Primary-Secondary control loop the device uses an internal transconductance error amplifier with external compensation control. An external secondary-side RC compensation network should be connecting to COMP1.

The resulting loop feedback path through the internal isolation channel to the primary-side PWM is automatic and completely user transparent.
Voltage feedback input is provided at the FB1 pin. At FB1, an internal reference of 1V (nominal) is compared to a resistor divided voltage from Output #1. This sets the desired Output #1 voltage level. With the top resistor in the feedback divider designated R2 and the bottom resistor designated R1 (again refer to Figure 5) the programmed voltage for Output #1 is equal to Vref times (R1+R2)/R1. So, for example, with R1=5K, R2=20K, and Vref=1V, the output voltage is set to 5V.

Low-load Current Operation - DCM

The primary output (#1) uses both DCM and Pulse Skipping (Burst Mode) design techniques to optimize power efficiency. When a low-load output power condition is detected, the Controller automatically enters a discontinuous current mode (DCM) of operation.

Over-voltage Protection

Output #1 has a built-in over-voltage monitor set to +10% of nominal voltage. If tripped, the output shuts down until within +5% of the nominal voltage at which point normal operation is then resumed.

If Voltage Margining is used (see Software Mode Operation on 38) the over-voltage protection tracks to the margining selected.

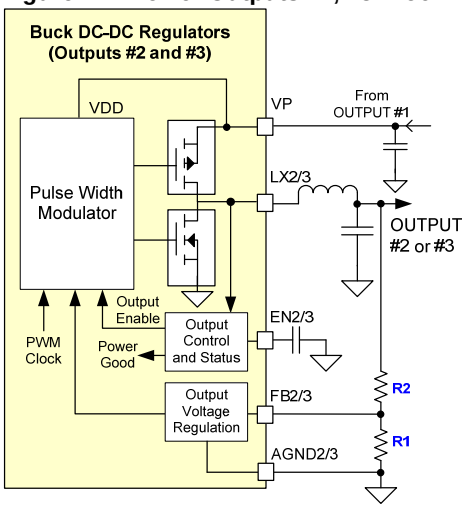
Power Outputs #2 and #3

Secondary-side Outputs #2 and #3 (see Figure 12) are identical synchronous current mode PWM DC-DC Buck Regulators with:

– Integrated PMOS and NMOS Power FETs
– Independent low-noise remote ground sensing (AGND2, AGND3)
– Output drivers (LX2, LX3)
– Feedback voltage controls (FB2, FB3)

– Output power enable/sequencing (EN2, EN3)

Figure 12 - Power Outputs #2, #3 Block Diagram



Under normal operation the regulator uses the PWM to generate driver signals for internal high-side and low-side MOSFETs. To produce these PWM loop controlled outputs an error signal from the voltage-error amplifier is compared with a ramp signal generated by an oscillator in the PWM.
A high-side switch is turned on at the beginning of the oscillator cycle and turns off when the ramp voltage exceeds the internally generated reference signal or the current-limit threshold is exceeded. A low-side switch is then turned on for the remainder of the oscillator cycle.

Loop Feedback and Compensation

Voltage feedback is provided at the FBx (FB2 / FB3) pins. At FBx an internal reference of 800mV (nominal) is compared to a resistor divided voltage from the Output (#2/#3). This sets the desired Output voltage level, which is equal to Vref times (R1+R2)/R1.
Maximum voltage output level is constrained by the input level of VP: VOUT23 (max) = VP – 0.7V (typ).
Loop compensation is integrated for Outputs #2 and #3.

Current-Limit and Current Sense

Each regulator provides cycle-by-cycle current limiting to ensure that the maximum current limits are not exceeded. For each PWM cycle during which the maximum current limit is tripped, a short-circuit counter is incremented. This counter is reset to zero if and only if two consecutive PWM cycles do not contain current limit events. If the counter reaches 16 a short-circuit event is declared and both Output #2 and Output #3 supplies are powered down. After 256 cycles of wait time both Outputs will attempt restarts. If the short-circuit persists the counter will begin to increment and the cycle will repeat itself.
Note that the internal Regulators for Output #2 and Output #3 are coupled together such that if one declares a short-circuit event they both reset regardless of the short-circuit counter status of the other.

Over-voltage Protection

Outputs #2/#3 each have built-in over-voltage monitors set to +10% of nominal voltage. If tripped the output is shut down until within +5% of nominal voltage, normal operation is then resumed.
If Voltage Margining is used (see Software Mode Operation on 38) the over-voltage protection tracks to the margining selected.

Power Output #4

Secondary-side Output #4 is a synchronous current mode PWM DC-DC controller that drives external NMOS Power FETs and supports buck or boost topologies. Boost or buck operation is selected by the BUCK_EN pin.

Key Features:

– Independent low-noise remote sensing ground (AGND4)
– Current Sense inputs (ISENP4, ISENN4)
– High Side and Low Side NMOS FET drivers (HSD4, LSD4)
– DC-DC switch sense and remote sense (LX4, LX4_SENSE)
– Feedback voltage control (FB4)
– Error amplifier compensation input (COMP4)
– Output power enable/sequencing input (EN4)
– PWM Dimmable LED Driver in Boost Mode

For typical Buck operation (Figure 13) the controller uses the PWM and generates driver signals for both high-side and low-side MOSFETs. To produce these PWM loop controlled outputs an error signal from the voltage-error amplifier is compared with a ramp signal generated by an oscillator in the PWM.
The external high-side switch is turned on at the beginning of the oscillator cycle and turns off when the ramp voltage exceeds the internally generated reference signal or the current-limit threshold is exceeded. The external low-side switch is then turned on for the remainder of the oscillator cycle.
For typical Boost operation (see Figure 14) the controller uses the PWM and generates only a low-side driver signal for a single external MOSFET. To produce this PWM loop controlled output an error signal from the voltage-error amplifier is compared with the ramp signal generated by an oscillator in the PWM.
The internal low-side switch is turned on at the beginning of the oscillator cycle and turns off when the ramp voltage exceeds the internally generated reference signal or the current-limit threshold is exceeded. The diode conducts for the remainder of the oscillator cycle.

Figure 13 - Power Output #4 Block Diagram - BUCK

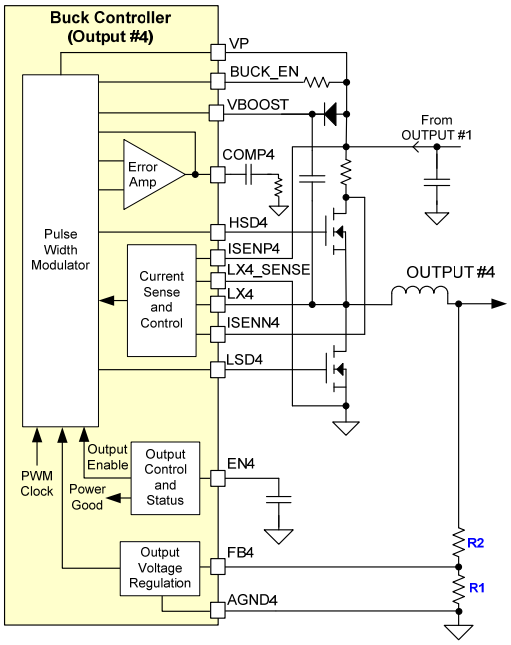
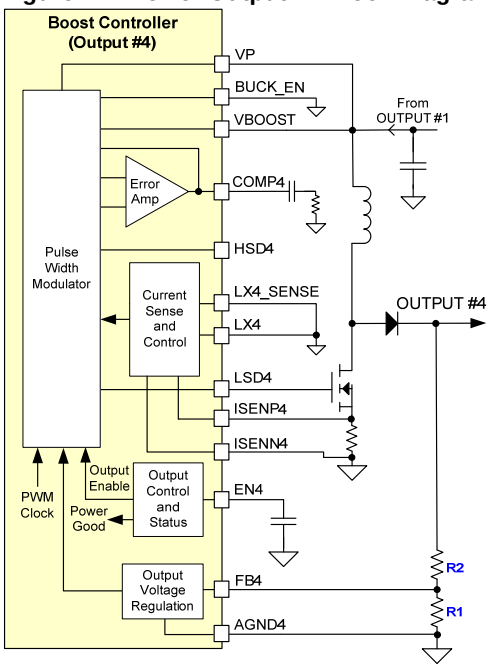


Figure 14 - Power Output #4 Block Diagram - BOOST



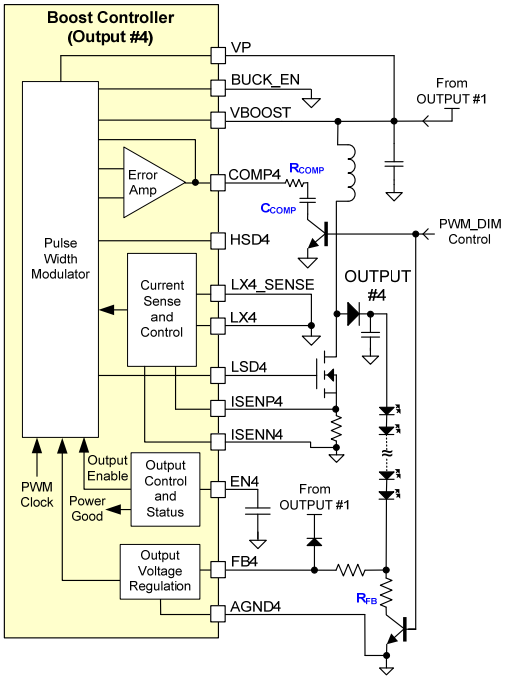
Extending the Boost mode to a PWM dimmable LED Driver (Figure 15) requires only the addition of external circuitry to hold the COMP4 and FB4 signal levels when the external PWM dim controller switches to dim (control on). The figure shows a low cost bipolar transistor solution, with an additional diode and resistor on FB4 to protect it from LED string voltage during dimming.

Compensation and Loop Feedback

As shown in Figure 13 and Figure 14 voltage feedback is provided at the FB4 pin in both Buck and Boost modes. At FB4 an internal reference of 800mV (nominal) is compared to a resistor divided voltage from Output #4 to control the voltage level. With the top resistor in the feedback divider designated R2 and the bottom resistor designated R1 the programmed voltage for Output #4 is equal to Vref times (R1+R2)/R1. So, in Boost mode operation, with R1=100, R2=1.43K, and Vref=0.8V, the output voltage is set to 12V.

In the LED Driver Boost application, Figure 15, the R_{FB} resistor is used to keep a constant LED string current rather than a constant output voltage as was the case in the other (two resistor divider) control feedback loops described above. The other resistor in the feedback loop path now is connected directly to FB4 for enhanced pin protection from the LED string voltage during dimming. The diode to Output #1 is also for FB4 pin protection.

Figure 15 - Power Output #4 Block Diagram - BOOST LED Driver



The COMP4 pin is connected to an external RC loop compensation network allowing design flexibility to optimize the system performance while insuring loop stability. In the LED Driver Boost application, again Figure 9, the compensation is held constant during dimming (control on) by the external transistor, and resumes compensation after PWM dimming control is removed (control off). Please refer to the AS1860 Design Guide, AN080, for details).

Current-Limit and Current Sense

The Controller provides cycle-by-cycle current limiting to ensure that current limits are not exceeded, using an external resistor sensed at ISENP4 and ISENN4.
For each PWM cycle during which the maximum ISENP4-to-ISENN4 sensed current limit voltage is tripped, a short-circuit counter is incremented. This counter is reset to zero if and only if two consecutive PWM cycles do not contain current limit events. If the counter reaches 16 a short-circuit event is declared and Output #4 is powered down. After 256 clock cycles of wait time Output #4 will attempt a restart, if the short-circuit persists the counter will begin to increment and the cycle will repeat itself.

Over-voltage Protection

Output #4 has a built-in over-voltage monitor set to +10% of nominal voltage. If tripped the output is shut down until within +5% of nominal voltage, normal operation is then resumed.
If Voltage Margining is used (see Software Mode Operation) the over-voltage protection tracks to the margining selected.

HARDWARE MODE OPERATION

The Hardware mode of operation is designed to provide basic control and status of the device via hardware (pin) control signals. Hardware mode functions and operation are described below.
(Please also refer to the Akros document AN080 for a detailed Design Guide.)

Device Initialization & Hardware Mode Selection

Primary-side digital logic is initialized while the MODE pin is Low, A required external capacitor between MODE and 48N provides the power-on reset input required to initialize the device.
Hardware (HW) mode is selected when the MODE pin is also pulled-up High (in addition to the power-on reset capacitor to 48N). The VDD3V_OUT pin can be used for the MODE pin pull-up power source by using a 17.8KΩ (maximum) resistor from MODE to VDD3V_OUT.
Secondary-side digital logic is initialized while the SEC_EN pin is Low, a required external capacitor between SEC_EN and SGND will provide the power-on reset input required to initialize the secondary-side.

HW Mode Power Output Controls

Power Outputs #2 thru #4 each have independent output enable pins (EN2, EN3, and EN4) that enable the corresponding power output, and, can also be used to delay the power outputs relative to each other. Note that Output #1, the main device power output, is always enabled and does not have an output enable pin.
The ENx pins have internal pull-ups, so outputs are enabled when an ENx pin is simply connected to an external timing capacitor (C_{ENX}), see Figure 16.

As shown in Figure 17, a Low voltage (ground) on an ENx pin disables the corresponding power output. In addition, if an output is not used the associated FBx pin should in fact be pulled High to prevent a disabled output from affecting PGOOD status.

Figure 16 - HW Mode Output(s) Hardware Enabled

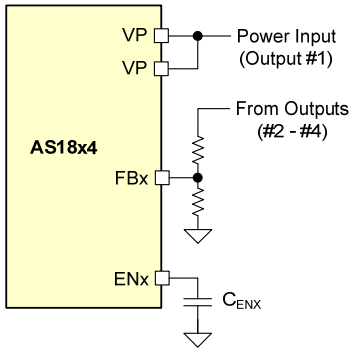
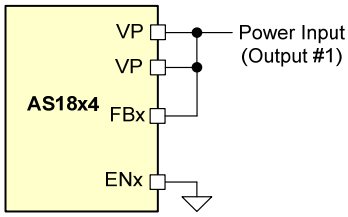


Figure 17 - HW Mode Output(s) Hardware Disabled



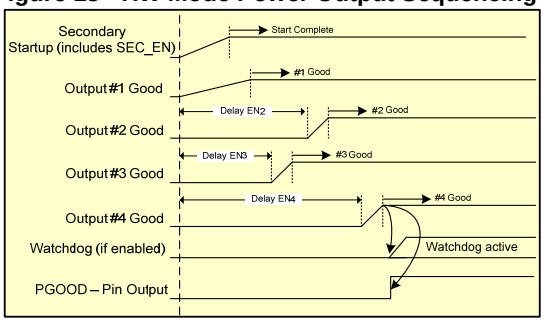
HW Mode Power Output Sequencing

Connecting a grounded external capacitor to an ENx pin establishes a delay before the corresponding power output is turned on. Each power output delay capacitor can be selected to create a user defined power-on sequence.
The time delay (T_{ENX}) in seconds for a capacitor (C_{ENX}) is defined by the formula:

$$T_{ENX} = \frac{0.8 C_{ENX}}{10 \mu A} \text{ (must be > 8ms)}$$

For example, a 200nF cap creates an output delay of 16ms. Each ENx pin has an internal 0.8V threshold detector and sources 10µA. When the ENx pin reaches 0.8V, enable delay timing begins.
Each ENx delay must be greater than 8ms for proper device startup assuming a typical 10nF capacitor on SEC_EN. All delays for power outputs #2-#4 are synchronized to the beginning of the Output #1 voltage ramp (see Figure 18).

Figure 18 - HW Mode Power Output Sequencing Example

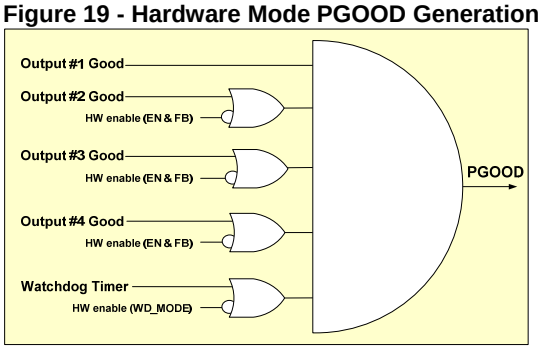


HW Mode Power Monitoring (PGOOD)

All Outputs (1-4) are monitored for power good status if enabled (2-4 can be disabled). Once a supply output reaches a stable state, its internal power good status signal is asserted. An output's power good is declared (good) at +/- 5% and at fault (bad) at +/- 10% of final voltage value. In either transition case (good to/from bad), continuous operation of 10µS is required before the state change is declared. The user sees the resulting status on the PGOOD pin (10ms minimum pulse).

In Hardware mode, the PGOOD pin is the logical AND of all enabled Power Outputs and any Watchdog timeout events (if enabled) as shown in Figure 19.

Figure 19 - Hardware Mode PGOOD Generation



If any of power outputs (2-4) are not required, the unused output(s) should be permanently disabled using the ENx and FBx pins as described in HW Mode Power Output Controls on 34. Permanently disabling an unused output is required to assure correct PGOOD signal "ANDing".

HW Mode Watchdog Timer

Watchdog Configuration

The Watchdog timer is configured by the WD_MODE pin as follows:

– When the WD_MODE pin is set High the Watchdog timer is set for a 32 second timeout period.
– When the WD_MODE pin is Floating the Watchdog timer is set for a 1 second timeout period. Decoupling the pin to 48N is also required.
– When the WD_MODE pin is set Low the Watchdog timer function is disabled.

Watchdog Service

The Watchdog timer is serviced by pulsing the WDOG pin for at least 100ns (here a pulse is defined as a continuous level of either polarity after the 1st edge). Correct platform usage is to service before the watchdog timeout period expires.

Watchdog Timeout

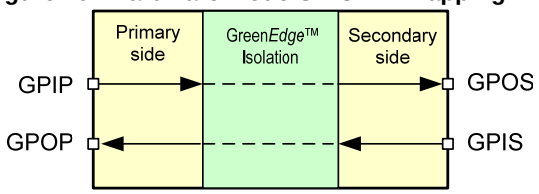
If the Watchdog times out, the following occur:

– The PGOOD pin is pulsed Low for 10ms (min). If coincident with any voltage fault events the PGOOD output pulse could be longer. This pulse can be used for PD platform level alarm or reset.
– Operation of the Watchdog timer is automatically initialized and restarted.

HW Mode General-Purpose I/O Operation

In Hardware mode, the GPIO pins provide a means for controlling and monitoring isolated primary-side signals from the secondary-side of the AS1860.
The secondary-side GPOS and GPIS pins map to the primary-side pins GPIP and GPOP as shown in Figure 20.

Figure 20 - Hardware Mode GPIO Pin Mapping



SOFTWARE MODE OPERATION

Software mode operation allows a host controller to access the AS1860 internal registers via an I²C interface. Access to these registers provides extensive status and control functions. Software mode functions and operation details are described below.
(Please also refer to Akros document AN082 for a detailed Software Users Guide.)

Device Initialization and Software Mode Selection

Primary-side digital logic is initialized while the MODE pin is Low, A required external capacitor between MODE and 48N provides the power-on reset input required to initialize the device.
Software (SW) mode is selected when the MODE pin uses just this initialization capacitor.

Secondary-side digital logic is initialized while the SEC_EN

pin is Low, a required external capacitor between SEC_EN and SGND will provide the power-on reset required to initialize the secondary-side.

SW Mode Power Output Controls

Once enabled in hardware, Power Outputs (2-4) can be independently enabled or disabled in both Hardware (via pin control) and Software (via I²C register).

Each output has an independent enable pin (EN2, EN3, EN4) for hardware enabling, and, can also be used to delay one voltage output relative to other. Note that Output #1, the main device power output, is always enabled and does not have an output enable pin or software control mode.

Any power output (2-4) to be software controlled must first have been enabled in hardware. The ENx pins have internal pull-ups so outputs are power-on enabled when the ENx pins float. See Figure 21.

As shown in Figure 22, a low voltage (ground) on an ENx pin disables the corresponding power output; any hardware-disabled output will not be controllable in software. Note that if an output is not used, the associated FBx pin should in fact be pulled High, which prevents a disabled output from affecting PGOOD status.

Figure 21 - SW Mode Output(s) Hardware Enabled

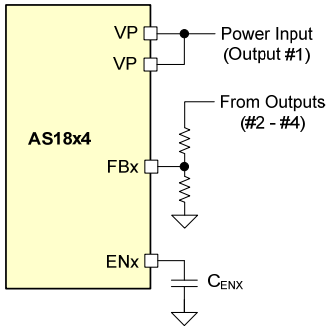
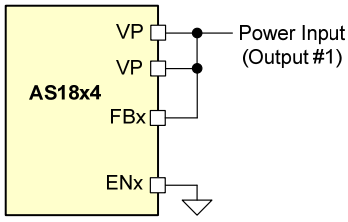


Figure 22 - SW Mode Output(s) Hardware Disabled



SW Mode Power Output Sequencing

Connecting a grounded external capacitor to an ENx pin establishes a delay before the corresponding power output is turned on. Each power output delay capacitor can be selected to create a user defined power-on sequence.

The time delay (T_{ENX}) in seconds for a capacitor (C_{ENX}) is defined by the formula:

$$T_{ENX} = \frac{0.8 C_{ENX}}{10 \mu A} \text{ (must be > 8ms)}$$

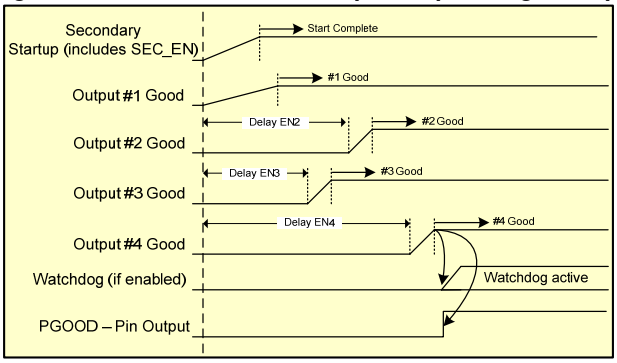
For example, a 200nF cap creates an output delay of 16ms. Each ENx pin has an internal 0.8V threshold detector and sources 10µA. When the ENx pin reaches 0.8V, enable delay timing begins.

Each ENx delay must be greater than 8ms for proper device startup assuming a typical 10nF capacitor on SEC_EN. All delays for power outputs (2-4) are synchronized to the beginning of the Output #1 voltage ramp (see Figure 23).

SW Mode Power Status Monitoring (PGOOD)

Each power output (1-4) is monitored for power good status. Once a supply output reaches a stable state its internal power good status signal is asserted. An output's power status is declared good at +/- 5% and at fault (bad) at +/- 10% of final voltage value. In either transition case (good to/from bad) a continuous operation of 10µS is required before state change is declared.

Figure 23 - SW Mode Power Output Sequencing Example

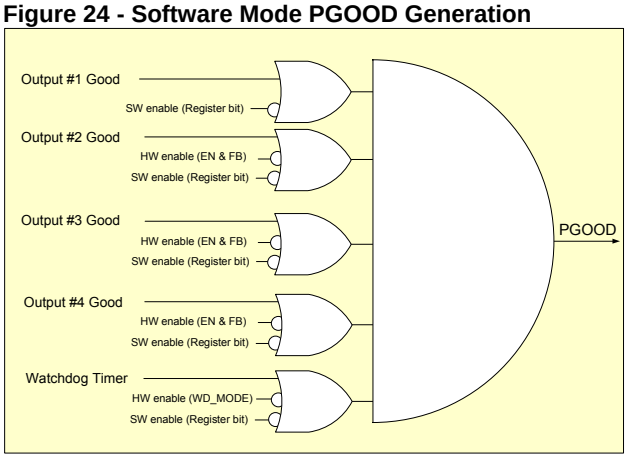


As shown in Figure 24, once all enabled outputs are good the user will see the resulting device power status on both the PGOOD pin and the Global PGOOD bit of Register 00h.
Power Good status for each supply is available in the Alarms and Power Status register (00h).
Operation of the PGOOD pin is defined by register 03h as shown in Table 26. Register 03h allows the user to exclude any individual output's power good status from affecting the PGOOD pin by clearing the associated output's mask bit. If the default values in register 03h are used, PGOOD is the logical AND of all four power status outputs. As shown in

Figure 18, a fault on any of the supplies will drive the PGOOD pin Low (10ms minimum).
In addition, the Watchdog timer status can be included / excluded in the PGOOD pin logic. Register 04h, bit 2 allows the user to either mask or allow a Watchdog timeout to generate a PGOOD pulse.
The PGOOD pin can be used as part of a board reset logic chain as it is asserted (High) only when all the enabled power outputs are stable.
If any of power outputs (2-4) are not required, the unused output(s) should be permanently disabled using ENx and FBx pins as described in SW Mode Power Output Controls on 36. Permanently disabling an output will override any register control associated with a disabled output.

Power voltage monitoring will not restart any of the supplies. A PGOOD fault will restore all registers except the history register (Reg 05h) to default state unless bit 4 in the device control register (Reg 06h) is set.

Figure 24 - Software Mode PGOOD Generation



History Register

The PGOOD & Watchdog History register (05h) is used to identify the source of a PGOOD fault. One bit is provided for each power output (1-4) and one for the Watchdog timer. In the event of a PGOOD fault, the bit corresponding to the particular power output that caused the PGOOD fault is set. Similarly, in the event of a Watchdog timeout the Watchdog Timeout bit is set.
Once set these bits are latched, they will not change even after the PGOOD fault is resolved unless there is a user command to do so. Therefore the user must clear this register as desired. The PGOOD & Watchdog History register is described in Table 28.

PD Voltage and Current Measurements

The AS1860 contains an A/D converter that measures PD input current to 5-bit accuracy and PD voltage to 8-bit accuracy. The A/D converter measurements are updated automatically at a 100Hz (minimum) rate, and may be accessed at any valid I²C clock rate. A/D values are available in the PD Voltage (0Bh) and PD Current (0Ch) registers (see Table 34 and Table 35).

Current measurement is valid only for PoE PD operation and not during Local Power operation. However, voltage measurement is valid for both PoE and Local Power operation.

PD Over-Current Alarm Threshold

Register 0Dh (see Table 36) allows the user to specify a maximum PD current value that when exceeded sets the PD Over-current Alarm bit in register 00h.

SW Mode Power Margining

Each of the four voltage outputs can be independently margined. Output #1 has a margining range of -5% to +5% while Outputs (2-4) can be independently margined from -8% to +6%.
These are configured via the Margin Control registers 0Eh and 0Fh. This feature allows engineering and/or manufacturing testing where, for example, it is useful to make test adjustments to compensate for PC board trace IR drops. See Table 37 and Table 38 for details.
If voltage margining is used, the AS1860 over-voltage protection tracks to the margining selected for any output.

SW Mode EMI Performance Control

In Software Mode the AS1860 provides two additional methods to generate PWM clocks for optimum EM radiation performance: PRBS Randomization and Fractional-N.

PWM Clocks - PRBS Randomization

This technique enables a randomized PRBS sequence to modulate the clocks thus spreading the noise across the band and reducing the peaks. PRBS randomization is selected via register 0Ah as shown in Table 33.

PWM Clocks - Fractional-N

PWM clocks and harmonics can be a major source power supply EMI. Fractional-N clocking provides an “FM like” modulation on the PWM clocks that spreads out the spectral energy thereby reducing peaks in EMI tested frequency bands. One of three modulation rates can be selected via register 0Ah as shown in Table 33.

SW Mode General-Purpose I/O & ADC

As shown in Figure 25, the GPOP, GPIP, and ADCIN pins provide a means for controlling and monitoring isolated Primary-side signals from the Secondary side of the AS1860. GPIO and A/D functions are updated automatically at a

100Hz (minimum) rate, and may be accessed at any valid I²C clock rate.

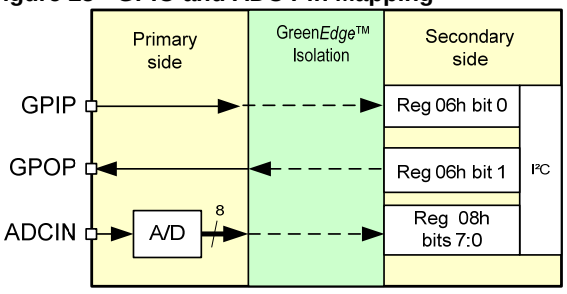
General-Purpose I/O Pins

The GPOP bit in the Device Control register (06h) specifies the state of the GPOP output pin. The state of GPIP input pin is reflected in GPIP bit located in the same register. Maximum measurement latency is defined in Table 6.

General-Purpose ADC (ADCIN Pin)

The Primary-side ADCIN pin is an input to an internal A/D converter with a continuous sample/conversion rate. The A/D process is automatic and therefore requires no user action to initiate. This internal 8-bit A/D sub-system contains a successive approximation A/D, track/hold circuitry, internal voltage reference, and conversion clocking. Reading the converted value is done in the A/D Voltage register (08h). Maximum measurement latency is found in Table 6.
In addition, the A/D Alarm Threshold register (09h) allows the user to specify a maximum A/D value that when exceeded automatically sets the A/D Over-threshold Alarm bit in register 00h.

Figure 25 - GPIO and ADC Pin Mapping



SW Mode Watchdog Timer Operation

The Watchdog timer is serviced using either the WDOG pin or the Watchdog Service Control bit in Register 04h. Correct platform usage is to service before the watchdog timeout occurs. If a Watchdog timeout occurs, the PGOOD pin can generate an output pulse (10ms minimum) that may be used for PD platform level alarm or reset. In addition, an interrupt can be generated and the status can be interrogated by querying the Interrupt Status register (02h) which has a bit to indicate Watchdog timeout.

Watchdog Timer Modes

In Software mode (MODE pin Floating with cap to 48N), the WD_MODE pin selects one of three Watchdog timer operating modes as follows:

Watchdog Timer Function Disabled

When the WD_MODE pin is set Low, the Watchdog timer function is disabled.

Watchdog Timer Enabled at Startup

When the WD_MODE pin is connected to an external capacitor (to 48N), the watchdog timer function is enabled at startup. At startup the watchdog timeout counter defaults to the maximum period of 32 seconds. The timeout period may be changed via the Watchdog Timeout register (07h) as described below.

Watchdog Timer Disabled at Startup

Setting the WD_MODE pin High disables the Watchdog timer function at startup and can only be enabled through software. At startup the watchdog timeout counter defaults to the maximum period of 32 seconds. Once the Watchdog is enabled the timeout period may be changed via the Watchdog Timeout register (07h) as described below.

Watchdog Timer Operation

Watchdog Enable

Enabling of the watchdog function in software must be done with two consecutive writes as follows:

1. The first write is to the Watchdog register (04h) bit “Enable Watchdog”, plus any other Watchdog bit masks (for Interrupts, PGOOD, and Register Reset functionality).

2. The next write must be to register 00h with the value BBh with no other intervening read or write operation to the AS1860. The time between the two writes can be infinite, but the operation will not be enabled until the second write. If a write/read occurs to any other register or if a write occurs but the value is NOT BBh, the Enable Watchdog bit is cleared.

Note that once enabled, watchdog operation cannot be disabled.

Watchdog Service

To service the watchdog via software, the user must issue two consecutive writes as follows:

1. The first write is to the Watchdog register (04h) bit “Watchdog Service Control”.
2. The next write must be to register 00h with value AAh with no other intervening read or write operation to the AS1860. The time between the two writes can vary; however, the second write must be completed before a watchdog timeout occurs. If the watchdog times out before the second write or the second write is not to the 00h register or the data value is not “AAh”, then the service request to the watchdog timer is cancelled.

To service the watchdog via hardware (a valid operation in Software mode) the WDOG pin must be pulsed for at least 100ns (continuous pulse of either polarity after the 1st edge).

Correct platform usage is to service before the watchdog timeout period expires.

Watchdog Timeout Period

At startup the watchdog timeout counter defaults to the maximum period of 32 seconds. The current user programmed value in the Watchdog Timeout register (07h) is always used for watchdog timeouts. A value of
FFh in this register gives the maximum timeout of 32 seconds. A value 01h sets the minimum period of 125ms. Note that 00h is reserved and is not to be used. Intervening values are multiples of 125ms (e.g. a value of 04h = 500ms).

Watchdog Timeout

If the Watchdog times out, the following occur:

– The Watchdog Timeout bit in the History register (05h) is set.
– If the Watchdog Interrupt mask bit is set (register 04h) and interrupts are enabled, the Watchdog Timeout bit in the Interrupt Status register (02h) is set and the INTB pin is driven Low.
– If the Watchdog PGOOD mask bit is set (register 04h), a 10ms (min.) Low pulse is output at the PGOOD pin. If coincident with other voltage fault events the PGOOD output pulse could be extended.
– If the Watchdog Register Reset mask bit is NOT set (register 04h), the AS1860 registers are reset. This resets the Watchdog Timeout register value to 32 seconds. (Note that an independent PGOOD fault will also reset the registers unless bit 4 in device control register, Reg 06h, is set).
– If the Watchdog Register Reset mask bit is set (register 04h), operation of the Watchdog timer is automatically initialized, with the currently programmed value, and restarted.

SW Mode Interrupt Operation

Interrupts are disabled after a device power on. The Device Control register (06h) is used to enable (or disable) interrupts at a global device level.

The Interrupt Mask (01h) and Interrupt Status (02h) registers are used to enable alarms and service any resulting alarms.

Interrupt Masking

Positive masking is used; therefore a “1” indicates that the specified fault or alarm will cause an interrupt. Interrupts (except for watchdog timeout) are level-driven, thus if a fault condition is active upon enabling it will immediately generate an interrupt.

Interrupt Status

A read from the Interrupt Status register will return the conditions which have caused an interrupt, and will immediately clear all such pending interrupts. Note that interrupts (except for watchdog timeout) are level driven, so if a fault condition still exists upon interrupts being cleared an interrupt will be re-asserted after a minimum off time of 10µs.

I^2C INTERFACE

The AS1860 provides a standard I^2C compatible slave interface that allows a host controller (master) to access its single-byte registers. Note the requirement of “Repeated Start” for I^2C reads.
The Primary-side GPIO pin read/write or ADCIN pin conversion read/write have a 10ms (maximum) pin-to/from-register timing.
The AS1860 registers are summarized in Table 22 and described in Table 23 through Table 38.
The I^2C interface is active when the AS1860 is in Software mode. There are four pins associated with the I^2C interface:

– SDIO: bi-directional serial data
– SCL: clock input
– INTB: interrupt output
– I2C_ADR: device address configuration

Start/Stop Timing

The master device initiates and terminates all I^2C interface operations by asserting Start and Stop conditions respectively.

As shown in Figure 20, a START condition is specified when the SDIO line transitions from High-to-Low while the clock (SCL) is High. A STOP condition is specified when SDIO transitions from Low-to-High while SCL is High.

Data Timing

As shown in Figure 26, data on the SDIO line may change only when SCL is Low and must remain stable during the High period of SCL. All address and data words are serially transmitted as 8-bit words with the MSB sent first.

Acknowledge (ACK)

ACK and NACK are generated by the addressed device that receives data on SDIO. After each byte is transmitted, the receiving interface sends back an ACK to indicate the byte was received. As shown in Figure 27, to generate an ACK, the transmitter first releases the SDIO line (High) during the Low period of the ACK clock cycle. The receiver then pulls the SDIO line Low during the High period of the clock cycle.
A NACK occurs when the receiver does NOT pull the SDIO line Low during the High period of the clock cycle.
Device address/operation words, register address words, and write data words are transmitted by the master and are acknowledged by the AS1860. Read data words transmitted by the device are also acknowledged by the master.

Figure 26 - I²C Interface Start/Stop and Data Timing

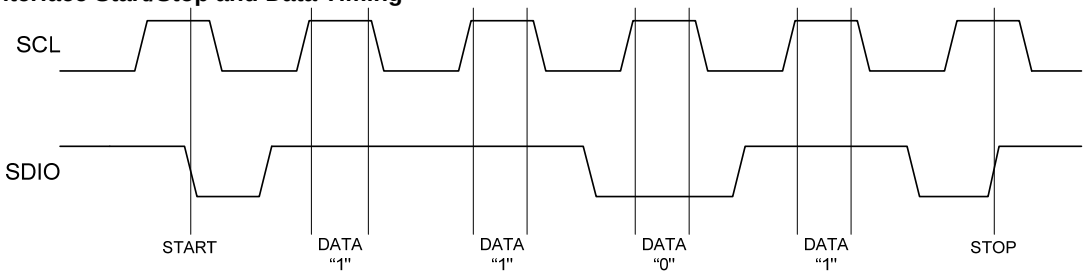
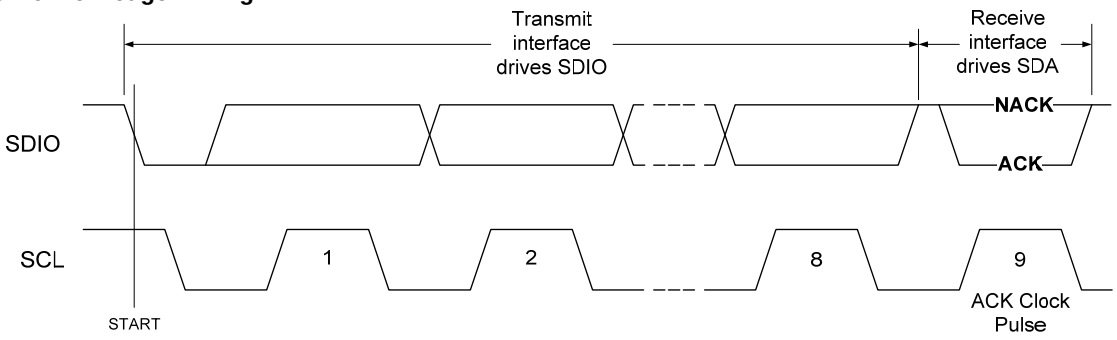


Figure 27 - I²C Acknowledge Timing



Device Address Configuration

The I²C interface is designed to support a multi-device bus system. At the start of an I²C read or write operation, the AS1860 compares its configured device address to the address sent by the master. The AS1860 will only respond (with ACK) when the addresses match.

The device address consists of 7 bits plus a read/write bit. As shown in Table 20, bits A7, A6, A5 and A4 of the AS1860 device address are internally fixed to values A7 = 0, A6 = 1, A5 = 0 and A4 = 0.

The I2C_ADR pin is used to configure bits A3 thru A1 (using an external resistor). The device establishes the bit values of A3 thru A1 during start-up by measuring current flow through this resistor.
Note that A0 functions as the read/write operation bit.

Table 20 - AS1860 Device Address Configuration

Bit	Function	Description
A7	Fixed device address bits	Internally fixed to 0
A6		Internally fixed to 1
A5		Internally fixed to 0
A4		Internally fixed to 0
A3 A2 A1	Configurable device address bits	Device address bits A3, A2 and A1 are configured by connecting a 1% resistor between pin I2C_ADR and ground (48N) as follows: 100KΩ□ sets A3, A2, A1 = 1,1,1 86.6KΩ□ sets A3, A2, A1 = 1,1,0 75.0KΩ□ sets A3, A2, A1 = 1,0,1 61.9KΩ □sets A3, A2, A1 = 1,0,0 49.9KΩ□ sets A3, A2, A1 = 0,1,1 37.4KΩ □sets A3, A2, A1 = 0,1,0 29.4KΩ □sets A3, A2, A1 = 0,0,1 12.4KΩ □sets A3, A2, A1 = 0,0,0
A0	$R/\overline{W}$	Specifies read or write operation

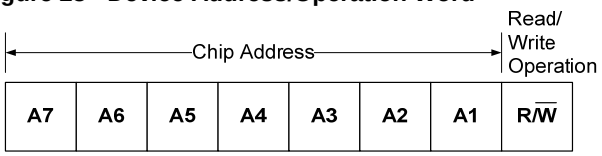
Device Address/Operation Word

Following a START condition the host transmits an 8-bit device address/operation word to initiate a read or write operation. This word consists of a 7-bit device address and the read/write operation bit as shown in Figure 28.

The AS1860 compares the received device address with its configured device address and sends back an ACK only when the addresses match.

Bit 0 is the read/write operation bit. A read operation is specified when the R/$\overline{W}$ bit is set High; a write operation when set Low.

Figure 28 - Device Address/Operation Word



Register Address Word

For write operations (after the AS1860 acknowledges receipt of the Device Address/Write Word) the master sends the target 8-bit register address word to specify the AS1860 register to be accessed. Table 21 specifies the valid AS1860 register addresses.

Data Word

The 8-bit data word contains read/write data. Data is transferred with the MSB sent first.

Write Cycle

Figure 29 illustrates the sequence of operations to perform an AS1860 register write cycle.

Read Cycle

Figure 30 illustrates the sequence of operations to perform an AS1860 register read cycle. Note that the master must first perform a "dummy write" operation to write the AS1860 internal address pointer to the target register address.
After the AS1860 sends back an ACK, the master sends a repeated START, followed by a device address read word (R/$\overline{W}$ bit = 1). The AS1860 then transmits an ACK followed by the data word that reflects the contents of the target register.
Upon receipt of the register address word, the AS1860 sends back an ACK.

Table 21 - AS1860 Register Address Word

I²C Register Address Word								Selected AS1860 Register (Hex)
A7	A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	0	0	0	0	00
0	0	0	0	0	0	0	1	01
0	0	0	0	0	0	1	0	02
0	0	0	0	0	0	1	1	03
0	0	0	0	0	1	0	0	04
0	0	0	0	0	1	0	1	05
0	0	0	0	0	1	1	0	06
0	0	0	0	0	1	1	1	07
0	0	0	0	1	0	0	0	08
0	0	0	0	1	0	0	1	09
0	0	0	0	1	0	1	0	0A
0	0	0	0	1	0	1	1	0B
0	0	0	0	1	1	0	0	0C
0	0	0	0	1	1	0	1	0D
0	0	0	0	1	1	1	0	0E
0	0	0	0	1	1	1	1	0F

Register Descriptions

The AS1860 contains 16 single byte (8-bit) registers. The registers are accessible via the I²C interface when Software mode is enabled.

Table 22 provides a summary of the AS1860 registers and bit functions. Table 23 through Table 38 provides detailed description of the function and operation of each register.

Figure 29 - I²C Interface Write Cycle Timing

Figure 30 - I²C Interface Read Cycle Timing (with Repeated Start)

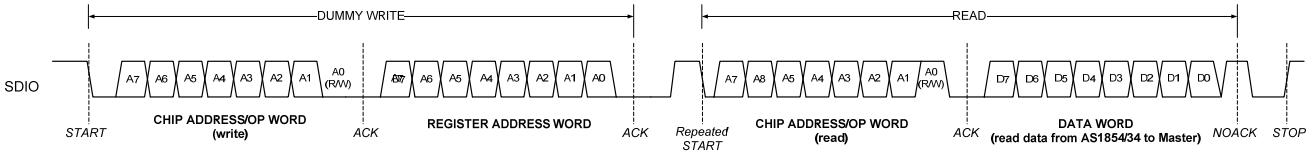


Table 22 - AS1860 Register and Bit Summary

Register	Addr (hex)	Access	Data Bits D7	D6	D5	D4	D3	D2	D1	D0
Alarms and Power Status	00	Read-Only	Over-Current Alarm	Over-Temp Alarm	A/D Over-Threshold Alarm	Output #4 Fault	Output #3 Fault	Output #2 Fault	Output #1 Fault	Global PGOOD Fault
Interrupt Mask	01	R/W	Over-Current Alarm	Over-Temp Alarm	A/D Over-Threshold Alarm	Output #4 Fault	Output #3 Fault	Output #2 Fault	Output #1 Fault	reserved
Interrupt Status	02	Read-Only	Over-Current Alarm	Over-Temp Alarm	A/D Over-Threshold Alarm	Output #4 Fault	Output #3 Fault	Output #2 Fault	Output #1 Fault	Watchdog Timeout
PGOOD Voltage Masks	03	R/W	reserved	reserved	reserved	Output #4 Mask	Output #3 Mask	Output #2 Mask	Output #1 Mask	reserved
Watchdog Enable, Mask, Service	04	R/W	reserved	reserved	reserved	Watchdog Enable	Watchdog Interrupt Mask	Watchdog PGOOD Mask	Watchdog Register Reset Mask	Watchdog Service Control
PGOOD & Watchdog History	05	R/W	reserved	reserved	reserved	Output #4 caused PGOOD fault	Output #3 caused PGOOD fault	Output #2 caused PGOOD fault	Output #1 caused PGOOD fault	Watchdog Timeout elapsed
Device Control and I/O Status	06	R/W	reserved	Reset all registers	Enable Interrupts	Disable PGOOD reset	reserved	reserved	GPOP	GPIP
Watchdog Timeout	07	R/W	WDOG timeout counter (8 bits, in 125ms increments)							
ADCIN Voltage Read	08	Read-Only	ADCIN pin input voltage measurement (8 bits)							
ADCIN Alarm Threshold	09	R/W	Alarm Threshold for ADCIN (8 bits)							
PD Status & System Clock Control	0A	R/W	reserved	LDET	AT_DET	CLIM (not valid in Local Power mode)	PWM Clock Modulate Enable	PWM Clock Modulate Type	PWM Clock Modulation Amount D1, D0	

PD Voltage Read	0B	Read-Only	PD input voltage measurement (Valid during both PoE and Local Power operation modes)				
PD Current Read	0C	Read-Only	reserved	reserved	reserved	PD input current measurement (PoE only, does not measure Local Power current)	
PD Over-Current Alarm Threshold	0D	R/W	reserved	reserved	reserved	PD over-current alarm trip threshold	
Outputs 1,2 Disable & Margin Control	0E	R/W	Output #2 Disable Control	Output #2 Voltage Margin setting (D6, D5, D4)	reserved	Output #1 Voltage Margin setting (D2, D1, D0)	
Outputs 3,4 Disable & Margin Control	0F	R/W	Output #4 Disable Control	Output #4 Voltage Margin setting (D6, D5, D4)	Output #3 Disable Control	Output #3 Voltage Margin setting (D2, D1, D0)	

Table 23 - Alarms and Power Status (Read-Only) - 00h

Bit	Function	Description	Reset State
D7	PD Over-current Alarm	1 = PD has exceeded current limit defined by PD Current Threshold register 0 = No alarm	0
D6	Internal Over-temp Alarm	1 = Temp has tripped warning Threshold 0 = No alarm	0
D5	A/D Threshold Alarm	1 = A/D measurement is > A/D Alarm Threshold register setting 0 = No alarm	0
D4	Power Output #4 Fault	1 = Output #4 Fault, not within spec 0 = Output in spec This bit always tracks the Output 4 voltage status regardless of whether the output is disabled in hardware and/or is masked off by Register 03.	0
D3	Power Output #3 Fault	1 = Output #3 Fault, not within spec 0 = Output in spec This bit always tracks the Output 3 voltage status regardless of whether the output is disabled in hardware and/or is masked off by Register 03.	0
D2	Power Output #2 Fault	1 = Output #2 Fault, not within spec 0 = Output in spec This bit always tracks the Output 2 voltage status regardless of whether the output is disabled in hardware and/or is masked off by Register 03.	0
D1	Power Output #1 Fault	1 = Output #1 Fault, not within spec 0 = Output in spec This bit always tracks the Output 1 voltage status regardless of whether the output is masked off by Register 03.	0
D0	Global PGOOD Fault	1 = At least one enabled output not within spec 0 = All enabled outputs within spec This bit always tracks the PGOOD pin, so both hardware disabled outputs and Register 03 masks will affect it.	0

Table 24 - Interrupt Mask (R/W) - 01h

Bit	Function	Description (see also Alarms and Power Reg)	Reset State
D7	PD Over-current Alarm	1 = mask on (interrupt possible) 0 = masked off (no interrupt possible)	0
D6	Internal Over-temp Alarm	1 = mask on (interrupt possible) 0 = masked off (no interrupt possible)	0
D5	A/D Threshold Alarm	1 = mask on (interrupt possible) 0 = masked off (no interrupt possible)	0

D4	Interrupt upon Power Output #4 Fault	1 = mask on (interrupt possible) 0 = masked off (no interrupt possible)	0
D3	Interrupt upon Power Output #3 Fault	1 = mask on (interrupt possible) 0 = masked off (no interrupt possible)	0
D2	Interrupt upon Power Output #2 Fault	1 = mask on (interrupt possible) 0 = masked off (no interrupt possible)	0
D1	Interrupt upon Power Output #1 Fault	1 = mask on (interrupt possible) 0 = masked off (no interrupt possible)	0
D0	reserved	do not write to this data bit	0

Table 25 - Interrupt Status (Read-Only) - 02h

Bit	Function	Description (see also Alarms and Power Reg)	Reset State
D7	PD Over-current Alarm	1 = Fault 0 = normal operation	0
D6	Internal Over-temp Alarm	1 = Fault 0 = normal operation	0
D5	A/D Threshold Alarm	1 = Fault 0 = normal operation	0
D4	Power Output #4 Fault	1 = Fault 0 = normal operation	0
D3	Power Output #3 Fault	1 = Fault 0 = normal operation	0
D2	Power Output #2 Fault	1 = Fault 0 = normal operation	0
D1	Power Output #1 Fault	1 = Fault 0 = normal operation	0
D0	Watchdog Timeout	1 = Timeout 0 = no timeout	0

Table 26 - PGOOD Voltage Masks (R/W) - 03h

Bit	Function	Description	Reset State
D7	reserved	do not write to this data bit	0
D6	reserved	do not write to this data bit	0
D5	reserved	do not write to this data bit	0
D4	Output #4 masked from PGOOD pin	1= Output #4 part of PGOOD pin or register status 0= Output #4 not part of PGOOD	1
D3	Output #3 masked from PGOOD pin	1= Output #3 part of PGOOD pin or register status 0= Output #3 not part of PGOOD	1
D2	Output #2 masked from PGOOD pin	1= Output #2 part of PGOOD pin or register status 0= Output #2 not part of PGOOD	1
D1	Output #1 masked from PGOOD pin	1= Output #1 part of PGOOD pin or register status 0= Output #1 not part of PGOOD	1
D0	reserved	do not write to this data bit	0

Table 27 - Watchdog Enable, Mask, Service (R/W) - 04h

Bit	Function	Description	Reset State
D7	reserved	do not write to this data bit	0
D6	reserved	do not write to this data bit	0
D5	reserved	do not write to this data bit	0
D4	Watchdog Enable	To change D4, D3, D2, or D1 a two stage write operation must occur: Stage 1. The Watchdog Enable bit (D4) must be set along with any other (D3-D1) desired bit changes. If D4 is not set the entire write operation is ignored. Stage 2. A write to Reg 0 with data BB (hex) must be the next I^2C operation to this device. If not, write will be ignored. Once this operation is complete (and D4 is set) the D4-D1 bits are sticky and cannot be reset. **D4 (Watchdog Enable):** 1 = enable watchdog countdown operation (timeout value set in watchdog timeout register). 0 = watchdog disabled **D3 (Watchdog Interrupt Mask):** 1 = mask on, interrupt possible 0 = masked off, no interrupt possible **D2 (Watchdog PGOOD Mask):** 1 = mask on, Watchdog part of PGOOD operation 0 = mask off, Watchdog not part of PGOOD operation **D1 (Watchdog Register Reset Disable Mask):** 1 = mask on, a Watchdog timeout will not reset I^2C registers 0= mask off, a Watchdog timeout will reset I^2C registers	D4 = 0
D3	Watchdog Interrupt Mask		D3 = 0
D2	Watchdog PGOOD Mask		D2 = 1
D1	Watchdog Register Reset Mask		D1 = 0
D0	Watchdog Service Control	1 = enable software service of Watchdog 0 = no software service of Watchdog Servicing the Watchdog is a 2-step procedure, after writing a "1" to this bit the next I^2C operation to the AS1860 must be a write to Reg 0 with data AA (hex).	0

Table 28 - PGOOD & Watchdog History (R/W) - 05h

Bit	Function	Description	Reset State
D7	reserved	do not write to this data bit	0
D6	reserved	do not write to this data bit	0
D5	reserved	do not write to this data bit	0
D4	Output #4 PGOOD history	1 = Output #4 caused PGOOD fault 0 = Output #4 did not cause PGOOD fault	0
D3	Output #3 PGOOD history	1 = Output #3 caused PGOOD fault 0 = Output #3 did not cause PGOOD fault	0
D2	Output #2 PGOOD history	1 = Output #2 caused PGOOD fault 0 = Output #2 did not cause PGOOD fault	0
D1	Output #1 PGOOD history	1 = Output #1 caused PGOOD fault 0 = Output #1 did not cause PGOOD fault	0
D0	Watchdog history	1 = Watchdog timeout occurred 0 = No Watchdog timeout occurred	0

Table 29 - Device Control and I/O Status (R/W) - 06h

Bit	Function	Description	Reset State
D7	reserved	do not write to this data bit	0
D6	Reset all registers	1 = force reset all registers 0 = no resets	0
D5	Enable Interrupts	1 = enable interrupts that are masked on 0 = no interrupts enabled	0
D4	Disable PGOOD reset	1 = PGOOD fault will not reset registers 0 = PGOOD fault will reset registers	0
D3	reserved	do not write to this data bit	0
D2	reserved	do not write to this data bit	0
D1	General-Purpose Output (GPOP)	GPOP pin reflects the state of this bit	0
D0	General-Purpose Input (GPIP)	This bit reflects the state of the GPIP pin	0

Table 30 - Watchdog Timeout (R/W) - 07h

Bit	Function	Description	Reset State
D7	D7 of 8-bit watchdog timer	Watchdog timeout counter value (125ms increments),	1
D6	D6 of 8-bit watchdog timer	used in Software Mode only.	1
D5	D5 of 8-bit watchdog timer	FF = max value (32 sec)	1
D4	D4 of 8-bit watchdog timer	01 = min value (125ms)	1
D3	D3 of 8-bit watchdog timer	00 = reserved, do not use	1
D2	D2 of 8-bit watchdog timer		1
D1	D1 of 8-bit watchdog timer		1
D0	D0 of 8-bit watchdog timer		1

Table 31 - ADCIN Voltage (Read-Only) - 08h

Bit	Function	Description	Reset State
D7	D7 of 8-bit voltage measure	8-bit measurement of voltage at ADCIN pin (primary	0
D6	D6 of 8-bit voltage measure	side). The A/D runs continuously with a 100Hz sampling	0
D5	D5 of 8-bit voltage measure	rate (minimum), and can be read at full I^2C speed.	0
D4	D4 of 8-bit voltage measure	FF (hex) = 2.5 V	0
D3	D3 of 8-bit voltage measure	00 (hex) = 0 V	0
D2	D2 of 8-bit voltage measure	step size = 9.80 mV	0
D1	D1 of 8-bit voltage measure		0
D0	D0 of 8-bit voltage measure		0

Table 32 - ADCIN Alarm Threshold (R/W) - 09h

Bit	Function	Description	Reset State
D7	D7 of 8-bit A/D Interrupt Threshold	8 bit Threshold for A/D Alarm Interrupt (if enabled) from	1
D6	D6 of 8-bit A/D Interrupt Threshold	ADCIN input pin.	1
D5	D5 of 8-bit A/D Interrupt Threshold	FF (hex) = 2.5V	1
D4	D4 of 8-bit A/D Interrupt Threshold	00 (hex) = 0 V	1
D3	D3 of 8-bit A/D Interrupt Threshold	step size = 9.80 mV	1
D2	D2 of 8-bit A/D Interrupt Threshold		1
D1	D1 of 8-bit A/D Interrupt Threshold		1
D0	D0 of 8-bit A/D Interrupt Threshold		1

Table 33 - PD Status and System Clock Control (R/W) - 0Ah

Bit	Function	Description	Reset State
D7	reserved	do not write to this data bit	0
D6	LDET	1 = Local power supply detected 0 = no Local power supply detected	0
D5	AT_DET	1 = IEEE® 802.3at, or, Local Power mode detection 0 = IEEE® 802.3af mode detection	0
D4	CLIM	1 = 750ma (min) PoE current limit 0 = 375ma (min) PoE current limit Note that CLIM status is not valid in Local Power mode (LDET status bit D6=1).	0

D3	PWM Clock Modulation Enable	1 = Clock modulation on 0 = off	0
D2	PWM Clock Modulation Type	1 = Fractional-n (see D1, D0 for modulation amount) 0 = Random (PRBS)	0
D1 D0	PWM Fractional-n Modulation Amount (not used for PRBS modulation)	D1, D0: 1,1 = reserved (do not use) 1,0 = 10% 0,1 = 5% 0,0 = 2%	0,0

Table 34 - PD Voltage (Read-Only) - 0Bh

Bit	Function	Description	Reset State
D7	D7 of 8-bit voltage measure	8-bit measurement of PD input voltage (primary side).	0
D6	D6 of 8-bit voltage measure	Also valid during Local Power Operation.	0
D5	D5 of 8-bit voltage measure	FF (hex) = 60 V (±1%)	0
D4	D4 of 8-bit voltage measure	00 (hex) = 0 V	0
D3	D3 of 8-bit voltage measure	step size = 235.3 mV	0
D2	D2 of 8-bit voltage measure		0
D1	D1 of 8-bit voltage measure		0
D0	D0 of 8-bit voltage measure		0

Table 35 - PD Current (Read-Only) - 0Ch

Bit	Function	Description	Reset State
D7	reserved	5-bit measurement of PD input current (primary side). PoE	n/a
D6	reserved	current measurement only, not valid during Local Power	n/a
D5	reserved	operating mode.	n/a
D4	D4 of 5-bit current measurement	**With CLIM = Low**	0
D3	D3 of 5-bit current measurement	D4, D3, D2, D1, D0	0
D2	D2 of 5-bit current measurement	11111 = 400 mA (±10%)	0
D1	D1 of 5-bit current measurement	00000 = 0 mA	0
D0	D0 of 5-bit current measurement	step size = 12.90 mA **With CLIM = High** D4, D3, D2, D1, D0 11111 = 800 mA (±10%) 00000 = 0 mA step size = 25.81 mA	0

Table 36 - PD Over-Current Alarm Threshold (R/W) - 0Dh

Bit	Function	Description	Reset State
D7	reserved	The over-current alarm bit is set when the PD input	n/a
D6	reserved	current (primary side) measurement exceeds this 5-bit	n/a
D5	reserved	value, not valid during Local Power operating mode.	n/a
D4	D4 of 5-bit current alarm trip setting	**With CLIM = Low**	1
D3	D3 of 5-bit current alarm trip setting	D4, D3, D2, D1, D0	1
D2	D2 of 5-bit current alarm trip setting	11111 = 400 mA (±10%)	1
D1	D1 of 5-bit current alarm trip setting	00000 = 0 mA	1
D0	D0 of 5-bit current alarm trip setting	step size = 12.90 mA **With CLIM = High** D4, D3, D2, D1, D0 11111 = 800 mA (±10%) 00000 = 0 mA step size = 25.81 mA	1

Table 37 - Outputs 1, 2 Disable & Margin Control (R/W) - 0Eh

Bit	Function	Description	Reset State
D7	Output #2: Disable Control	0 = Normal output operation, with bits D6, D5, D4 defining margining operation. 1 = Output #2 is disabled.	0
D6 D5 D4	Voltage Margin for Output #2	D6, D5, D4 (with D7=0): 1,1,1 = -2% 1,1,0 = -4% 1,0,1 = -6% 1,0,0 = -8% 0,1,1 = +6% 0,1,0 = +4% 0,0,1 = +2% 0,0,0 = no margining	0,0,0
D3	reserved	do not write to this bit	0
D2 D1 D0	Voltage Margin for Output #1	D2, D1, D0: 1,1,1 = reserved, do not use 1,1,0 = reserved, do not use 1,0,1 = reserved, do not use 1,0,0 = +5% 0,1,1 = +2.5% 0,1,0 = -2.5% 0,0,1 = -5% 0,0,0 = no margining	0,0,0

Table 38 - Outputs 3, 4 Disable & Margin Control (R/W) - 0Fh

Bit	Function	Description	Reset State
D7	Output #4: Disable Control	0 = Normal output operation, with bits D6, D5, D4 defining margining operation. 1 = Output #4 is disabled.	0
D6 D5 D4	Voltage Margin for Output #4	D6, D5, D4 (with D7=0): 1,1,1 = -2% 1,1,0 = -4% 1,0,1 = -6% 1,0,0 = -8% 0,1,1 = +6% 0,1,0 = +4% 0,0,1 = +2% 0,0,0 = no margining	0,0,0
D3	Output #3: Disable Control	0 = Normal output operation, with bits D2, D1, D0 defining margining operation. 1 = Output #3 is disabled.	0
D2 D1 D0	Voltage Margin for Output #3	D2, D1, D0 (with D3=0): 1,1,1 = -2% 1,1,0 = -4% 1,0,1 = -6% 1,0,0 = -8% 0,1,1 = +6% 0,1,0 = +4% 0,0,1 = +2% 0,0,0 = no margining	0,0,0

POWER OVER ETHERNET OVERVIEW

Power over Ethernet (PoE) offers an economical alternative for powering end network appliances such as IP telephones, wireless access points, security and web cameras, and other powered devices (PDs). The PoE standard IEEE® Std. 802.3af is intended to standardize the delivery of power over the Ethernet cables in order to accommodate remotely powered client devices. IEEE® Std. 802.3af defines a method for recognizing PDs on the network and supplying different power levels according to power level classes with which each PD is identified. By employing this method, designers can create systems that minimize power usage, allowing more devices to be supported on an Ethernet network.

The end of the link that provides power through the Ethernet cables is referred to as the power sourcing equipment (PSE). The powered device (PD) is the end of the link that receives the power. The PoE method for recognizing a PD and determining the correct power level to allocate uses the following sequence:

1. Reset - Power is withdrawn from the PD if the applied voltage falls below a specified level.
2. Signature Detection - during which the PD is recognized by the PSE.
3. Classification - during which the PSE reads the power requirement of the PD. The Classification level of a PD identifies how much power the PD requires from the Ethernet line. This permits optimum use of the total power available from the PSE. (Classification is considered optional by IEEE® standard 802.3af.)
4. ON operation - during which the allocated level of power is provided to the PD.

This sequence occurs as progressively rising voltage levels from the PSE as shown in Figure 29.

A summary of the PoE design framework is shown in Table 39.

Table 39 - PoE Design Framework Summary

Requirement	Value
Maximum power to the PD	12.95W (Type 1) 25.5W (Type 2)
Voltage at the PSE Interface	44-57V (Type 1) 50-57V (Type 2)
Maximum operating current	350mA (Type 1) 600mA (Type 2)
Min voltage at the PD interface	37V (Type 1) 42.5V (Type 2)

Power Feed Alternatives for 10/100/1000M Ethernet Systems

The Power Sourcing Equipment (PSE) supplies power to a single PD per node. A PSE located in the Data Terminal Equipment or Repeater is called an endpoint PSE, while a PSE located between MDIs is called a Mid-span PSE. Figure 31 illustrates the two power feed options allowed in the 802.3af/at standard for 10/100/1000M Ethernet systems (full duplex twisted pair data signaling is used in 1000M Ethernet).

In Alternative A, a PSE powers the end station by feeding current along the twisted pair cable used for the 10/100/1000M Ethernet signal via center taps on the Ethernet transformers. On the line side of the transformers for the PD, power is delivered through pins 1 and 2 and returned through pins 3 and 6.

In Alternative B, a PSE powers the end station by feeding power through pins 4, 5, 7and 8. In a 10/100/1000M system, this is done through the center taps of the Ethernet transformer. In a 10/100M system, power is applied directly to the spare cable pairs without using transformers.

The IEEE® Std. 802.3af/at standards are intended to be fully compliant with all existing non-powered Ethernet systems. As a result the PSE is required to detect via a well-defined procedure whether or not the connected device is PD compliant and classify (optional in legacy 802.3af applications) the needed power prior to supplying it to the device. Maximum allowed voltage is 57V to stay within SELV (Safety Extra Low Voltage) limits.

802.3AT SPECIFICATION

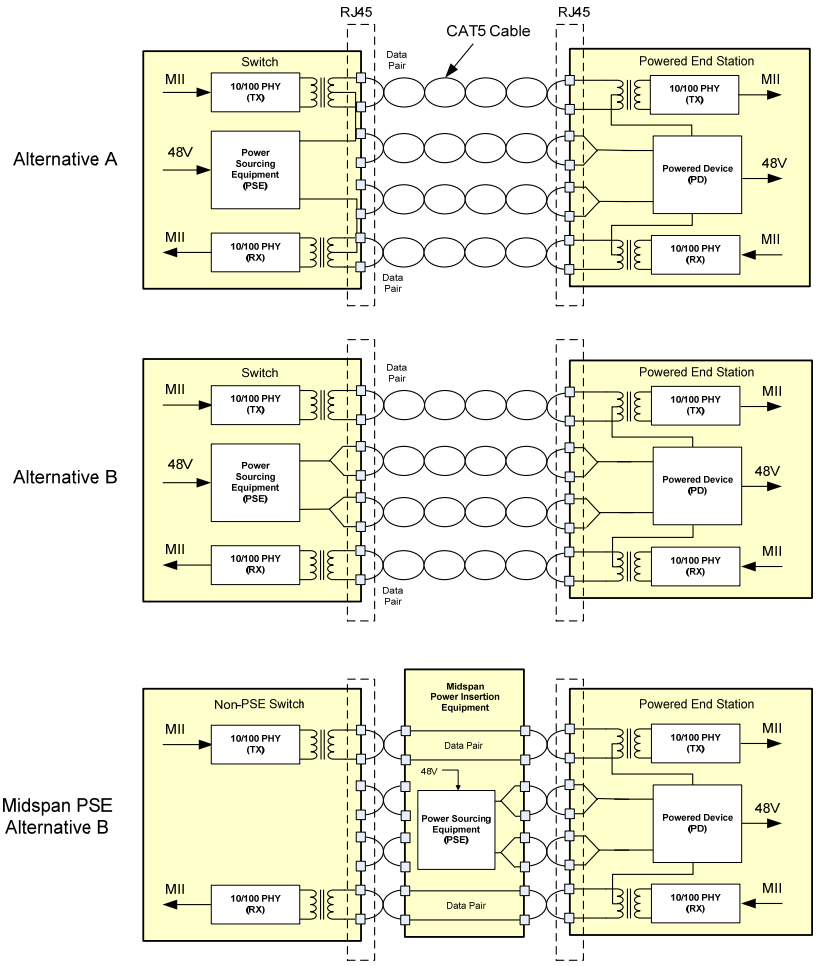
The AS1860 has been designed to be compatible with the IEEE 802.3at high power PoE standard. These devices are capable of providing the power needs of VoIP with video streaming, 802.11n multi-radio WAPs, and IP cameras with PTZ.

The AS1860 provides the normal signature resistance during detection phase for the PSE to recognize a PD. Both devices also support the two-event classification method specified in the 802.3at standard (backward compatible to 802.3af classification modes) and can detect a Type 2 PSE. If the AS1860 detects a Type 2 PSE they will indicate this either on the AT_DET pin or in I^2C register 0A (hex) in the AS1860 software mode. AT_DET pin is active high.

The AS1860 will issue the correct AT_DET state before PGOOD signal transitions to an "all good" state.

For a PD that is 802.3at compliant, Class must be set to Class 4 using appropriate RCLASS resistor.

Figure 31 - IEEE® Std. 802.3af Power Feeding Schemes



60W/90W Applications

The PoE specification, 802.3at, was updated in 2009 to agree the standard for delivering up to 30W from a PSE. Power delivery was limited to two of the four pairs which exist in Ethernet cables. Since then several new applications such as Thin Clients, high power multiple band WAP's and Communication clusters have emerged that benefit from the Network controlled power management provided by PoE. This has led to the need for PD controllers that can safely deliver up to 90W which the AS1860 provides.

In applications above 30W, power is applied to all four pairs in the Ethernet cable. Typically, two PSE's are connected to two separate pairs so that each pair now transfers 30W/45W. At this time there is no standard for this configuration but the AS1860 provides the flexibility to complete this link in a number of different ways.

LLDP COMMUNICATION

One of the most commonly deployed schemes for identifying the power capability of a Powered Device (PD) is using Link Layer Discovery Protocol (LLDP). In this protocol, the PSE communicates LLDP packets to the PD over Ethernet lines so that the PSE determines the power capability of the PD. In applications using the AS1860, 60W/90W capability of the PD can be communicated to the PSE in a number of ways:-

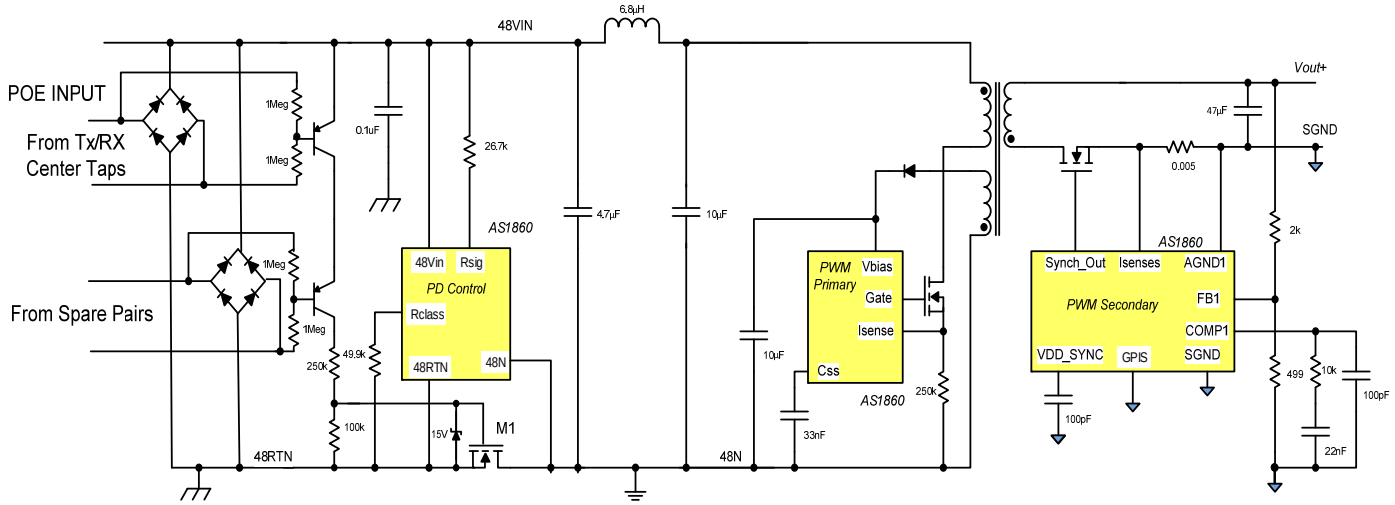
a) A logic level can be set on the PD board or a bit set in the local PD microcontroller that responds to the PSE LLDP communications that the PD is capable of processing 60/90W

b) An external Power FET (M1) is used in the AS1860 applications for 60W/90W to pass the high currents needed for the high power requirements. M1 will be turned ON by driving it's gate terminal high which is accomplished in a number of ways shown in the following sections. The voltage on the gate of M1 can be read on the primary side using the GPIP pin and transferred to the secondary side onto the GPOS pin. The logic level of GPOS can be communicated to the PSE to confirm that 60/90W is available.

Four Pair Voltage Sense Enabled

The four pair sensing circuit enables the external bypass MOSFET after the application of a second PSE (four pair conducting). For proper PSE/PD handshaking and inrush current limiting it is assumed that only one PSE is applied initially and the second PSE applies power after the AT signature and classification is complete for the first. The second PSE is turned on without handshaking.

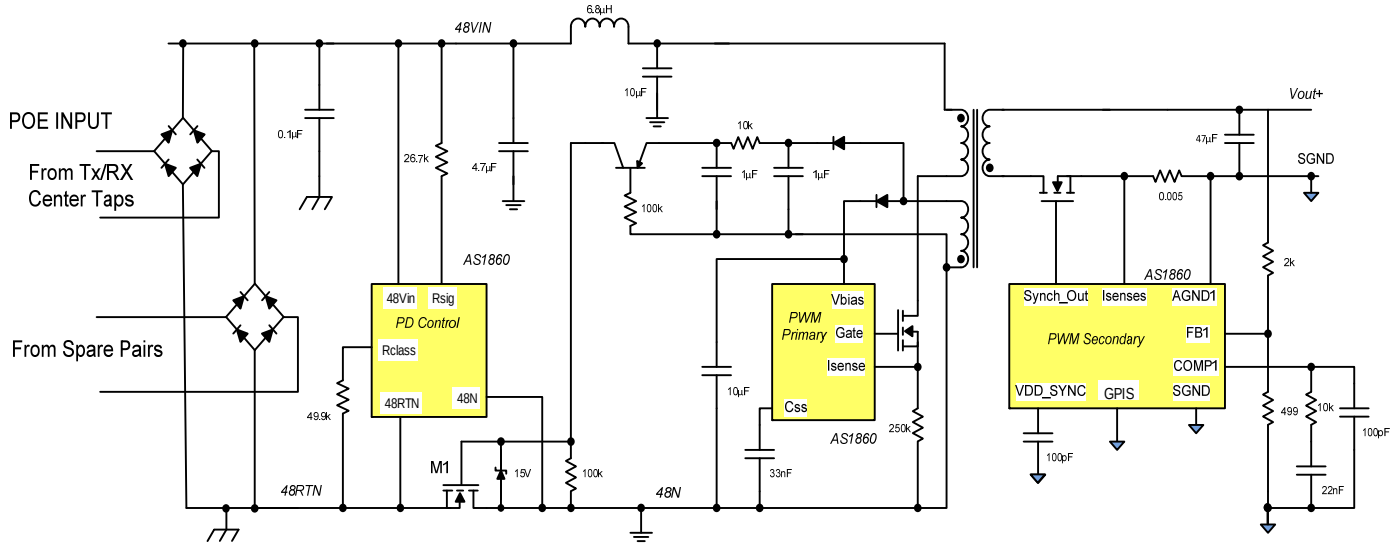
Figure 32 – Four Pair Sensing enabling external MOSFET M1



Switching Converter Primary Bias Enabled

The Switching Converter Primary Bias method develops a bias from the DC-DC converter and applies this to the external bypass MOSFET. After signature, classification and inrush of one PoE pair, the switching converter is enabled. Once the converter starts switching the bias winding is peak detected to develop the gate drive for the external bypass MOSFET, M1. Additional delay is added by way of an RC filter. In order to limit any leakage current prior to inrush complete (before internal bypass MOSFET is enabled) a PNP transistor is used to hold off the gate drive to M1.

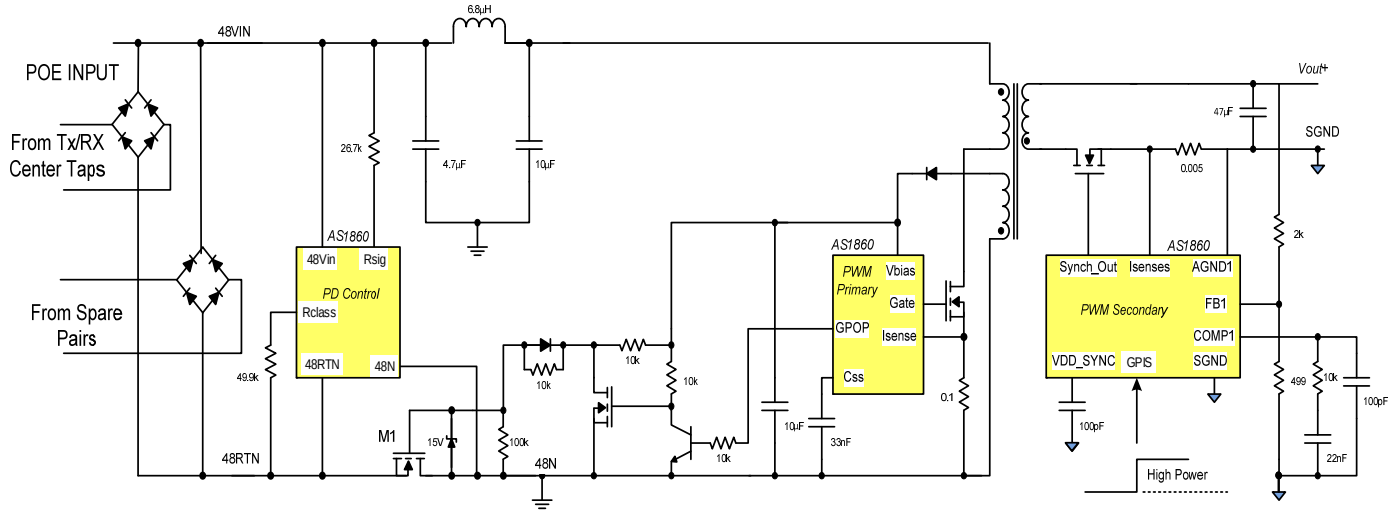
Figure 33 – Primary bias enabling external MOSFET M1



Secondary side Logic Enable

The secondary referenced logic enabled circuit accepts a logic signal from the secondary (GPIS) and applies it through the AS1860 isolation barrier to GPOP which allows the primary bias rail to be applied to the external bypass MOSFET (M1) gate.

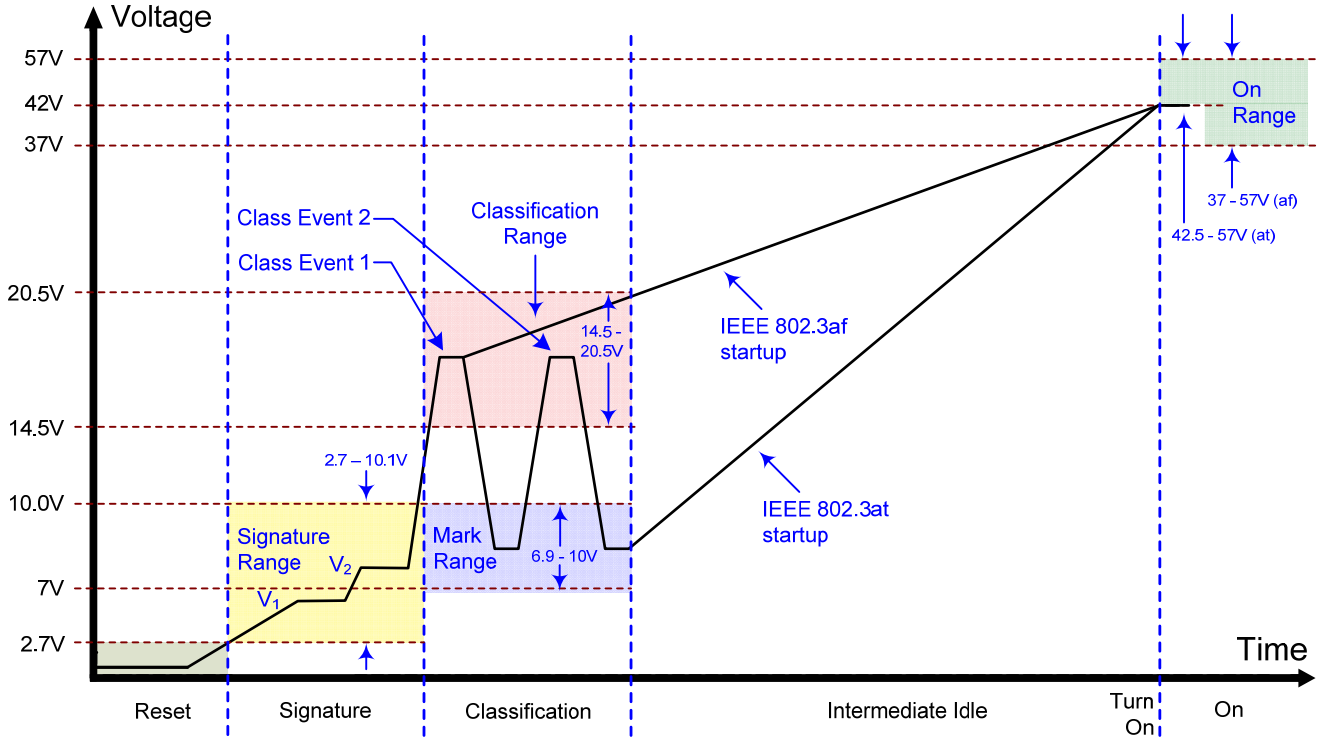
Figure 34 – Secondary side logic control of external MOSFET M1



POE POWER-ON SEQUENCE

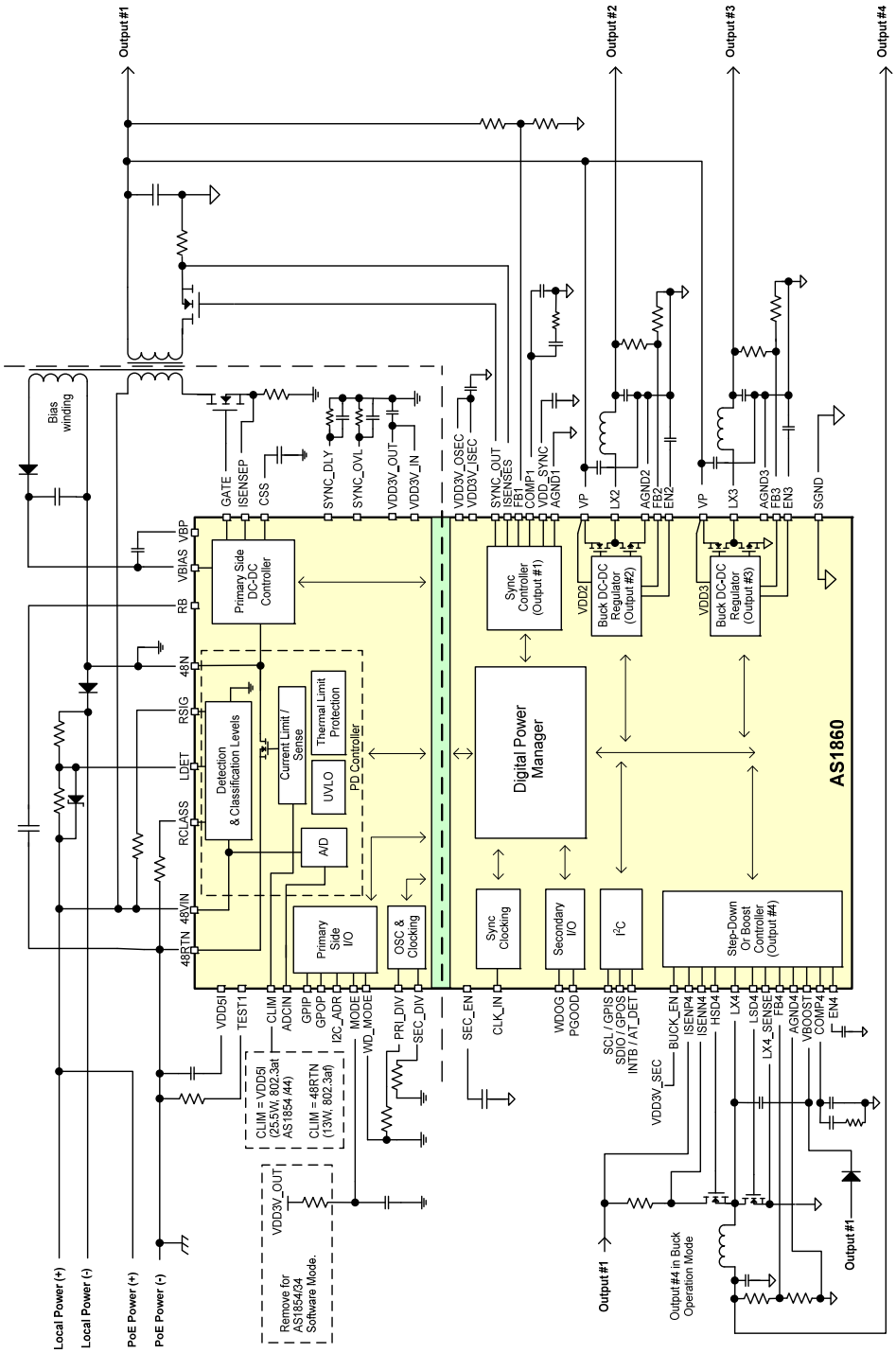
The power-on sequence for PoE operation is shown in Figure 29. The waveform reflects typical voltages present at the PD during signature, classification and power-on.

Figure 35 - PoE Power-On Sequence Waveform



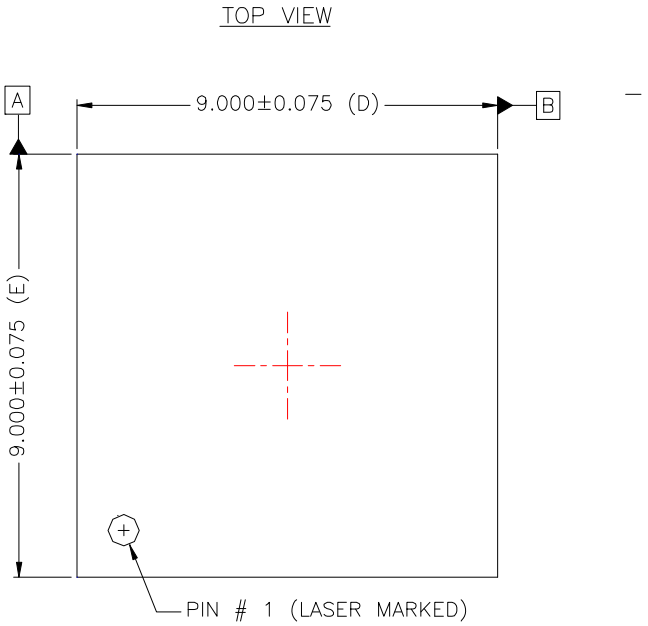
1. Voltages V1 and V2 are applied by the PSE to extract a signature value.
2. The PSE takes current/impedance readings during Class/Mark Events to determine the class of the PD. At this time, the PD presents a load current determined by the resistance connected to the RCLASS pin.
3. After the PSE measures the PD load current, if it is a high-power PSE, it presents a mark voltage (6.9-10V), followed by a second classification voltage. The PD responds by presenting a load current as determined by the resistor on the RCLASS pin. After the PSE measures the PD load current the second time and determines that is can deliver the requested power, it moves into the On state by raising the voltage to approximately 42V after which the PD operates over the On Range.

Figure 36 - Typical Isolated Synchronous Flyback Application

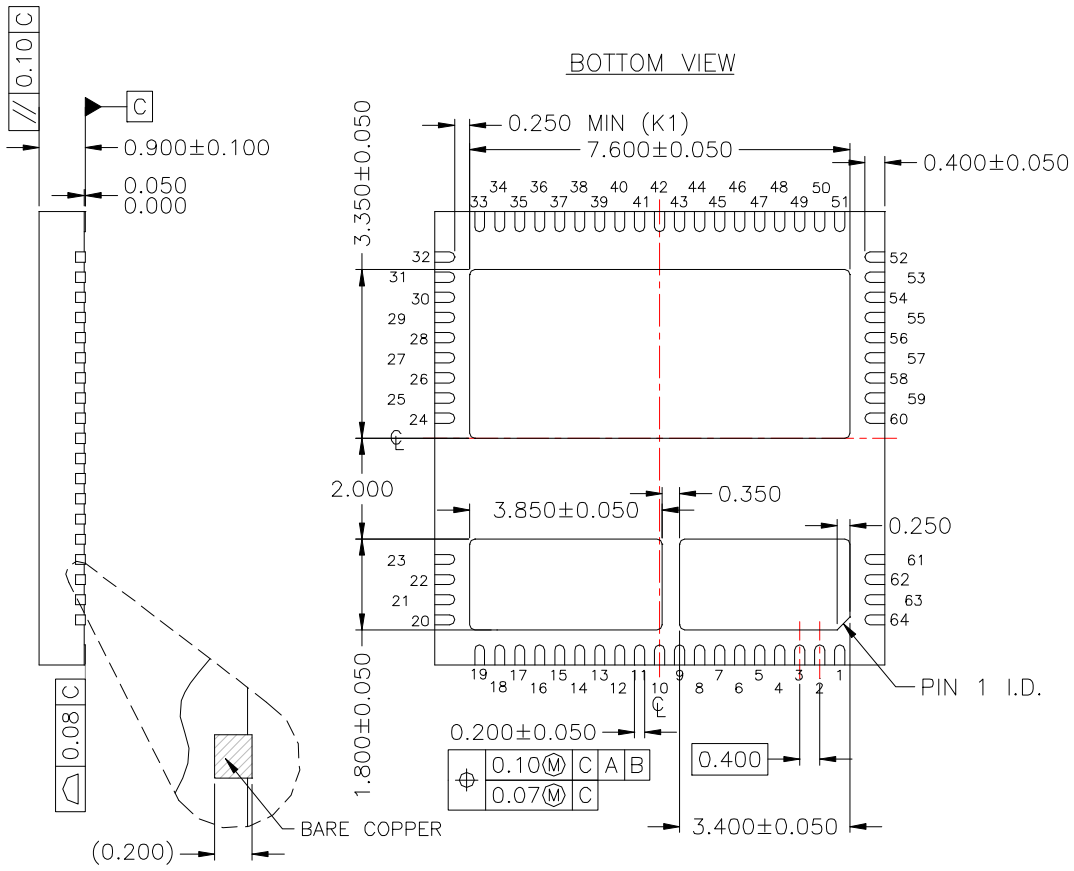


PACKAGE SPECIFICATIONS

Figure 37 - 64-Pin QFN Dimensions



NOTE :
1. Controlling Dimensions in mm.
2. REFER TO JEDEC MO-220 FOR DIMENSION NOT SHOWN HERE.
3. AVAILABLE LEADFRAME PART NUMBER : 16-064-374.


BOTTOM VIEW
0.10 C
C
0.900±0.100
0.050
0.000
0.08 C
(0.200)
BARE COPPER
3.350±0.050
2.000
1.800±0.050
0.250 MIN (K1)
7.600±0.050
0.400±0.050
3.850±0.050
0.350
0.250
0.200±0.050
0.10 M C A B
0.07 M C
0.400
3.400±0.050
PIN 1 I.D.

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