

DATA SHEET

AS225-313LF: PHEMT GaAs IC 1 W Low-Loss 0.1 to 6 GHz SPDT Switch

Applications

- WLAN 802.11a/b/g

Features

- Positive low voltage control (0/3 V)
- Low insertion loss (0.6 dB, 0.1 to 6 GHz)
- High linearity (IIP3 = +53 dBm @ 3 V)
- PHEMT process
- Miniature QFN (6-pin, 2 x 3 mm) package (MSL1, 260 °C per JEDEC J-STD-020)



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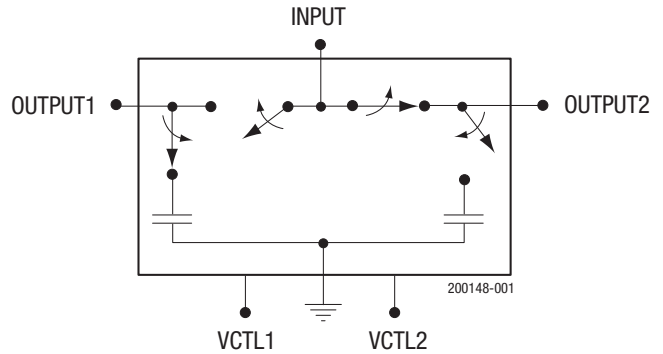


Figure 1. AS225-313LF Functional Block Diagram

Description

The AS225-313LF is a 0.1 to 6 GHz PHEMT GaAs IC single-pole, double-throw (SPDT) antenna switch. Designed for WLAN applications, this device is capable of switching 1 W microwave signals with 3 V control voltage while maintaining high-linearity performance. The switch covers the entire 802.11a, b, and g frequency ranges. The low-loss, high-isolation, high-linearity, and low-cost features make this switch ideal for Wireless LAN systems.

Figure 1 shows the functional block diagram of the AS225-313LF. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

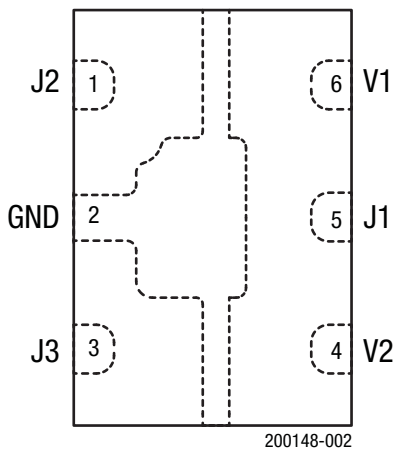


Figure 2. AS225-313LF Pinout (Top View)

Table 1. SKY13290-313LF Signal Descriptions

| Pin | Name | Description | Pin | Name | Description |
|-----|------|--|-----|------|---|
| 1 | J2 | RF input/output. According to the logic voltage levels applied to the V1 and V2 pins, this port is either connected to J1 using a low insertion loss path or isolated from J1. | 4 | V2 | DC control voltage input 2. The logic voltage applied to this pin, along with the voltage level applied to the V1 pin, determines the states of the RF paths between J1/J2 and J1/J3. |
| 2 | GND | Ground. Equipotential port, internal circuit common, which must connected to the PCB ground or common using the lowest possible impedance. | 5 | J1 | RF input/output. According to the logic voltage levels applied to the V1 and V2 pins, this port is either connected to J2 or to J3 using a low insertion loss path and isolated from the other RF port. |
| 3 | J3 | RF input/output. According to the logic voltage levels applied to the V1 and V2 pins, this port is either connected to J1 using a low insertion loss path or isolated from J1. | 6 | V1 | DC control voltage input 1. The logic voltage applied to this pin, along with the voltage level applied to the V2 pin, determines the states of the RF paths between J1/J2 and J1/J3. |

Electrical and Mechanical Specifications

The absolute maximum ratings for the AS225-313LF are shown in Table 2. Electrical specifications are provided in Tables 3 and 4.

The state of the AS225-313LF is determined by the logic provided in Table 5. Typical performance characteristics are shown in Figures 3, 4, and 5.

Table 2. AS225-313LF Absolute Maximum Ratings¹

| Parameter | Symbol | Minimum | Maximum | Units |
|-----------------------|------------------|---------|---------|-------|
| Input power @ 0/3 V | | | +32 | dBm |
| Input power @ 0/5 V | | | +35 | dBm |
| Operating voltage | | | 8 | V |
| Operating temperature | T _A | -40 | +85 | °C |
| Storage temperature | T _{STG} | -65 | +150 | °C |

¹ Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

ESD HANDLING: *Although this device is designed to be as robust as possible, electrostatic discharge (ESD) can damage this device. This device must be protected at all times from ESD when handling or transporting. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD handling precautions should be used at all times.*

Table 3. AS225-313LF Electrical Specifications¹
(Z₀ = 50 Ω, V_{CTRL} = 0/3 V, C_{BLOCK} = 15 pF, T_A = 25 °C, Unless Otherwise Noted)

| Parameter | Test Condition | Frequency | Min | Typ | Max | Units |
|----------------|----------------|------------------|-----|------|------|-------|
| Insertion loss | J1–J2, J1–J3 | 0.10 to 6.00 GHz | | 0.60 | 0.75 | dB |
| | | 2.40 to 2.50 GHz | | 0.50 | 0.65 | dB |
| | | 5.15 to 5.85 GHz | | 0.60 | 0.70 | dB |
| Isolation | J1–J2, J1–J3 | 0.10 to 6.00 GHz | 18 | 20 | | dB |
| | | 2.40 to 2.50 GHz | 18 | 20 | | dB |
| | | 5.15 to 5.85 GHz | 19 | 21 | | dB |
| Return loss | J1–J2, J1–J3 | 0.10 to 6.00 GHz | 18 | 20 | | dB |
| | | 2.40 to 2.50 GHz | 23 | 25 | | dB |
| | | 5.15 to 5.85 GHz | 21 | 23 | | dB |

¹ Performance is guaranteed only under the conditions listed in this table.

Table 4. AS225-313LF Electrical Characteristics¹
(Z₀ = 50 Ω, V_{CTRL} = 0/3 V, C_{BLOCK} = 15 pF, T_A = 25 °C, Unless Otherwise Noted)

| Parameter | Condition | Frequency | Min | Typ | Max | Units |
|----------------------------|---|-----------|-----|-------|------|-------|
| Switching characteristics: | | | | | | |
| Rise, fall | 10/90% or 90/10% RF | | | 20 | | ns |
| On, off | 50% CTL to 90/10% RF | | | 35 | | ns |
| P1dB | @ 3 V | 5200 MHz | | +30 | | dBm |
| | @ 5 V | 5200 MHz | | +34 | | dBm |
| 2 nd harmonic | P _{IN} = +22 dBm, V _C = 3 V V _C = 5 V | 2450 MHz | | +70 | | dBc |
| | | 2450 MHz | | +75 | | dBc |
| 3 rd harmonic | P _{IN} = +22 dBm, V _C = 3 V V _C = 5 V | 2450 MHz | | +68 | | dBc |
| | | 2450 MHz | | +70 | | dBc |
| Input IP3 | Two-tone 15 dBm, 5 MHz spacing: V _{CTL} = 0/3 V V _{CTL} = 0/5 V | 5200 MHz | | +53 | | dBm |
| | | 5200 MHz | | +55 | | dBm |
| Control voltage | V _C HIGH | | 2.5 | 3.00 | 5.00 | V |
| | V _C LOW | | | -0.25 | 0.25 | V |
| Gate leakage | V _C = 3 V | | | 10 | 100 | μA |
| | V _C = 5 V | | | 15 | 200 | μA |

¹ Performance is guaranteed only under the conditions listed in this table.

Table 5. AS225-313LF Truth Table^{1,2}

| V1 | V2 | J1–J2 | J1–J3 |
|-------------------|-------------------|----------------|----------------|
| 0 | V _{HIGH} | Isolation | Insertion loss |
| V _{HIGH} | 0 | Insertion loss | Isolation |

¹ All other conditions not recommended.

² V_{HIGH} = 2.5 to 5 V.

Typical Performance Characteristics

($Z_0 = 50 \Omega$, $V_{CTRL} = 0/3 V$, $C_{BLOCK} = 15 pF$, Unless Otherwise Noted)

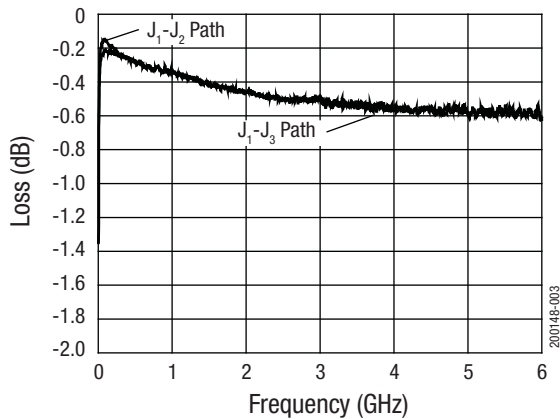


Figure 3. Insertion Loss vs Frequency

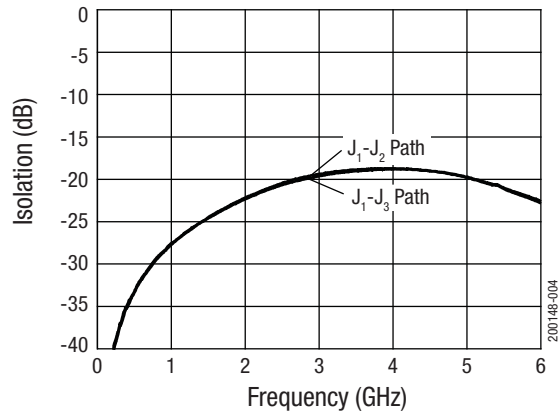


Figure 4. Isolation vs Frequency

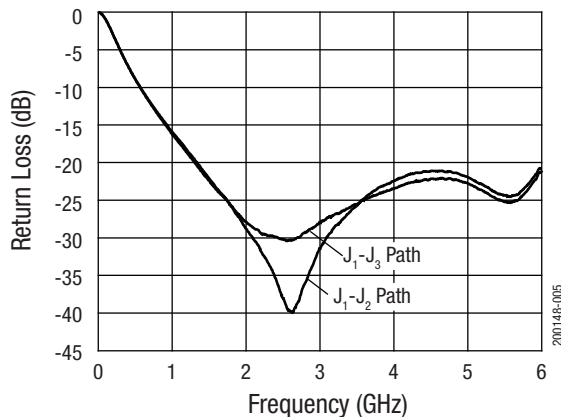


Figure 5. Return Loss vs Frequency

Evaluation Board and Package Dimensions

The AS225-313LF Evaluation Board is used to test the performance of the AS225-313LF SPDT switch. An Evaluation Board schematic diagram is provided in Figure 6. An assembly drawing for the Evaluation Board is shown in Figure 7.

Package Dimensions

The PCB layout footprint for the AS225-313LF is shown in Figure 8. The typical part marking is shown in Figure 9. Package dimensions are shown in Figure 10. The tape and reel dimensions are provided in Figure 11.

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The AS225-313LF is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C for 5 seconds. They can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

For additional information, refer to the *Discrete Devices and IC Switch/Attenuators Tape and Reel Package Orientation* Application Note.

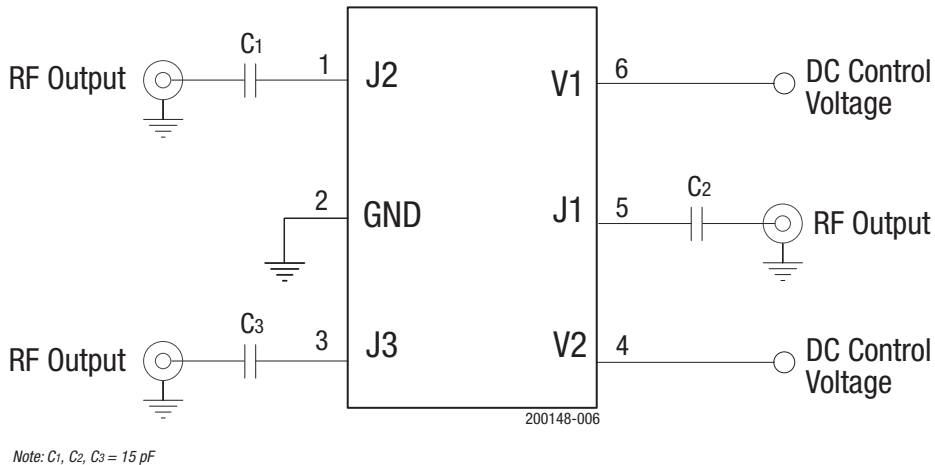


Figure 6. AS225-313LF Evaluation Board Schematic

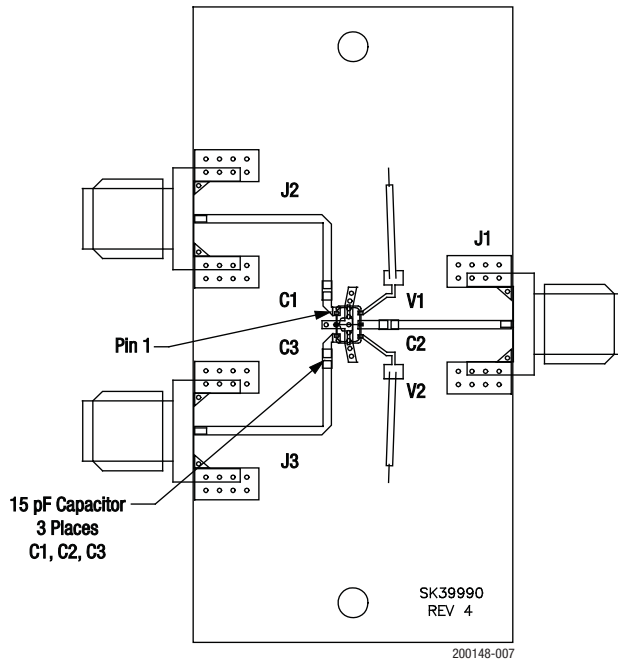


Figure 7. AS225-313LF Evaluation Board Assembly Drawing

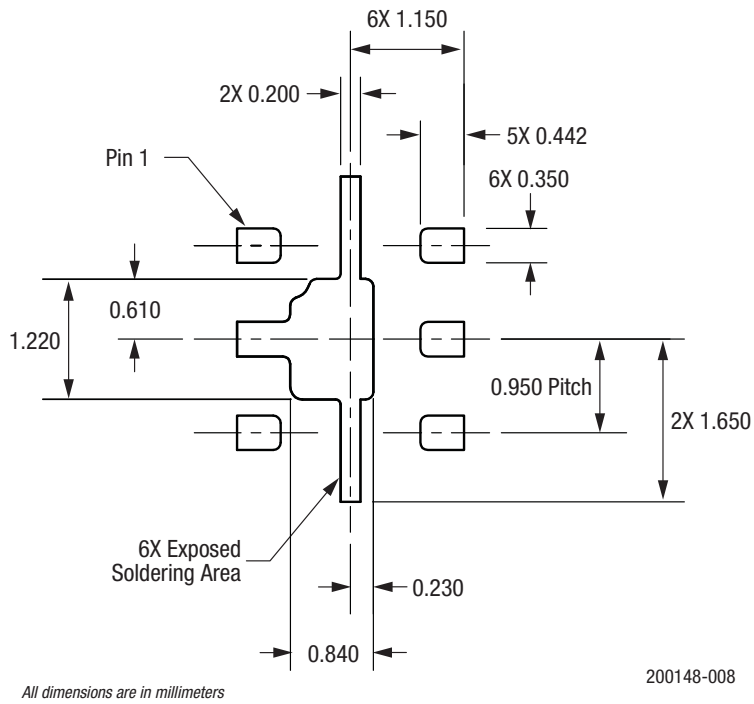


Figure 8. AS225-313LF PCB Layout Footprint (Top View)

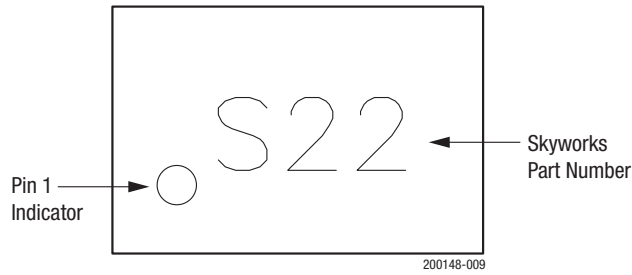
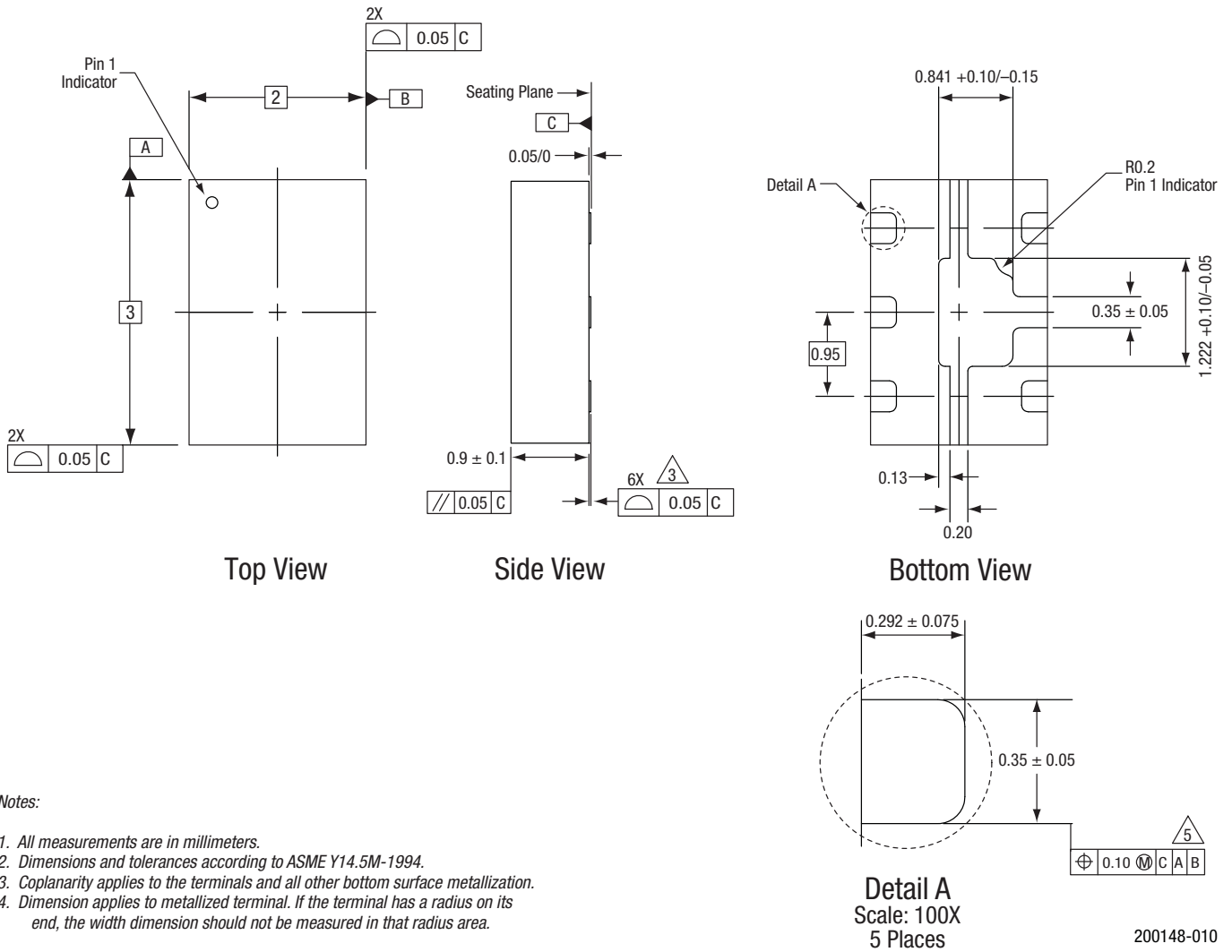


Figure 9. AS225-313LF Typical Part Marking (Top View)



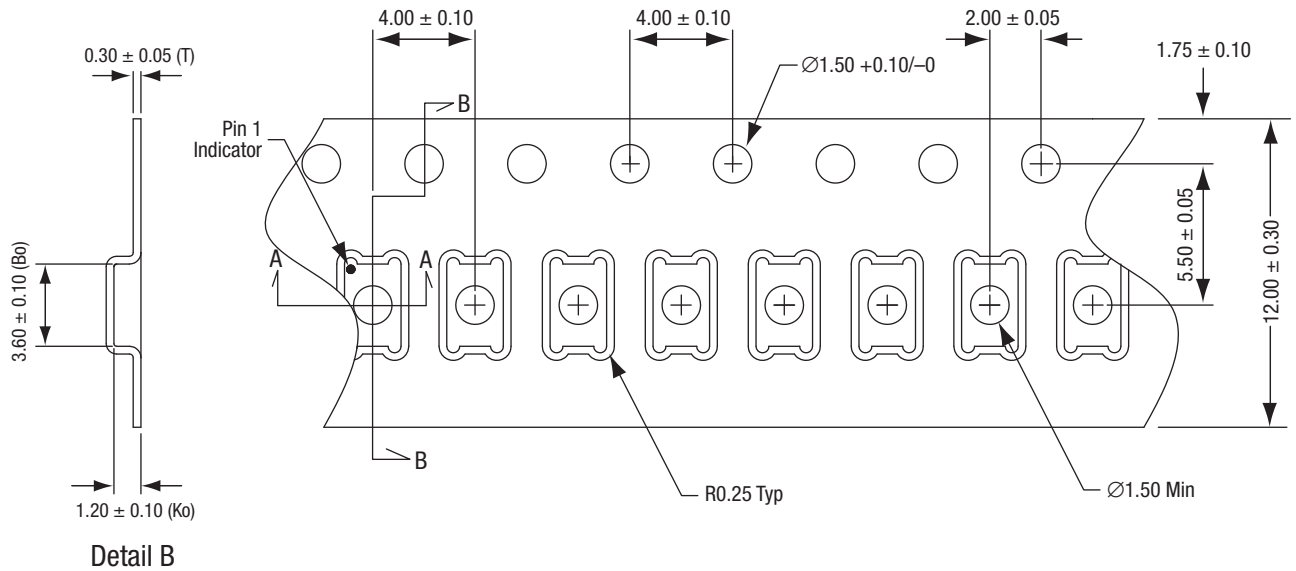
Notes:

1. All measurements are in millimeters.
2. Dimensions and tolerances according to ASME Y14.5M-1994.
3. Coplanarity applies to the terminals and all other bottom surface metallization.
4. Dimension applies to metallized terminal. If the terminal has a radius on its end, the width dimension should not be measured in that radius area.

Figure 10. AS225-313LF Package Dimensions

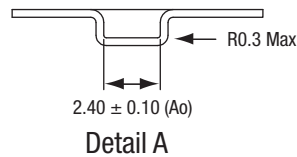
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Notes:

1. Carrier tape: black conductive polystyrene, non-bakeable material.
2. Cover tape material: transparent conductive HSA with 9.20 mm width.
3. ESD-surface resistivity is $\geq 1 \times 10^5 \sim \leq 1 \times 10^{10}$ Ohms/square per EIA, JEDEC TNR Specification.
4. All measurements are in millimeters.



200148-011

Figure 11. AS225-313LF Tape and Reel Dimensions

Ordering Information

| Model Name | Manufacturing Part Number | Evaluation Board Part Number |
|-------------------------|---------------------------|------------------------------|
| AS225-313LF SPDT Switch | AS225-313LF | AS225-313LF-EVB |

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