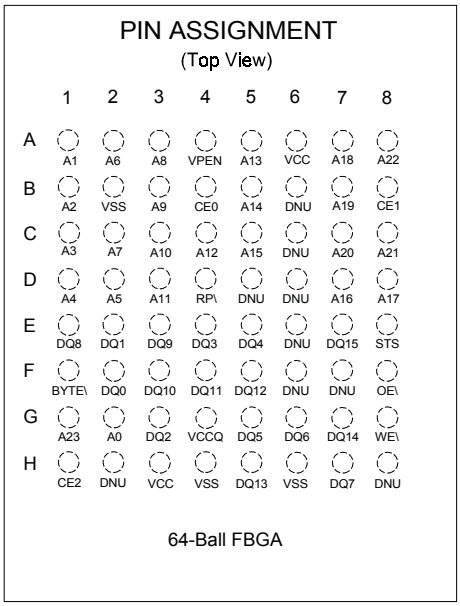
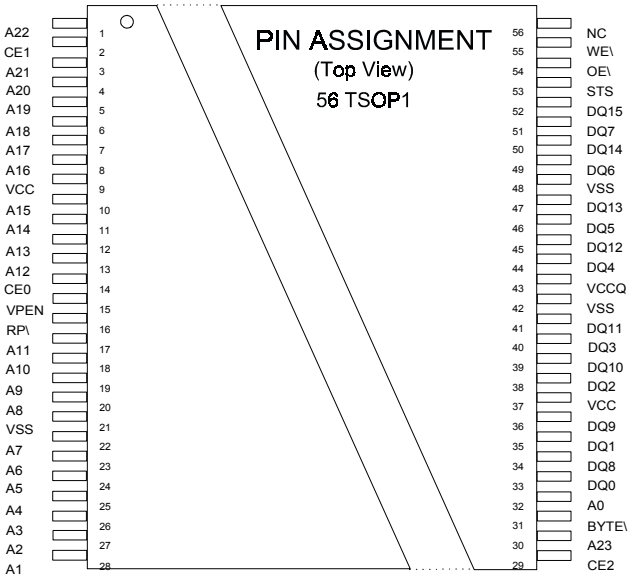
micross components

transforming specialty electronics

PEM
AS28F128J3A
Q-Flash

Plastic Encapsulated Microcircuit
128Mb, x8 and x16 Q-FLASH Memory
Even Sectored, Single Bit per Cell Architecture





FEATURES

- 100% Pin and Function compatible to Intel's MLC Family
- NOR Cell Architecture
- 2.7V to 3.6V VCC
- 2.7V to 3.6V or 5V VPEN (Programming Voltage)
- Asynchronous Page Mode Reads
- Manufacturer's ID Code:
  - ✓ Numonyx 0x89h
- Industry Standard Pin-Out
- Fully compatible TTL Input and Outputs
- Common Flash Interface [CFI]
- Scalable Command Set
- Automatic WRITE and ERASE Algorithms
- 5.6us per Byte effective programming time
- 128 bit protection register
  - ✓ 64-bit unique device identifier
  - ✓ 64-bit user programmable OTP cells
- Enhanced data protection feature with use of VPEN=VSS
- Security OTP block feature
- 100,000 ERASE cycles per BLOCK
- Automatic Suspend Options:
  - ✓ Block ERASE SUSPEND-to-READ
  - ✓ Block ERASE SUSPEND-to-PROGRAM
  - ✓ PROGRAM SUSPEND-to-READ
- Available Operating Ranges:
  - ✓ Enhanced [**-ET**] -40°C to +105°C
  - ✓ Mil-Temperature [**-XT**] -55°C to +125°C

For in-depth functional product detail and Timing Diagrams, please reference Numonyx's full product Datasheet:

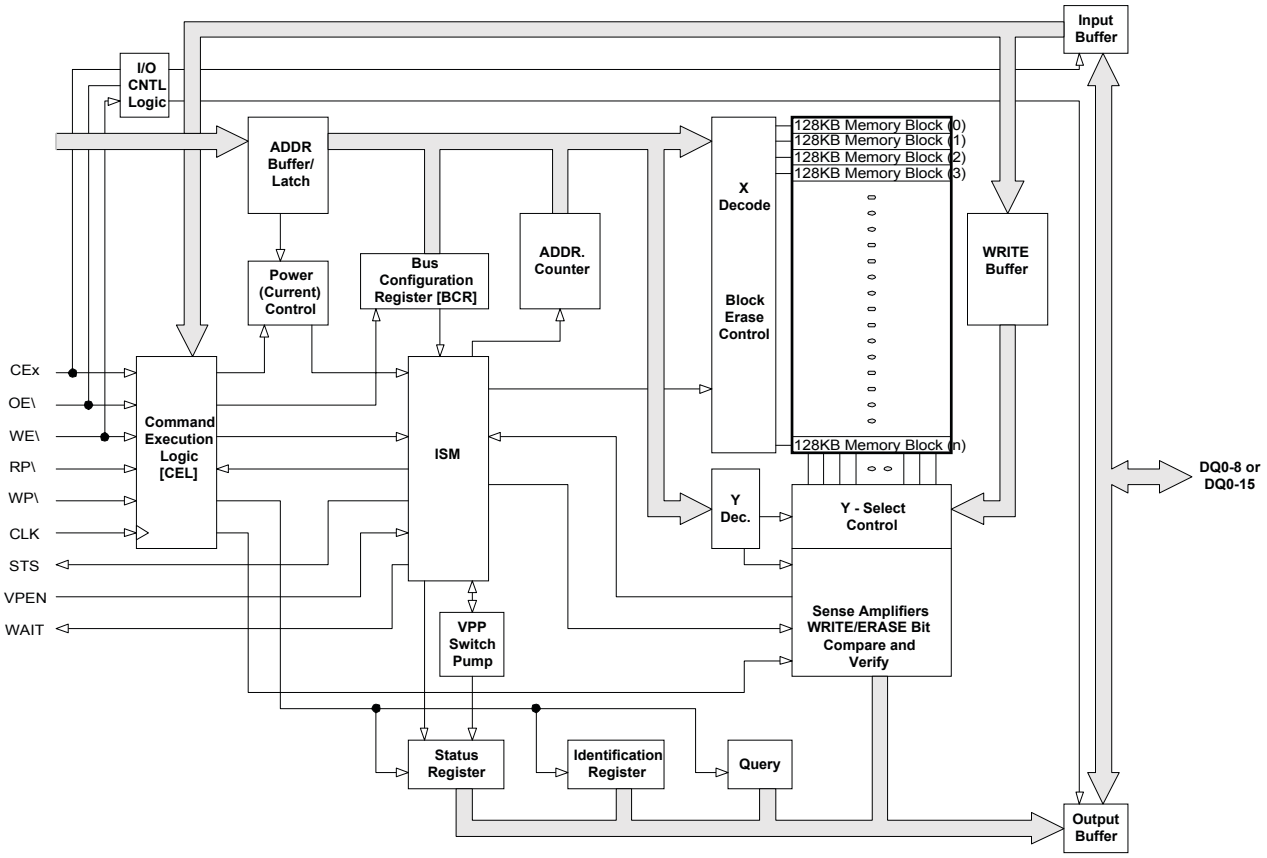
EMBEDDED FLASH MEMORY (J3-65nm)
Dated: March 2010

GENERAL DESCRIPTION

Micross' AS28F128J3A Enhanced or Mil-Temp variant of Numonyx's Q-Flash family of devices, is a nonvolatile, electrically block-erasable (FLASH), programmable memory device manufactured using Numonyx's 0.15um process technology. This device containing 134,217,728 bits organized as either 16,777,218 (x8) or 8,388,608 bytes (x16). The device is uniformly sectored with one hundred and twenty eight 128KB ERASE blocks.

This device features in-system block locking. They also have a Common FLASH Interface [CFI] that permits software algorithms to be used for entire families of devices. The software is device-independent, JEDEC ID-independent with forward and backward compatibility.

Functional Block Diagram:



Additionally, the Scaleable Command Set [SCS] allows a single, simple software driver in all host systems to work with all SCS compliant FLASH memory devices. The SCS provides the fastest system/device data transfer rates and minimizes the device and system-level implementation costs.

To optimize the processor-memory interface, the device accommodates VPEN, which is switchable during BLOCK ERASE, PROGRAM, or LOCK BIT configurations and in addition can be hard-wired to VCC all dependent on the end application(s). VPEN is treated as an input pin to enable ERASING, PROGRAMMING, and BLOCK LOCKING. When VPEN is lower than the VCC lockout voltage (VLKO), all program functions are disabled. BLOCK ERASE SUSPEND mode enables the user to stop BLOCK ERASE to READ data from or PROGRAM data to any other blocks. Similarly, PROGRAM SUSPEND mode enables the user to SUSPEND PROGRAMMING to READ data or execute code from any un-suspended block(s).

VPEN serves as an input with 2.7V, 3.3V or 5V levels for application programming. VPEN in this Q-Flash device can provide data protection when connected to ground. This pin also enables PROGRAM or ERASE LOCKOUT functions/ controls during power transitions.

This device is an even-sectored device architecture offering individual BLOCK LOCKING that can LOCK and UN-LOCK a block using the SECTOR LOCK BITS command sequence.

Status [STS] is a logic signal output that gives an additional indicator of the internal state machine [ISM] activity by providing a hardware signal of both the status and status masking. This status indicator minimizes central processing unit overhead and system power consumption. In the default mode, STS acts as an RY/BY\ pin. When LOW, STS indicates that the ISM is performing a BLOCK ERASE, PROGRAM, or LOCK BIT configuration. When HIGH, STS indicates that the ISM is ready for a new command.

Three Chip Enable (CEx) pins are used for enabling and disabling the device by activating the device's control logic, input buffer, decoders, and sense amplifiers.

BYTE\ enables the device to be used in x8 or x16 configuration. Byte=Low (logic 0) selects and 8-bit mode with address zero (A0) selecting the High or Low Byte and Byte=High (logic 1) selects the 16-bit or Word mode. When the device is in Word mode, address one (A1) becomes the low order address bit and address zero (A0) becomes a no-connect (NC).

RP\ is used to reset the device. When the device is disabled and RP\ is at VCC, the STANDBY mode is enabled. A reset time (tRWH) is required after RP\ switches to a High (logic 1) and the outputs become valid. Likewise, the device has a wake time (tRS) from RP\ High until WRITES to the Command User Interface [CUI] are recognized, RESETS the ISM and clears the status register.

Chip Enable Truth Table

CE2	CE1	CE0	Device
VIL	VIL	VIL	Enabled
VIL	VIL	VIH	Disabled
VIL	VIH	VIL	Disabled
VIL	VIH	VIH	Disabled
VIH	VIL	VIL	Enabled
VIH	VIL	VIH	Enabled
VIH	VIH	VIL	Enabled
VIH	VIH	VIH	Disabled

Capacitance

Parameter/Condition	Symbol	Typ	Max	Units
Input Capacitance	Cin	5	8	pF
Output Capacitance	Cbyte	14	16	pF
	Cout	5	12	pF

Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for any duration or segment of time may affect device reliability.

Absolute Maximum Ratings

Voltage	Min	Max	Units	Notes
Temperature Under Bias	-55	125	°C	
Storage Temperature	-65	125	°C	
Short Circuit Current		100	mA	1

Notes
1: All specified voltages are with respect to GND. Minimum DC voltage is -0.5v on input/output pins and -0.2v on Vcc and VPEN pins. During transitions, this level may undershoot to -2.0v for periods </= 20ns. Maximum DC voltage on input/output pins, Vcc and VPEN is VCC+0.5V which, during transitions, may overshoot to Vcc + 2.0v for periods <20ns.

Pin Description Table

Signal Name	Symbol	Type	Pin	Description
Address	A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, A12,A13,A14,A15, A16,A17,A18,A19, A20,A21,A22,A23	Input	32,28,27,26, 25,24,23,22, 20,19,18,17, 13,12,11,10, 8,7,6,5, 4,3,1,30	Address Inputs during READ and WRITE Operations. A0 is only used in x8 mode and will be a NC in x16 mode.
Chip Enables	CE0, CE1, CE2	Input	14, 2, 29	Three Chip Enable pins for Multiple devices. See chart for function
Write Enable	WE\	Input	55	Write Control
Reset/Power Down	RP\	Input	16	Reset/Power-Down, When Low the control pin resets the status Reg.and ISM to array READ mode.
Output Enable	OE\	Input	54	Output Enable control enable data output buffers when Low, and when High the output buffers are disabled
Byte Mode Control	BYTE\	Input	31	Configuration Control pin. When High the device is in x16 mode, when Low the device is in Byte mode (x8)
Programming Voltage	VPEN	Input	15	Necessary Voltage pin for Programming, Erasing or configuring lock bits. Typically connected to VCC. When VPEN</=VPENLK, this enables Hardware Write Protect.
Status Pin/Flag	STS	Output	53	Indicates the status of the ISM. When configured in level mode, STS acts as a RY/BY\ pin. When configured in its pulse mode, it can pulse to indicate PROGRAM and or ERASE completion.
Input/Output Voltage	VCCQ	Supply	43	Separate/Isolated Voltage supply for Input/Output bus. Allows voltage matching to different interface standards.
Supply Voltage	VCC	Supply	9, 37	Power Supply: 2.7V-3.6V
Digital Ground	GND	Supply	21,42,48	Ground
No Connect(s)	NC	-	1,30,56	No electrical connection or function

Bus Operations

Mode	RP\	CE0	CE1	CE2	OE\	WE\	VPEN	DQ	Notes	Address	STS Default Mode
Read Array	VIH	Enabled	Enabled	Enabled	VIL	VIH	X	Dout	1,2,3	X	High-Z (VOH with External PU)
Output Disable	VIH	Enabled	Enabled	Enabled	VIH	VHI	X	High-Z		X	X
Standby	VIH	Disabled	Disabled	Disabled	X	X	X	High-Z		X	X
Reset/Power-Down	VIL	X	X	X	X	X	X	High-Z		X	High-Z (VOH with External PU)
Read Identifier Codes	VIH	Enabled	Enabled	Enabled	VIL	VIH	X		4	See Table 31 of Numonyx DS	High-Z (VOH with External PU)
Read Query	VIH	Enabled	Enabled	Enabled	VIL	VIH	X		5	See CFI Query of Numonyx DS	High-Z (VOH with External PU)
Read Status (ISM off)	VIH	Enabled	Enabled	Enabled	VIL	VIH	X			X	X
Read Status (ISM on)	VIH	Enabled	Enabled	Enabled	VIL	VIH	X	Dout		X	X
Write	VIH	Enabled	Enabled	Enabled	VIH	VIL	VPENH	Din	3,6,7	X	X

Notes
1 Refer to DC Characteristics. When VPEN</= VPENLK, memory contents can be read but not altered
2 X can be VIL or VIH for control and address pins, and VPENLK or VPENH for VPEN. See DC Characteristics for VPENLK and VPENH voltages
3 In default mode, STA is VOL when the ISM is executing internal Block Erase, Program, or lock bit configuration algorithms. It is VOH when the ISM is not busy, in block erase suspend mode, program suspend mode, or reset/power-down mode.
4 See Read Identifier codes of the Numonyx Datasheet (DS)
5 See Read Query Mode Command section of the Numonyx Datasheet (DS)
6 Command Writes involving block erase, program, or lock bit configuration are reliably executed when VPEN=VPENH and VCC is within Specification
7 Refer to Table 19 on page 35 of the Numonyx Datasheet (DS)

DC Electrical Characteristics

(TA=Min/Max temperatures of Operational Range chosen)

V_{CCQ}		2.7 - 3.6V				
V_{CC}		2.7 - 3.6V				
Symbol	Parameter	Typ	Max	Units	Test Conditions	Notes
I_{LI}	Input and V_{PEN} Load Current	-	±1	µA	$V_{CC} = V_{CC}$ Max; $V_{CCQ} = V_{CCQ}$ Max $V_{IN} = V_{CCQ}$ or V_{SS}	1
I_{LO}	Output Leakage Current	-	±10	µA	$V_{CC} = V_{CC}$ Max; $V_{CCQ} = V_{CCQ}$ Max $V_{IN} = V_{CCQ}$ or V_{SS}	1
I_{CCS}	V_{CC} Standby Current	50	400	µA	CMOS Inputs, $V_{CC} = V_{CC}$ Max; $V_{CCQ} = V_{CCQ}$ Max, Device is disabled, RP# = V_{CCQ} ± 0.2 V	1,2,3
		0.71	2	mA	TTL Inputs, $V_{CC} = V_{CC}$ Max, $V_{CCQ} = V_{CCQ}$ Max, Device is disabled, RP# = V_{IH}	
I_{CCD}	V_{CC} Power-Down Current	50	400	µA	RP# = V_{SS} ± 0.2 V, I_{OUT} (STS) = 0 mA	
I_{CCR}	8-Word Page	15	20	mA	CMOS Inputs, $V_{CC} = V_{CC}$ Max, $V_{CCQ} = V_{CCQ}$ Max using standard 8 word page mode reads. Device is enabled. f = 5 MHz, I_{OUT} = 0 mA	1,3
		30	54	mA	CMOS Inputs, $V_{CC} = V_{CC}$ Max, $V_{CCQ} = V_{CCQ}$ Max using standard 8 word page mode reads. Device is enabled. f = 33 MHz, I_{OUT} = 0 mA	
I_{CCW}	V_{CC} Program or Set Lock-Bit Current	35	60	mA	CMOS Inputs, $V_{PEN} = V_{CC}$	1,4
		40	70	mA	TTL Inputs, $V_{PEN} = V_{CC}$	
I_{CCE}	V_{CC} Block Erase or V_{CC} Blank Check or Clear Block Lock-Bits Current	35	70	mA	CMOS Inputs, $V_{PEN} = V_{CC}$	1,4
I_{CCBC}		40	80	mA	TTL Inputs, $V_{PEN} = V_{CC}$	
I_{CCWS}	V_{CC} Program Suspend or Block Erase Suspend Current	-	10	mA	Device is enabled	1,5
I_{CCES}						

Notes
1. All currents are in RMS unless otherwise noted. These currents are valid for all product versions (packages and speeds).
2. Includes STS.
3. CMOS inputs are either VCC ± 0.2 V or VSS ± 0.2 V. TTL inputs are either VIL or VIH.
4. Sampled, not 100% tested.
5. ICCWS and ICCES are specified with the device selected. If the device is read or written while in erase suspend mode, the device's current draw is ICCR and ICCWS.

DC Voltage specifications

V_{CCQ}		2.7 - 3.6V				
V_{CC}		2.7 - 3.6V				
Symbol	**Parameter**	**Min**	**Max**	**Units**	**Test Conditions**	**Notes**
V_{IL}	Input Low Voltage	-0.5	0.8	V	-	2,5,6
V_{IH}	Input High Voltage	2.0	V_{CCQ}+0.5	V	-	2,5,6
V_{OL}	Output Low Voltage	-	0.4	V	$V_{CC} = V_{CC}$Min $V_{CCQ} = V_{CCQ}$ Min I_{OL} = 2 mA	1,2
		-	0.2	V	$V_{CC} = V_{CC}$Min $V_{CCQ} = V_{CCQ}$ Min I_{OL} = 100 µA	
V_{OH}	Output High Voltage	0.85 × V_{CCQ}	-	V	$V_{CC} = V_{CC}$Min $V_{CCQ} = V_{CCQ}$ Min I_{OH} = 2.5 mA	1,2
		V_{CCQ} – 0.2	-		$V_{CC} = V_{CC}$Min $V_{CCQ} = V_{CCQ}$ Min I_{OH} = 100 µA	
V_{PENLK}	V_{PEN} Lockout during Program, Erase and Lock-Bit Operations	-	2.2	V	-	2,3
V_{PENH}	V_{PEN} during Block Erase, Program, or Lock-Bit Operations	2.7	3.6	V	-	3
V_{LKO}	V_{CC} Lockout Voltage	-	2.0	V	-	4

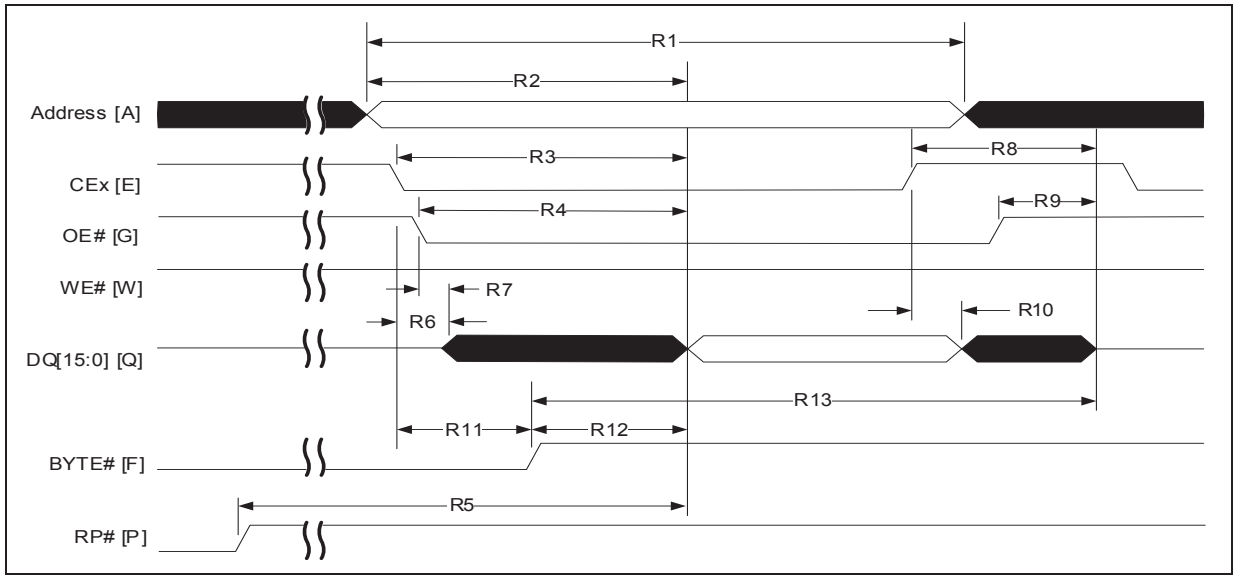
Notes
1. Includes STS.
2. Sampled, not 100% tested.
3. Block erases, programming, and lock-bit configurations are inhibited when VPEN ≤ VPENLK, and not guaranteed in the range between VPENLK (max) and VPENH (min), and above VPENH (max).
4. Block erases, programming, and lock-bit configurations are inhibited when VCC < VLKO, and not guaranteed in the range between VLKO (min) and VCC (min), and above VCC (max).
5. Includes all operational modes of the device.
6. Input/Output signals can undershoot to -1.0V referenced to VSS and can overshoot to VCCQ + 1.0V for duration of 2ns or less, the VCCQ valid range is referenced to VSS.

Read Operations

Asynchronous Specifications V_{CC} = 2.7 V–3.6 V [3] and V_{CCQ} = 2.7 V–3.6 V[3]						
#	Sym	Parameter	Min	Max	Unit	Notes
R1	t_{AVAV}	Read/Write Cycle Time	115	-	ns	1,2
R2	t_{AVQV}	Address to Output Delay	115	-	ns	1,2
R3	t_{ELQV}	CEX to Output Delay	115	-	ns	1,2
R4	t_{GLQV}	OE# to Non-Array Output Delay	-	50	ns	1,2,4
R5	t_{PHQV}	RP# High to Output Delay	-	210	ns	1,2
R6	t_{ELQX}	CEX to Output in Low Z	0	-	ns	1,2,5
R7	t_{GLQX}	OE# to Output in Low Z	0	-	ns	1,2,5
R8	t_{EHQZ}	CEX High to Output in High Z	-	25	ns	1,2,5
R9	t_{GHQZ}	OE# High to Output in High Z	-	15	ns	1,2,5
R10	t_{OH}	Output Hold from Address, CEX, or OE# Change, Whichever Occurs First	0	-	ns	1,2,5
R11	t_{ELFL}/t_{ELFH}	CEX Low to BYTE# High or Low	-	10	ns	1,2,5
R12	t_{FLQV}/t_{FHQV}	BYTE# to Output Delay	-	1	ns	1,2
R13	t_{FLQZ}	BYTE# to Output in High Z	-	1	µs	1,2,5
R14	t_{EHEL}	CEx High to CEx Low	0	-	µs	1,2,5
R15	t_{APA}	Page Address Access Time	-	25	ns	5,6
R16	t_{GLQV}	OE# to Array Output Delay	-	25	ns	1,2,4

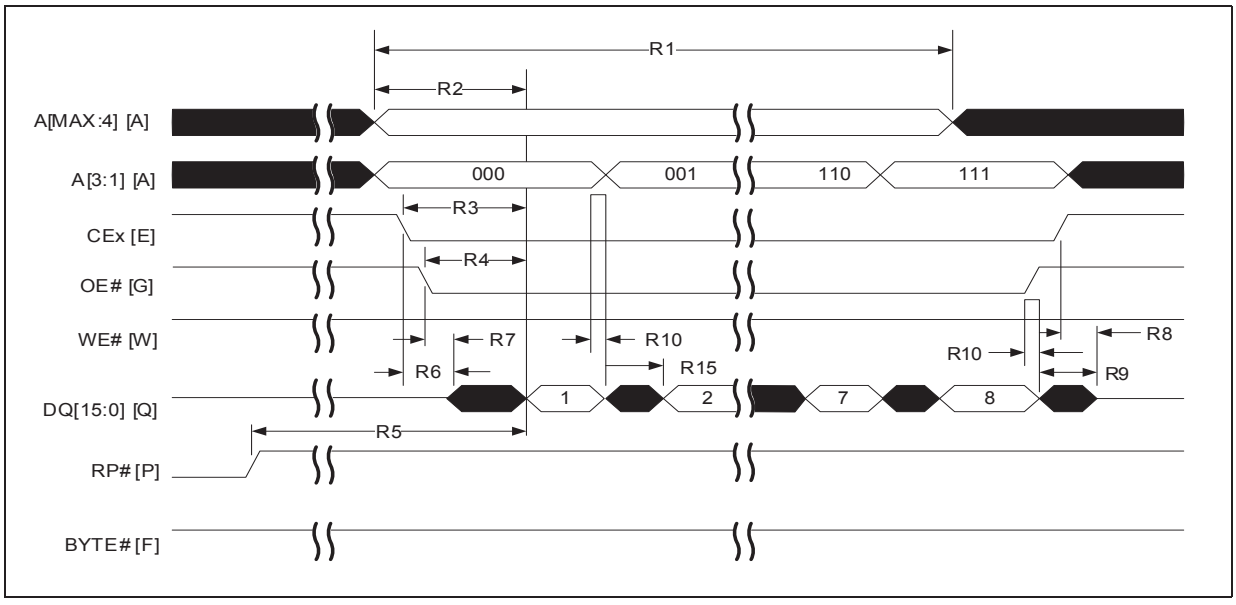
Notes
1. CEX low is defined as the combination of pins CE0, CE1 and CE2 that enable the device. CEX high is defined as the combination of pins CE0, CE1, and CE2 that disable the device
2. See AC Input/Output Reference Waveforms for the maximum allowable input slew rate.
3. OE# may be delayed up to tELQV-tGLQV after the falling edge of CEX
4. See Figure 13, “AC Input/Output Reference Waveform” , “Transient Equivalent Testing Load Circuit” for testing characteristics.
5. Sampled, not 100% tested.
6. For devices configured to standard word/byte read mode, R15 (tAPA) will equal R2 (tAVQV).

Single-Word Asynchronous Read Waveform



Notes
1. CEX low is defined as the combination of pins CE0, CE1, and CE2 that enable the device. CEX high is defined as the combination of pins CE0, CE1, and CE2 that disable the device
2. When reading the flash array a faster tGLQV (R16) applies. For non-array reads, R4 applies (i.e., Status Register reads,query reads, or device identifier reads).

8-Word Asynchronous Page Mode Read



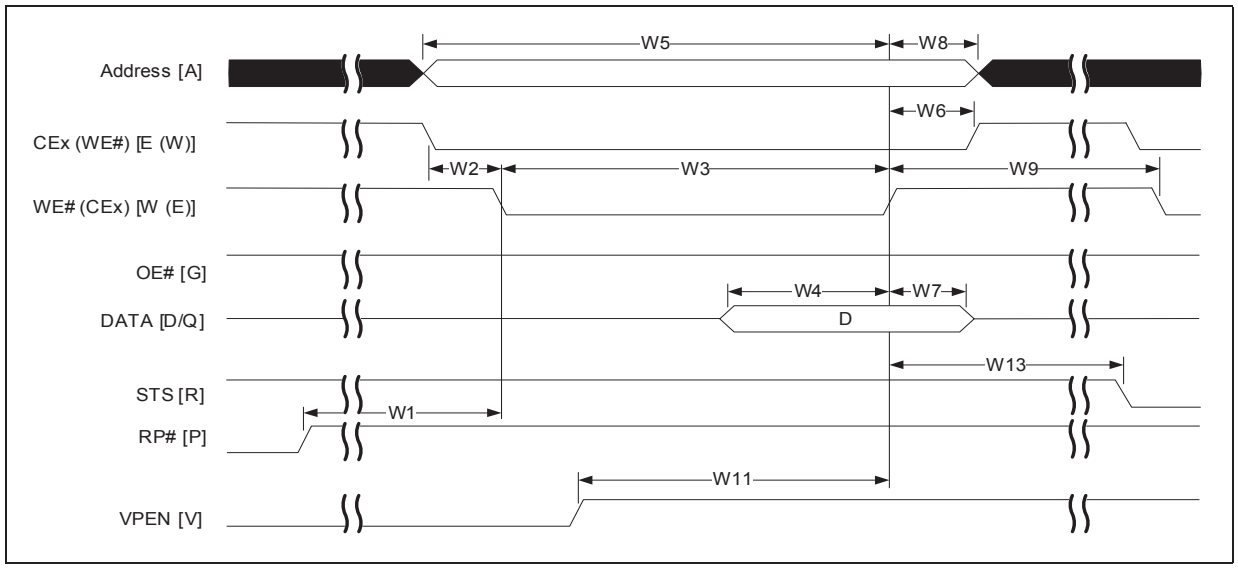
Notes
1. CEX low is defined as the combination of pins CE0, CE1, and CE2 that enable the device. CEX high is defined as the combination of pins CE0, CE1, and CE2 that disable the device
2. In this diagram, BYTE# is asserted high.

Write Operations

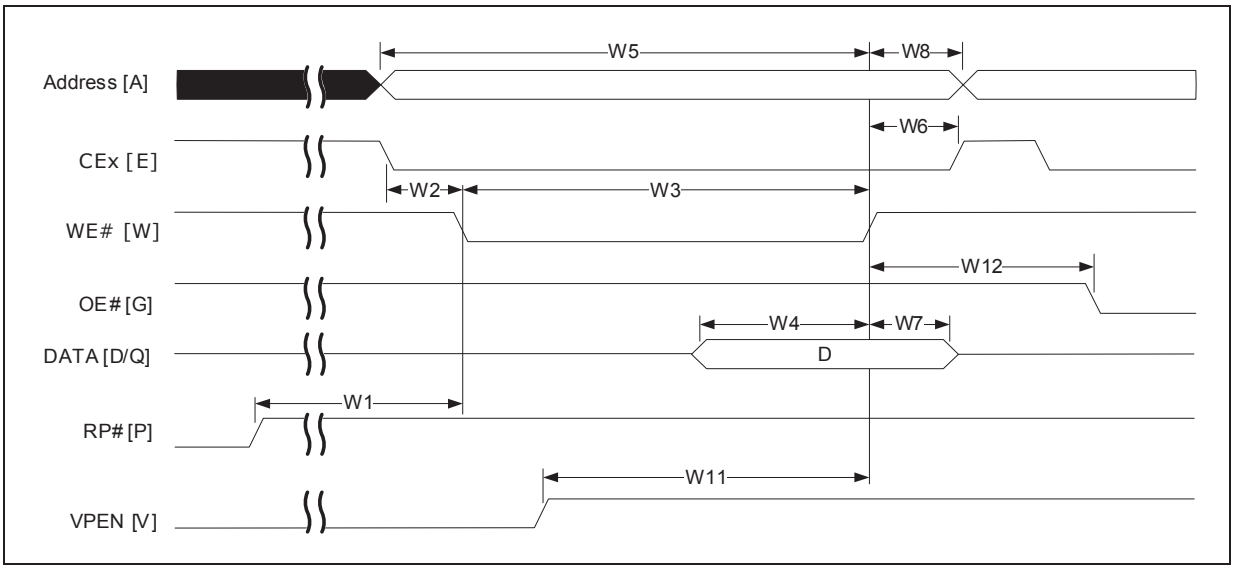
#	Symbol	Parameter	Valid for all speeds		Unit	Notes
			Min	Max		
W1	t_{PHWL} (t_{PHEL})	RP# High Recovery to WE# (CEX) Going Low	210	-	ns	
W2	t_{ELWL} (t_{WLEL})	CEx (WE#) Low to WE# (CEx) Going Low	0			1,2,3,5
W3	t_{WP}	Write Pulse Width	60			1,2,3,5
W4	t_{DVWH} (t_{DVEH})	Data Setup to WE# (CEx) Going High	50			1,2,3,6
W5	t_{AVWH} (t_{AVEH})	Address Setup to WE# (CEx) Going High	55			1,2,3,6
W6	t_{WHEH} (t_{EHWH})	CEx (WE#) Hold from WE# (CEx) High	0			1,2,3
W7	t_{WHDX} (t_{EHDX})	Data Hold from WE# (CEx) High	0			1,2,3
W8	t_{WHAX} (t_{EHAX})	Address Hold from WE# (CEx) High	0			1,2,3
W9	t_{WPH}	Write Pulse Width High	30			1,2,3,7
W11	t_{VPWH} (t_{VPEH})	V_{PEN} Setup to WE# (CEx) Going High	0			1,2,3,4
W12	t_{WHGL} (t_{EHGL})	Write Recovery before Read	35			1,2,3,8
W13	t_{WHRL} (t_{EHRL})	WE# (CEx) High to STS Going Low	-	500		1,2,3,9
W15	t_{QVVL}	V_{PEN} Hold from Valid SRD, STS Going High	0			1,2,3,4,9,10

Notes
1. CEX low is defined as the combination of pins CE0, CE1, and CE2 that enable the device. CEX high is defined as the combination of pins CE0, CE1, and CE2 that disable the device
2. Read timing characteristics during block erase, program, and lock-bit configuration operations are the same as during read-only operations. Refer to AC Characteristics–Read-Only Operations.
3. A write operation can be initiated and terminated with either CEX or WE#.
4. Sampled, not 100% tested.
5. Write pulse width (tWP) is defined from CEX or WE# going low (whichever goes low last) to CEX or WE# going high (whichever goes high first). Hence, tWP = tWLWH = tELEH = tWLEH = tELWH.
6. Refer to Table 18, “Enhanced Configuration Register” on page 32 for valid AIN and DIN for block erase, program, or lock-bit configuration.
7. Write pulse width high (tWPH) is defined from CEX or WE# going high (whichever goes high first) to CEX or WE# going low (whichever goes low first). Hence, tWPH = tWHWL = tEHEL = tWHEL = tEHWL.
8. For array access, tAVQV is required in addition to tWHGL for any accesses after a write.
9. STS timings are based on STS configured in its RY/BY# default mode.
10. VPEN should be held at VPENH until determination of block erase, program, or lock-bit configuration success (SR[5:3,1] = 0).

Asynchronous Write Waveform



Asynchronous Write to Read Waveform

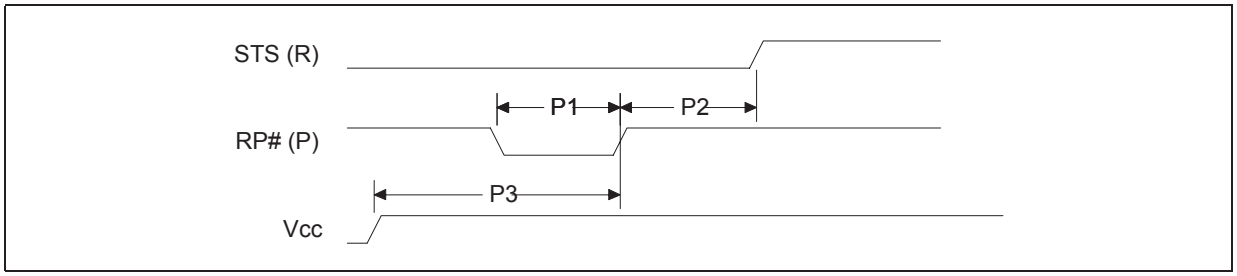


Configuration Performance

#	Symbol	Parameter		Typ	Max	Unit	Notes
W200	$t_{PROG/W}$	Program Time	Single word	40	175	µs	1,2,3,4,6
W250	t_{PROG}	Buffer Program Time	Aligned 16 Words BP Time (32Byte)	128	654	µs	1,2,3,4,5,6
			Aligned 256 Words BP Time (512Byte)	720	3600	µs	1,2,3,4,5,6
W501	$t_{ERS/AB}$	Block Erase Time		1.0	4.0	sec	1,2,3,4,6
W650	t_{lks}	Set Lock-Bit Time		50	60	µs	1,2,3,4,6
W651	t_{lkc}	Clear Block Lock-Bits Time		0.5	1	sec	1,2,3,4,6
W600	$t_{SUSP/P}$	Program Suspend Latency Time to Read		15	20	µs	1,2,3,6
W601	$t_{SUSP/E}$	Erase Suspend Latency Time to Read		15	20	µs	1,2,3,6
W602	$t_{ERS/SUSP}$	Erase to Suspend		500	-	µs	1,7
W652	t_{STS}	STS Pulse Width Low Time		500	-	ns	1
W702	$t_{BC/MB}$	blank check	Array Block	3.2	-	ms	-

Notes
1. Typical values measured at TA = +25 °C and nominal voltages. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.
2. These performance numbers are valid for all speed versions.
3. Sampled but not 100% tested.
4. Excludes system-level overhead.
5. These values are valid when the buffer is full, and the start address is aligned.
6. Max values are measured at worst case temperature, data pattern and VCC corner within 100K cycles. But for W650, W651, W600 and W601, the Max value are expressed at +25 °C or -40 °C.
7. W602 is the typical time between an initial block erase or erase resume command and then a subsequent erase suspend command. Violating the specification repeatedly during any particular block erase may cause erase failures.

AC Waveform for Reset Operation



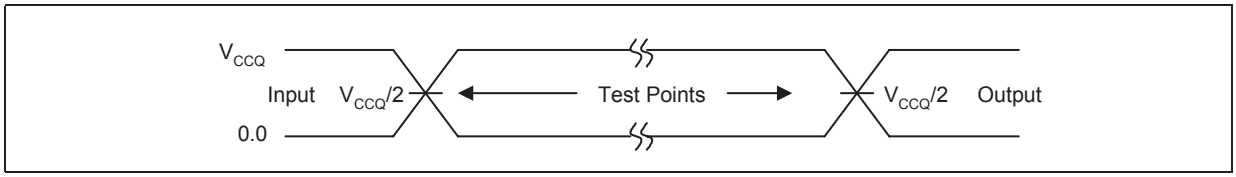
Note: STS is shown in its default mode (RY/BY#).

Reset Specifications

#	Symbol	Parameter		Min	Max	Unit	Notes
P1	t_{PLPH}	RP# Pulse Low Time (If RP# is tied to VCC, this specification is not applicable)	RP# is asserted during block erase, program or lock-bit configuration operation	25	-	µs	1
			RP# is asserted during read	100	-	ns	1
P2	t_{PHRH}	RP# High to Reset during Block Erase, Program, or Lock-Bit Configuration		-	100	ns	1,2
P3	t_{VCCPH}	Vcc Power Valid to RP# de-assertion (high)		60	-	µs	-

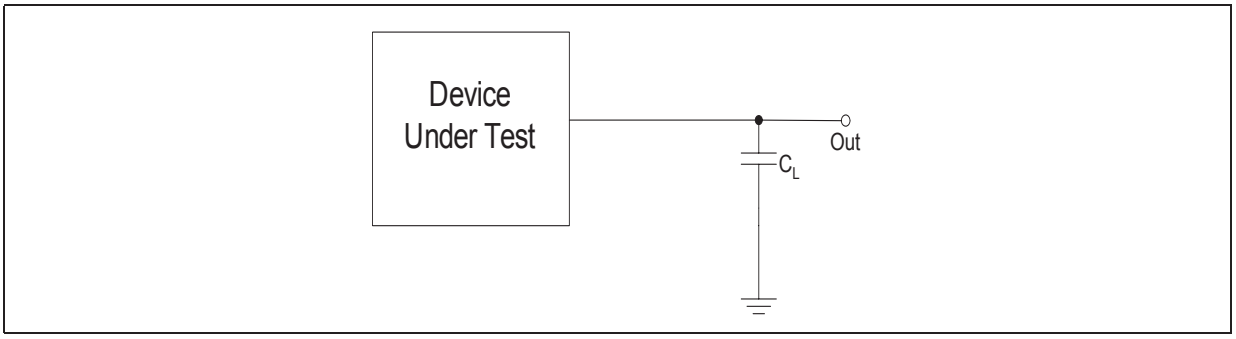
Notes
1. These specifications are valid for all product versions (packages and speeds).
2. A reset time, tPHQV, is required from the latter of STS (in RY/BY# mode) or RP# going high until outputs are valid.

AC Input/Output Reference Waveform



Notes
AC test inputs are driven at VCCQ for a Logic "1" and 0.0 V for a Logic "0." Input timing begins, and output timing ends, at VCCQ/2 V (50% of VCCQ). Input rise and fall times (10% to 90%) < 5 ns.

Transient Equivalent Testing Load Circuit



Note: C_L Includes Jig Capacitance

Test Configuration

Test Configuration	C_L (pF)
$V_{CCQ} = V_{CCQMIN}$	30

Memory Command Set Operations

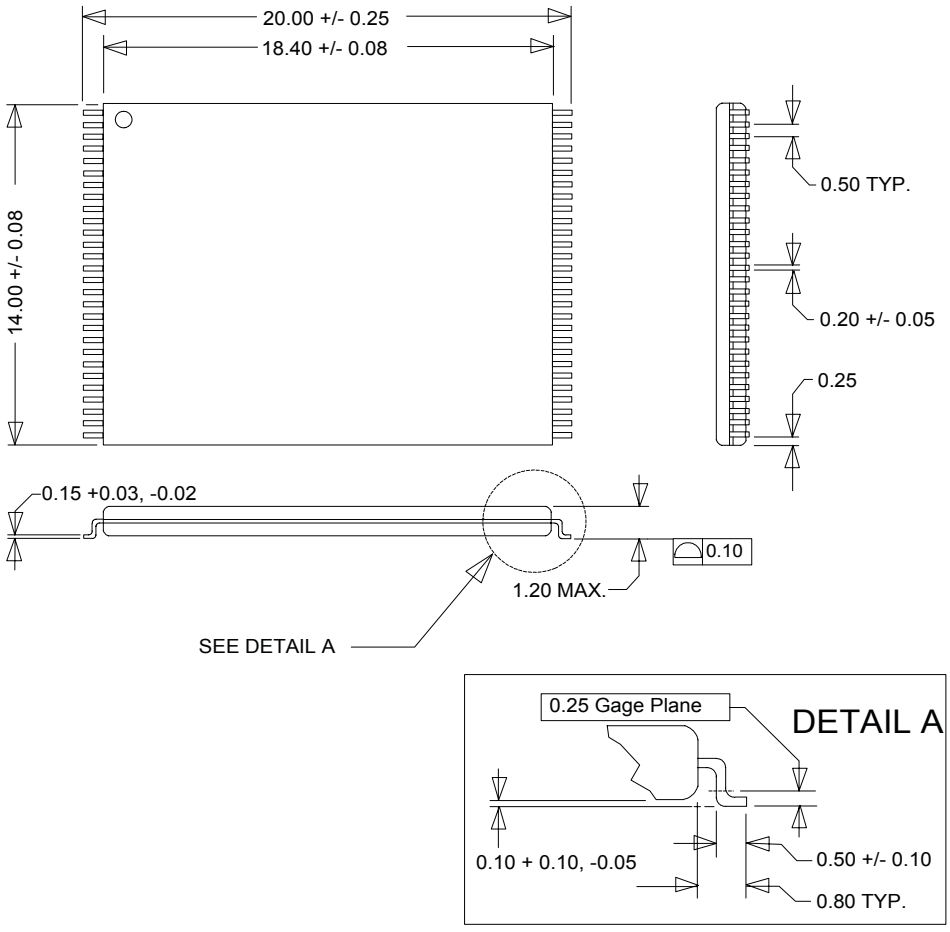
Command	Scalable or Basic Command Set [SCS or BCS]	Bus Cycles	First Bus Cycle			Second Bus Cycle			Notes
			Operation	Address	Data	Operation	Address	Data	
READ ARRAY	SCS/BCS	1	WRITE	X	FFh				
READ IDENTIFIER CODES	SCS/BCS	>/=2	WRITE	X	90h	READ	IA	ID	1
READ QUERY	SCS		WRITE	X	98h	READ	QA	QD	
READ STATUS REGISTER	SCS/BCS	2	WRITE	X	70h	READ	X	SRD	2
CLEAR STATUS REGISTER	SCS/BCS	1	WRITE	X	50h				
WRITE TO BUFFER	SCS/BCS	>2	WRITE	BA	E8h	WRITE	BA	N	3,4,5
WORD/BYTE PROGRAM	SCS/BCS	2	WRITE	X	40h or 10h	WRITE	PA	PD	6,7
BLOCK ERASE	SCS/BCS	2	WRITE	BA	20h	WRITE	BA	D0h	5,6
BLOCK ERASE/PROGRAM SUSPEND	SCS/BCS	1	WRITE	X	B0h				7,8
BLOCK ERASE/PROGRAM RESUME	SCS/BCS	1	WRITE	X	D0h				7
CONFIGURATION	SCS	2	WRITE	X	B8h	WRITE	X	CC	
SET BLOCK LOCK BITS	SCS	2	WRITE	X	60h	WRITE	BA	01h	
CLEAR BLOCK LOCK BITS	SCS	2	WRITE	X	60h	WRITE	X	D0h	
PROTECTION PROGRAM		2	WRITE	X	C0h	WRITE	PA	PD	

Key:
[IA] Identifier Code address
[ID] Data read from identifier Code
[BA] Address within a Block
[QA] Query data base Address
[PA] Address of Memory location to be programmed
[QD] Data read from Query data base
[SRD] Data read from Status Register

Notes
[1] Following the READ IDENTIFIER CODES command, READ operations access manufacturer, device, and block lock codes.
[2] If the ISM is running, only DQ7 is valid; DQ15-DQ8 and DQ6-DQ0 are placed in High-Z
[3] After the WRITE-to-BUFFER command is issued, check the XSR to make sure a buffer is available for WRITING
[4] The number of Bytes/words to be written to the write buffer = n+1, where n=byte/word count argument. Count ranges on this device for byte mode are n=00H to n=1Fh and for word mode, n=0000h to 000Fh. The third and consecutive bus cycles, as determined by n, are for writing data into the write buffer. The CONFIRM command (D0h) is expected after exactly n+1 WRITE cycles; any other command at that point in the sequence aborts the WRITE-to-BUFFER operation.
[5] The WRITE-to-BUFFER or ERASE operation does not begin until a CONFIRM command (D0h) is issued
[6] Attempts to issue a BLOCK ERASE or PROGRAM to a locked block will fail
[7] Either 40h or 10h is recognized by the ISM as the byte/word program setup
[8] PROGRAM SUSPEND can be issued after either the WRITE-to-BUFFER or WORD/BYTE PROGRAM operation is initiated. The CLEAR BLOCK LOCK BITS operation simultaneously clears all block lock bits.

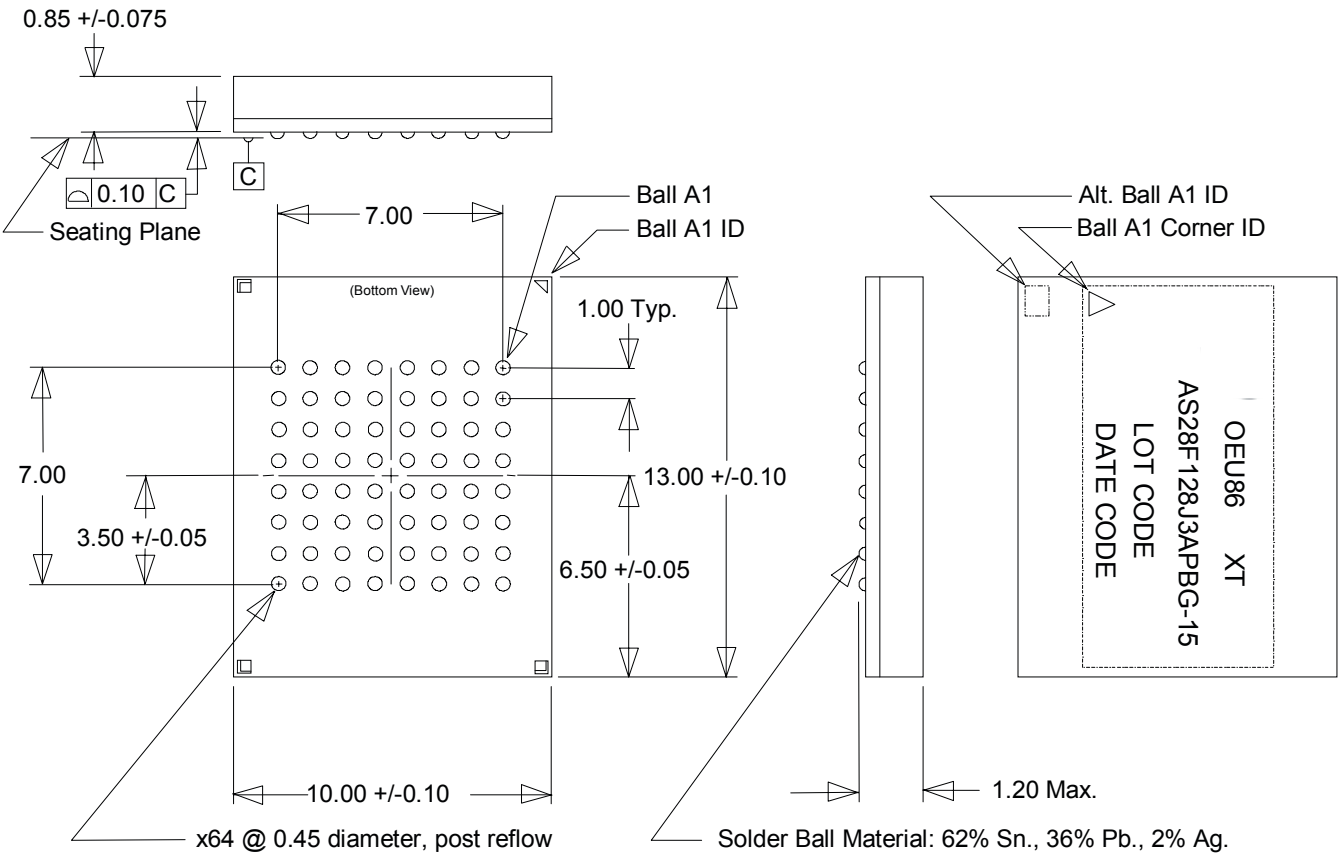
Mechanical Diagram

TSOP, Type 1, 56 Pin
(Dimensions in mm)



Mechanical Diagram

PBGA, 10mm x 13mm, 64 Ball w/ 1.00 Pitch
(Dimensions in mm)



Ordering Information

Part Number	Configuration	Speed (ns)	Pkg.	Comments
Enhanced Operating Range (-40°C to +105°C)				
AS28F128J3ARG-15/ET	128Mb, x8/x16 Q-Flash	115	TSOP1-56	
AS28F128J3APBG-15/ET	128Mb, x8/x16 Q-Flash	115	FBGA-64	Consult Factory, MOQ's Apply
Extended Operating Range (-55°C to +125°C)				
AS28F128J3ARG-15/XT	128Mb, x8/x16 Q-Flash	115	TSOP1-56	
AS28F128J3APBG-15/XT	128Mb, x8/x16 Q-Flash	115	FBGA-64	Consult Factory, MOQ's Apply

DOCUMENT TITLE

Plastic Encapsulated Microcircuit

128Mb, x8 and x16 Q-FLASH Memory

Even Sectored, Single Bit per Cell Architecture

REVISION HISTORY

Rev #	History	Release Date	Status
5.5	Updated with Numonyx Info	March 2009	Release
5.6	Added Micross Information	March 2010	Release
5.7	Updated DC Electrical Characteristics table, added DC Voltage Characteristics table, Added read operations table, added single word asych read waveform, added 8-word asych page mode read diagram, added write operations table, added asynch write waveform diagram, added asynch write to read waveform diagram, added config performance table, added ac waveform for reset operation diagram, added reset specifications table, added ac test conditions, changed reference to Numonyx J3-65nm device datasheet dated March 2010, page 1	May 2011	Release
5.8	Updated DC Electrical Characteristics	August 2013	Release