AS3500 AS3501 AS3502

DataSheet, Confidential

Low Power Ambient Noise-Cancelling Speaker Driver

1 General Description

The AS3500/01/02 are speaker driver with Ambient Noise Cancelling function for handsets, headphones or ear pieces. It is intended to improve quality of e.g. music listening, a phone conversation etc. by reducing background ambient noise.

The fully analog implementation allows the lowest power consumption, lowest system BOM cost and most natural received voice enhancement otherwise difficult to achieve with DSP implementations. The device is designed to be easily applied to existing architectures.

An internal OTP-ROM can be optionally used to store the microphones gain calibration settings.

The AS3500/01/02 can be used in different configurations for best trade-off of noise cancellation, required filtering functions and mechanical designs.

The simpler feed-forward topology is used to effectively reduce low frequency background noise. The feed-back topology with either 1 or 2 filtering stages can be used to reduce noise for a larger frequency range, and to even implement transfer functions like speaker equalization, Baxandall equalization, high/low shelving filter and to set a predefined loop bandwidth.

The filter loop is optimized by the user for specific handset electrical and mechanical designs by dimensioning simple R, C components.

Most handset implementations will make use of a single noise detecting microphone. Two microphones could be used to allow for increased flexibility of their location in the handset mechanical design. Using the bridged mode allows to even drive high impedance headsets.

2 Key Features

Microphone Input

- 128 gain steps @0.375dB and MUTE with AGC
- differential, low noise microphone amplifier
- single ended or differential mode
- supply for electret microphone
- MIC gain OTP programmable

High Efficiency Headphone Amplifier

- 2x34mW, 0.1% THD @ 16Ω, 1.5V supply, 100dB SNR
- bridged mode for e.g. 300Ω loads
- click and pop less start-up and mode switching

Line Input

- volume control via serial interface or volume pin
- 64 steps @ 0.75dB and MUTE, pop-free gain setting
- single ended stereo or mono differential mode

ANC processing

- feed-forward cancellation
- feed-back cancellation with filter loop transfer function definable via simple RC components
- simple in production SW calibration
- 12-30dB noise reduction (headset dependent)
- 10-2000Hz wide frequency active noise attenuation (headset dependent)

Monitor Function

- for assisted hearing, i.e. to monitor announcements
- fixed (OTP prog.) ambient sound amplification to compensate headphone passive attenuation
- volume controlled ambient sound amplification mixed with fixed (OTP prog.) attenuation of LineIn

Incremental Functions

- ANC with or without music on the receiving path
- improved dynamic range playback
- simple and low cost single noise detection microphone implementation
- OTP ROM for automatic trimming during production

Performance Parameter

- 5/3.8mA @ 1.5V stereo/mono ANC; <1uA quiescent
- extended PSRR for 217Hz

Interfaces

- 2 wire serial control mode & volume inputs
- calibration via Line-In or 2-wire serial interface
- single cell or fixed 1.0-1.8V supply with internal CP

Package

- AS3500, AS3501 QFN24 [4x4] 0.5mm pitch
- AS3502 QFN32 [5.x5] 0.5mm pitch

3 Applications

Ear pieces, Headsets, Hands-Free Kits, Mobile Phones, Voice Communicating Devices

Figure 1. AS3501 Feed Forward ANC Block Diagram

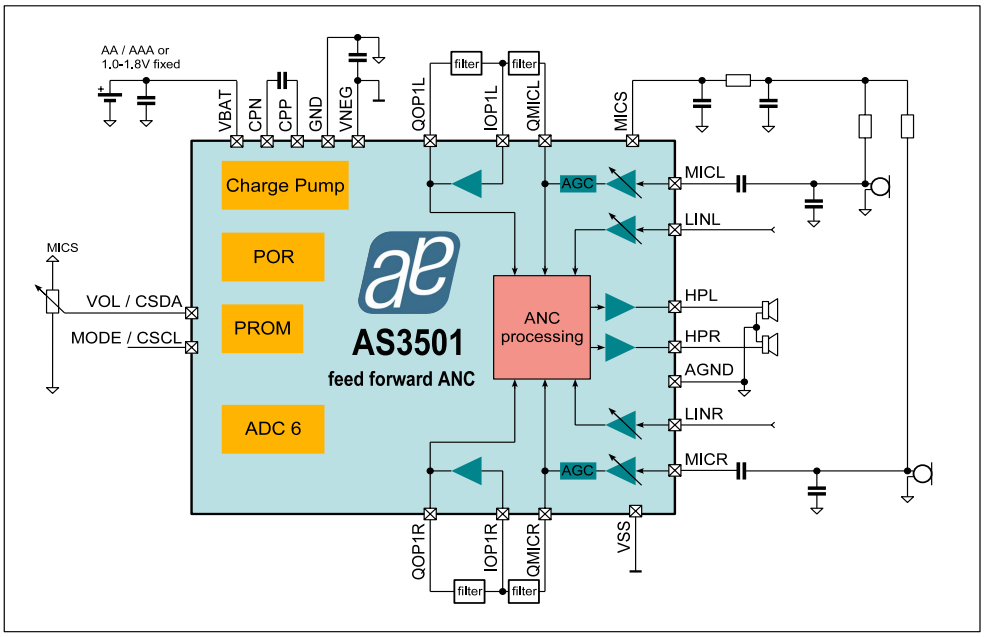
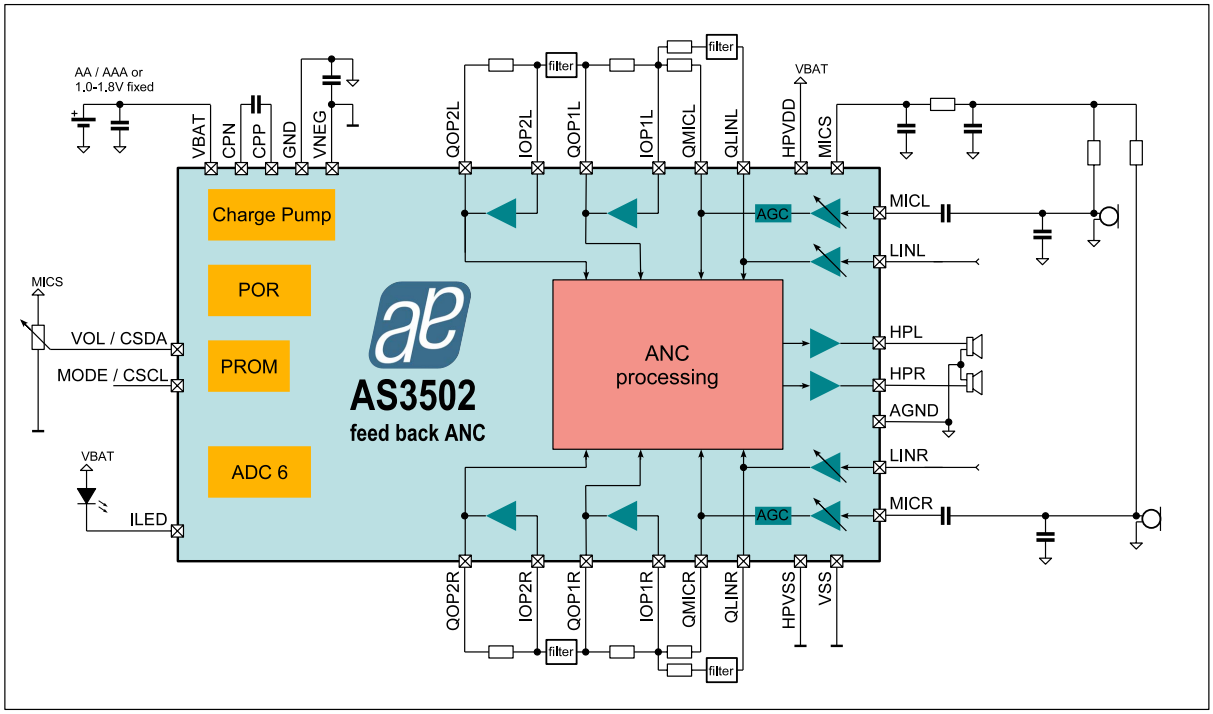


Figure 2. AS3502 Feed-Back Block Diagram



Contents

Revision History

Table 1. Revision History

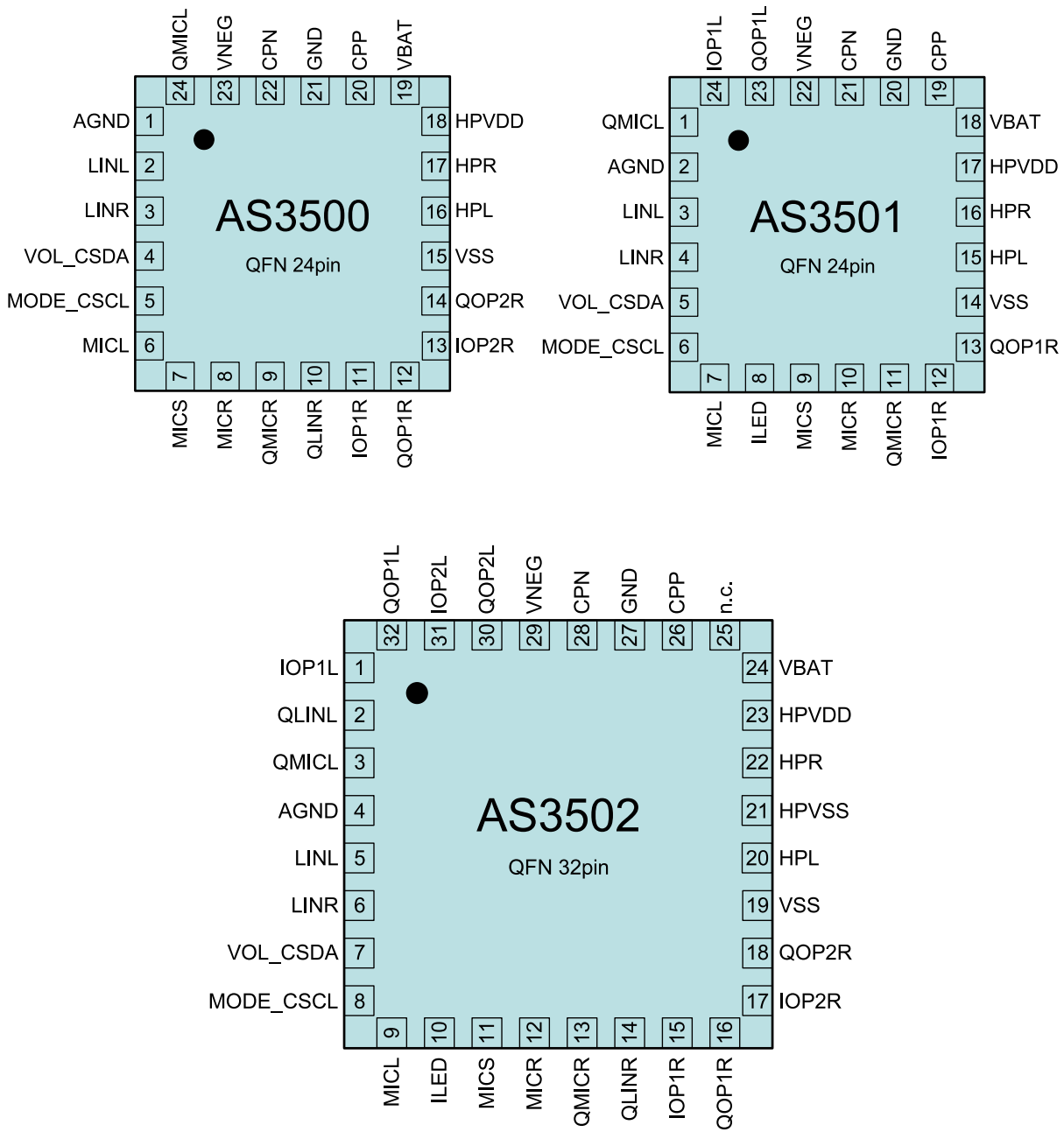
Revision	Date	Owner	Description
1.0	18.5.2009	pkm	official release

4 Pinout

4.1 Pin Assignment

Please observe that pin assignment may change in preliminary data sheets.

Figure 3. Pin Assignments (Top View)



4.2 Pin Description

Please observe that pin description may change in preliminary data sheets.

Table 2. Pin Description for AS3500 AS3501 AS3502

AS3500	AS3501	AS3502	Pin Name	Type	Description
-	24	1	IOP1L	ANA IN	Filter OpAmp1 Input Left Channel
-	-	2	QLINL	ANA OUT	Line In GainStage Output Left Channel
24	1	3	QMICL	ANA OUT	MIC GainStage Output Right Channel
1	2	4	AGND	ANA IN	Analog Reference
2	3	5	LINL	ANA IN DIG IN	Line In Left Channel During Appl Trim Mode Write – CSDA During Appl Trim Mode Burn - VNEG
3	4	6	LINR	ANA IN DIG IO	LineIn Right Channel During Appl Trim Mode Write – CSCL During Appl Trim Mode Burn - Clock
4	5	7	VOL_CSDA	MIXED IO	Serial Interface Data ADC Input for volume regulation
5	6	8	MODE_CSCL	DIG IN	Mode Pin (PowerUp/Dn, Monitor) Serial Interface Clock
6	7	9	MICL	ANA IN	Microphone In Left Channel
-	8	10	ILED	ANA OUT	Current Output for on-indication LED
7	9	11	MICS	ANA OUT	Microphone Supply
8	10	12	MICR	ANA IN	Microphone Input Right Channel
9	11	13	QMICR	ANA OUT	MIC GainStage Output Right Channel
10	-	14	QLINR	ANA OUT	Line In GainStage Output Right Channel
11	12	15	IOP1R	ANA IN	FilterOpAmp1 Input Right Channel
12	13	16	QOP1R	ANA IN	Filter OpAmp1 Output Right Channel
13	-	17	IOP2R	ANA IN	Filter OpAmp2 Input Right Channel
14	-	18	QOP2R	ANA OUT	Filter OpAmp2 Output Right Channel
15	14	19	VSS	SUP IN	Core and Periphery Circuit VSS Supply
16	15	20	HPL	ANA OUT	Headphone Output Left Channel
-	-	21	HPVSS	SUP IN	Headphone VSS Supply
17	16	22	HPR	ANA OUT	Headphone Output Right Channel
18	17	23	HPVDD	SUP IN	Headphone VDD Supply
19	18	24	VBAT	SUP IN	VNEG ChargePump Positive Supply
-	-	25	n.c.	-	
20	19	26	CPP	ANA OUT	VNEG ChargePump Flying Capacitor Positive Terminal
21	20	27	GND	GND	VNEG ChargePump Negative Supply
22	21	28	CPN	ANA OUT	VNEG ChargePump Flying Capacitor Negative Terminal
23	22	29	VNEG	SUP IO	VNEG ChargePump Output
-	-	30	QOP2L	ANA OUT	Filter OpAmp2 Output Left Channel
-	-	31	IOP2L	ANA IN	Filter OpAmp2 Input Left Channel
-	23	32	QOP1L	ANA OUT	Filter OpAmp1 Output Right Channel

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 3 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 8 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The device should be operated under recommended operating conditions.

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
Reference Ground				Defined as in GND
Supply terminals	-0.5	2.0	V	Applicable for pin VBAT, HPVDD
Ground terminals	-0.5	0.5	V	Applicable for pins AGND
Negative terminals	-2.0	0.5	V	Applicable for pins VNEG, VSS, HPVSS
Voltage difference at VSS terminals	-0.5	0.5	V	Applicable for pins VSS, HPVSS
Pins with protection to VBAT	VNEG -0.5	5.0 VBAT+0.5	V	Applicable for pins CPP, CPN
Pins with protection to HPVDD	VSS -0.5	5.0 HPVDD+0.5	V	Applicable for pins LINL/R, MICL/R, ILED, HPR, HPL, QMICL/R, QLINL/R, IOPx, QOPx
other pins	VSS -0.5	5		applicable for pins MICS, VOL_CSDA, MODE_CSCL
Input Current (latch-up immunity)	-100	100	mA	Norm: JEDEC 17
Continuous Power Dissipation (T_A = +70ºC)				
Continuous Power Dissipation	-	200	mW	P_T[1] for QFN16/24/32 package
Electrostatic Discharge				
Electrostatic Discharge HBM		+/-2	kV	Norm: JEDEC JESD22-A114C
Temperature Ranges and Storage Conditions				
Operating Temperature Range	-20	+85	ºC	
Junction Temperature		+110	ºC	
Storage Temperature Range	-55	+125	ºC	
Humidity non-condensing	5	85	%	
Bump Temperature (soldering)				
Package Body Temperature		260	°C	Norm IPC/JEDEC J-STD-020C, reflects moisture sensitivity level only
Solder Profile	235	245	°C	peak temperature
	30	45	s	well time above 217 °C
Moisture Sensitive Level	3		1	Represents a max. floor live time of 168h

1. Depending on actual PCB layout and PCB used

6 Electrical Characteristics

VBAT = 1.0V to 1.8V, T_A = -20ºC to +85ºC. Typical values are at VBAT = 1.5V, T_A = +25ºC, unless otherwise specified.

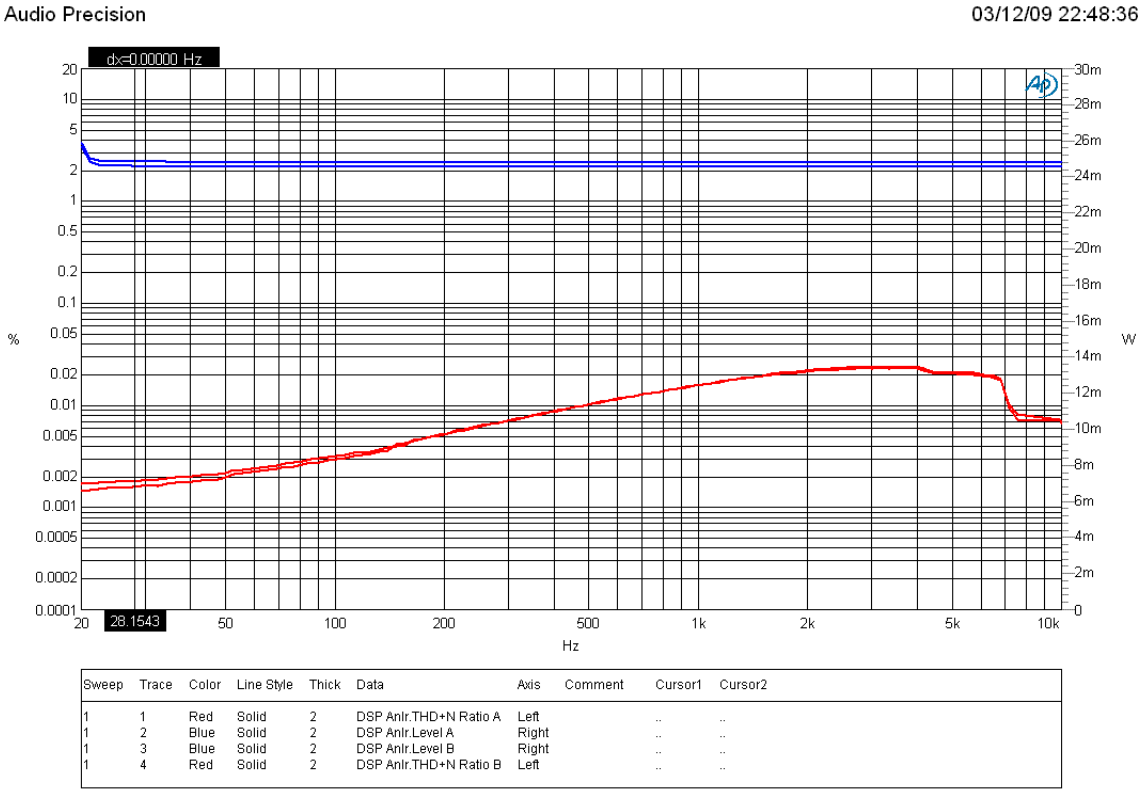
Table 4. Electrical Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
Supply Voltages					
GND	Reference Ground		0	0	V
VBAT, HPVDD	Battery Supply Voltage		1.0	1.8	V
VNEG	ChargePump Voltage		-1.8	-0.7	V
VSS	Analog neg. Supply Voltages HPVSS, VSS, VNEG		-1.8	-0.7	V
V_{DELTA-}	Difference of Ground Supplies GND, AGND	To achieve good performance, the negative supply terminals should be connected to low impedance ground plane.	-0.1	0.1	V
$V_{DELTA--}$	Difference of Negative Supplies VSS, VNEG, HPVSS	Charge pump output or external supply	-0.1	0.1	V
V_{DELTA+}	Difference of Positive Supplies	VBAT-HPVDD	-0.25	0.25	V
other pins					
V_{MICS}	Microphone Supply Voltage	MICS	0	3.6	V
V_{HPVDD}	pins with diode to HPVDD	MICL/R, ILED, HPR, HPL, QMICL/R, QLINL/R, IOPx, QOPx	VSS	3.6	V
V_{VBAT}	pins with diode to VBAT	CPP, CPN	VNEG	VBAT	V
$V_{CONTROL}$	Control Pins	MODE_CSCL, VOL_CSDA	VSS	3.7	V
V_{TRIM}	Line Input & Application Trim Pins	LINL, LINR	VNEG -0.5 or -1.8	HPVDD +0.5 or 1.8	V

7 Typical Operating Characteristics

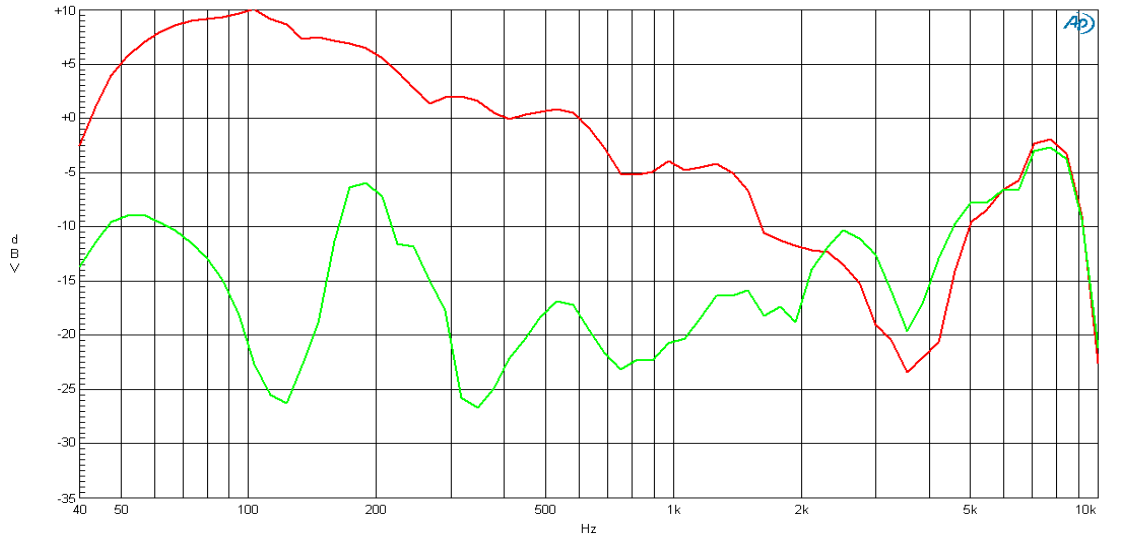
VBAT = +1.5V, T_A = +25ºC, unless otherwise specified.

Figure 4. THD vs. frequency @ 1.5V, 16Ω, 25mW



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1	Cursor2
1	1	Red	Solid	2	DSP Anlr.THD+N Ratio A	Left		..	..
1	2	Blue	Solid	2	DSP Anlr.Level A	Right		..	..
1	3	Blue	Solid	2	DSP Anlr.Level B	Right		..	..
1	4	Red	Solid	2	DSP Anlr.THD+N Ratio B	Left		..	..

Figure 5. Typical Performance Data, FF configuration



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
5	1	Red	Solid	2	DSP Anlr.Bandpass BlSmooth	Left	AMS PassiveL
7	1	Green	Solid	2	DSP Anlr.Bandpass BlSmooth	Left	AMS Active 1001 L

8 Detailed Description

8.1 Audio Line Input

8.1.1 General

The chip features one line input. The blocks can work in mono differential or in stereo single ended mode.

In addition to the 12.5-25kΩ input impedance, LineIn has a termination resistor of 10kΩ which is also effective during MUTE to charge eventually given input capacitors.

8.1.2 Gain Stage

The Line In gain stage is designed to have 63 gain steps of 0.75dB with a max gain of 0dB plus MUTE.

In default, the gain will be ramped up from MUTE to 0dB during startup. There is a possibility to make the playback volume user controlled by the VOL pin with an ADC converted VOL voltage or UP/DN buttons.

In monitor mode the gain stage can be set to an fixed default attenuation level for reducing the loudness of the music.

8.1.3 Parameter

VBAT=1.5V, T_A= 25°C, unless otherwise mentioned

Table 5. Line Input Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{LIN}	Input Signal Level			0.6* VBAT	VBAT	V_{PEAK}
R_{LIN}	Input Impedance	0dB gain (12.5k // 10k)		5.6		kΩ
		-46.5dB gain (25k // 10k)		7.2		kΩ
		MUTE		10		kΩ
Δ_{RLIN}	Input Impedance Tolerance			±30		%
C_{LIN}	Input Capacitance			5		pF
A_{LIN}	Programmable Gain		-46.5		+0	dB
	Gain Steps	discrete logarithmic gain steps		0.75		dB
	Gain Step Accuracy			0.5		dB
$A_{LINMUTE}$	Mute Attenuation			100		dB
Δ_{ALIN}	Gain Ramp Rate	PotiMode, Tinit=100ms		20		ms/ step
		ButtonMode, Tinit=400ms		80		
		MonitorMode		8		
V_{ATTACK}	Limiter Activation Level	HPL/R start of neg. clipping				V_{PEAK}
V_{DECAY}	Limiter Release Level	HPL/R		VNEG +0.3		V_{PEAK}
t_{ATTACK}	Limiter Attack Time			4		µs
t_{DECAY}	Limiter Decay Time			8		ms

8.2 Microphone Input

8.2.1 General

The AFE offers two microphone inputs and one low noise microphone voltage supply (microphone bias). The inputs can be switched to single ended or differential mode.

8.2.2 Gain Stage & Limiter

The Mic GainStage has programmable Gain within -6dB…+41.625dB in 128 steps of 0.375dB.

As soft-start function is implemented for an automatic gain ramping implemented with steps of 4ms to fade in the audio at the end of the start-up sequence.

A limiter automatically attenuates high input signals. The AGC has 127 steps with 0.375dB with a dynamic range of the full gain stage.

In monitor mode the gain stage can be set to an fixed (normally higher) gain level or be controlled by the VOL pin.

8.2.3 Supply

The MICS charge pump is providing a proper microphone supply voltage for the AAA supply. Since AAA batteries are operating down to 1.0V, the direct battery voltage cannot be used for mic-supply. There are 2 modes.

The first mode SWITCH-MODE for 1.8V supply is to have just a switch from VBAT to MICS. With this switch, the microphone current is switched off in idle mode.

The second mode CHAREGPUMP_MODE for AAA batteries is the real charge pump mode, in this mode a positive voltage is generated of about 2* VBAT.

It is also possible to switch off the microphone supply if not needed (e.g. playback without ANC)

8.2.4 Parameter

VBAT=1.5V, T_A= 25°C unless otherwise mentioned

Table 6. Microphone Input Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{MICIN}0$	Input Signal Level	A_{MIC} = 30dB		20		mV_P
$V_{MICIN}1$		A_{MIC} = 36dB		10		mV_P
$V_{MICIN}2$		A_{MIC} = 42dB		5		mV_P
R_{MICIN}	Input Impedance	MICP to AGND		7.5		kΩ
Δ_{MICIN}	Input Impedance Tolerance			-7 +33		%
C_{MICIN}	Input Capacitance			5		pF
A_{MIC}	Programmable Gain		-6		+41.6	dB
	Gain Steps	discrete logarithmic gain steps		0.375		dB
	Gain Step Precision			0.15		dB
Δ_{AMIC}	Gain Ramp Rate	Tinit=64ms		4		ms/ step
V_{ATTACK}	Limiter Activation Level	V_{PEAK} related to VBAT or VNEG		0.67		1
V_{DECAY}	Limiter Release Level			0.4		1
$A_{MICLIMIT}$	Limiter Gain Overdrive	127 @ 0.375dB		41.625		dB
t_{ATTACK}	Limiter Attack Time			5		µs/ step
$t_{DECAY-DEB}$	Limiter Decay Debouncing Time			64		ms
t_{DECAY}	Limiter Decay Time			4		ms/ step

Table 6. Microphone Input Parameter (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{MICS}	Microphone Supply Voltage			VBAT*2-240mV		V
$I_{MICSMIN}$	Min. Microphone Supply Current	VBAT=+1.0V VNEG=-0.7V MICS=+1.75V		650		uA
R_{OUT_CP}	CP Output Resistance			1300		Ω

8.3 Headphone Output

8.3.1 General

The headphone output is a true ground output using VNEG as negative supply, designed to provide the audio signal with 2x12mW @ 16Ω–64Ω, which are typical values for headphones. It is also capable to operate in bridged mode for higher impedance (e.g. 300Ω) headphone. In this mode the left output is carrying the inverted signal of the right output.

8.3.2 Input Multiplexer

The signal from the line-input gain stage gets summed at the input of the headphone stage with the microphone gain stage output, the first filter opamp output or the second filter opamp output. The microphone gain stage output is used per default. It is also possible to playback without ANC by only using the line-input gain stage with no other signal on the multiplexer.

For the monitor mode the setting of this input multiplexer can be changed to an other source, normally to the microphone.

8.3.3 No-Pop Function

The No-Pop startup of the headphone stage takes 60ms to 120ms dependent on the supply voltage.

8.3.4 No-Clip Function

The headphone output stage gets monitored by comparator stages which detect if the output signal starts to clip.

This signal is used to reduce the LineIn gain to avoid distortion of the output signal. A hystereses avoids jumping between 2 gain steps for a signal with constant amplitude.

8.3.5 Over-current protection

The over-current protection has a threshold of 150-200mA and a debouncing time of 8us. The stage is forced to OFF mode in an over-current situation. After this the headphone stage tries to power up again every 8ms as long as the over-current situation still exists or the stage is turned off manually.

8.3.6 Parameter

VBAT=1.5V, T_A= 25°C, unless otherwise mentioned

Table 7. Headphone Output Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{L_HP}	Load Impedance	stereo mode	16			Ω
C_{L_HP}	Load Capacitance	stereo mode			100	pF
P_{HP}	Nominal Output Power	RL=16Ω-64Ω	12			mW
P_{SRRHP}	Power Supply Rejection Ratio	200Hz-20kHz, 720mVpp, RL=16Ω		90		dB

8.4 Operational Amplifier

8.4.1 General

While AS3501 offers only one operational amplifiers for feed-forward ANC, AS3500 and AS3502 feature an additional second operational amplifier stage to perform feed-back ANC or any other additional needed filtering.

Both operational amplifiers stages can be activated and used individually. While OP1 stage is always configured as inverting amplifier OP2 stage can be also switched to a non-inverting mode with an adjustable gain of 0..+10.5dB.

8.4.2 Parameter

VBAT=1.5V, T_A= 25°C, unless otherwise mentioned

Table 8. Headphone Output Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{L_OP}	Load Impedance	single ended	1			kΩ
C_{L_OP}	Load Capacitance	single ended			100	pF
GBW_{OP}	Gain Band Width			4.3		MHz
V_{OS_OP}	Offset Voltage				6	mV
V_{EIN_HP}	Equivalent Input Noise	200Hz-20kHz		2.6		uV

8.5 SYSTEM

8.5.1 General

The system block handles the power up and power down sequencing. As well as the mode switching.

8.5.2 Power Up/Down Conditions

The chip powers up when one of the following condition is true:

Table 9. Power UP Conditions

#	Source	Description
1	MODE pin	In stand-alone mode, MODE pin has to be driven high to turn on the device
2	I2C start	In I2C mode, a I2C start condition turns on the device

The chip automatically shuts off if one of the following conditions arises:

Table 10. Power DOWN Conditions

#	Source	Description
1	MODE pin	Power down by driving MODE pin to low
2	SERIF	Power down by SERIF writing 0h to register 20h bit <0>
3	Low Battery	Power down if VBAT is lower than the supervisor off-threshold
4	VNEG CP OVC	Power down if VNEG is higher than the VNEG off-threshold

8.5.3 Start-up Sequence

The start-up sequence depends on the used mode.

In stand-alone mode the sequence runs automatically, in I2C mode the sequence runs till a defined state and waits then for an I2C command. Either the automatic sequence is started by setting the CONT_PWRUP bit in addition to the PWR_HOLD bit. If only the PWR_HOLD is set all enable bits for headphone, microphone, etc have to be set manually.

8.5.4 Mode Switching

When the chip in stand-alone mode (no I2C control) the mode can be switched with different levels on the MODE pin.

Table 11. Operation Modes

MODE	MODE pin	Description
OFF	LOW	Chip is turned off
ANC	HIGH	Chip is turned on and active noise cancellation is active
MONITOR	TRI-STATE	Chip is turned on and monitor mode is active In Monitor mode a different (normally higher) microphone preamplifier gain can be chosen to get an amplification of the surrounding noise. This volume can be either fixed or be controlled by the VOL input. To get rid of the low pass filtering needed for the noise cancellation, the headphone input multiplexer can be set to a different (normally to MIC) source. In addition the LineIn gain can be lowered to reduce the loudness of the music currently played back.

In I2C mode the monitor mode can be activated be setting the corresponding bit in the system register.

8.5.5 Status Indication

AS3501and AS3502 features a on-status information via the current output pin ILED. The current can be controlled in 3 steps and be switched off, by setting the PWM accordingly (0%, 25%, 50% and 100% duty cycle of a 50kHz PWM signal).

If LOW_BAT is active, ILED switches to blinking with 1Hz, 50% duty cycle and 50% current setting.

8.6 VNEG Charge Pump

8.6.1 General

The VNEG charge pump uses one external 1uF capacitor to generate a negative supply voltage out of the battery input voltage to supply all audio related blocks. This allows a true-ground headphone output with no more need of external dc-decoupling capacitors.

8.6.2 Parameter

VBAT=1.5V, T_A= 25^{o}C, unless otherwise mentioned

Table 12. Headphone Output Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IN}	input voltage	VBAT	1.0	1.5	1.8	V
V_{OUT}	output voltage	VNEG	-0.7	-1.5	-1.8	V
C_{EXT}	external flying capacitor			1		uF

8.7 OTP Memory & Internal Registers

8.7.1 General

The OTP memory consists of OTP register and the OTP fuses.The OTP register can be written as often as wanted but will lose the content on power off. The OTP fuses are intended to store basic chip configurations as well as the micro-phone gain settings to optimize the ANC performance and get rid of sensitivity variations of different microphones. Burning the fuses can only be once and is a permanent change, which means the fuses keep the content even if the chip is powered down.

When the chip is controlled by a microcontroller via I2C, the OTP memory don’t has to be used.

8.8 2-Wire-Serial Control Interface

8.8.1 General

There is an I2C slave block implemented to have access to 64 byte of setting information.

The I2C address is: Adr_Group8 - audio processors

- 8Eh_write
- 8Fh_read

8.8.2 Protocol

Table 13. 2-Wire Serial Symbol Definition

Symbol	Definition	RW	Note
S	Start condition after stop	R	1 bit
Sr	Repeated start	R	1 bit
DW	Device address for write	R	1000 1100b (8Ch)
DR	Device address for read	R	1000 1101b 8Dh)
WA	Word address	R	8 bit
A	Acknowledge	W	1 bit
N	No Acknowledge	R	1 bit
reg_data	Register data/write	R	8 bit
data (n)	Register data/read	W	8 bit
P	Stop condition	R	1 bit
WA++	Increment word address internally	R	during acknowledge
	AS3500 AS3501 AS3502 (=slave) receives data		
	AS3500 AS3501 AS3502 (=slave) transmits data		

Figure 6. Byte Write

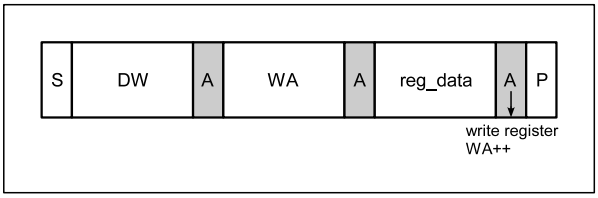
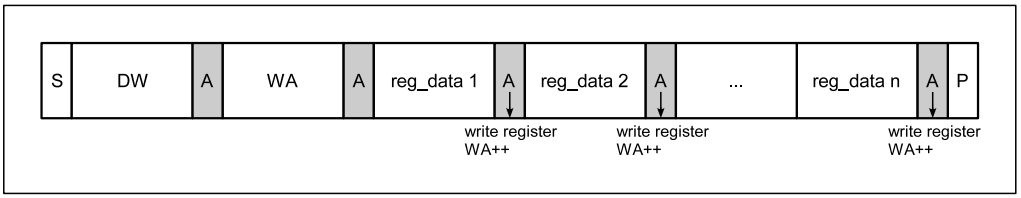


Figure 7. Page Write

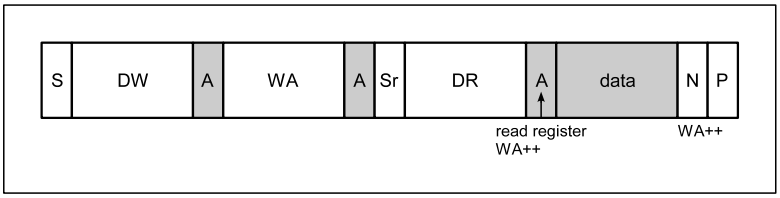


Byte Write and Page Write formats are used to write data to the slave.

The transmission begins with the START condition, which is generated by the master when the bus is in IDLE state (the bus is free). The device-write address is followed by the word address. After the word address any number of data bytes can be sent to the slave. The word address is incremented internally, in order to write subsequent data bytes on subsequent address locations.

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address, or simply with a new transmission START followed by the device-read address, when the bus is in IDLE state. The device-read address is always followed by the 1st register byte transmitted from the slave. In Read Mode any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

Figure 8. Random Read

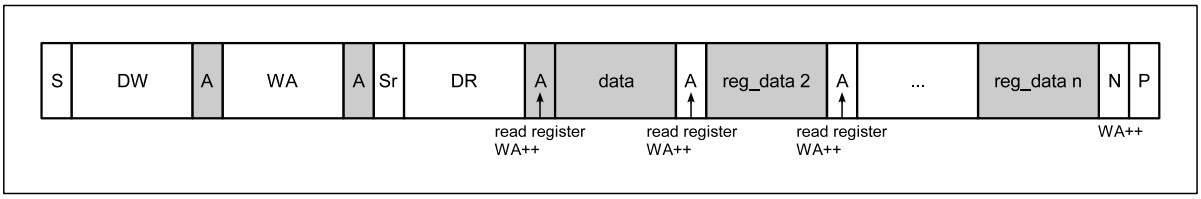


Random Read and Sequential Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

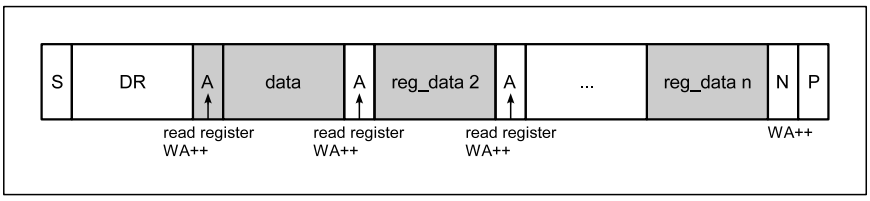
In order to change the data direction a repeated START condition is issued on the 1st SCL pulse after the acknowledge bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state the slave transmits register data located by the previous received word address vector. The master responds to the data byte with a not-acknowledge, and issues a STOP condition on the bus.

Figure 9. Sequential Read



Sequential Read is the extended form of Random Read, as more than one register-data bytes are transferred subsequently. In difference to the Random Read, for a sequential read the transferred register-data bytes are responded by an acknowledge from the master. The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-address counter). To terminate the transmission the master has to send a not-acknowledge following the last data byte and generate the STOP condition subsequently.

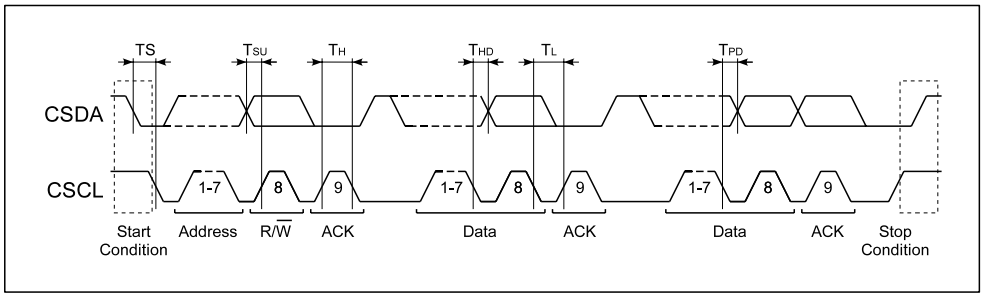
Figure 10. Current Address Read



To keep the access time as small as possible, this format allows a read access without the word address transfer in advance to the data transfer. The bus is idle and the master issues a START condition followed by the Device-Read address. Analogous to Random Read, a single byte transfer is terminated with a not-acknowledge after the 1st register byte. Analogous to Sequential Read an unlimited number of data bytes can be transferred, where the data bytes has to be responded with an acknowledge from the master. For termination of the transmission the master sends a not-acknowledge following the last data byte and a subsequent STOP condition.

8.8.3 Parameter

Figure 11. 2-Wire Serial Timing



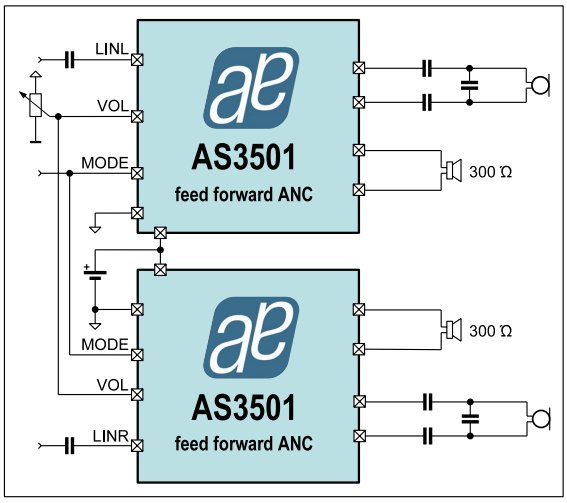
DVDD =2.9V, T_{amb}=25ºC; unless otherwise specified

Table 14. 2-Wire Serial Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CSL}	CSCL, CSDA Low Input Level	(max 30%DVDD)	0	-	0.87	V
V_{CSH}	CSCL, CSDA High Input Level	CSCL, CSDA (min 70%DVDD)	2.03	-	5.5	V
HYST	CSCL, CSDA Input Hysteresis		200	450	800	mV
V_{OL}	CSDA Low Output Level	at 3mA	-	-	0.4	V
Tsp	Spike insensitivity		50	100	-	ns
T_H	Clock high time	max. 400kHz clock speed	500			ns
T_L	Clock low time	max. 400kHz clock speed	500			ns
T_{SU}		CSDA has to change Tsetup before rising edge of CSCL	250	-	-	ns
T_{HD}		No hold time needed for CSDA relative to rising edge of CSCL	0	-	-	ns
TS		CSDA H hold time relative to CSDA edge for start/stop/rep_start	200	-	-	ns
T_{PD}		CSDA prop delay relative to lowgoing edge of CSCL		50		ns

9 Application Information

Figure 12. AS3501 High Performance Application in Bridged Mode for high impedance headsets



For high impedance headphones two AS3501 can be used in a bridged mode each one driving one side of the headphone load as differential output to get 24mW output power per channel. Also the microphone inputs can be used in differential mode to reduce the noise level.

Figure 13. AS3500 Feed-Forward ANC Block Diagram

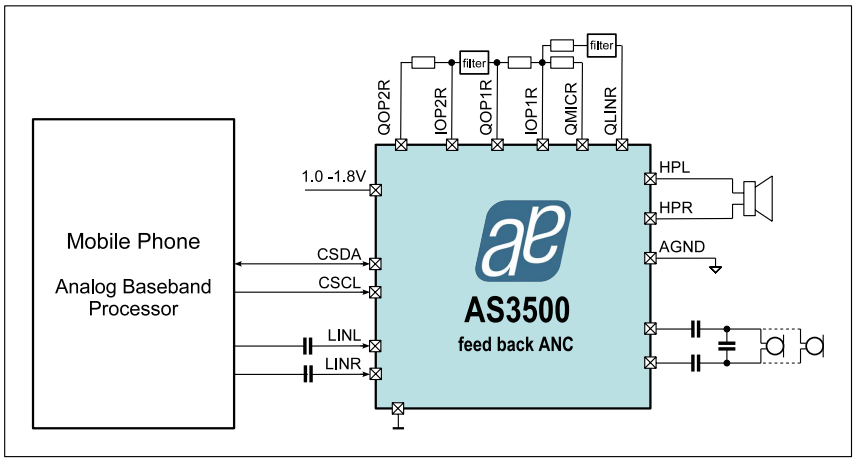


Figure 14. AS3502 on Music Player with ANC

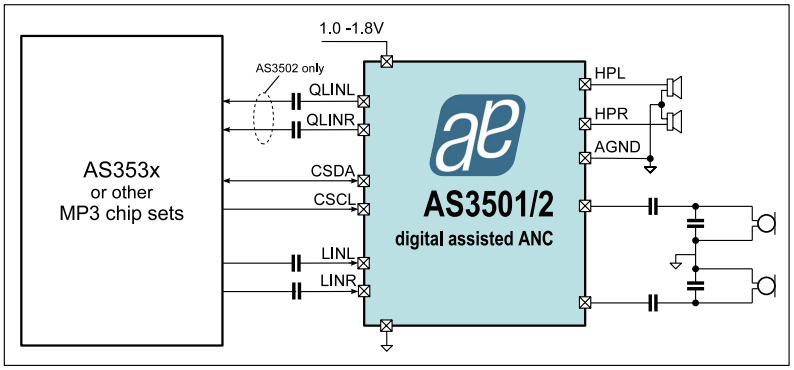


Figure 15. AS3501 feed-forward application example

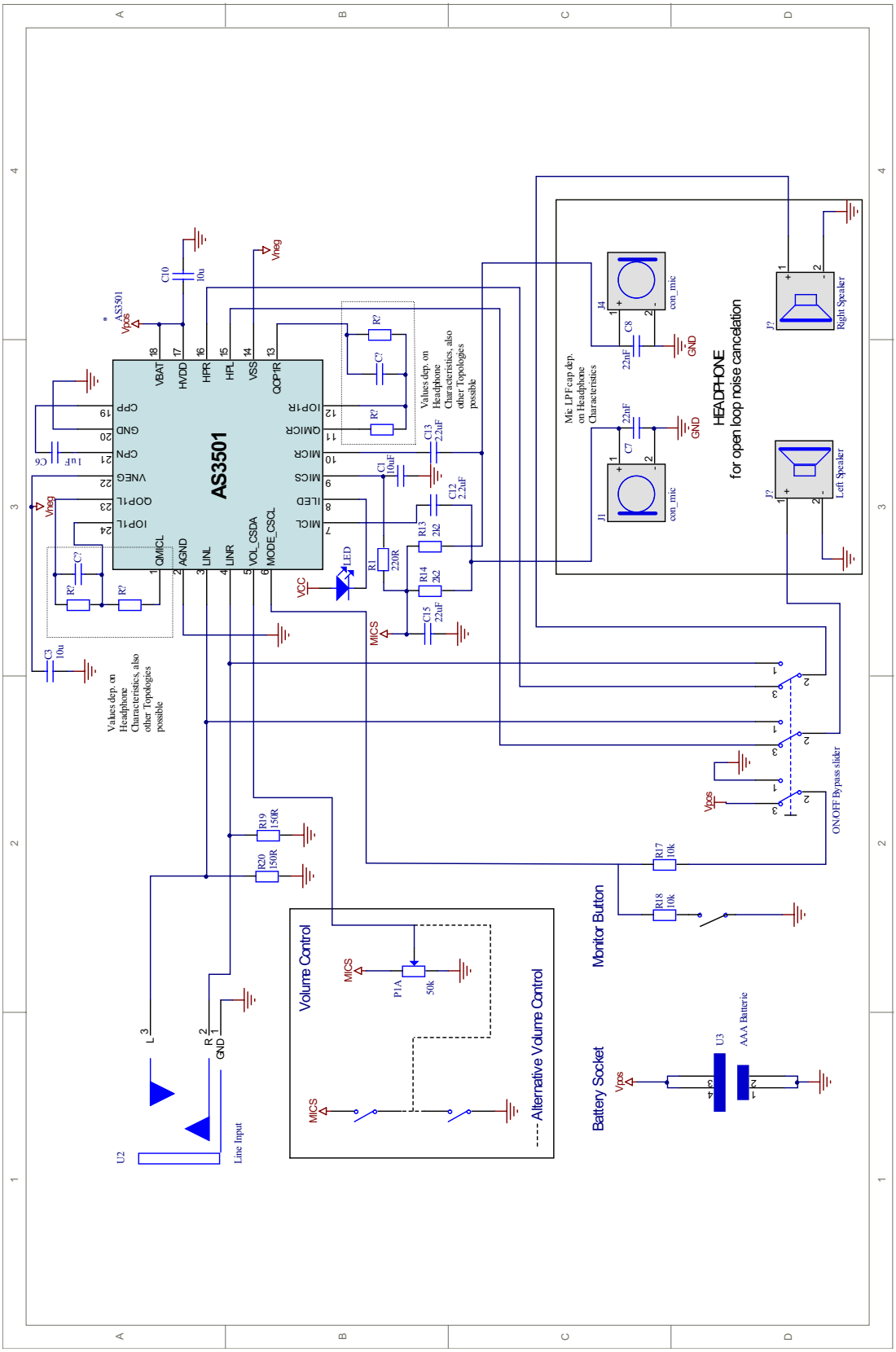


Figure 16. AS3502 feed-back application example

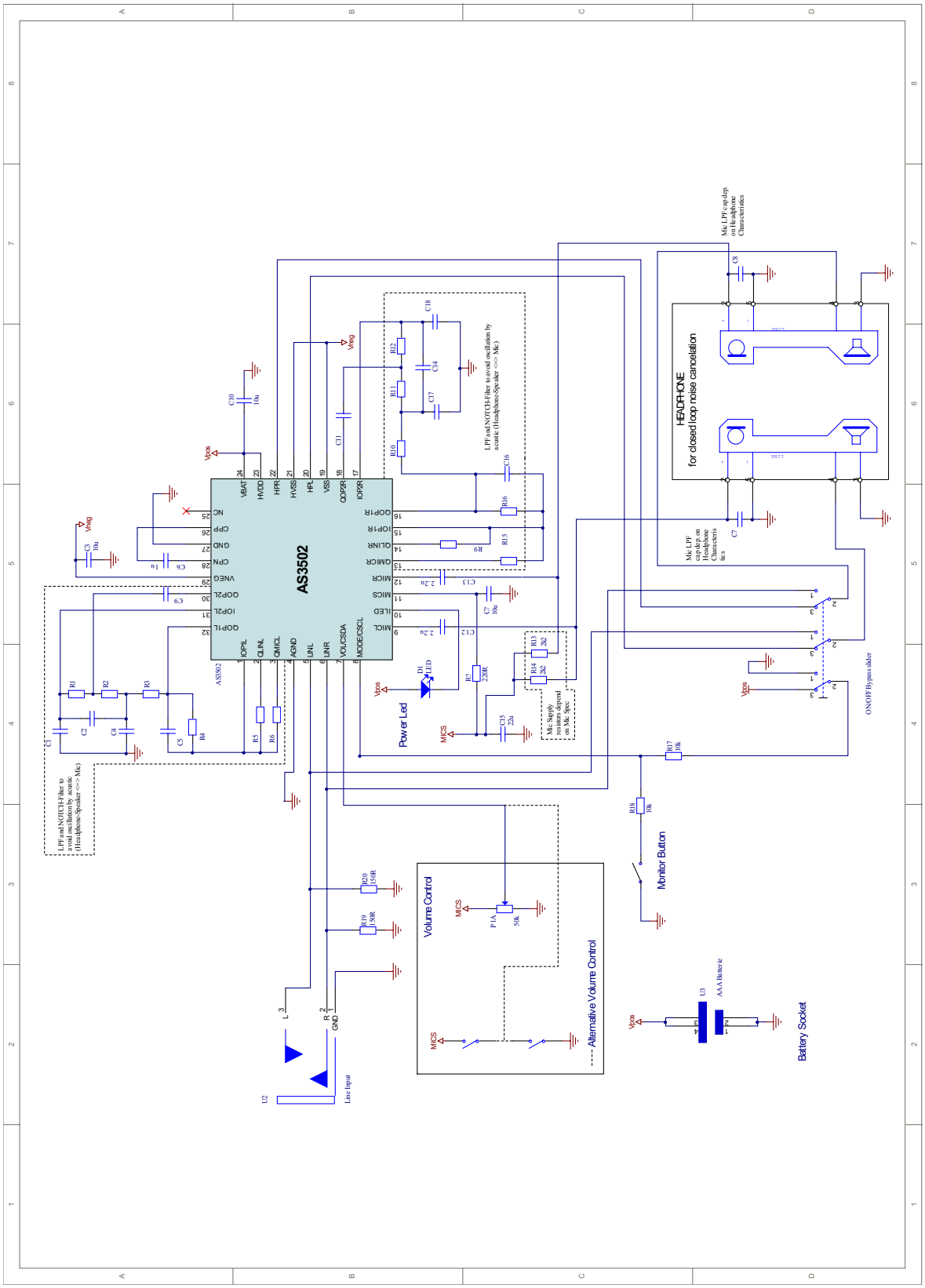
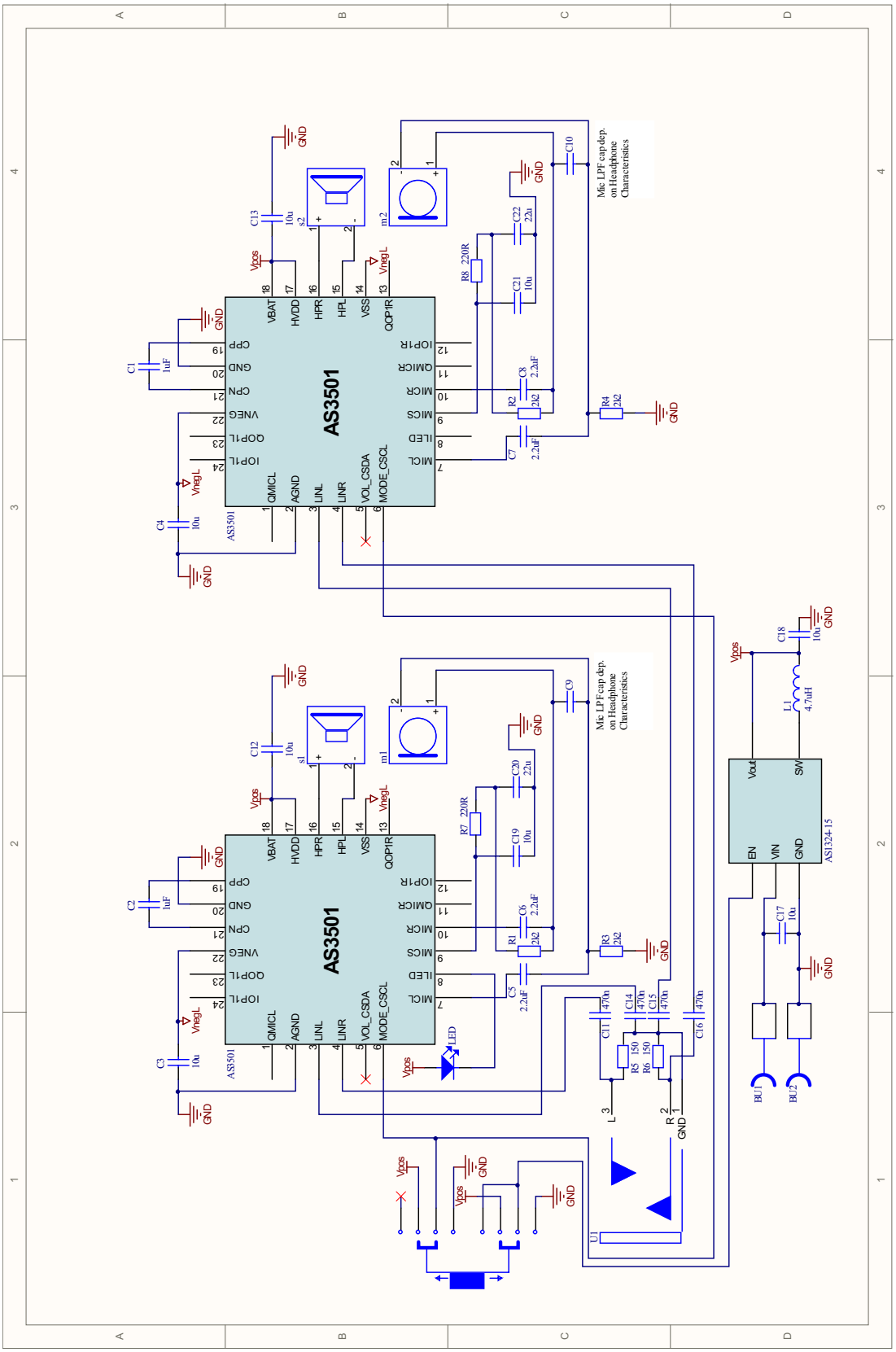


Figure 17. AS3501 Li-Ion battery bridged mode differential feed forward application example



10 Package Drawings and Markings

Figure 18. QFN Marking

Table 15. Package Code AYWWZZZ

A	Y	WW	ZZZ
B ... for Green	year	working week assembly / packaging	free choice

Figure 19. AS3500, AS3501; QFN24 0.4mm pitch

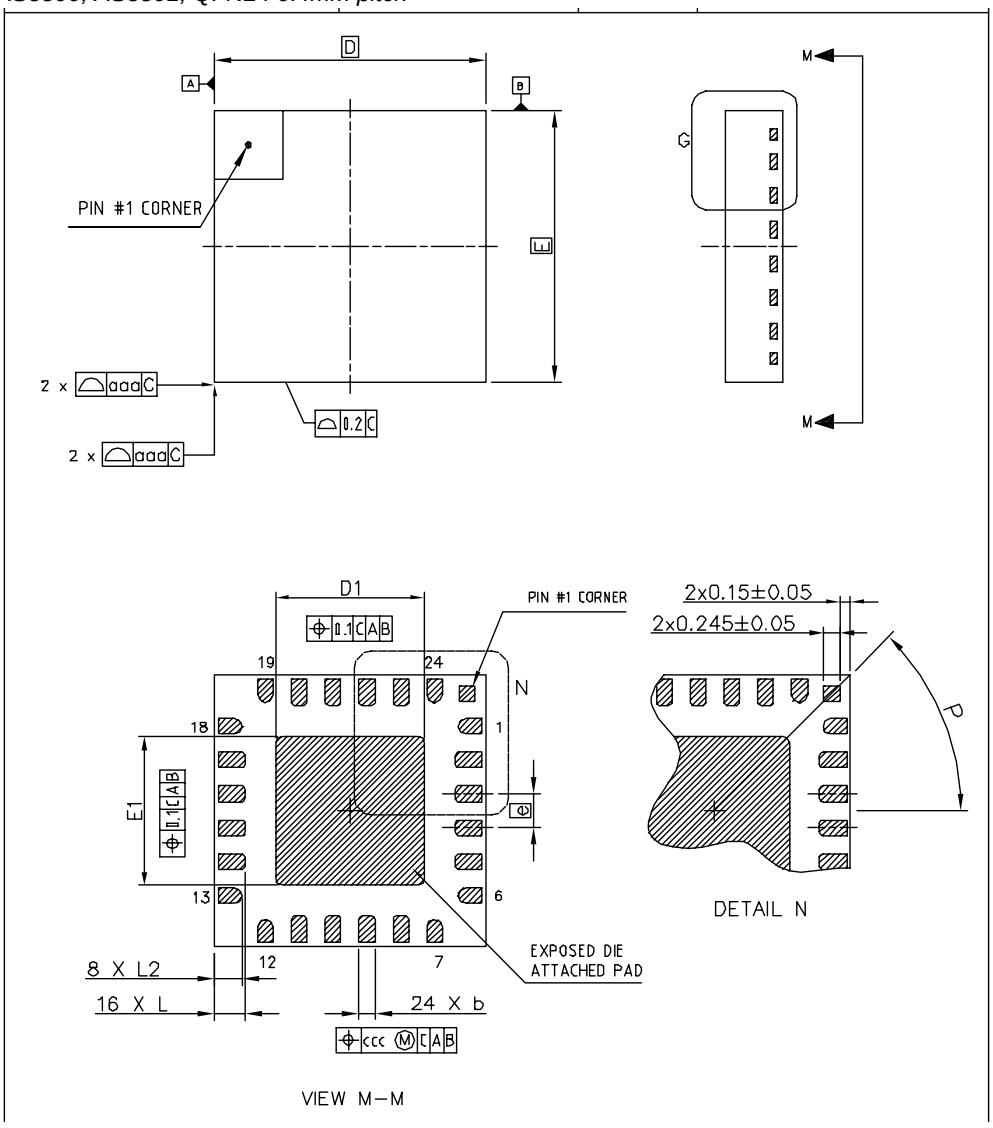
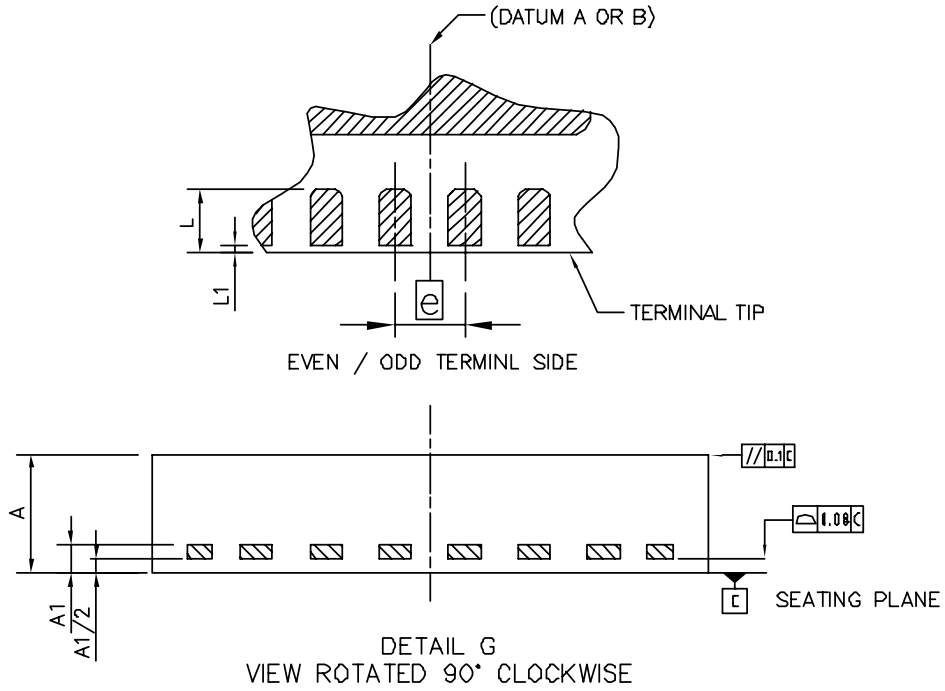


Figure 20. AS3500, AS3501; QFN24 0.4mm pitch details



DIM	MIN	NOM	MAX
A	0.75	0.85	0.95
A1	0.19		0.21
b	0.18	0.23	0.28
D		4.0 BSC	
E		4.0 BSC	
e		0.50 BSC	
D1	2.10	2.20	2.30
E1	2.10	2.20	2.30
L	0.40	0.50	0.60
L1			0.10
L2	0.30	0.40	0.50
P		45° REF	
aaa		0.10	
ccc		0.10	

NOTES

1.0 DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.

2.0 ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

3.0 DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP. DIMENSION L1 REPRESENTS TERMINAL FULL BACK FROM PACKAGE EDGE UP TO 0.1mm IS ACCEPTABLE.

4.0 COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.

5.0 RADIUS ON TERMINAL IS OPTIONAL.

UNIT	DIMENSION AND TOLERANCE	REFERENCE DOCUMENT
Millimeter(mm)	ASME Y14.5M	JEDEC MO-220

Figure 21. AS3502; QFN32 0.4mm pitch

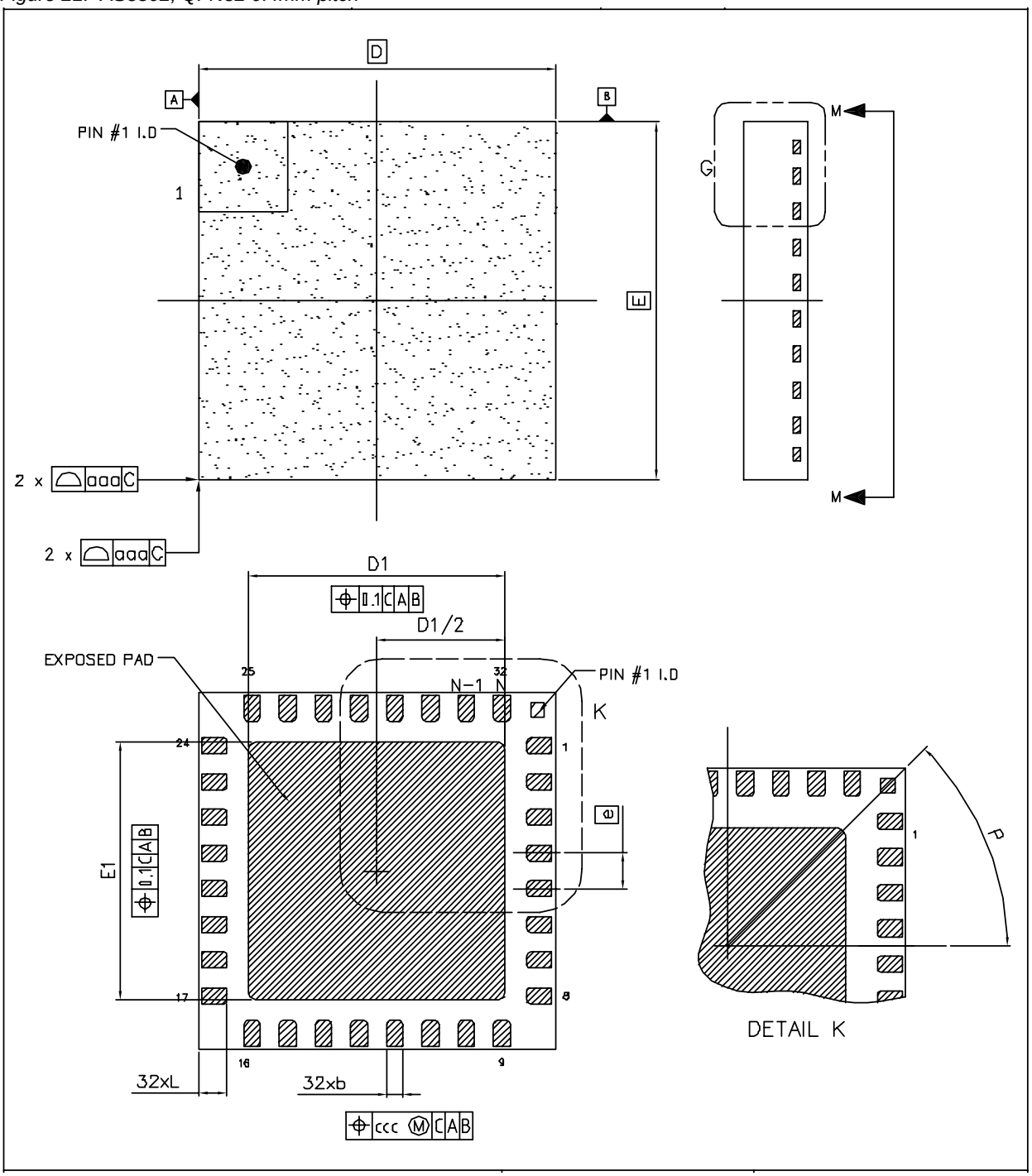
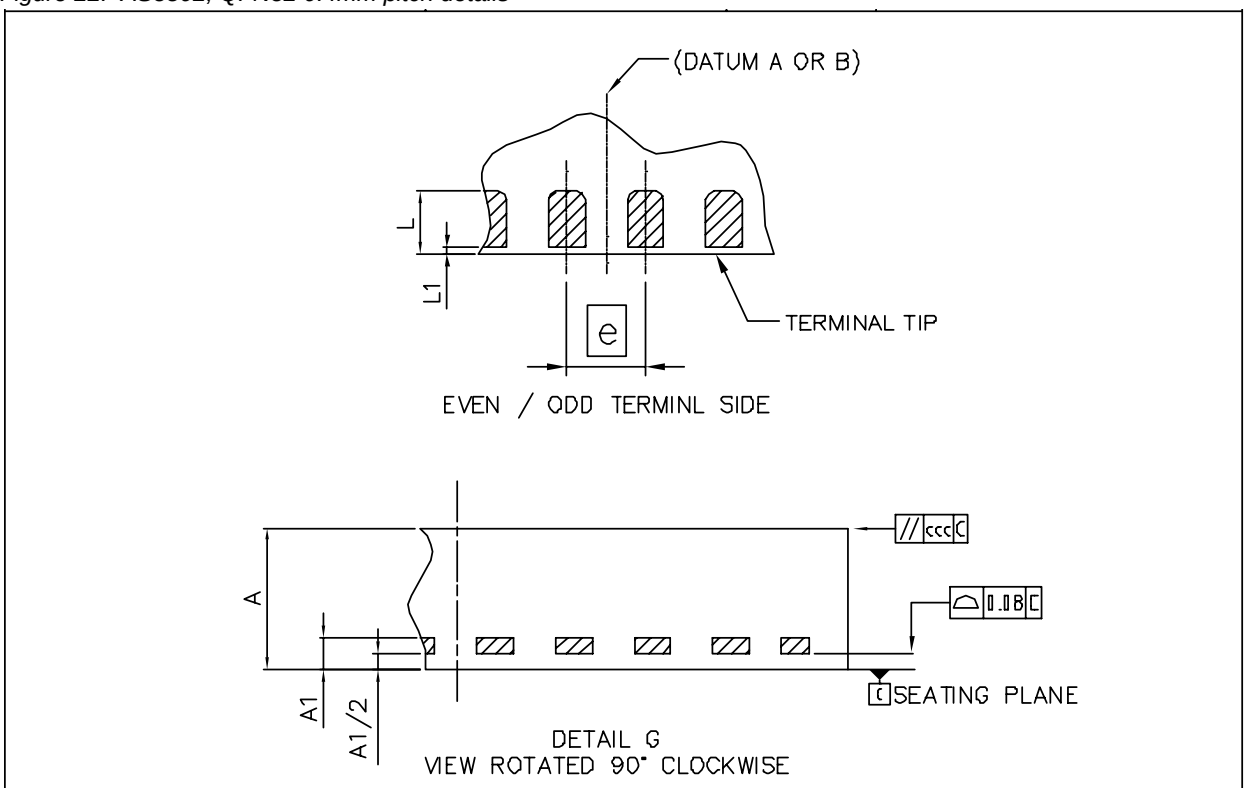


Figure 22. AS3502; QFN32 0.4mm pitch details



DIM	MIN	NOM	MAX
A	0.80		1.00
A1		0.203 REF	
b	0.18	0.23	0.30
D		5.00 BSC	
E		5.00 BSC	
D1	3.50	3.60	3.70
E1	3.50	3.60	3.70
e		0.50 BSC	
L	0.30	0.40	0.50
L1			0.10
P		45° BSC	
aaa		0.15	
ccc		0.10	

NOTES

1.0 DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.

2.0 ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

3.0 DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP. DIMENSION L1 REPRESENTS TERMINAL FULL BACK FROM PACKAGE EDGE UP TO 0.1mm IS ACCEPTABLE.

4.0 COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.

5.0 RADIUS ON TERMINAL IS OPTIONAL.

UNIT	DIMENSION AND TOLERANCE	REFERENCE DOCUMENT
Millimeter(mm)	ASME Y14.5M	JEDEC MO-220

11 Ordering Information

Table 16. Ordering Information

Model	Description	Delivery Form	Package
AS3500-EQFP	Low Power Ambient Noise-Cancelling Speaker Driver	Tape & Reel dry pack	QFN 24 [4.0x4.0x0.85mm] 0.5mm pitch
AS3501-EQFP	Low Power Ambient Noise-Cancelling Speaker Driver	Tape & Reel dry pack	QFN 24 [4.0x4.0x0.85mm] 0.5mm pitch
AS3502-EQFP	Low Power Ambient Noise-Cancelling Speaker Driver	Tape & Reel dry pack	QFN 32 [5.0x5.0x0.85mm] 0.5mm pitch

Copyrights

Disclaimer

Devices sold by austriamicrosystems AG are covered by the warranty and patent indemnification provisions appearing in its Term of Sale. austriamicrosystems AG makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. austriamicrosystems AG reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with austriamicrosystems AG for current information. This product is intended for use in normal commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically not recommended without additional processing by austriamicrosystems AG for each application. For shipments of less than 100 parts the manufacturing flow might show deviations from the standard production flow, such as test flow or test location.

The information furnished here by austriamicrosystems AG is believed to be correct and accurate. However, austriamicrosystems AG shall not be liable to recipient or any third party for any damages, including but not limited to personal injury, property damage, loss of profits, loss of use, interruption of business or indirect, special, incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data herein. No obligation or liability to recipient or any third party shall arise or flow out of austriamicrosystems AG rendering of technical or other services.

Contact Information

Headquarters
austriamicrosystems AG
A-8141 Schloss Premstaetten, Austria

Tel: +43 (0) 3136 500 0
Fax: +43 (0) 3136 525 01

For Sales Offices, Distributors and Representatives, please visit:

http://www.austriamicrosystems.com/contact